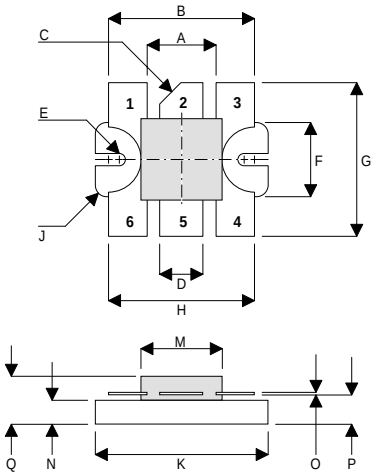
D1006UK

METAL GATE RF SILICON FET

MECHANICAL DATA



DV

PIN 1	SOURCE	PIN 2	DRAIN
PIN 3	SOURCE	PIN 4	SOURCE
PIN 5	GATE	PIN 6	SOURCE

DIM	mm	Tol.	Inches	Tol.
A	9.09	0.13	0.358	0.005
B	19.3	0.13	0.760	0.005
C	45°	5°	45°	5°
D	5.71	0.13	0.225	0.005
E	1.65R	0.13	0.065R	0.005
F	9.78	0.13	0.385	0.005
G	20.32	0.25	0.800	0.010
H	19.30	0.13	0.760	0.005
J	1.52R	0.13	0.060R	0.005
K	10.77	0.13	0.424	0.005
M	22.86	0.13	0.900	0.005
N	3.17	0.13	0.125	0.005
O	0.13	0.02	0.005	0.001
P	4.19	0.13	0.165	0.005
Q	6.35	REF	0.250	REF

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 120W – 28V – 175MHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **LOW C_{rss}**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN – 14 dB MINIMUM**

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS from 1 MHz to 200 MHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P_D	Power Dissipation	220W
BV_{DSS}	Drain – Source Breakdown Voltage	70V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	30A
T_{stg}	Storage Temperature	–65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions			Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0	I_D = 100mA		70			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 28V	V_{GS} = 0				6	mA
I_{GSS}	Gate Leakage Current	V_{GS} = 20V	V_{DS} = 0				1	μA
$V_{GS(th)}$	Gate Threshold Voltage*	I_D = 10mA	V_{DS} = V_{GS}		1		7	V
g_{fs}	Forward Transconductance*	V_{DS} = 10V	I_D = 6A		4.8			S
G_{PS}	Common Source Power Gain	P_O = 120W			14			dB
η	Drain Efficiency	V_{DS} = 28V	I_{DQ} = 1.2A		50			%
VSWR	Load Mismatch Tolerance	f = 175MHz			20:1			—
C_{iss}	Input Capacitance	V_{DS} = 0V	V_{GS} = –5V	f = 1MHz			360	pF
C_{oss}	Output Capacitance	V_{DS} = 28V	V_{GS} = 0	f = 1MHz			180	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 28V	V_{GS} = 0	f = 1MHz			15	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

$R_{THj–case}$	Thermal Resistance Junction – Case	Max. 0.8°C / W

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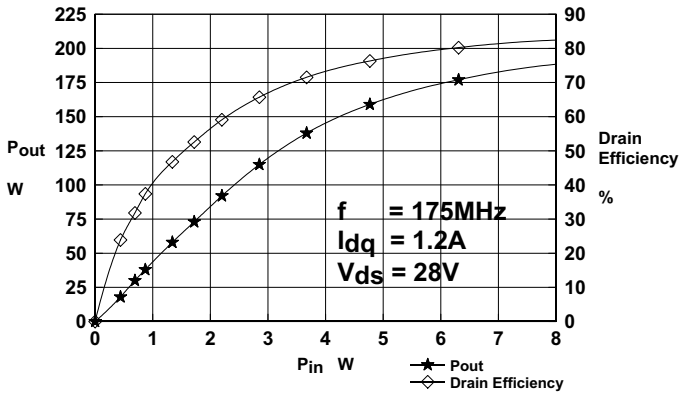

Figure 1.
Power Output and Efficiency vs.Input Power

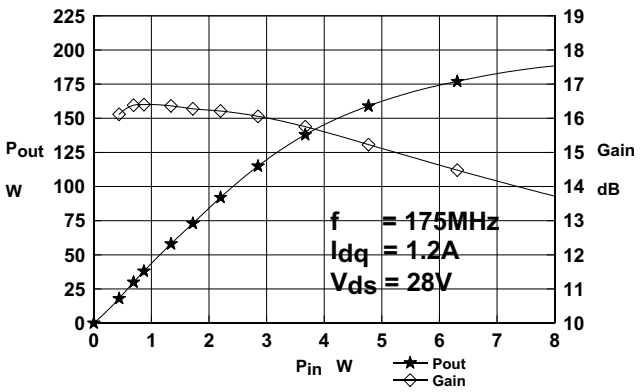

Figure 2.
Power Output and Gain vs. Input Power

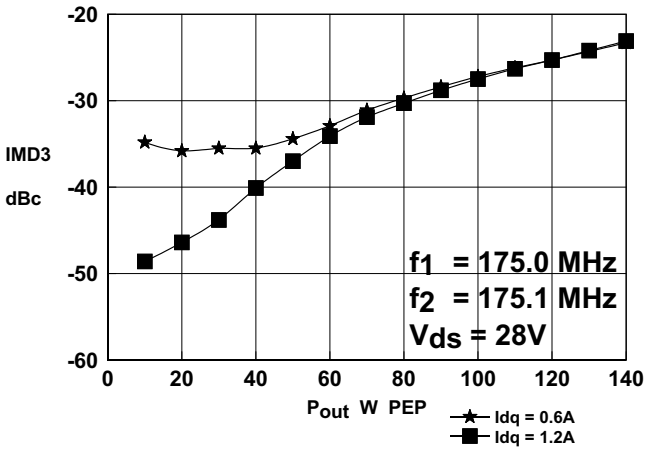

Figure 3.
IMD vs Output Power

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OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
175	0.5 - j0.6	1.7 - j0.1

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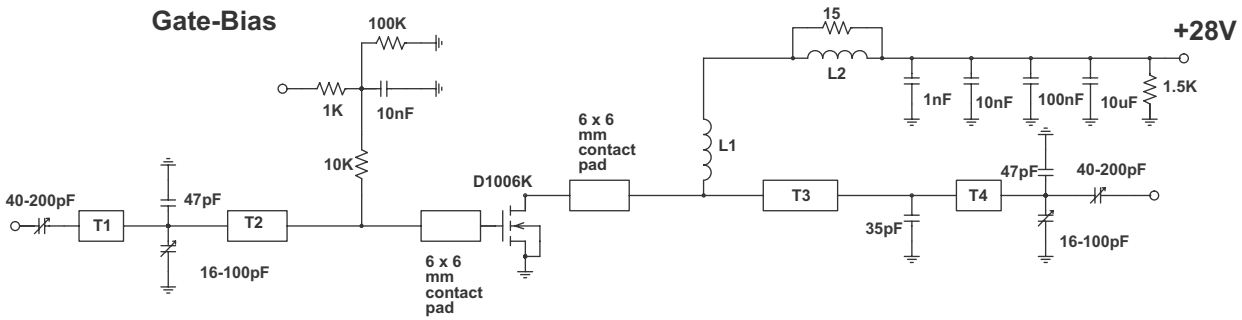

175 MHz Test Fixture

Substrate 1.6mm PTFE/glass, Er = 2.5
All microstrip lines W = 5mm

T1	10mm
T2	23.5mm
T3	25mm
T4	6mm
L1	9 turns 20swg encamelled copper wire, 6mm i.d.
L2	11 turns 19swg enamelled copper wire on Fair-Rite FT82 ferrite core

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