Description

The μPB8282 and μPB8283 are 8-bit latches with three-state output buffers. The μPB8282 is non-inverting and the μPB8283 inverts the input data. These devices are ideal for demultiplexing the address/data buses on the 8085A/8086 microprocessors. The μPB8282/83 are fabricated using NEC's Schottky bipolar process.

Features

- ☐ Support μPB8080, 8085A, 8048, 8086 family systems
- ☐ Transparent during active strobe
- ☐ Fully parallel 8-bit data register and buffer
- ☐ High output drive capability (32 mA) for driving the system data bus
- ☐ Three-state outputs

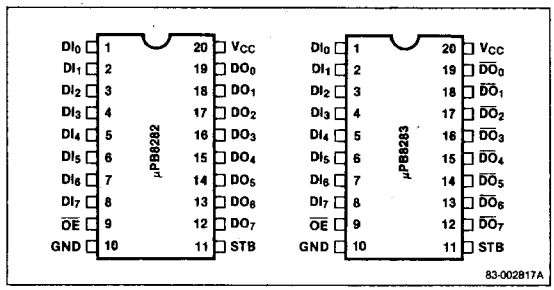
Ordering Information

Part Number	Package Type	Output Drive Capability
μPB8282C	20-pin plastic DIP	32 mA
μPB8283C	20-pin plastic DIP	32 mA

Pin Identification

No.	Symbol	Function
1-8	DI_0-DI_7	Data in
9	$\overline{OE}$	Output enable
10	GND	Ground
11	STB	Strobe
12-19	(μPB8282) DO_7-DO_0 (μPB8283) $\overline{DO}_7$-$\overline{DO}_0$	Data out
20	V_{CC}	Power supply

Pin Configurations



Pin Functions

$\overline{OE}$ (Output Enable)

This active low input control signal enables the contents of the data latches onto the data output pins (B_0-B_7). When $\overline{OE}$ goes high, the output buffers become high impedance.

STB (Strobe)

This input control pulse strobes data at input A_0-A_7 into the data latches. Data is latched at STB's high to low transition. When active high, STB admits input data.

DI_0-DI_7 (Data In)

When data that satisfies the STB strobe setup time requirements is input to these pins, it is latched into the data latches.

DO_0-DO_7 (μPB8282) (Data Out) $\overline{DO}_0$-$\overline{DO}_7$ (μPB8283)

When $\overline{OE}$ is active (low), it outputs data to the DO_0-DO_7 pins. When $\overline{OE}$ is inactive high, DO_0-DO_7 are high impedance. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

GND (Ground)

This is the ground.

V_{CC} (Power Supply)

This is the +5 V power supply.

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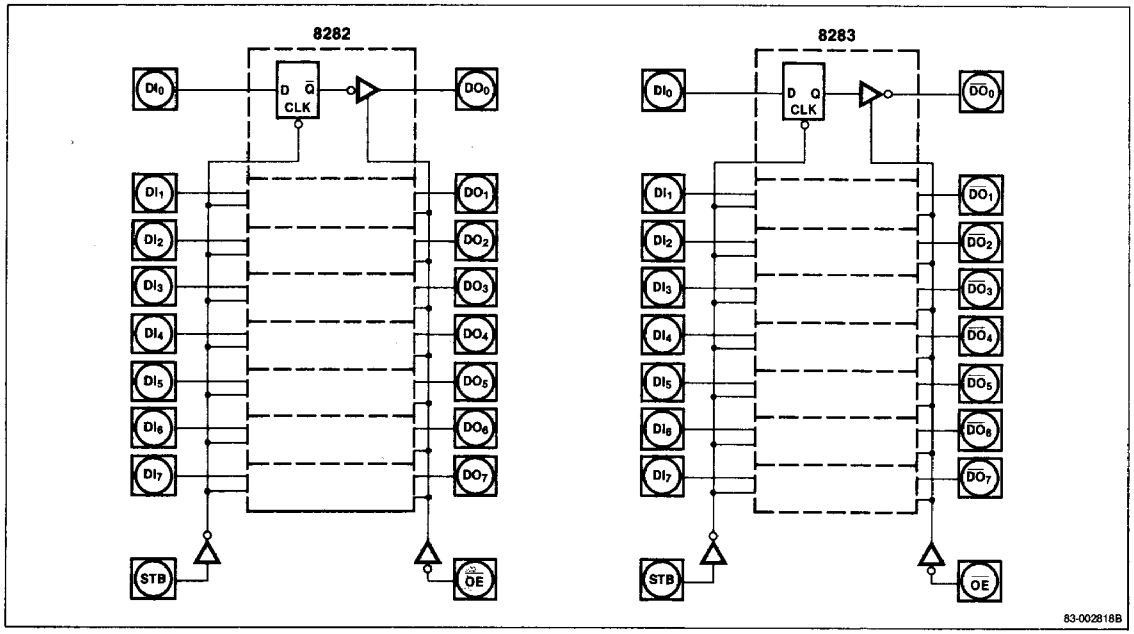
Block Diagrams



Functional Description

The μPB8282/83 are 8-bit latches with three-state output buffers. Data on the inputs is latched into the data latches on a high-to-low transition of the STB line. When STB is high, the latches appear transparent. The $\overline{OE}$ input enables the latched data to be transferred to the output pins. When $\overline{OE}$ is high, the outputs are put in the three-state condition. $\overline{OE}$ will not cause transients to appear on the data outputs.

Absolute Maximum Ratings

T_A = 25°C

Operating temperature	0°C to +70°C
Storage temperature	−65°C to +150°C
All output and supply voltages	−0.5 to +7 V
All input voltages	−1.0 V to 5.5 V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input clamp voltage	V_C		−1	V	I_C = −5 mA
Power supply current	I_{CC}		160	mA	
Forward input current	I_F		−0.2	mA	V_F = 0.45 V
Reverse input current	I_R		50	μA	V_R = 5.25 V
Output low voltage	V_{OL}		0.45	V	I_{OL} = 32 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = −5 mA
Output off current	I_{OFF}		±50	μA	V_{OFF} = 0.45 to 5.25 V
Input low voltage	V_{IL}		0.8	V	V_{CC} = 5.0 V (1)
Input high voltage	V_{IH}	2.0		V	V_{CC} = 5.0 V (1)
Input capacitance	C_{IN}		12	pF	V_{BIAS} = 2.5 V, V_{CC} = 5 V, T_A = 25°C, F = 1 MHz

Note:

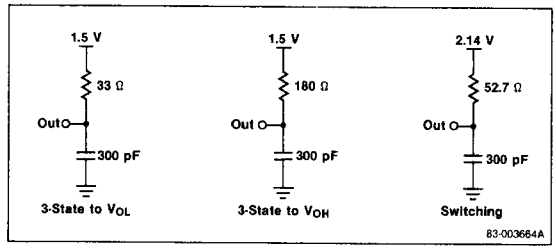
(1) Output loading I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

AC Characteristics

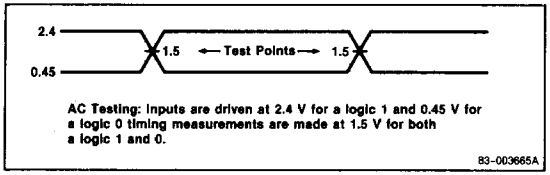
T_A = 0°C to +70°C; V_{CC} = 5 V ± 10%
I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

Parameter	Symbol	Limits Min	Limits Max	Unit
Input to output delay	t_{IVOV}			
—Inverting		5	22	ns
—Non-inverting		5	30	ns
STB to output delay	t_{SHOV}			
—Inverting		10	40	ns
—Non-inverting		10	45	ns
Output disable time	t_{EHOZ}	5	22	ns
Output enable time	t_{ELOV}	10	30	ns
Input to STB setup time	t_{IVSL}	0		ns
Input to STB hold time	t_{SLIX}	25		ns
STB high time	t_{SHSL}	15		ns
Input, output rise time	t_{ILIH}, t_{OLOH}		20	ns
Input, output fall time	t_{IHIL}, t_{OHOL}		12	ns

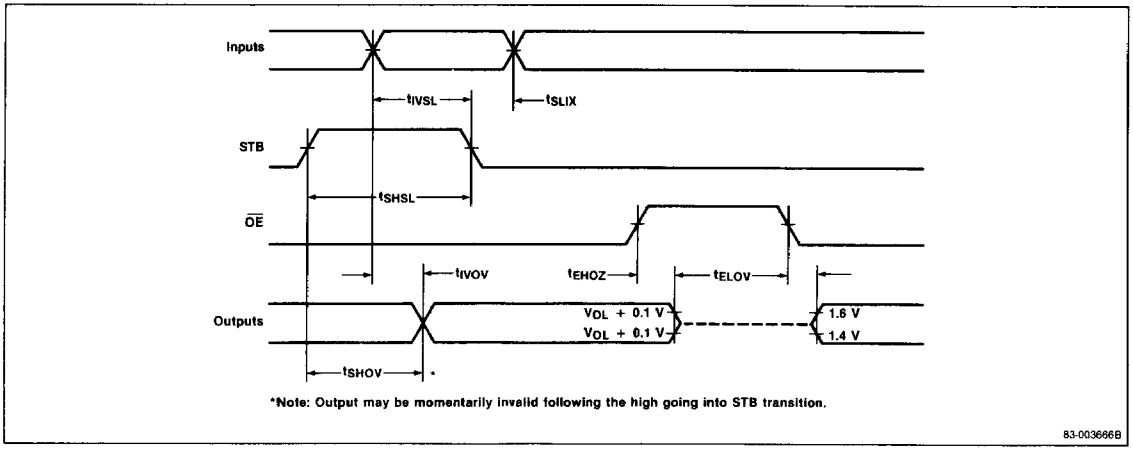
Load Circuits



AC Test Points



Timing Waveform



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