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# **PRODUCT INFORMATION**

*Vol.85*

## **Digital Satellite TV Broadcast Receiver Chip Set Developed**

### **First result of Sanyo's business alliance with IBM: Main decoder system circuits implemented on 5 chips.**

Sanyo formed an extensive business alliance with International Business Machines, Inc. in July of 1998 regarding System on Chip (SoC) products for digital information-processing consumer products and is now developing products under this ongoing agreement. Now, as the first products resulting from this alliance, Sanyo and IBM have jointly developed a video TS decoder and a microcontroller with an on-chip OSD function; two chips that form the core of a chip set for digital satellite TV broadcast receivers. Sanyo is committed to continuing to develop new products under this alliance.

**LA7788V, LC74100E, LC74150E, LC85800E, LC74180E**

#### **Overview**

Digital TV broadcasting from the broadcast satellites (a counterpart of the DBS in the U.S.) is scheduled to begin in December 2000 in Japan, and there are now many activities associated with this development taking place in many areas. Which of the broadcast corporations with major commercial stations as their parent bodies will participate has been decided, and these players are now preparing to start broadcasting. Furthermore, manufacturers of BS digital receivers for the Japanese market see the Sydney Olympics scheduled for the years 2000 as a practical target for the start of business related to BS digital broadcasting.

Although the availability of low-cost receivers is seen as the key to growth for BS digital broadcasting, the only activity from receiver manufacturers currently is the introduction of full-spec (1080-line interlaced) products that support image quality equivalent to HDTV, such as NHK's Hi-Vision. As a result, only extremely high-priced products are expected to appear in the near future. The alternative is the standard mode (480-line, interlaced or progressive scan) specification, which makes popularly-priced receivers practical. Although the image quality provided is inferior to that of full-spec devices, standard mode can provide better quality than that of the satellite TV broadcasts currently available in Japan. Thus standard mode could provide the driving force for rapid expansion of the BS digital market, as long as the price of the receiving systems can be lowered.

Sanyo, in preparation for the expected smooth growth of the BS digital TV market, has now developed a BS digital TV set chip set that is aimed both at popularly-priced BS digital TVs that support standard display mode and at set-top boxes (STB) that allow users to enjoy BS digital broadcasts on existing TV sets. This chip set consists of five chips: the LA7788V, the LC74100E, the LC74150E, the LC74180E, and the LC85800E.

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Both the LC74150E and LC74180E take advantage of IBM's IP and leading-edge Blue Logic™ programs, and were developed jointly by Sanyo and IBM. These two ICs form the core of this chip set, and represent the first result of the business alliance between Sanyo and IBM.

Each of the five chips in this chip set provides unique and powerful features. The LA7788V uses a direct quadrature downconverter that features an AGC (automatic gain control) circuit with a wide control range giving TV circuit designers wide design latitudes. In particular, this device can be used both for BS receivers and receivers for broadcasts from communication satellites (CS broadcasts) currently used by independent broadcasters in the Japanese market.

The LC74100E conforms to the BS digital broadcast standards for the Japanese market, and integrates the main functions of the demodulation block on a single chip, thus allowing the demodulation block circuit to be simplified. When combined with the LA7788V, many peripheral devices can be dispensed with; in particular, no separate tuning PLL IC is required.

The LC85800E is an audio decoder that supports MPEG2 AAC. It also incorporates a Sanyo-original virtual 3D sound-processing function allowing TV sets implemented with this chip set to support multichannel audio broadcasts with a 2-channel speaker system.

The LC74150E supports all the digital TV and video formats used in Japan and the US, and provides decoded outputs for all input formats in standard format (480 lines, interlaced or progressive scan). The LC74150E adopts a Sanyo-developed down-decoding algorithm that provides several advantages including a reduction in the amount of memory required, and is an optimal decoder for both set-top boxes that target use with existing consumer TV sets and popularly-priced BS digital TV sets.

The LC74180E microcontroller adds an OSD (on-screen display) controller to IBM's PowerPC 401™ CPU core. This microcontroller integrates all required functions, including data RAM, DRAM control, external memory control, and peripheral functions on a single chip, and also includes a multifunction OSD controller that supports the input and output of 480-line video in either interlaced or progressive scan mode.

Although this newly designed chip set supports standard mode output specifications, it is also able to down-decode full-spec signals. This feature allows it to provide a high level of image quality. A BS digital reception system can be easily implemented simply by combining this chip set with a D/A converter, memory, and a few other components. Products implemented with this chip set can bring the promise of digital satellite TV to the average consumer.

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## Features

- BS digital broadcast decoding system implemented in 5 chips
- The LA7788V adopts a direct conversion scheme that allows the number of components to be reduced since an IF stage is not required.
- The LC74150E integrates a transport stream separator and a video decoder in a single chip.
- The LC74180E integrates data RAM, DRAM control, external memory control, and peripheral functions on a single chip.
- The LC74180E is a multifunction high-performance microcontroller based on IBM's leading-edge PowerPC 401™ core.

## Specifications

### LA7788V (Direct conversion circuit)

- I/Q downconverter
- 90° quadrature oscillator
- Supports input frequencies from 950 to 2200 MHz.
- Built-in prescaler
- Package: SSOP30

### LC74100E (Conforms to Japan's BS digital broadcast transmission standards.)

- Built-in A/D converter for digitally modulated signal quantization
- TC8PSK, QPSK, and BPSK demodulation functions
- Error correction
- Built-in TMCC circuit
- On-chip memory for deinterleaving
- Miniature package: QFP100

### LC85800E (Audio decoder)

- Supports MPEG2 AAC streams (LC profile)
- Two-channel output (Also provides a Sanyo-developed virtual 3D output.)
- Package: QFP100

### LC74150E (TS + video decoder)

- Video decoder outputs HDTV (MP@HL) downconverted to 480-line interlaced or progressive scan video.
- Supports both TS decoding and MP@HL video decoding with 32 Mb of external memory (SDRAM).
- Maximum input bit rate: 80 Mbps
- Package: QFP208

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[TS Decoder Block]

- Includes 48 data separation filters (48PID).

[Video Decoder Block]

- Supports digital BS broadcasts (Japan) and the US ATV 18 format.

## **LC74180E (Microcontroller with on-chip OSD controller)**

- OSD function supports 480-line interlaced or progressive scan video
- Instruction cache: 4 KB (1024 words × 32 bits)
- Data cache: 2 KB (512 words × 32 bits)
- Data RAM: 2 KB (512 words × 32 bits)
- Smart card interface: 2 channels
- UART: One full-duplex channel (Modem interface)
- Serial I/O: One 3-wire, clock synchronous, 8-bit channel
- I<sup>2</sup>C: One multi-master I<sup>2</sup>C bus channel
- External SDRAM controller for use with the OSD function (4 or 16 Mb)
- Package: QFP240

\*: PowerPC 401™ and Blue Logic™ are registered trademarks of International Business Machines, Inc.

## **Sample Availability**

This chip set will be available in sample quantities in November 1999 and in production quantities (10,000 units/month) in June 2000.

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