Ordering number : ENN7106

Monolithic Digital IC

LB11823M

Direct PWM Drive Brushless Motor Predriver for OA Products

Overview

The LB11823M is a direct PWM drive predriver IC for use with three-phase power brushless motors. The LB11823M can implement a motor drive circuit with the desired output capacity (voltage and current) by using appropriate external transistors. Due to its built-in FG amplifier and other features, this device is optimal for motor drive in OA products that use power brushless motors.

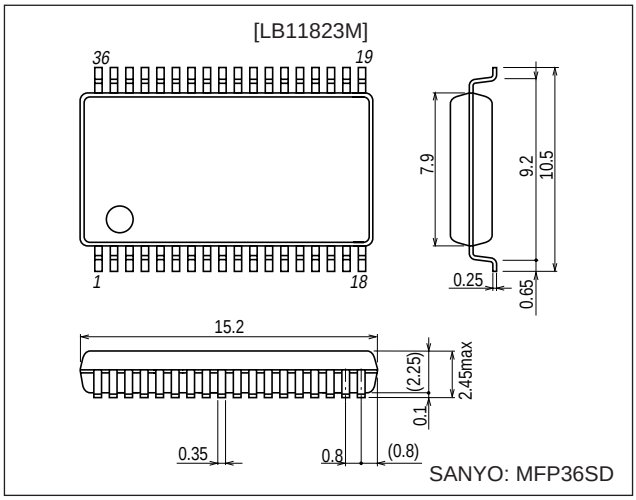
Functions and Features

- Three-phase bipolar drive
- Direct PWM drive
- Built-in FG amplifier and Schmitt comparator circuits
- Braking function (short-circuit braking)
- Built-in forward/reverse switching circuit
- Full complement of built-in protection circuits, including current limiter, undervoltage protection circuit, motor lockup protection circuit, and thermal protection circuit.
- Can be controlled by either a command voltage or the duty of an input PWM signal.

Package Dimensions

unit: mm

3129-MFP36SD



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$ max	$V_{CC}1$ pin	14.5	V
Supply voltage 2	$V_{CC}2$ max	$V_{CC}2$ pin	14.5	V
Supply voltage 3	$V_{CC}3$ max	$V_{CC}3$ pin	20	V
Output current	I_O max	Pins UL, VL, WL, UH, VH, WH	40	mA
RF pin applied voltage	VRF max		4	V
LVS pin applied voltage	VLVS max		20	V
TOC pin applied voltage	VTOC max		$V_{CC}2$	V
VCTL pin applied voltage	VCTL max		14.5	V

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Parameter	Symbol	Conditions	Ratings	Unit
Allowable power dissipation	Pd max	Independent IC	0.9	W
Operating temperature	Topr		–20 to +100	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	V_{CC}1-1	V_{CC}1 pin	8 to 13.5	V
Supply voltage range 1-2	V_{CC}1-2	V_{CC}1 pin, with V_{CC}1-VREG short-circuited	4.5 to 5.5	V
Supply voltage range 2	V_{CC}2	V_{CC}2 pin	4.5 to V_{CC}1	V
Supply voltage range 3	V_{CC}3	V_{CC}3 pin	13.5 to 19	V
Output curent	I_O	Pins UL, VL, WL, UH, VH, WH	30	mA
12V constant-voltage output current	I12REG		–50	mA
5V constant-voltage output current	IREG		–20	mA
HP pin applied voltage	VHP		0 to 13.5	V
HP pin output current	IHP		0 to 10	mA
FGS pin applied voltage	VFGS		0 to 13.5	V
FGS pin output current	IFGS		0 to 7	mA

Electrical Characteristics at Ta = 25°C, V_{CC}1 = 12 V, V_{CC}2 = VREG

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	I_{CC}1-1			15	21	mA
Supply current 2	I_{CC}1-2	Stop mode		3.5	5	mA
Output block						
Output voltage 1-1	V_{OUT}1-1	Low level I_O = 400 µA		0.1	0.3	V
Output voltage 1-2	V_{OUT}1-2	Low level I_O = 10 mA		0.8	1.1	V
Output voltage	V_{OUT}2	High level I_O = –20 mA	V_{CC}1 – 1.1	V_{CC}1 – 0.9		V
Temperature coefficient 1-1	ΔV_{OUT}1-1	Design target value*, Low level I_O = 400 µA		0.2		mV/°C
Temperature coefficient 1-2	ΔV_{OUT}1-2	Design target value*, Low level I_O = 10 mA		–1.5		mV/°C
Temperature coefficient 2	ΔV_{OUT}2	Design target value*, High level I_O = –20 mA		1.5		mV/°C
12 V Regulator-voltage output (12REG pin)						
Output voltage	V12REG	V_{CC}3 = 15 V, I_O = –30 mA	11.7	12.1	12.6	V
Voltage regulation	Δ12VREG1	V_{CC}3 = 13.5 to 19 V, I_O = –30 mA		150	300	mV
Load regulation	Δ12VREG2	I_O = –5 to –45 mA, V_{CC}3 = 15 V		100	200	mV
Temperature coefficient	Δ12VREG3	Design target value*		2		mV/°C
5 V Regulator-voltage output (VREG pin)						
Output voltage	VREG		4.7	5.0	5.3	V
Voltage regulation	ΔVREG1	V_{CC}1 = 8 to 13.5 V		40	100	mV
Load regulation	ΔVREG2	IO = –5 to –20 mA		5	30	mV
Temperature coefficient	ΔVREG3	Design target value*		0		mV/°C

Note*: These items are design target values and are not tested.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hall Amplifier Block						
Input bias current	IHB (HA)		–2	–0.5		µA
Common-mode input voltage range 1	VICM1	Hall device used	0.5		$V_{CC}1 - 2.0$	V
Common-mode input voltage range 2	VICM2	For input one-side bias (Hall IC application)	0		$V_{CC}1$	V
Hall input sensitivity			50			mVp-p
Hysteresis width	ΔV_{IN} (HA)		20	30	50	mV
Input voltage L → H	VSLH (HA)		5	15	25	mV
Input voltage H → L	VSHL (HA)		–25	–15	–5	mV
VCTL pin						
Input voltage 1	VCTL1	Output duty 0%	1.05	1.4	1.75	V
Input voltage 2	VCTL2	Output duty 100%	3.0	3.5	4.1	V
Input bias current 1	IB1 (CTL)	VCTL = 0 V	–80	–60		µA
Input bias current 2	IB2 (CTL)	VCTL = 5 V		60	80	µA
PWM oscillator (PWM pin)						
Output H level voltage	V_{OH} (PWM)		2.75	3.0	3.25	V
Output L level voltage	V_{OL} (PWM)		1.0	1.2	1.3	V
External C charge current	ICHG	VPWM = 2.1 V	–60	–45	–30	µA
Oscillator frequency	f (PWM)	C = 1000pF	17.6	22	26.8	kHz
Amplitude	V (PWM)		1.6	1.8	2.1	Vp-p
TOC pin						
Input voltage 1	VTOC1	Output duty 0%	2.72	3.0	3.30	V
Input voltage 2	VTOC2	Output duty 100%	0.99	1.2	1.34	V
Input voltage 1L	VTOC1L	Design target value*, 0% with $V_{CC}2$ = 4.7 V	2.72	2.80	2.90	V
Input voltage 2L	VTOC2L	Design target value*, 100% with $V_{CC}2$ = 4.7 V	0.99	1.08	1.17	V
Input voltage 1H	VTOC1H	Design target value*, 0% with $V_{CC}2$ = 5.3 V	3.08	3.20	3.30	V
Input voltage 2H	VTOC2H	Design target value*, 100% with $V_{CC}2$ = 5.3 V	1.11	1.22	1.34	V
HP pin						
Output saturation voltage	VHPL	I_O = 7 mA		0.15	0.5	V
Output leakage current	IHP leak	V_O = 13.5 V			10	µA
FGS pin						
Output saturation voltage	VFGS	I_O = 5 mA		0.15	0.5	V
Output leakage current	IFGS leak	V_O = 13.5 V			10	µA
FG amplifier						
Input offset voltage	V_{IO} (FG)		–10		10	mV
Input bias current	IB (FG)		–1		1	µA
Output H level voltage	V_{OH} (FG)	IFG0 = –0.2 mA	VREG – 1.2	VREG – 0.8		V
Output L level voltage	V_{OL} (FG)	IFG0 = 0.2 mA		0.8	1.2	V
FG input sensitivity		Gain 100-fold	3			mV

Note*: These items are design target values and are not tested.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Common phase input voltage range	VICM		1.2		VREG – 2.0	V
Next-stage Schmidt width			40	80	140	mV
Operation frequency range					10	kHz
Open loop GAIN		f (FG) = 2 kHz	45	49		dB
CSD oscillator (CSD pin)						
Output H level voltage	V_{OH} (CSD)		3.2	3.6	4.0	V
Output L level voltage	V_{OL} (CSD)		0.9	1.1	1.3	V
External C charge current	ICHG1		–14	–10	–6	µA
External C discharge current	ICHG2		7	11	15	µA
Oscillator frequency	f (CSD)	C = 0.01 µF		200		Hz
Amplitude	V (CSD)		2.2	2.5	2.75	Vp-p
Current limiter circuit (RF pin)						
Limiter voltage	VRF		0.45	0.5	0.55	V
Low-voltage protection circuit (LVS pin)						
Operating voltage	VSDL		3.6	3.8	4.0	V
Release voltage	VSDH		4.1	4.3	4.5	V
Hysteresis width	ΔVSD		0.35	0.5	0.65	V
Thermal shutdown operation (Overheat protection circuit)						
Thermal shutdown operating temperature	TSD	Design target value* (junction temperature)	125	145	165	°C
Hysteresis width	ΔTSD	Design target value* (junction temperature)	20	25	30	°C
PWMIN pin						
Input frequency	f (PI)				50	kHz
H level input voltage	V_{IH} (PI)		2.0		VREG	V
L level input voltage	V_{IL} (PI)		0		1.0	V
Input open voltage	V_{IO} (PI)		VREG – 0.5		VREG	V
Hysteresis width	V_{IS} (PI)		0.2	0.3	0.4	V
H level input current	I_{IH} (PI)	VPWMIN = VREG	–10	0	10	µA
L level input current	I_{IL} (PI)	VPWMIN = 0 V	–130	–96		µA
S/S pin						
H level input voltage	V_{IH} (SS)		2.0		VREG	V
L level input voltage	V_{IL} (SS)		0		1.0	V
Input open voltage	V_{IO} (SS)		VREG – 0.5		VREG	V
Hysteresis width	VIS (SS)		0.2	0.3	0.4	V
H level input current	I_{IH} (SS)	VS/S = VREG	–10	0	10	µA
L level input current	I_{IL} (SS)	VS/S = 0 V	–130	–96		µA
F/R pin						
H level input voltage	V_{IH} (FR)		2.0		VREG	V
L level input voltage	V_{IL} (FR)		0		1.0	V
Input open voltage	V_{IO} (FR)		VREG – 0.5		VREG	V
Hysteresis width	V_{IS} (FR)		0.2	0.3	0.4	V
H level input current	I_{IH} (FR)	VF/R = VREG	–10	0	10	µA
L level input current	I_{IL} (FR)	VF/R = 0 V	–130	–96		µA

Note*: These items are design target values and are not tested.

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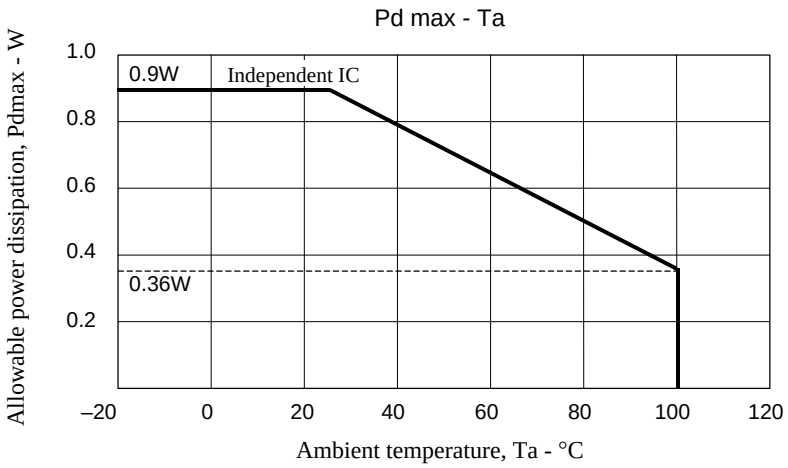
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
BR pin						
H level input voltage	V_{IH} (BR)		2.0		VREG	V
L level input voltage	V_{IL} (BR)		0		1.0	V
Input open voltage	V_{IO} (BR)		VREG – 0.5		VREG	V
Hysteresis width	V_{IS} (BR)		0.2	0.3	0.4	V
H level input current	I_{IH} (BR)	VBR = VREG	–10	0	10	µA
L level input current	I_{IL} (BR)	VBR = 0 V	–130	–96		µA
REVSEL pin						
H level input voltage	V_{IH} (REVSEL)		2.0		VREG	V
L level input voltage	V_{IL} (REVSEL)		0		1.0	V
Input open voltage	V_{IO} (REVSEL)		VREG – 0.5		VREG	V
H level input current	I_{IH} (REVSEL)	VREVSEL = VREG	–10	0	10	µA
L level input current	I_{IL} (REVSEL)	VREVSEL = 0 V	–130	–96		µA

Note*: These items are design target values and are not tested.



Three-Phase logic Truth Table (IN = [H] indicates a condition in which IN+ > IN–.)

	F/R = L			F/R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	—
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

When the OFF mode is selected during reversing at the REVSEL pin, it is necessary to specify the Hall input condition.
With F/R = "L", the condition in which the Hall input is entered in the order from 1 to 6 in the above table is considered the forward rotation and that in the reverse order is considered reversing.
With F/R = "H", the condition in which the Hall input is entered in the order from 6 to 1 in the above table is considered the forward rotation and that in the reverse order is considered reversing.

S/S pin

Input condition	Condition
H or open	Stop
L	Start

REVSEL pin

Input condition	Condition
H or open	—
L	OFF mode for reversing

BR pin

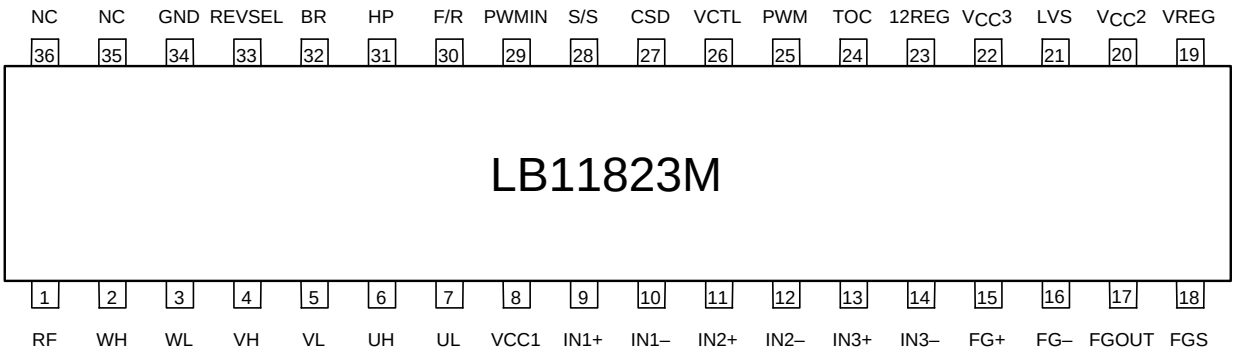
Input condition	Condition
H or open	—
L	Brake

PWMIN pin

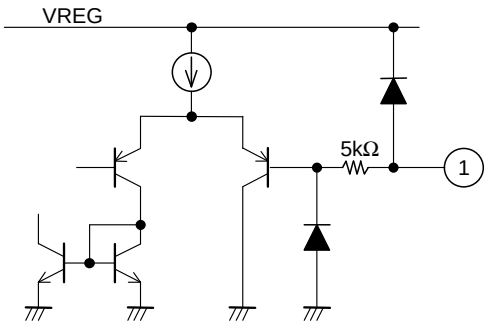
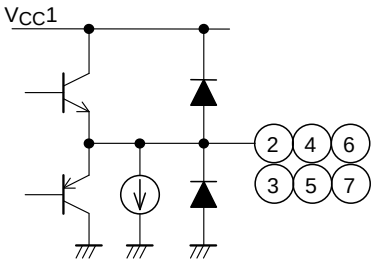
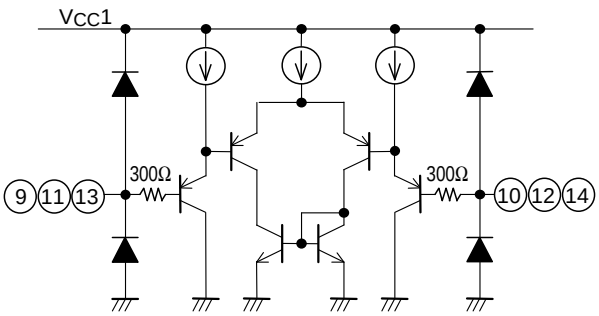
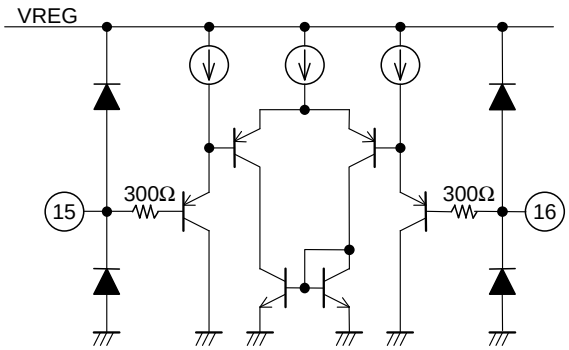
Input condition	Condition
H or open	Output OFF
L	Output ON

When S/S and PWMIN pins are not used, set the input to the L level voltage.
When REVSEL and BR pins are not used, set the input to the H level voltage or the open condition.

Pin Assignment



Pin Description

Pin No.	Symbol	Pin Description	Equivalent circuit
1	RF	Output current detection Connect a resistor (Rf) between this pin and ground. Set with the maximum output current I_{OUT} = 0.5/Rf.	
2 4 6 3 5 7	WH VH UH WL VL UL	Output pin (external TR drive output) Duty control made on UH, VH, and WH sides.	
8	$V_{CC}1$	Power supply (output and Hall input blocks). Normally used with the 12 V power supply. Connect to $V_{CC}2$ and VREG for application with the 5 V single power supply. Connect a capacitor between this pin and GND for stabilization.	
9 10 11 12 13 14	IN1+ IN1– IN2+ IN2– IN3+ IN3–	Hall amplifier input. IN+ > IN– is the input high state, and the reverse is the input low state. Connect a capacitor between the s IN+ and IN– inputs if there is noise in the Hall sensor signals.	
15 16	FGIN+ FGIN–	FG amplifier inputs IN+ is the noninverting input. IN– is the inverting input.	

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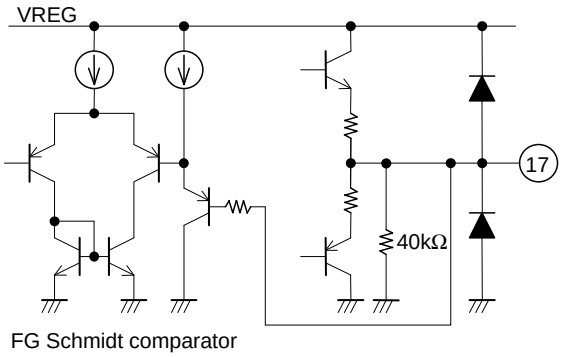
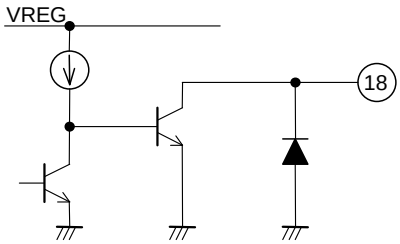
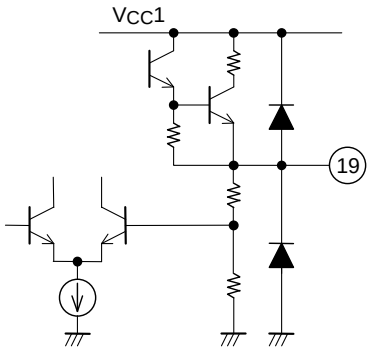
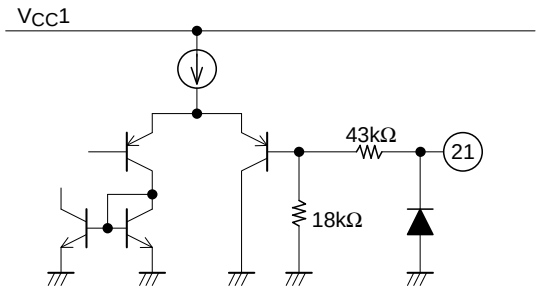
Pin No.	Symbol	Pin Description	Equivalent circuit
17	FG OUT	FG amplifier output pin	 FG Schmidt comparator
18	FGS	FG Schmidt output pin	
19	VREG	Regulated-voltage output pin (5V output) Connect a capacitor (about 0.1µF) between this pin and ground for stabilization.	
20	$V_{CC}2$	Power pin (PWM oscillation, PWM comparator, VCTL amp). Normally connect to VREG. In applications that apply a voltage externally to the VCTL or TOC pin and use a fixed output duty, variations in the duty can be suppressed by connecting this pin to $V_{CC}1$ (12 V).	
21	LVS	Voltage detection pin for low-voltage protection. To detect the supply voltage of 5 V or more, connect the zenor diode in series to set the detection voltage.	

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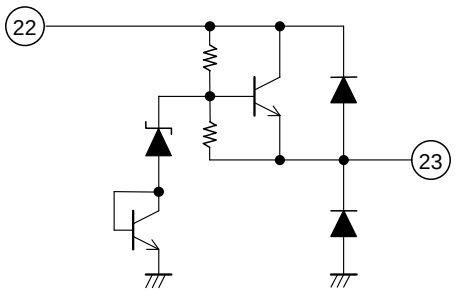
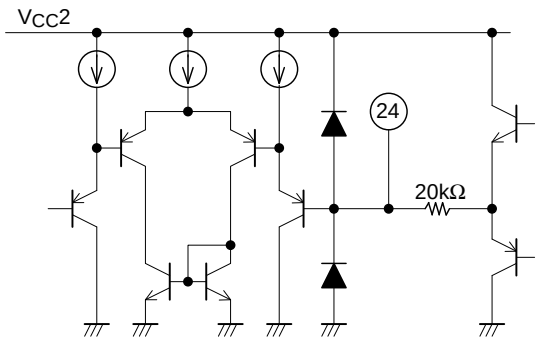
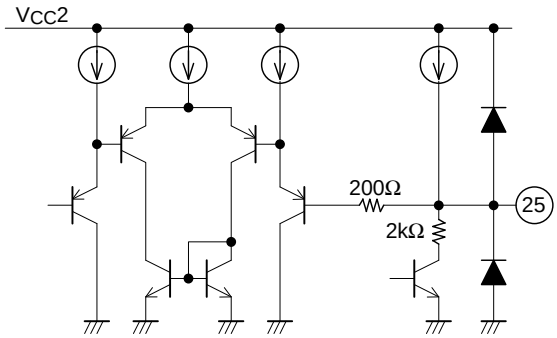
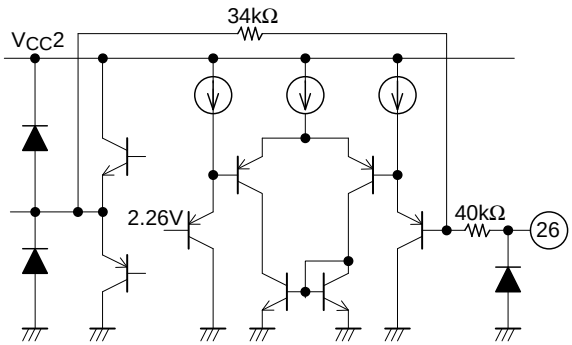
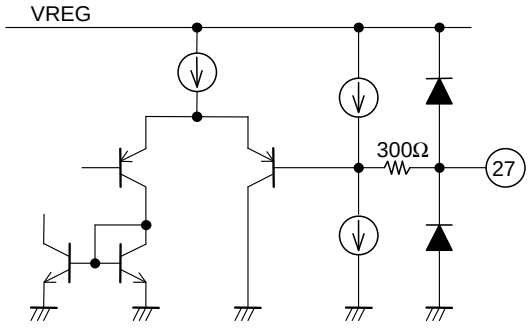
Pin No.	Symbol	Pin Description	Equivalent circuit
22 23	$V_{CC}3$ 12REG	Power pin ($V_{CC}3$) for use during application with the supply voltage of 12 V or more. 12 V is generated at the 12 REG pin. To use the 12REG pin, connect this pin to $V_{CC}1$. When not used, keep both $V_{CC}3$ and 12 REG open or connect them to GND.	
24	TOC	PWM waveform comparator pin. Normally used in the open condition. By inputting the voltage directly into this pin, the output duty can be controlled without using the VCTL amp.	
25	PWM	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND.	
26	VCTL	Control voltage input pin. For control with this pin, set the PWMIN pin to the L level.	
27	CSD	Pin to set the operation time of motor lock protection circuit and to set the initial reset pulse. Connect a capacitor between this pin and GND. When the protection circuit is not to be used, connect a capacitor and resistor (150kΩ, 4700pF) in parallel between this pin and GND.	

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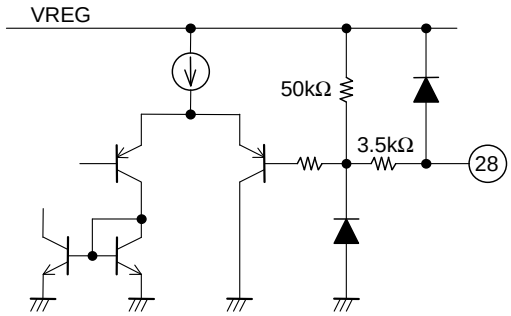
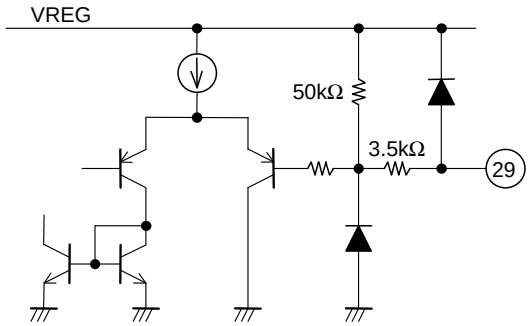
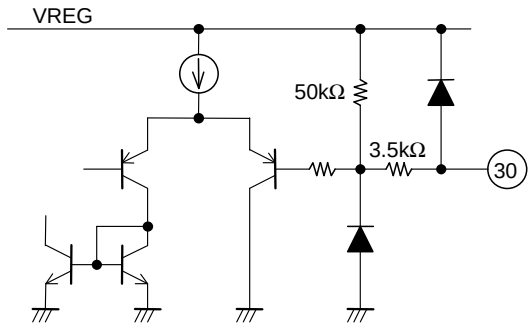
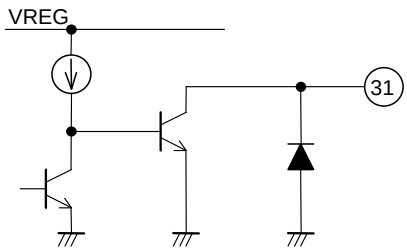
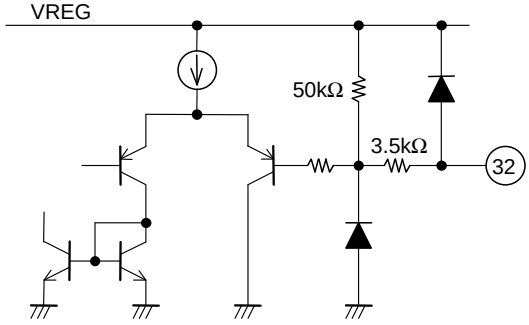
Pin No.	Symbol	Pin Description	Equivalent circuit
28	S/S	Start/stop control pin. Start with L and stop with H or in the open condition	
29	PWM IN	PWM pulse input pin. Output drive with L and output OFF with H or in the open condition. For control with this pin, apply the voltage of VCTL2 voltage or more to the VCTL pin.	
30	F/R	Forward/reverse input pin	
31	HP	Hall signal three-phase synthesis output signal	
32	BR	Brake input pin. Brake with L and normal rotation with H or in the open condition.	

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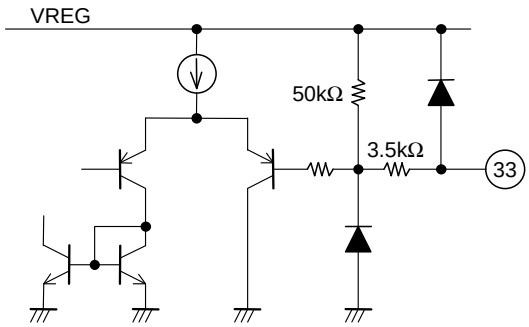
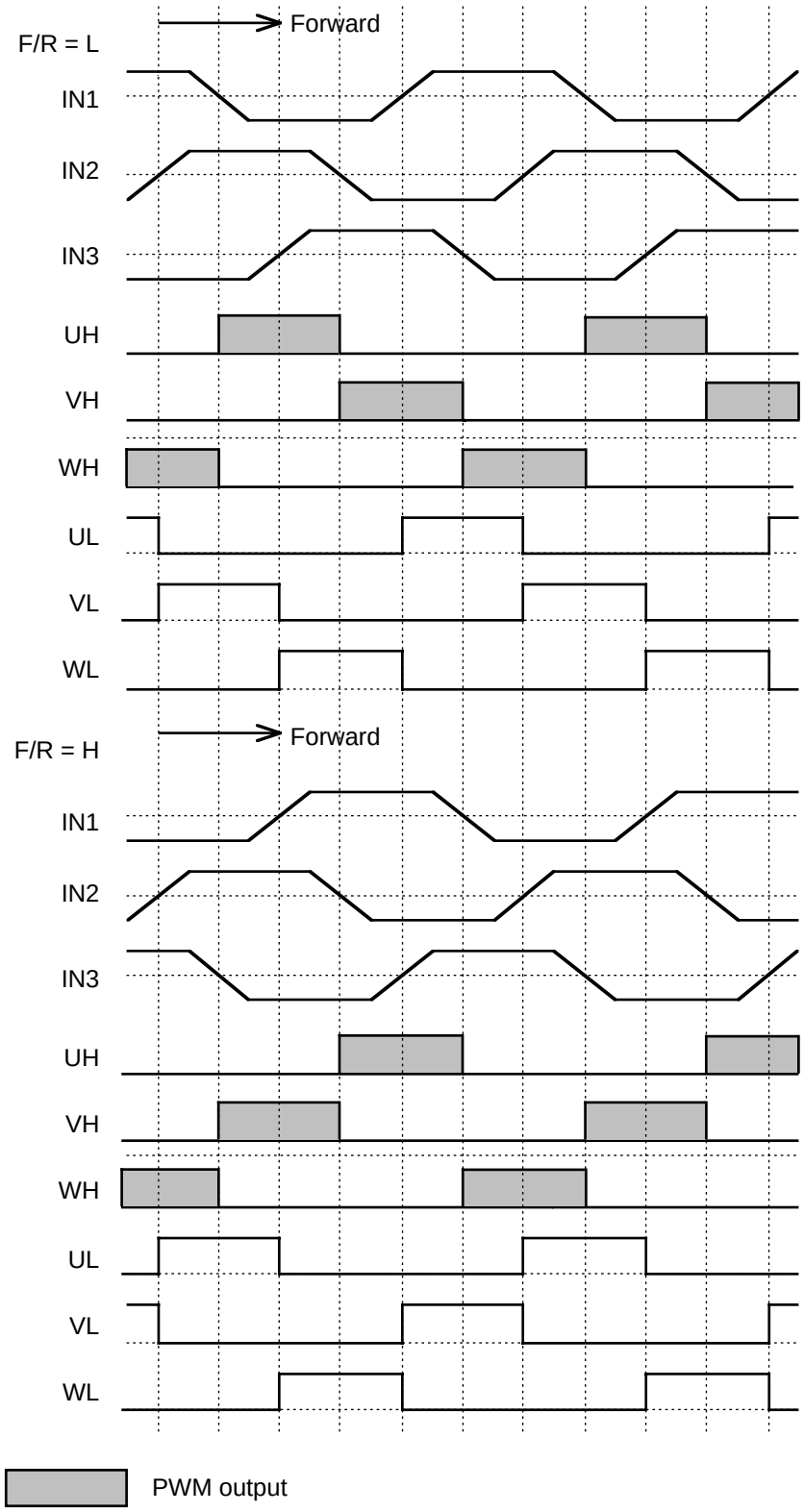
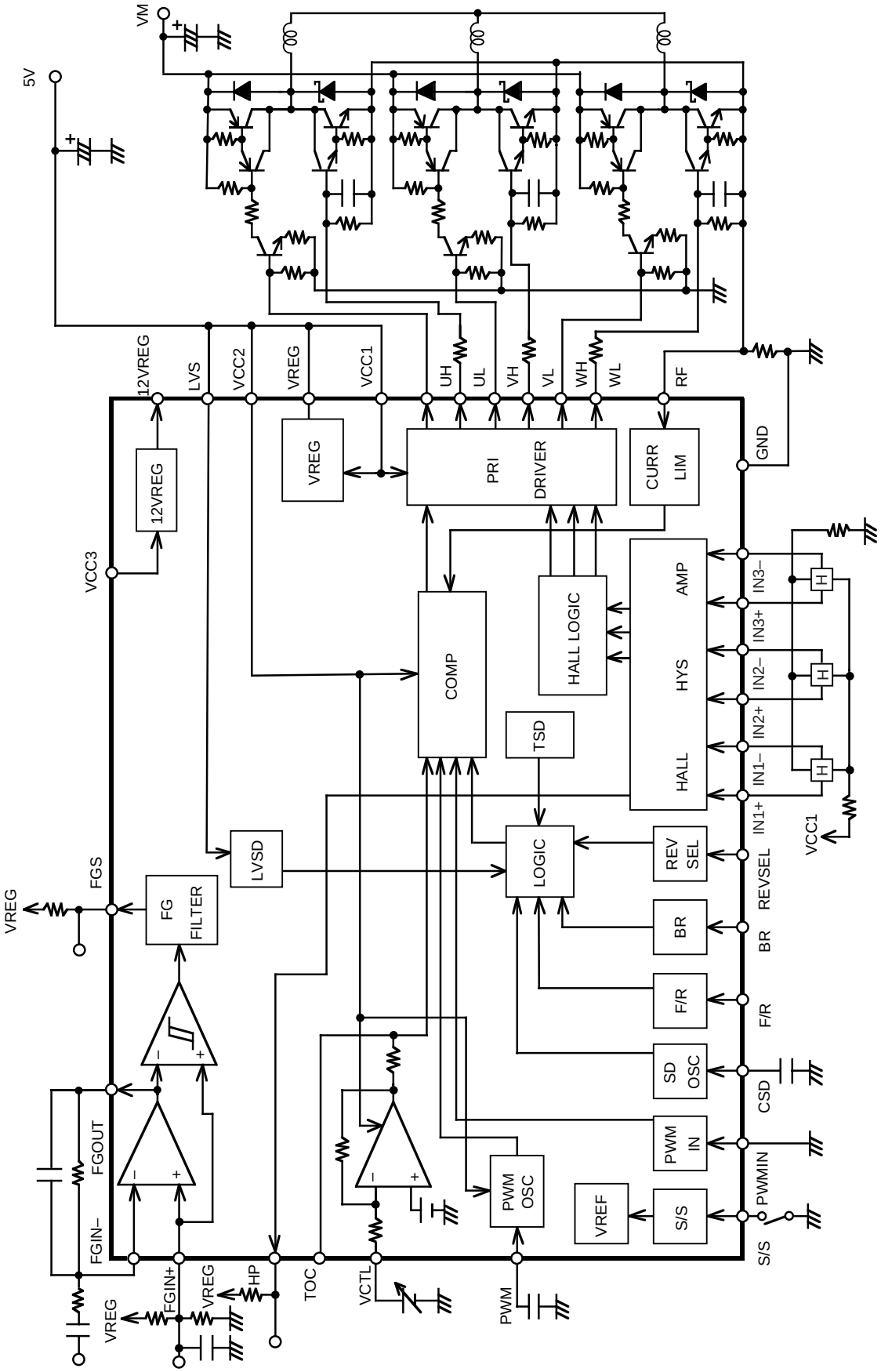
Pin No.	Symbol	Pin Description	Equivalent circuit
33	REV SEL	Reverse OFF selector pin. Effective with L and ineffective with H or in the open condition.	
34	GND	GND pin	
35 36	NC	NC pin that can be used for wiring	

Hall-Effect Sensor Input/Output Timing Chart

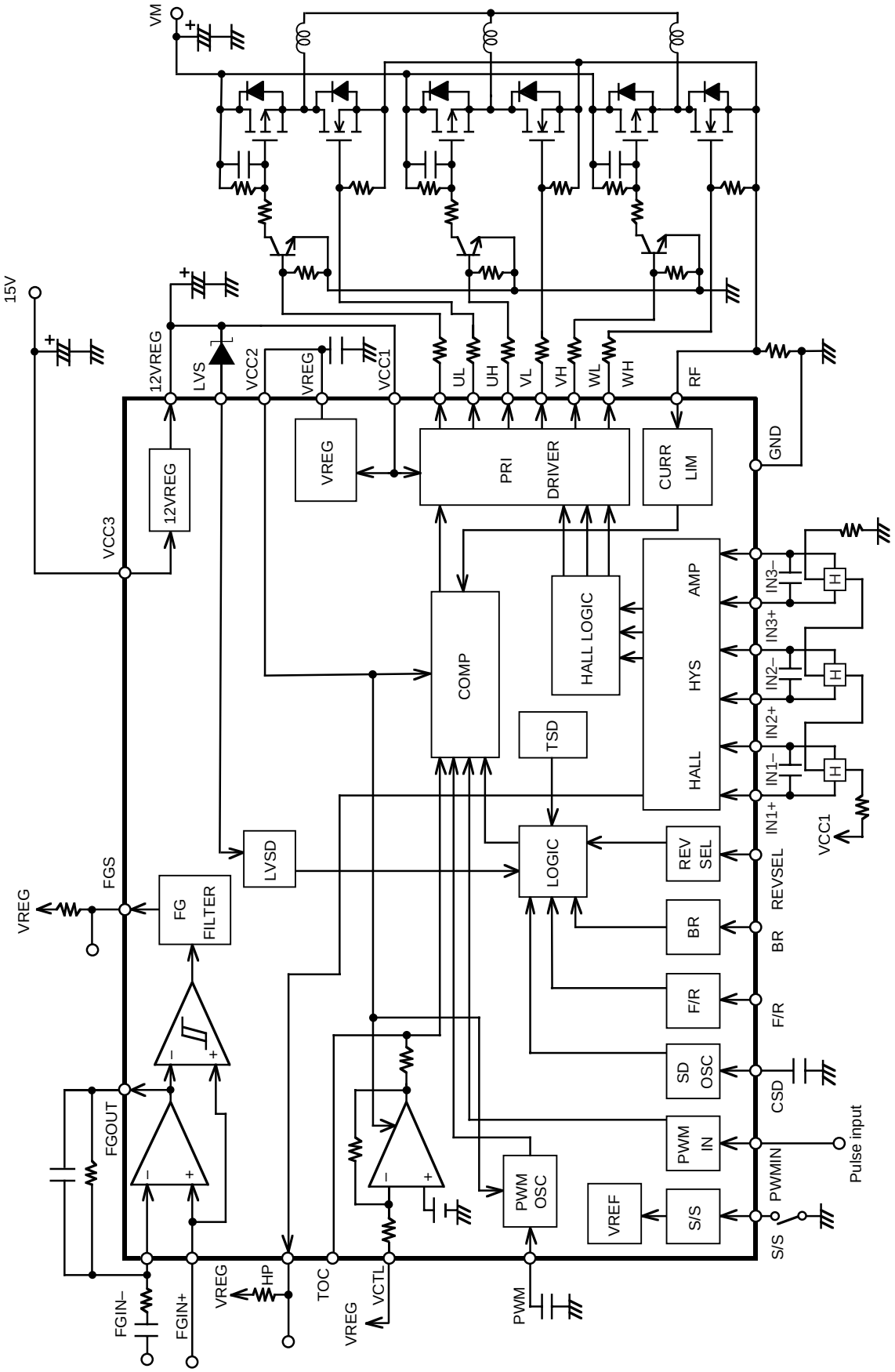


Sample Application Circuit

(1) Bipolar transistor drive (upper side PWM) using a 5 V power supply



(2) MOS transistor drive (lower side PWM) using a 15 V power supply



LB11823M Function Description

1. Output drive circuit

This IC employs a direct PWM drive method to minimize the power loss at output. The output TR is normally saturated in the ON condition, adjusting the motor drive power by changing the output on-duty. Output PWM switching is made on UH, VH, and WH output sides. Since UL – WL and UH – WH outputs are of the same output form, either lower PWM or upper PWM can be selected by changing the external output Tr connection method. Selection of diode to be connected to the non-PWM side output requires attention because there is a problem of reverse recovery time. (Unless a diode with the short reverse recovery time is selected, the through current flows in an instant when the PWM side Tr is turned ON.)

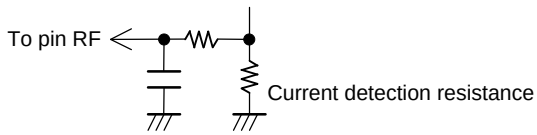
UL – WL and UH – WH outputs enter the high impedance condition at a time of stop or when the supply voltage is extremely low (below the allowable operation voltage). Accordingly, an appropriate measure (pull-down resistor, etc.) is necessary in the external circuit to prevent an incorrect action due to the leak current.

2. Current limiting circuit

The current limiting circuit performs limiting with the current determined from $I = V_{RF}/Rf$ (V_{RF} = 0.5 Vtyp, Rf : current detector resistance) (that is, this circuit limits the peak current).

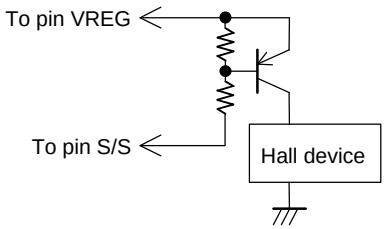
Limiting operation includes decrease in the output on-duty to suppress the current.

The current limiting circuit incorporates a filter circuit to prevent an incorrect action of current limiting operation due to detection of the reverse recovery current of output diode during PWM operation. This internal filter circuit will be enough to prevent trouble for normal application. In case of an incorrect action (diode reverse recovery current flowing for 1 μs or more), add an external filter circuit (R, C low pass filter, etc.).



3. Power save circuit

This IC enters the power save condition to decrease the current dissipation in the stop mode. In this condition, the bias current of most of circuits is cut off. Even in the power save condition, the 5 V regulator output (VREG) is given. If the bias current of Hall device is to be cut, 5V and Hall device may be connected via PNP Tr as a means to meet such needs.



4. Compatibility with various power supplies

To operate this IC with external 5V power supply (4.5 – 5.5 V), short-circuit $V_{CC}1$ and VREG pin for connection to power supply.

To operate this IC with external 12 V power supply (8 – 13.5 V), connect power supply to $V_{CC}1$ (5 V is generated at the VREG pin to function as a power supply to the control circuit).

To operate this IC with external 15 V power supply (13.5 – 19 V), connect power supply to $V_{CC}3$ and short-circuit 12REG and $V_{CC}1$ pins (12 V is generated at the 12REG pin to function as a power supply to $V_{CC}1$).

Connect the $V_{CC}2$ pin basically to the VREG pin. In an application in which the motor rotation speed is to be determined by the external fixed voltage (resistor division, etc.), set $V_{CC}2$ to 12 V (by connecting to $V_{CC}1$) to suppress variation of the output duty. (Variation of IC is difficult to affect adversely because of increase in the PWM oscillation amplitude and in the comparator dynamic range.)

5. PWM frequency

PWM frequency is determined from the capacity C (F) of capacitor connected to the PWM pin.

$$fPWM \fallingdotseq 1/(45000 \times C)$$

Connection of a 1000 pF capacitor causes oscillation of about 22 kHz. Excessively low PWM frequency causes causes a switching sound from the motor while excessively high PWM frequency causes increase in the power loss at the output. About 15 – 50 kHz is recommended. Capacitor GND should be arranged near the IC GND pin as much as possible to protect from the effect of output noise.

6. Drive method

The output duty can be controlled according to any of following methods.

- Control with the V_{CTL} pin voltage

  For the control voltage, refer to the electric characteristics. For control with the VCTL pin, set the PWMIN pin voltage to the L level.

- Control with the voltage applied to the TOC pin

  The TOC pin voltage and PWM oscillation waveform are compared to determine the output duty. The output duty becomes 0 % when the TOC pin voltage exceeds V_{OH} (PWM) (3.0 Vtyp) and 100% when it becomes lower than the V_{OL} (PWM) (1.2 Vtyp). For control with the TOC pin, set the PWMIN pin voltage to the L level.

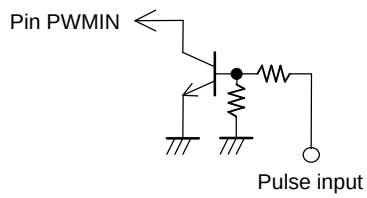
  For control with the input level other than the internal CTL amp control input level, external connection of amp allows setting to the arbitrary input level (with the external amp output connected to the TOC pin). For control from the TOC pin, fix the V_{CTL} pin voltage.

  For an application in which the regulated voltage is applied to the TOC pin through resistor division, etc., it is necessary to take into account the effect of resistor (about 20 kΩ) incorporated between the TOC pin and CTL amp output. (Variation about ±20%, temperature characteristics about +0.3%/°C). If the noise is included in the voltage to be applied to the TOC pin, chattering may occur in the output. In this case, stabilization with a capacitor is necessary.

- Pulse control with the PWMIN pin

  The output can be controlled on the basis of duty obtained by entering the pulse in the PWMIN pin. The output can be turned ON when the L-level input voltage is applied to the PWM pin and OFF when the H-level input voltage is applied. With the PWMIN pin open, the output becomes the H level and is turned OFF. If input with reversed logic is necessary, addition of external Tr (NPN) may be enough.

  For control with the PWMIN pin, set the V_{CTL} pin voltage that is more than the $V_{CTL}2$ voltage (output duty set to 100%) or connect the TOC pin to GND.



7. Hall input signal

The Hall input requires the signal input with an amplitude exceeding the hysteresis width (50 mV max). Considering the effect of noise and phase displacement, the input with the amplitude of 120 mV or more is recommended.

When the noise causes disturbance in the output waveform (at a time of phase change) or HP output (Hall signal three-phase synthesis output), insert a capacitor to the input to prevent such trouble. The Hall input is used as a signal to determine the input to the restriction protection circuit and the protection circuit during reverse. Though noise is ignored to a certain degree, due attention must be paid when using these protection circuits.

When all three phases of Hall input signal are entered, the output is turned OFF entirely (all of UL, VL, WL, UH, VH, and WH OFF).

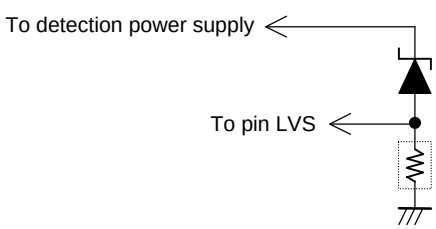
To enter the Hall IC output, fix one side of input (+ or –) to the voltage within the common-mode input range for Hall device. This will allow input from 0 to $V_{CC}1$ for another single-side input.

8. Circuit for low-voltage protection

This circuit detects the voltage applied to the LVS pin. When this voltage drops below the operation voltage (see the electric characteristics), the one-side output (UH, VH, and WH) is turned OFF. To prevent repetition of output ON/OFF near the protection activation voltage, the hysteresis is provided. Accordingly, the output is not recovered unless the voltage rises by about 0.5 V above the activation voltage.

The protection activation voltage is for the 5V system detection level. The detection level can be raised by connecting the zenor diode in series to the LVS pin and by shifting the detection level. The LVS pin inrush current at a time of detection is about 65 μA. To stabilize rise of the zenor diode voltage, increase the diode current by inserting the resistor between the LVS pin and GND.

When the protection circuit is not used, apply a voltage on a level where the protection is not activated, instead of setting the LVS pin open (output OFF with the pin open).



9. Motor lock protection circuit

A motor lock protection circuit is incorporated for protection of IC and motor when the motor is locked. When the Hall input signal is not changed for a certain period with the motor driving, the one-side output (UH, VH, WH) is turned OFF. The time is set by means of a capacity of a capacitor connected to the CSD pin.

Set time (s) ≒ 154 × C (μF)

Addition of a 0.01 μF capacitor causes a protection time of about 1.54 seconds. (Drive is turned OFF when one cycle of Hall input signal is longer than this time period.) The time to be set must have a sufficient allowance so that the protection is not activated at a normal motor startup. Select the capacitor of 4700 pF or more. The protection circuit is not activated when braking. To cancel the restriction protection condition, one of following steps must be taken:

- Stop mode (10 μs or more)
- Maintaining the output duty 0% condition through input of VCTL or PWMIN for more than the period of tCSD × 2. (tCSD (s) ≒ 0.5 × C (μF).
  When the 0.01 μF capacitor is added, maintaining for about 10 ms or more is necessary.)
- Re-application of power supply

The CSD pin acts also as an initial reset pulse generation pin and causes reset of the logic circuit when connected with GND. Accordingly, the motor drive condition can not be obtained. When this pin is not to be used, a resistor of about 150 kΩ and a capacitor of about 4700 pF must be connected to GND in parallel. When the restriction protection circuit is not used, following functions are also invalid:

- Protection circuit for the reverse mode
- Overheat protection circuit

10. Protection circuit at reverse

This circuit becomes effective when the REVSEL pin is set to the L level. When this protection is not necessary, either connect it to the VREG pin or keep it open.

When this circuit is effective, all outputs are OFF (all of UL, VL, WL, UH, VH, and WH OFF) when the drive is OFF (output duty 0%). If the condition is switched rapidly from the output drive condition to the drive OFF condition, the current flowing through the motor is returned to the power supply (the coil current flows through output upper and lower diodes to power supply). If this current causes a trouble, such as rise of the supply voltage, etc., it is necessary to reduce the duty in steps, instead of shutting of the drive suddenly.

Reverse condition is detected according to the input sequence of Hall signals (IN1, IN2, and IN3). When using this protection circuit, it is necessary to connect the Hall device with motor while considering the Hall input sequence. (See the three-phase logic truth table.) Reversing is judged when the Hall input is reversed by more than 120 degrees in the electrical angle. The drive is not shut OFF immediately after judgment of reverse, but the drive is continued for a certain period (equal to the motor lock protection set time) after drive start. If the reversing condition continues for a certain period (equal to the set time of motor lock protection), the drive is shut OFF (all OFF).

When the motor is reversing before it is driven, the drive is continued for a certain period (equal to the set time of motor lock protection). If the motor does not return to forward rotation within this period, the drive is shut OFF (all OFF).

To cancel the protection, one of following steps must be taken:

- Stop mode (10 μs or more)
- Maintaining the output duty 0% condition through input of V_{CTL} or PWMIN for more than the period of tCSD × 2. (tCSD(s) ≒ 0.5 × C (μF). When the 0.01 μF capacitor is added, maintaining for about 10 ms or more is necessary.)
- Re-application of power supply

11. Overheat protection circuit

One-side output (UH, VH,WH) is turned OFF when the junction temperature (Tj) exceeds a specified temperature (TSD). Since the minimum variation of TSD is 125°C, thermal design must be made so that Tj = 125°C is not exceeded except in the case of abnormality. Accordingly, Pdmax when Tj(max) = 125°C is 0.72 W (Ta = 25°C).

When the motor lock protection is not to be used by inserting in parallel the resistor of about 150kΩ and capacitor of about 4700pF between the CSD pin and GND, this overheat protection circuit does not function.

In this case, Tj(max) = 150°C, so that Pdmax = 0.9W (Ta = 25°C)

12. Forward/reverse rotation

To select forward or reverse in the rotation condition, a measure is taken to prevent flow of the through current (through current due to the output Tr OFF delay time at selection) at the output. Selection during rotation causes the current exceeding the current limit value to flow through the output Tr because of the motor coil resistance and motor reverse electromotive voltage condition. It is therefore necessary to select the external output Tr that is not damaged by this current or to select forward/reverse only when the motor rotation speed has decreased to a certain level.

13. Brake operation

Braking is made by setting the BR pin to the L level. Braking consists of a short-circuit brake condition in which all of one-side outputs (UH, VH, or WH) are turned ON while other outputs (UL, VL, WL) are turned OFF. A measure is taken to prevent flow of through current (through current due to output Tr OFF delay time at selection) when the brake is operated or cancelled. While braking is made, current limiting and motor lock protection circuits are not operative.

Short-circuit braking causes large current to flow through the output Tr because of motor coil resistance and the motor reverse electromotive voltage condition during operation. It is therefore necessary to select the external output Tr that is not damaged by this current or to activate braking only when the motor rotation speed has decreased to a certain level.

14. Power supply stabilization

This IC is of a switching drive type and the power line tends to be affected. It is therefore necessary to connect a capacitor of sufficient capacity for stabilization between the $V_{CC}1$ pin and GND.

To insert a diode in the power line to prevent breakdown through reverse connection of power supply, the power line becomes more readily affected. It is necessary to select a larger capacity.

To turn ON/OFF the power supply with a switch, etc., large distance between the switch and capacitor causes substantial deviation of the supply voltage due to the line inductance and inrush current into the capacitor. In certain cases, the withstand voltage may be exceeded. In this case, do not use a ceramic capacitor whose series impedance is low. Instead, use an electrolytic capacitor to suppress the inrush current and to prevent voltage rise.

15. VREG stabilization

To stabilize the VREG voltage that is the power supply for the control circuit, connect a 0.1μF or more capacitor between VREG and GND. The capacitor GND must be wired near the GND pin of IC as much as possible.

16. FG amplifier

Considering connection of the Hall device output, etc., the FG amplifier input does not incorporate the bias voltage. To enter pattern FG, etc., it is necessary to apply the bias voltage to the FGIN+ pin (by applying the $V_{REG}/2$ voltage determined through division with resistor from VREG, etc.).

There are a Schmidt comparator and filter circuit after the FG amplifier output, so that the noise is not readily included in the FGS output. FGOUT and FGS have the same logic.