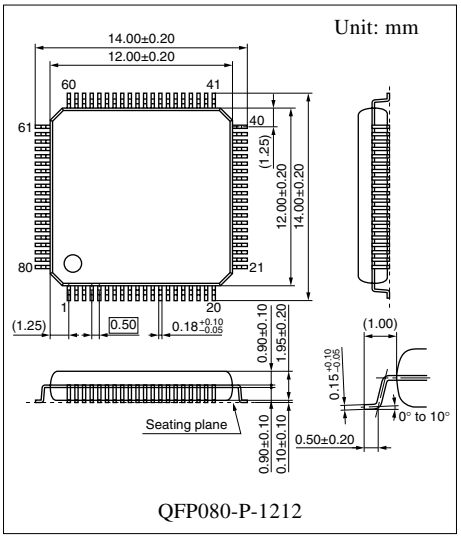
AN2101FH

Single chip, analog signal processor IC for CCD camera

■ Overview

The AN2101FH is a single chip IC optimal to process the video signal of a CCD camera, incorporating a luminance signal processor and an encoder. With built-in DACs (8-bit: 18-ch) for adjustment, various adjustments and controls are done with serial data.



QFP080-P-1212

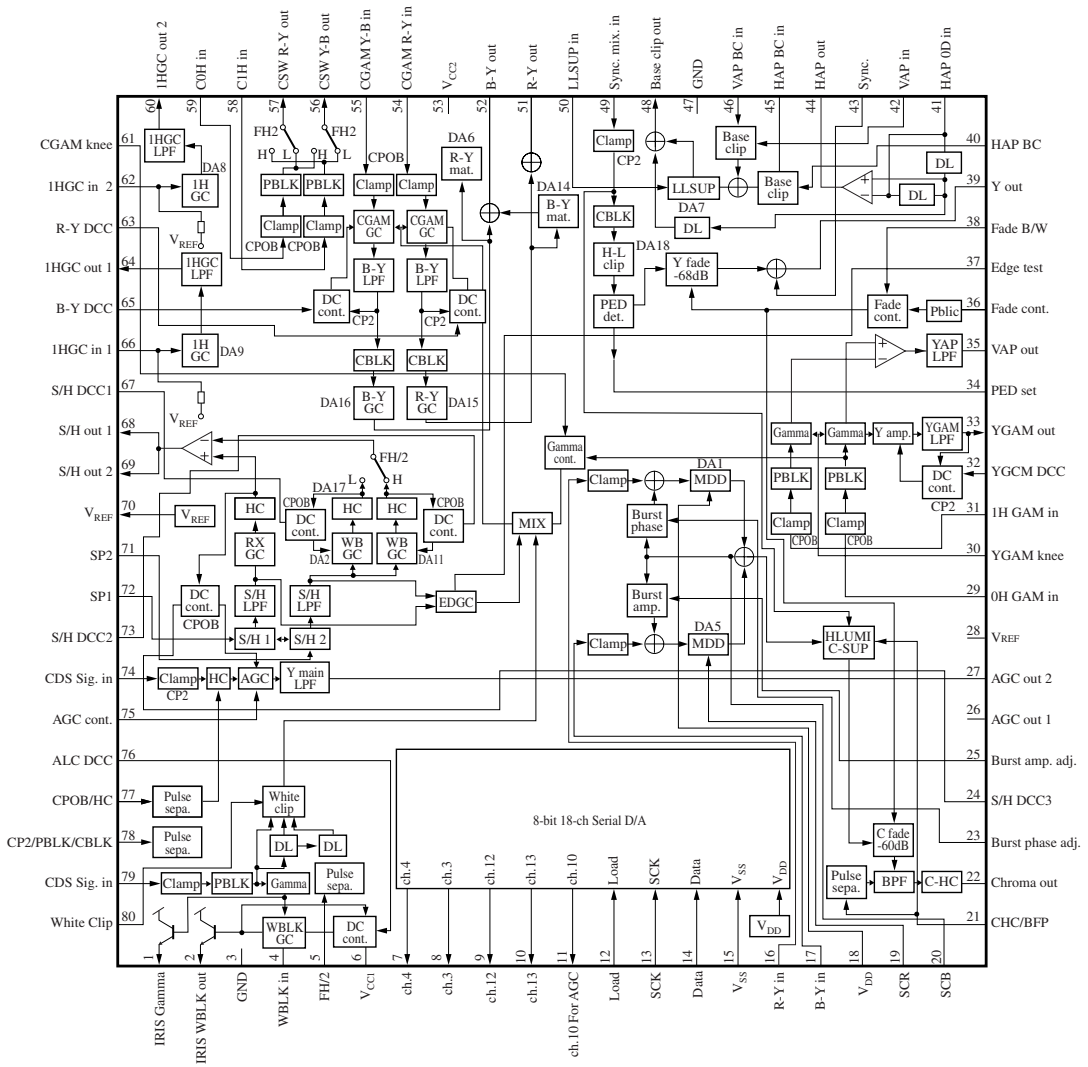
■ Features

- For 510H (250 000 pixels) CCD
- Applicable for both NTSC and PAL
- Y-LPF built in
- Adjustment-use DAC (8-bit: 18-ch) built in
- Iris γ built in

■ Applications

- A variety of CCD cameras such as video camera, surveillance camera, board camera, TV phone, TV conference system, input camera for PC, etc.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	IRIS GAM out	10	DAC output ch.1
2	IRIS WBLK out	11	DAC output ch.12
3	GND1	12	Load input
4	WBLK input	13	SCK input
5	FH/2 input	14	Data input
6	V_{CC1}	15	V_{SS}
7	DAC output ch.4	16	R-Y in
8	DAC output ch.3	17	B-Y in
9	DAC output ch.2	18	V_{DD}

■ Pin Descriptions (continued)

Pin No.	Description	Pin No.	Description
19	SCR	50	Luminance signal detection input (LLSUP)
20	SCB	51	R-Y out
21	BFP input/high colorfulness chroma clip setting	52	B-Y out
22	Chroma output	53	V_{CC2}
23	Burst phase setting	54	CGAM R-Y in
24	S/H DC stabilizing capacitance 3	55	CGAM Y-B in
25	Burst amplitude setting	56	CSW Y-B out
26	AGC out 1	57	CSW R-Y out
27	AGC out 2	58	C1H in
28	V_{REF} in (direct connection to pin 70)	59	C0H in
29	Luminance 0H in	60	Delay signal amp. output 2
30	Luminance gamma knee	61	Color difference gamma Knee
31	Luminance 1H in	62	Delay signal amp. input 2
32	Luminance gamma DC stabilizing capacitance	63	R-Y DC stabilizing capacitance
33	Luminance gamma output	64	Delay signal amp. output 1
34	Pedestal setting	65	B-Y DC stabilizing capacitance
35	V aperture output	66	Delay signal amp. input 1
36	Fade setting	67	S/H DC stabilizing capacitance 1
37	Edge test	68	S/H WB output 1
38	Fade level setting	69	S/H WB output 2
39	Luminance signal output	70	V_{REF} output
40	H aperture coring setting	71	SP2 input
41	H aperture generating circuit	72	SP1 input
42	V aperture coring setting	73	S/H DC stabilizing capacitance 2
43	Sync. input	74	CDS signal in (main)
44	H aperture output	75	AGC control
45	H aperture coring input	76	ALC DC stabilizing capacitance
46	V aperture coring input	77	CPOB input/luminance high cut setting
47	GND 2	78	CP2 / PBLK / CBLK input
48	Luminance contour correction output	79	CDS signal in (ALC)
49	Luminance sync. Mix. in	80	Color difference white clip setting

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5.5	V
Supply current	I_{CC}	130	mA
Power dissipation *2	P_D	360	mW
Operating ambient temperature *1	T_{opr}	−20 to +70	°C
Storage temperature *1	T_{stg}	−55 to +125	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
*2: The power dissipation shown is the value for T_a = 70°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	4.3 to 5.1	V

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit current	I_{TOT}	V_{CC} = 4.4 V	66	90	114	mA
Reference voltage 1	V_{REF}	V_{CC} = 4.4 V	1.50	1.60	1.70	V
Reference voltage 2	V_{DD}	V_{CC} = 4.4 V	3.30	3.40	3.50	V
Pulse separation CPOB	V_{CPOB}	V_{CC} = 4.4 V	2.90	3.20	3.50	V
Pulse separation PBLK	V_{PBLK}	V_{CC} = 4.4 V	1.45	1.75	2.05	V
Pulse separation CP2	V_{CP2}	V_{CC} = 4.4 V	2.60	2.80	3.10	V
Pulse separation CBLK	V_{CBLK}	V_{CC} = 4.4 V	0.75	1.05	1.35	V
Pulse separation FH/2	V_{FH2}	V_{CC} = 4.4 V	1.00	1.30	1.60	V
Pulse separation Sync.	V_{SYNC}	V_{CC} = 4.4 V	0.80	1.10	1.40	V
Pulse separation BFP	V_{BEP}	V_{CC} = 4.4 V	3.10	3.40	3.70	V
Pulse separation SP1	V_{SP1}	V_{CC} = 4.4 V	0.20	0.50	0.80	V
Pulse separation SP2	V_{SP2}	V_{CC} = 4.4 V	0.20	0.50	0.80	V
AGC maximum gain	G_{AG1}	V_{74} = 10 stair step, 50 mV[p-p]	21.5	23.5	27.5	dB
AGC minimum gain	G_{AG2}	V_{74} = 10 stair step, 1 200 mV[p-p]	−4.5	−2.0	0.5	dB
WB characteristics 1	V_{SH2}	V_{74} = sine wave 500 kHz, 500 mV[p-p]	270	400	530	mV[p-p]
WB characteristics 2	V_{SH7}	V_{74} = sine wave 500 kHz, 500 mV[p-p]	270	400	530	mV[p-p]
S/H characteristics 1	V_{SH9}	V_{74} = square wave 500 kHz, 1V[p-p]	430	630	830	mV[p-p]
S/H characteristics 2	V_{SH10}	V_{74} = square wave 500 kHz, 1V[p-p]	510	710	910	mV[p-p]
WB FH 2-step adjustment	V_{SHF}	V_{74} = C − GND	−6	0	6	mV[p-p]
Iris GC characteristic	V_{IR2}	V_{79} = 10 stair step, 1 200 mV[p-p]	580	780	980	mV[p-p]
Iris gate step	V_{WG}	V_{79} = C − GND	−20	0	20	mV[p-p]
Iris gamma 1	V_{IG1}	V_{79} = 10 stair step, 1 500 mV[p-p]	320	420	520	mV[p-p]
Iris gamma 2	G_{IG2}	V_{79} = 10 stair step, 1 500 mV[p-p]	2.0	3.5	5.0	dB

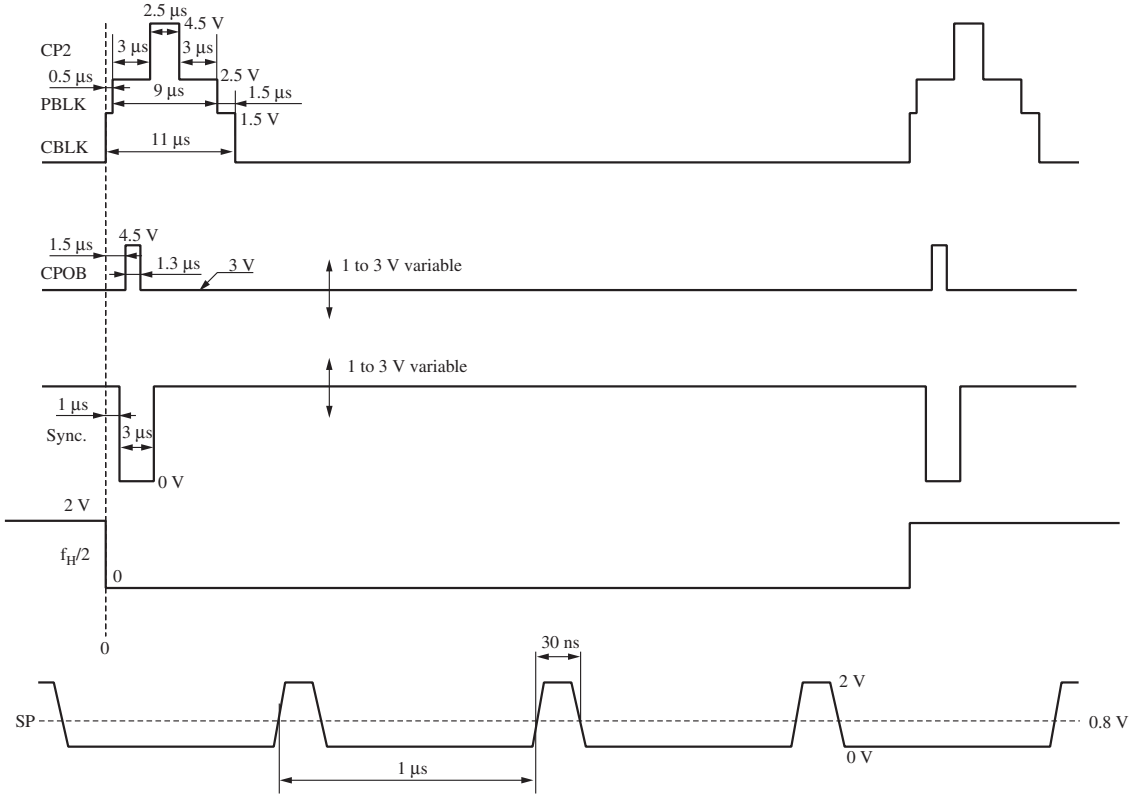
■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Iris gamma 3	G_{IG3}	V_{79} = 10 stair step, 1 500 mV[p-p]	4.0	5.5	—	dB
Iris BLK step difference	V_{WB}	V_{79} = C − GND	−20	0	20	mV[p-p]
Delay signal amp gain 1	G_{1H2}	V_{66} = sine wave, 500 kHz, 500 mV[p-p]	6.5	8.5	—	dB
Delay signal amp gain 2	G_{1H5}	V_{62} = sine wave, 500 kHz, 500 mV[p-p]	6.5	8.5	—	dB
Luminance gamma characteristic 1	V_{YG1}	V_{29} = 10 stair step, 700 mV[p-p]	450	550	650	mV[p-p]
Luminance gamma characteristic 2	G_{YG2}	V_{29} = 10 stair step, 700 mV[p-p]	−13	−11	−9	dB
Luminance gamma characteristic 3	G_{YG3}	V_{29} = 10 stair step, 1 500 mV[p-p]	2.0	4.0	6.0	dB
Luminance gamma BLK stage	V_{YGB}	V_{29} = C − GND	−20	0	20	mV[p-p]
V aperture gain	V_{VA1}	V_{31} = sine wave, 500 kHz, 300 mV[p-p]	−1 350	−1 150	−950	mV[p-p]
V aperture BLK step difference	V_{VAB}	V_{29} = V_{31} = C − GND	−20	0	20	mV[p-p]
After this, at V_{CC} = 5 V						
H aperture gain	V_{HA1}	V_{49} = sine wave, 4 MHz, 300 mV[p-p]	1 500	1 800	2 100	mV[p-p]
H aperture base clip	V_{HB2}	V_{45} = sine wave, 500 kHz, 100 mV[p-p]	0	30	60	mV[p-p]
V aperture base clip	V_{VB2}	V_{46} = sine wave, 500 kHz, 100 mV[p-p]	0	30	60	mV[p-p]
Luminance output amp gain	G_{Y1}	V_{49} = 10 stair step, 600 mV[p-p]	−1.5	0	1.5	dB
Luminance high clip level adjustment	V_{YH}	V_{49} = 10 stair step, 1V[p-p]	780	800	820	mV[p-p]
Luminance low clip level	V_{YL}	V_{49} = 10 stair step, −200 mV[p-p]	−40	−20	0	mV[p-p]
Synchronous signal output level	V_{YS}	V_{49} = C − GND	263	290	317	mV[p-p]
Pedestal control characteristic 1	V_{YP1}	V_{49} = C − GND	40	65	90	mV[p-p]
Pedestal control characteristic 2	V_{YP2}	V_{49} = C − GND	−30	−15	0	mV[p-p]
Luminance fade characteristic	G_{YFB}	V_{49} = 10 stair step, 600 mV[p-p]	—	−40	−26	dB
CSW(R-Y) gain	G_{CS1}	V_{58} = V_{59} = 10 stair step, 600 mV[p-p]	−1.5	0	1.5	dB
CSW(B-Y) gain	G_{CS2}	V_{58} = V_{59} = 10 stair step, 600 mV[p-p]	−1.5	0	1.5	dB
CSW(R-Y) BLK step difference	V_{CSB1}	V_{58} = V_{59} = C − GND	−20	0	20	mV[p-p]
CSW(B-Y) BLK step difference	V_{CSB2}	V_{58} = V_{59} = C − GND	−20	0	20	mV[p-p]
CSW(R-Y) BFH2 step difference	V_{CSF1}	V_{58} = V_{59} = C − GND	−20	0	20	mV[p-p]
CSW(B-Y) BFH2 step difference	V_{CSF2}	V_{58} = V_{59} = C − GND	−20	0	20	mV[p-p]
Color difference gamma characteristic 1	V_{CG1}	V_{29} = 10 stair step, 700 mV[p-p] V_{54} = 10 stair step, 350 mV[p-p]	170	230	290	mV[p-p]
Color difference gamma characteristic 2	G_{CG2}	V_{29} = 10 stair step, 700 mV[p-p] V_{54} = 10 stair step, 350 mV[p-p]	−12.5	−10.5	−8.5	dB
Color difference gamma characteristic 3	G_{CG3}	V_{29} = 10 stair step, 1 500 mV[p-p] V_{54} = 10 stair step, 750 mV[p-p]	1.0	2.5	4.0	dB
Color difference gamma characteristic 4	V_{CG4}	V_{29} = 10 stair step, 700 mV[p-p] V_5 = 10 stair step, 350 mV[p-p]	170	230	290	mV[p-p]
Color difference gamma characteristic 5	G_{CG5}	V_{29} = 10 stair step, 700 mV[p-p] V_{55} = 10 stair step, 350 mV[p-p]	−12.5	−10.5	−8.5	dB
Color difference gamma characteristic 6	G_{CG6}	V_{29} = 10 stair step, 1 500 mV[p-p] V_{55} = 10 stair step, 750 mV[p-p]	1.0	2.5	4.0	dB

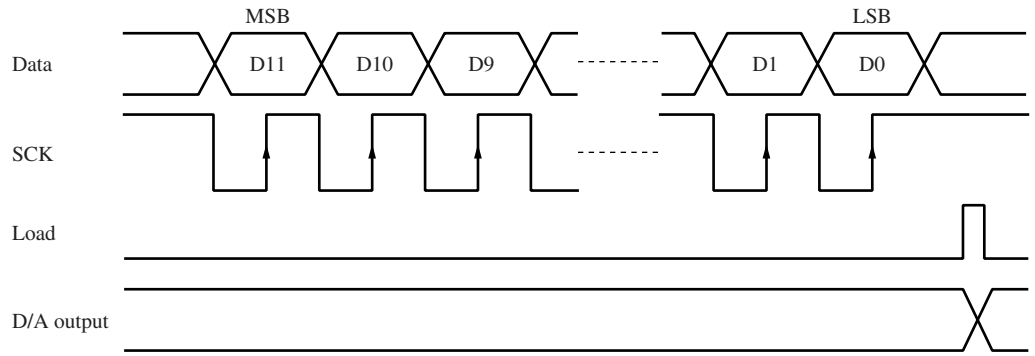
■ Electrical Characteristics at V_{CC} = 5 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
After this, at V_{CC} = 5 V (continued)						
Gamma control leak 1	V_{CGL1}	V_{29} = 10 stair step, 500 mV[p-p] V_{55} = C − GND	−70	0	70	mV[p-p]
Gamma control leak 2	V_{CGL2}	V_{29} = 10 stair step, 700 mV[p-p] V_{54} = C − GND	−70	0	70	mV[p-p]
R-Y gain characteristic	G_{CL1}	V_{54} = sine wave, 500 kHz, 200 mV[p-p]	9.5	11.5	13.5	dB
B-Y gain characteristic	G_{CL3}	V_{55} = sine wave, 500 kHz, 200 mV[p-p]	−1.5	0	1.5	dB
B-Y matrix characteristic	V_{CM1}	V_{54} = 10 stair step, 300 mV[p-p]	500	650	800	mV[p-p]
R-Y matrix characteristic	G_{CM2}	V_{55} = 10 stair step, 300 mV[p-p]	−2.0	0	2.0	dB
R-Y BLK step difference	V_{CB1}	V_{54} = C − GND	−20	0	20	mV[p-p]
B-Y BLK step difference	V_{CB2}	V_{54} = C − GND	−20	0	20	mV[p-p]
Burst level	V_{BU1}	V_{16} = white 200 mV[p-p] V_{17} = C − GND	260	300	325	mV[p-p]
Chroma output amplitude (R)	G_{CR1}	V_{16} = white 200 mV[p-p] V_{17} = C − GND	4.5	6.0	7.5	dB
Chroma output amplitude (B)	G_{CR3}	V_{16} = C − GND V_{17} = white 200 mV[p-p]	− 0.5	1.0	2.5	dB
Chroma high cut characteristic 1	G_{CH1}	V_{16} = white 400 mV[p-p] V_{17} = C − GND	7.0	8.5	10.0	dB
Chroma high cut characteristic 2	G_{CH2}	V_{16} = white 400 mV[p-p] V_{17} = C − GND	7.0	8.5	10.0	dB
Chroma fade characteristic	G_{CF}	V_{16} = white 200 mV[p-p] V_{17} = C − GND	—	−40	−20	dB
High luminance chroma suppress	G_{CS}	V_{16} = V_{49} = white 500 V[p-p] V_{17} = C − GND	—	−40	−20	dB
Chroma BPF gain	G_{BPF1}	V_{16} = sine wave, 4 MHz, 400 mV[p-p] V_{17} = C − GND	−4.5	−2.5	− 0.5	dB
Color difference edge suppress	G_{EDGE}	V_{54} = sine wave, 500kHz, 200 mV[p-p]	—	−40	−20	dB
Luminance LPF characteristic	—	V_{74} = sine wave, 4.77 MHz, 500 mV[p-p]	—	—	−15	dB
S/H LPF characteristic	—	V_{74} = sine wave, 3.5 MHz, 500 mV[p-p]	—	—	−15	dB
Luminance gamma LPF characteristic	—	V_{29} = sine wave, 4.77 MHz, 300 mV[p-p]	—	—	−15	dB
V aperture LPF characteristic	—	V_{31} = sine wave, 4.77 MHz, 300 mV[p-p]	—	—	−15	dB
Luminance white fade characteristic	—	V_{49} = C − GND	900	—	—	mV[p-p]
Color difference LPF characteristic	—	V_{54} = sine wave, 3.5 MHz, 200 mV[p-p]	—	—	−15	dB
DAC External output 1	V_7	Data 00 to FF	0.4	to	3.3	V
DAC External output 2	V_8	Data 00 to FF	0.4	to	3.3	V
DAC External output 3	V_9	Data 00 to FF	0.4	to	3.3	V
DAC External output 4	V_{10}	Data 00 to FF	0.4	to	3.3	V
DAC External output 5	V_{11}	Data 00 to FF	0.4	to	3.3	V

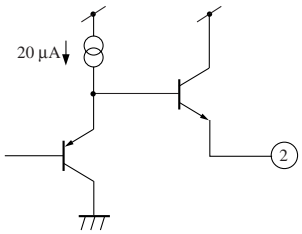
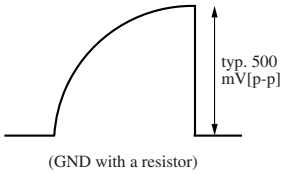
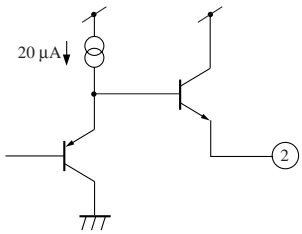
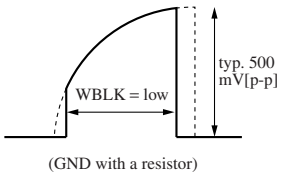
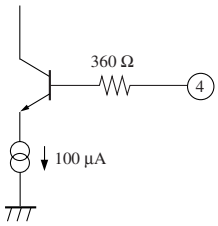
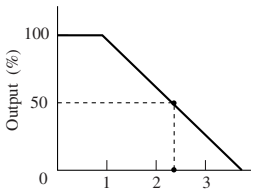
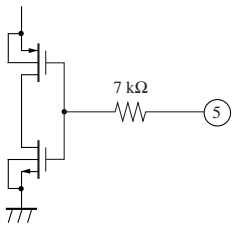
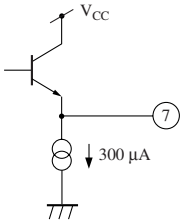
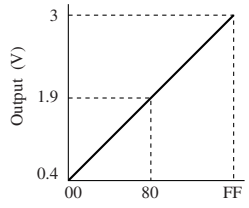
• Pulse timing chart



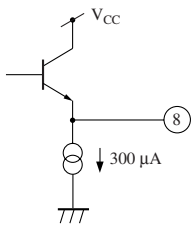
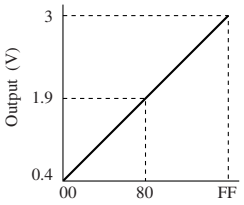
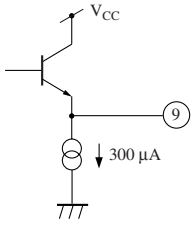
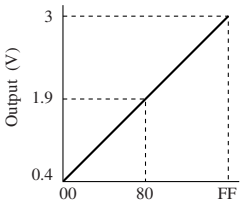
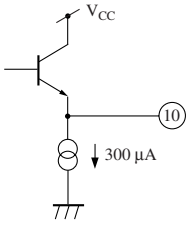
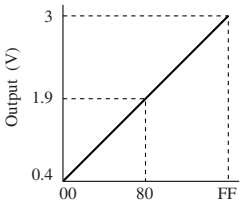
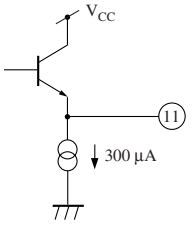
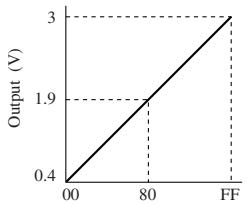
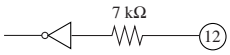
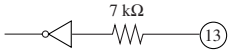
• DAC timing chart



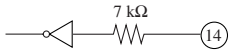
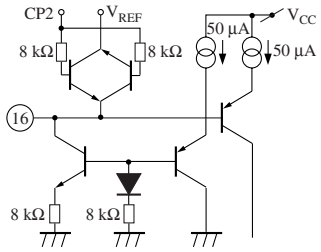
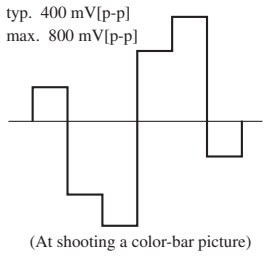
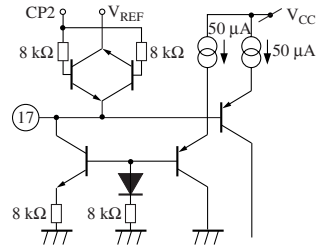
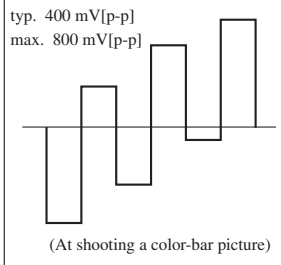
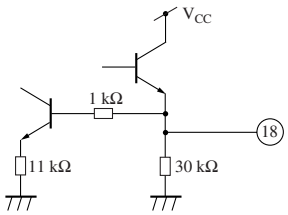
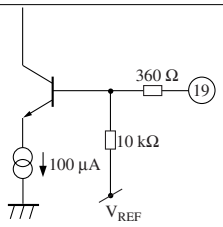
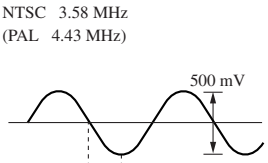
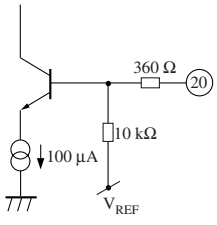
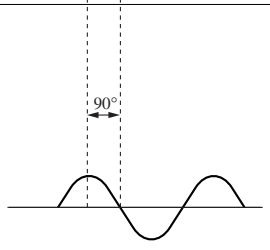
■ Terminal Equivalent Circuits

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
1	Iris γ output		• ALC γ Det. output • Output after BLK and γ-correction of the input signal from pin 79. • Output DC: 1.6 V	
2	Iris gate output		• ALC γ Det. gate output • After doing BLK and γ-correction on the signal inputted to pin 79, the gated signal with WBLK is outputted. • Output DC: 1.6 V	
3	GND	—	—	—
4	WBLK in		• Gate pulse input (gain control DC input) • Gates with pulse the input signal of pin 79 or controls with DC the gain of the input signal.	
5	FH/2 in		• FH/2 pulse input • Threshold voltage: 1.3 V	Refer to a timing chart
6	V_{CC1}	—	• typ. 4.5 V	DC
7	DA ch.4 output		• DA external output	

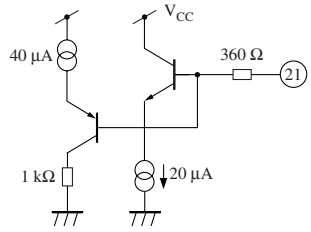
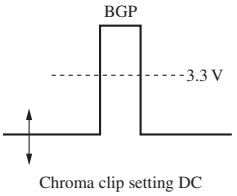
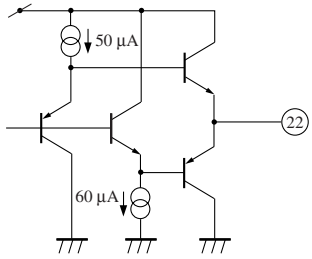
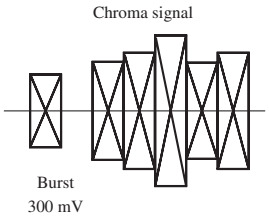
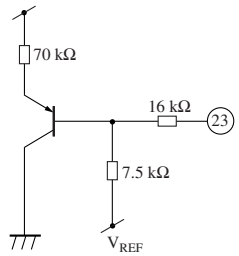
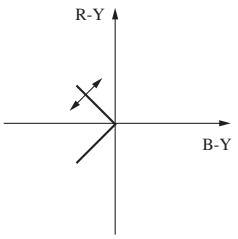
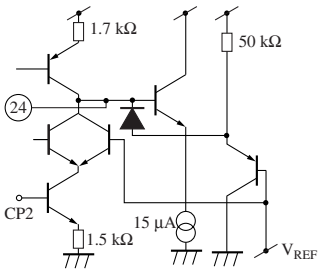
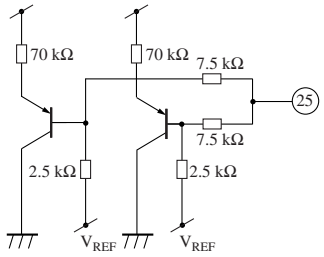
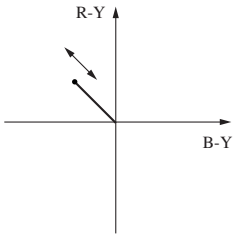
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
8	DA ch.3 output		• DA external output	
9	DA ch.2 output		• DA external output	
10	DA ch.1 output		• DA external output	
11	DA ch.12 output		• DA external output • GND for pin 77 in a test mode	 • Monitor DA7 to 16ch in a in a test mode
12	Load		• Serial data latch pulse input • Input impedance: 1 MΩ or more	Refer to a DAC timing chart
13	Clock		• Serial data shift clock input • Input impedance: 1 MΩ or more	Refer to a DAC timing chart

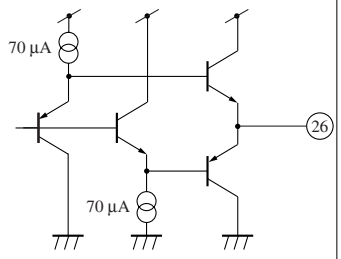
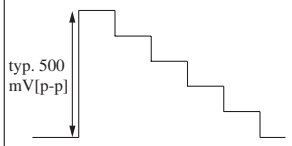
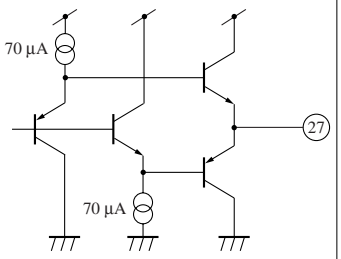
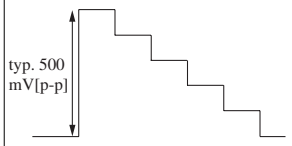
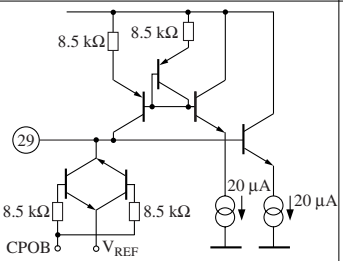
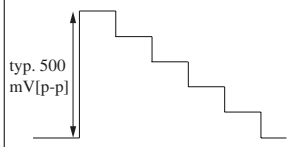
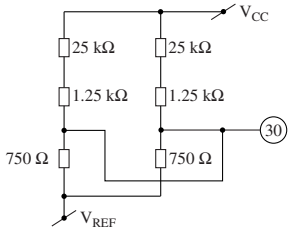
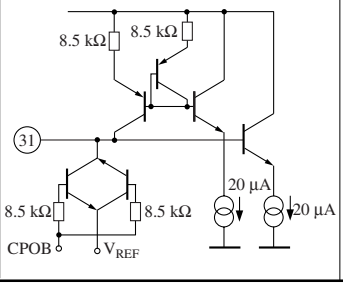
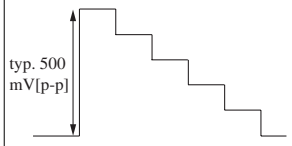
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
14	Data		• Data input for serial data shift • Input impedance: 1 MΩ or more	Refer to a DAC timing chart
15	V_{SS}	—	• GND	
16	R-Y in		• R-Y input (C coupling) • If R-Y color differential signal outputted from pin 51 is inputted, the signal is clamped to V_{REF} and modulated to chroma signal.	
17	B-Y in		• B-Y input (C coupling) • If B-Y color differential signal outputted from pin 52 is inputted, the signal is clamped to V_{REF} and modulated to chroma signal.	
18	V_{DD}		• Output DC: 3.4 V • To be used as a power source for an internal CMOS block including DACs, etc.	DC
19	SCR		• Rch sub carrier input • Modulates a color differential signal to a chroma signal, with a sub-carrier.	
20	SCB		• Bch sub carrier input • Modulates a color differential signal to a chroma signal, with a sub-carrier.	

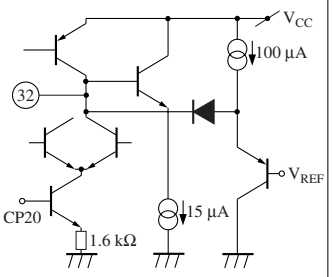
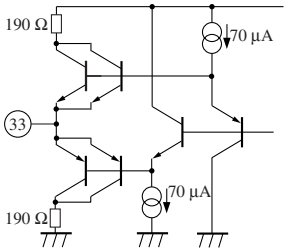
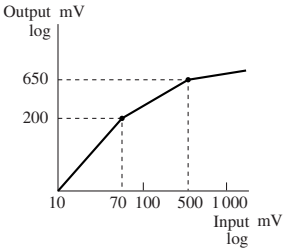
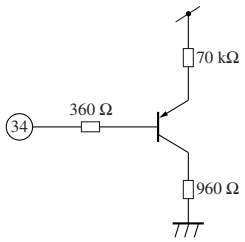
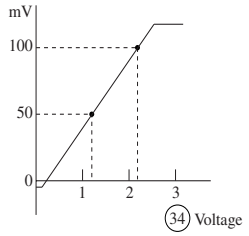
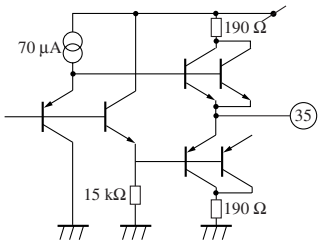
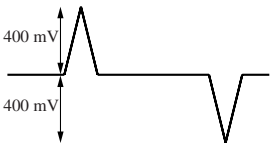
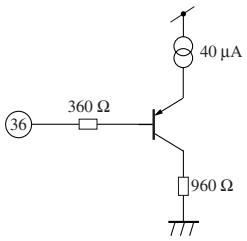
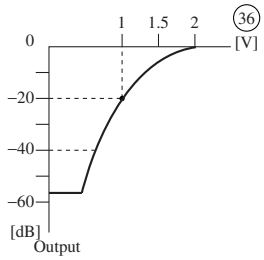
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
21	CHC/BFP		• Burst gate pulse input. Threshold: 3.3V • Its timing is of the burst signal timing. • Chroma clip setting input Sets a chroma suppress threshold for high luminance.	
22	C-out		• Chroma signal output • Output DC: 1.6 V • Output amplitude is clipped 2.5 times to a burst.	
23	Burst phase setting		• Burst phase setting NTSC; GND proximity PAL; V_{REF} proximity	
24	S/H DCC3		• DC control A.C. coupling	DC
25	Burst level setting		• Burst amplitude setting typ. V_{REF}	

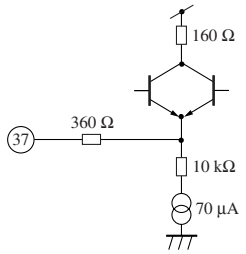
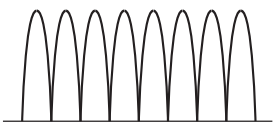
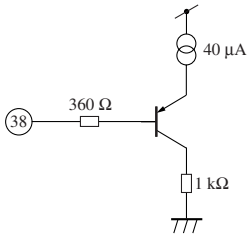
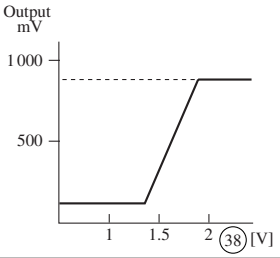
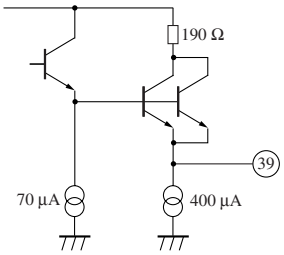
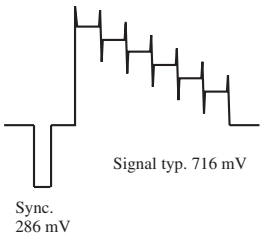
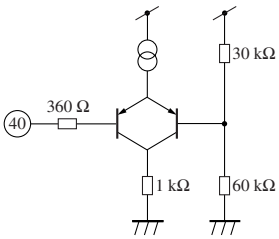
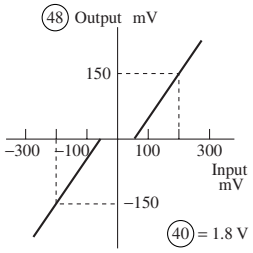
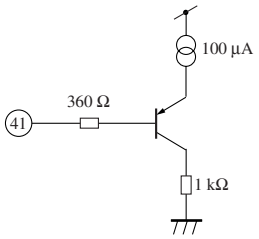
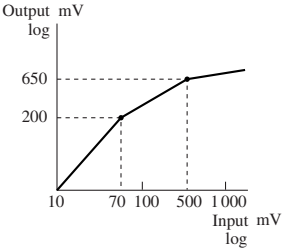
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
26	AGC out 1		• Luminance AGC output 1 Output DC: 1.6 V • Outputs, through AGC and LPF, a signal inputted to pin74. (Input to 1HCCD.)	 (At shooting a color-bar picture)
27	AGC out 2		• Luminance AGC output 2 Output DC: 1.6 V • Outputs, through AGC and LPF, a signal inputted to pin 74. (Input to pin 29.)	 (At shooting a color-bar picture)
28	V_{REF} input	—	• Connect to pin 70. • DC: 1.6 V	DC
29	0H GAM in		• Luminance signal (0H) input • Input the luminance signal outputted from pin 27.	 (At shooting a color-bar picture)
30	Yγ knee		• Luminance γ knee adjustment • Sets the knee point for luminance γ-correction typ. open	DC
31	1H GAN in		• Luminance signal (1H) input • Input, via 1HCCD, the luminance signal outputted from pin 26 after adjusting it to the same level as pin 27 output.	 (At shooting a color-bar picture)

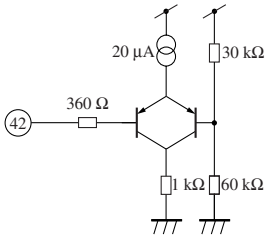
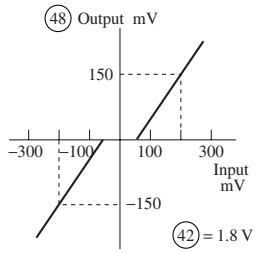
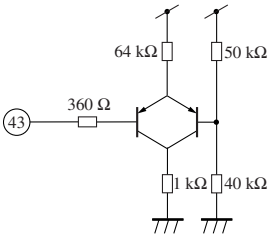
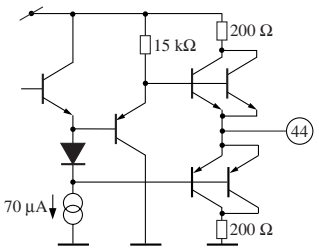
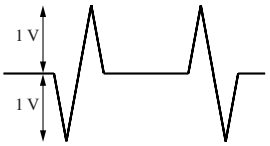
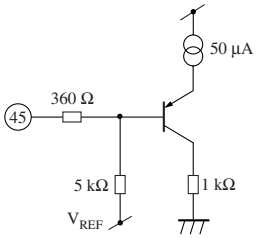
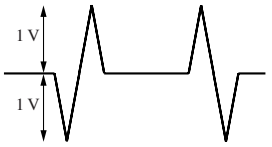
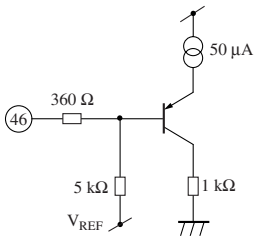
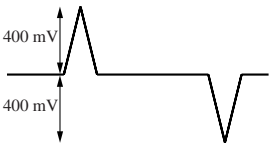
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
32	Y GAM DC		• DC control A.C. coupling • Clamps pin 33 output DC to V_{REF}.	DC
33	Y GAM out		• Luminance gamma output • γ correction on the luminance signal inputted to pin 29. Then clamps the output DC to V_{REF} and outputs it.	
34	PED set		• Pedestal level setting NTSC: Approx. 50 mV PAL: Approx. 0 mV	
35	VAP out		• Vertical contour correction signal output • Forms a vertical contour correction signal from the luminance signals of 0H and 1H inputted to pins 29 and pin 31, and outputs it.	
36	Fade cont.		• Fade control • Fading out (in) setting for the luminance and chroma signals.	

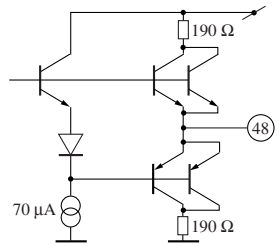
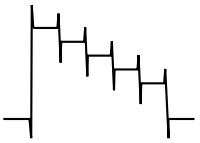
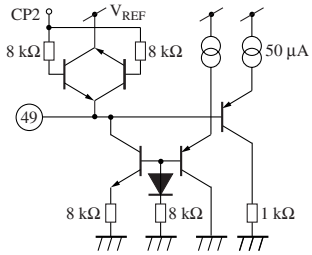
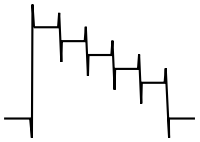
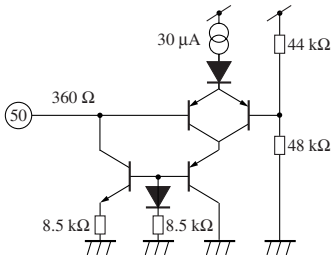
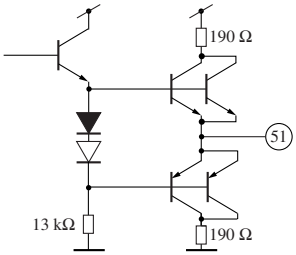
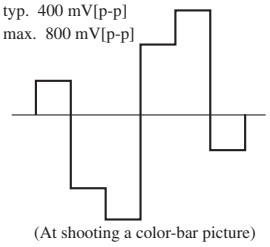
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
37	Edge test		• Edge signal detection • Output for testing	 1MHz edge-full-wave rectified voltage
38	Fade B/W		• Black and white fade changeover • Fade out level setting From black to white (0 mV[p-p] to 800 mV[p-p])	
39	Y out		• Luminance signal output • Outputs the luminance signal inputted to pin 49 after high clip, low clip, pedestal setting and sync. mix.	
40	HAP BC		• Horizontal contour correction noise rejection setting • Reduces the noise component of the horizontal contour correction signal inputted to pin 45.	
41	HAP 0D in		• Horizontal contour correction signal input • Input the luminance signal outputted from pin 33.	

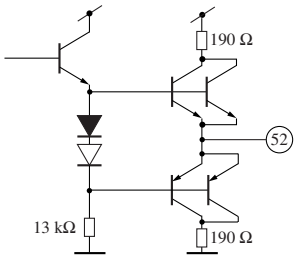
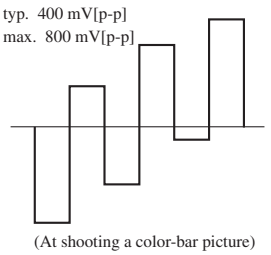
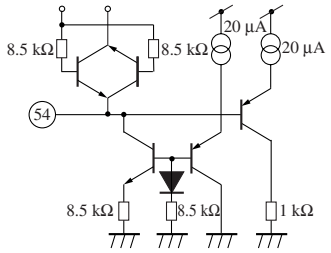
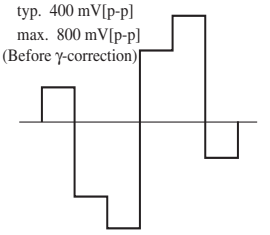
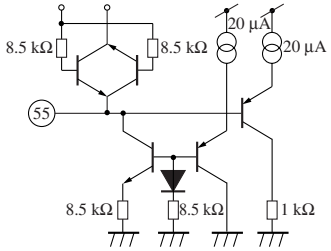
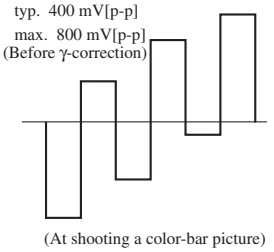
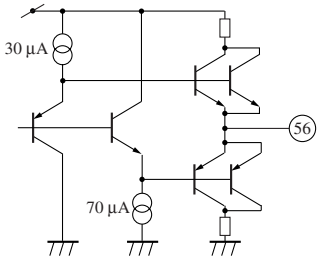
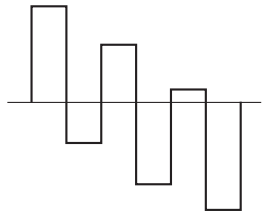
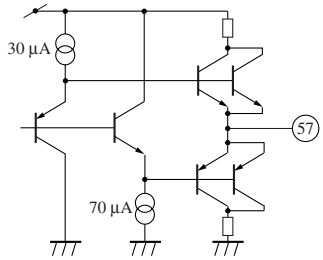
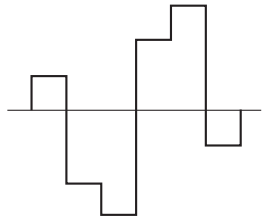
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
42	VAP BC		• Vertical contour correction noise rejection setting • To reduce the noise component of the vertical contour correction signal inputted to pin 46.	
43	Sync.		• Sync. pulse input threshold: 1.2 V	Refer to a timing chart
44	HAP out		• Horizontal contour correction signal output • Forms the horizontal contour correction signal from the luminance signal inputted to pin 41 and pin 42. Then, outputs it.	
45	HAP BC in		• Horizontal contour correction signal input • Input the horizontal contour correction signal outputted from pin 44.	
46	VAP BC in		• Vertical contour correction signal input • Input the vertical contour correction signal outputted from pin 35.	
47	GND	—	—	—

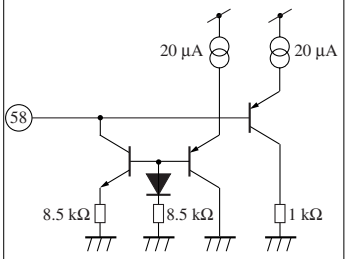
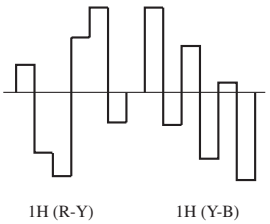
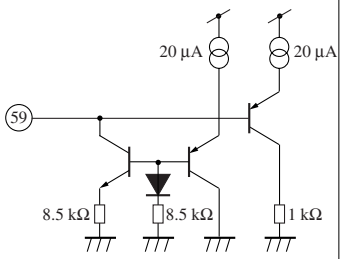
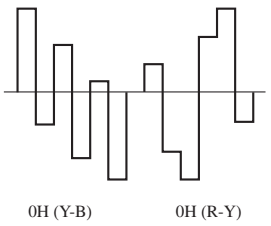
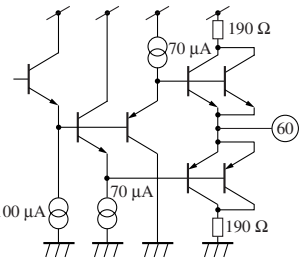
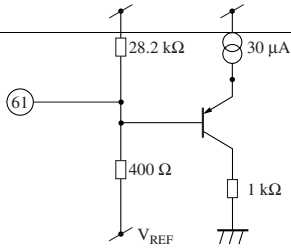
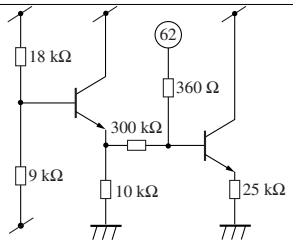
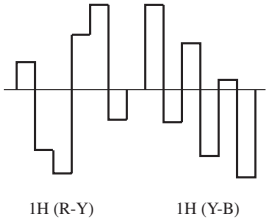
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
48	Base clip out		• Luminance output with a contour correction • Mixes the horizontal and vertical contour correction signals inputted to pin 45 and pin 46 with the noise-reduced luminance signal. Then output it.	
49	Sync. mix in		• Luminance sigunal input with a contour correction • Input the luminance signal outputted from pin 48.	
50	LLSUP in		• Luminance detection signal input • Input the DC which is made from integrating a luminance signal, so as to suppress the horizontal and vertical contour correction signals at a low luminance level.	
51	R-Y out		• Color difference (R-Y) output • The R-Y color difference signal inputted to pin 54 is outputted after γ-correction, LPF and color phase correction. • Input to pin 16.	

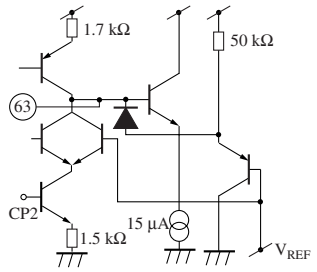
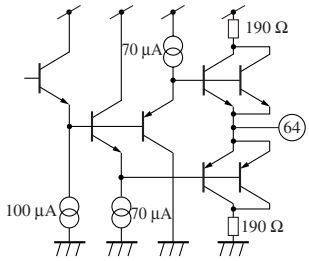
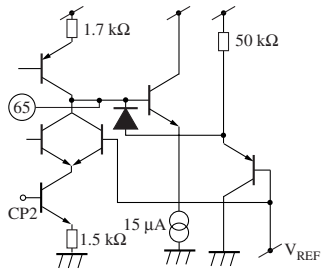
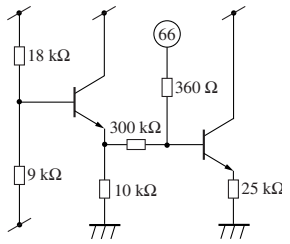
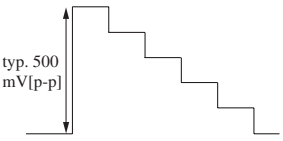
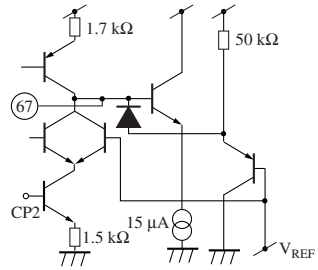
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
52	B-Y out		• Color difference (B-Y) output • The B-Y color difference signal inputted to pin 55 is outputted after γ-correction, LPF and color phase correction.	 (At shooting a color-bar picture)
53	V_{CC2}	—	• typ. 4.5 V	DC
54	CGAM R-Y in		• Color difference (R-Y) gamma input • Input the R-Y color difference signal outputted from pin 57.	 (At shooting a color-bar picture)
55	CGAM Y-B in		• Color difference (Y-B) gamma input • Input the Y-B color difference signal outputted from pin 56.	 (At shooting a color-bar picture)
56	CSW Y-B out		• Simultaneous output (Y-B) • Outputs the color difference line sequential signal inputted to pin 58 and pin 59 as a Y-B color difference signal by $f_H/2$ pulse.	
57	CSW R-Y out		• Simultaneous output (R-Y) • Outputs the color difference line sequential signal inputted to pin 58 and pin 59 as a R-Y color difference signal by $f_H/2$ pulse.	

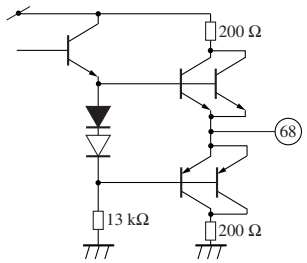
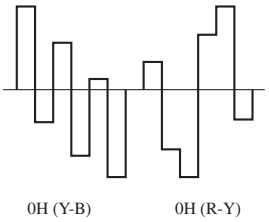
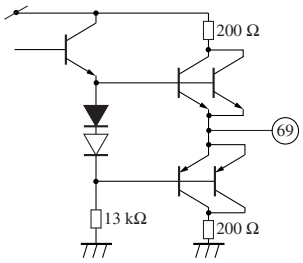
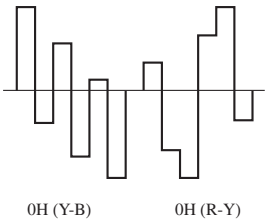
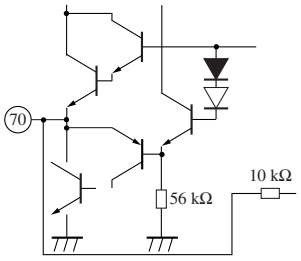
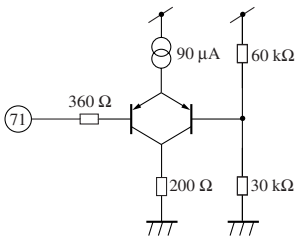
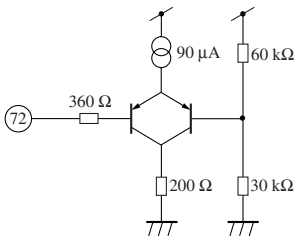
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
58	C1H in		• Simultaneous input (C1H) • Input the color difference line sequential signal from pin 60 after a 1HCCD gain adjustment.	
59	C0H in		• Simultaneous input (C0H) • Input the color difference line sequential signal outputted from pin 68.	
60	1HGC out 2		• CCD DL gain control output 2 • If the line sequential color differential signal outputted from pin 68 is inputted through a 1HCCD to pin 62, the same level signal as pin 69 output is outputted.	
61	C gamma knee		• Color difference γ -knee adjustment • Sets the knee point for color difference γ-correction. typ. open	DC
62	1HGC in 2		• CCD DL gain control input 2 • Input the color difference line sequential signal outputted from pin 68 via 1HCCD.	

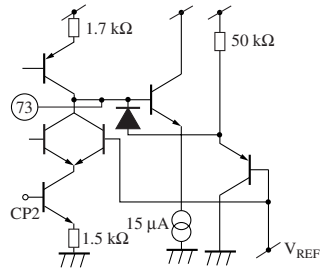
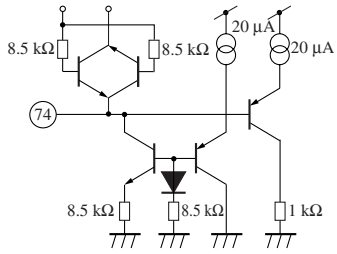
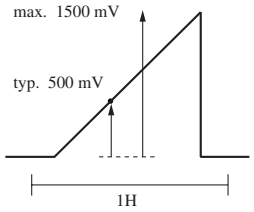
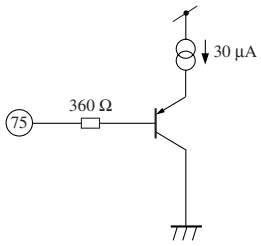
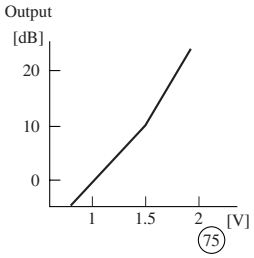
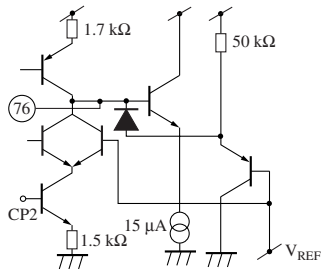
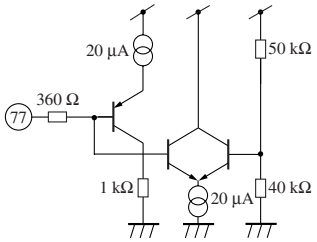
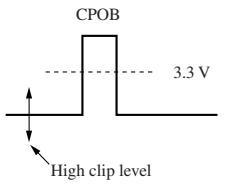
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
63	R-Y DCC		• DC control A.C. coupling • Clamps the R-Y color difference signal outputted from pin 51 to V_{REF} and then blanks it.	DC
64	1HGC out 1		• CCD DL gain control input 1 • If the luminance signal outputted from pin 27 is inputted through a 1H-CCD to pin 66, the same level signal as pin 26 is outputted.	Vertical aperture adjustment
65	B-Y DCC		• DC control A.C. coupling • Clamps the B-Y color difference signal outputted from pin 52 to V_{REF} and then blanks it.	DC
66	1HGC in 1		• CCD DL gain control output 1 • Input the luminance signal outputted from pin 27 via 1HCCD.	 (At shooting a color-bar picture)
67	S/H DCC1		• DC control A.C. coupling	DC

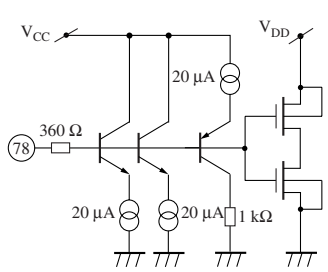
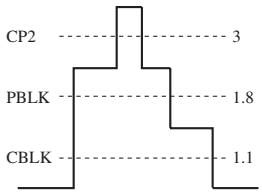
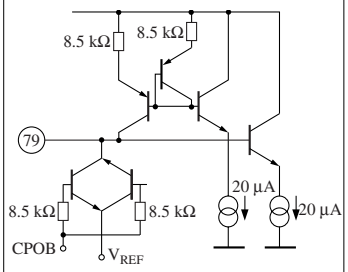
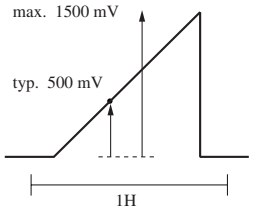
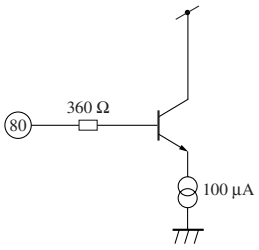
■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
68	S/H out 1		• S/H output 1 • Carries out the color separation and white balance for the CDS signal inputted to pin 74, then outputs it. • Input to 1HCCD.	
69	S/H out 2		• S/H output 2 • Outputs the same signal as pin 68 • Input it to pin 56	
70	V_{REF}		• V_{REF} (1.6 V) output • Impedance: Approx. 1 Ω • Input this voltage to pin 28.	DC
71	SP2		• Sampling pulse 2 input • Pulse threshold: 1 V	Refer to a pulse timing
72	SP1		• Sampling pulse 1 input • Pulse threshold: 1 V	Refer to a pulse timing

■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
73	S/H DCC2		• DC control A.C. coupling	DC
74	CDS S-G in 1		• CDS signal input 1 (AGC input) • Clamp input of CDS signal	
75	AGC cont.		• AGC control voltage input	
76	ALL DCC		• DC control A.C. coupling • Clamps ACC output to V_{REF} and gates it, then output it.	DC
77	CPOB/HC		• CPOB pulse input Threshold: 3.3 V • CDS input high clip: typ. about V_{REF} + 1.3 V	

■ Terminal Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent circuit	Description	Signal waveform
78	CP2/DBLK/ CBLK		• CP2 pulse input Threshold: 3 V • PBLK pulse input Threshold voltage: 1.8 V • CBLK pulse input Threshold voltage: 1.1 V	
79	CDS S-G in 2		• CDS signal input 2 (ALC input)	
80	White clip		• Color difference signal white clip DC setting • Sets the threshold voltage to clip the color difference signal at a high luminance level.	

■ Cautions on Use

- Keep pin 36 (fade-in) lower than 0.5 V that is for a fade mode.
- Note that pin 12DA external output becomes a test mode for DA output used inside, if pin 77 voltage is set to (0 V).
- Be cautious in use because pin 29 static surge breakdown voltage level is low as compared with other pins.

  Pin 29 breakdown level:

  C = 200PF +200 V

  –230 V to –240 V
- A power rise timing should be considered somewhere around 15 ms.

  If it differs much from it, it is likely to cause an abnormal operation.
- If you use this device without inputting a serial data, it is likely to cause an abnormal operation.

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