

### FEATURES

#### High Accuracy

- 0.02% Max Nonlinearity, 0 V to 2 V RMS Input
- 0.10% Additional Error to Crest Factor of 3

#### Wide Bandwidth

- 8 MHz at 2 V RMS Input
- 600 kHz at 100 mV RMS

#### Computes:

- True RMS
- Square
- Mean Square
- Absolute Value

#### dB Output (60 dB Range)

#### Chip Select/Power-Down Feature Allows:

- Analog "Three-State" Operation
- Quiescent Current Reduction from 2.2 mA to 350  $\mu$ A
- Side Brazed DIP, Low Cost Cerdip and SOIC

### PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms-to-dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms-to-dc converters and comparable to discrete and modular techniques in accuracy, bandwidth, and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600 kHz with inputs of 200 mV rms and up to 8 MHz when the input levels are above 1 V rms.

As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin, allowing direct dB measurement with a useful range of 60 dB. An externally programmed reference current allows the user to select the 0 dB reference voltage to correspond to any level between 0.1 V and 2.0 V rms.

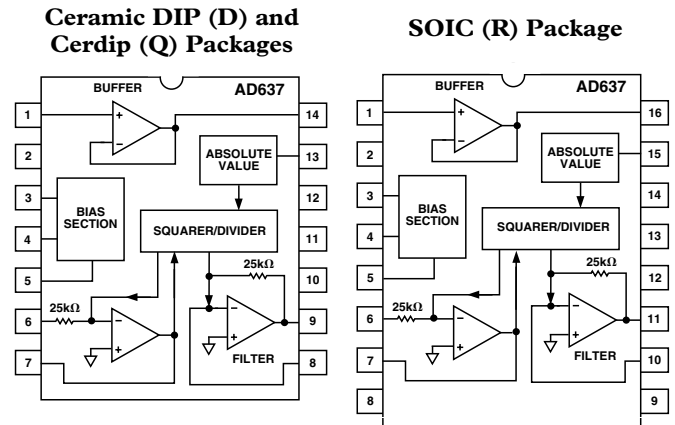
A chip select connection on the AD637 permits the user to decrease the supply current from 2.2 mA to 350  $\mu$ A during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wideband true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

### REV. F

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### FUNCTIONAL BLOCK DIAGRAMS



The AD637 is available in two accuracy grades (J and K) for commercial (0°C to 70°C) temperature range applications; two accuracy grades (A and B) for industrial (-40°C to +85°C) applications; and one (S) rated over the -55°C to +125°C temperature range. All versions are available in hermetically sealed, 14-lead side brazed ceramic DIPs as well as low cost cerdip packages. A 16-lead SOIC package is also available.

### PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean-square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor that sets the averaging time period. The value of this capacitor also determines low-frequency accuracy, ripple level, and settling time.
3. The chip select feature of the AD637 permits the user to power down the device during periods of nonuse, thereby decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used either as an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby increasing the accuracy of the measurement.

# AD637—SPECIFICATIONS (@ 25°C, and ±15 V dc unless otherwise noted.)

Model	AD637J/A			AD637K/B			AD637S			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION	$V_{OUT} = \sqrt{avg \times (V_{IN})^2}$			$V_{OUT} = \sqrt{avg \times (V_{IN})^2}$			$V_{OUT} = \sqrt{avg \times (V_{IN})^2}$			
CONVERSION ACCURACY										
Total Error, Internal Trim <sup>1</sup> (Fig. 2)	±1 ± 0.5			±0.5 ± 0.2			±1 ± 0.5			mV ± % of Reading
T <sub>MIN</sub> to T <sub>MAX</sub> vs. Supply, +V <sub>IN</sub> = +300 mV	30	150	±3.0 ± 0.6	30	150	±2.0 ± 0.3	30	150	±6 ± 0.7	mV ± % of Reading
vs. Supply, -V <sub>IN</sub> = -300 mV	100	300		100	300		100	300		μV/V
DC Reversal Error at 2 V	0.25			0.1			0.25			% of Reading
Nonlinearity 2 V Full Scale <sup>2</sup>	0.04			0.02			0.04			% of FSR
Nonlinearity 7 V Full Scale	0.05			0.05			0.05			% of FSR
Total Error, External Trim	±0.5 ± 0.1			±0.25 ± 0.05			±0.5 ± 0.1			mV ± % of Reading
ERROR VS. CREST FACTOR <sup>3</sup>	Specified Accuracy			Specified Accuracy			Specified Accuracy			
Crest Factor 1 to 2	±0.1			±0.1			±0.1			% of Reading
Crest Factor = 3	±1.0			±1.0			±1.0			% of Reading
Crest Factor = 10										
AVERAGING TIME CONSTANT	25			25			25			ms/μF C <sub>AV</sub>
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supply	0 to 7			0 to 7			0 to 7			V rms
Continuous RMS Level										V p-p
Peak Transient Input	±15			±15			±15			
Signal Range, ±5 V Supply	0 to 4			0 to 4			0 to 4			V rms
Continuous rms Level										V p-p
Peak Transient Input	±6			±6			±6			
Maximum Continuous Nondestructive Input Level (All Supply Voltages)	±15			±15			±15			V p-p
Input Resistance	6.4	8	9.6	6.4	8	9.6	6.4	8	9.6	kΩ
Input Offset Voltage	±0.5			±0.2			±0.5			mV
FREQUENCY RESPONSE <sup>4</sup>										
Bandwidth for 1% Additional Error (0.09 dB)										
V <sub>IN</sub> = 20 mV	11			11			11			kHz
V <sub>IN</sub> = 200 mV	66			66			66			kHz
V <sub>IN</sub> = 2 V	200			200			200			kHz
±3 dB Bandwidth										
V <sub>IN</sub> = 20 mV	150			150			150			kHz
V <sub>IN</sub> = 200 mV	1			1			1			MHz
V <sub>IN</sub> = 2 V	8			8			8			MHz
OUTPUT CHARACTERISTICS										
Offset Voltage vs. Temperature	±0.05 ±1 ±0.089			±0.04 ±0.5 ±0.056			±0.04 ±1 ±0.07			mV mV/°C
Voltage Swing, ±15 V Supply, 2 kΩ Load	0 to 12.0	13.5		0 to 12.0	13.5		0 to 12.0	13.5		V
Voltage Swing, ±3 V Supply, 2 kΩ Load	0 to 2	2.2		0 to 2	2.2		0 to 2	2.2		V
Output Current	6			6			6			mA
Short Circuit Current	20			20			20			mA
Resistance, Chip Select "High"	0.5			0.5			0.5			Ω
Resistance, Chip Select "Low"	100			100			100			kΩ
dB OUTPUT										
Error, V <sub>IN</sub> 7 mV to 7 V rms, 0 dB = 1 V rms	±0.5			±0.3			±0.5			dB
Scale Factor	-3			-3			-3			mV/dB
Scale Factor Temperature Coefficient	+0.33 -0.033			+0.33 -0.033			+0.33 -0.033			% of Reading/°C dB/°C
I <sub>REF</sub> for 0 dB = 1 V rms	5	20	80	5	20	80	5	20	80	μA
I <sub>REF</sub> Range	1 to 100			1 to 100			1 to 100			μA
BUFFER AMPLIFIER										
Input Output Voltage Range	-V <sub>S</sub> to (+V <sub>S</sub> - 2.5 V)			-V <sub>S</sub> to (+V <sub>S</sub> - 2.5 V)			-V <sub>S</sub> to (+V <sub>S</sub> - 2.5 V)			V
Input Offset Voltage	±0.8 ±2			±0.5 ±1			±0.8 ±2			mV
Input Current	±2 ±10			±2 ±5			±2 ±10			nA
Input Resistance	10 <sup>8</sup>			10 <sup>8</sup>			10 <sup>8</sup>			Ω
Output Current	(+5 mA, -130 μA)			(+5 mA, -130 μA)			(+5 mA, -130 μA)			mA
Short Circuit Current	20			20			20			mA
Small Signal Bandwidth	1			1			1			MHz
Slew Rate <sup>5</sup>	5			5			5			V/μs
DENOMINATOR INPUT										
Input Range	0 to 10			0 to 10			0 to 10			V
Input Resistance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage	±0.2 ±0.5			±0.2 ±0.5			±0.2 ±0.5			mV

Model	AD637J/A			AD637K/B			AD637S			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CHIP SELECT PROVISION (CS)										
RMS "ON" Level	Open or $2.4\text{ V} < V_C < +V_S$			Open or $2.4\text{ V} < V_C < +V_S$			Open or $2.4\text{ V} < V_C < +V_S$			
RMS "OFF" Level	$V_C < 0.2\text{ V}$			$V_C < 0.2\text{ V}$			$V_C < 0.2\text{ V}$			
$I_{OUT}$ of Chip Select	10			10			10			$\mu\text{A}$
CS "Low"	Zero			Zero			Zero			
CS "High"	Zero			Zero			Zero			
On Time Constant	$10\ \mu\text{s} + ((25\ \text{k}\Omega) \times C_{AV})$			$10\ \mu\text{s} + ((25\ \text{k}\Omega) \times C_{AV})$			$10\ \mu\text{s} + ((25\ \text{k}\Omega) \times C_{AV})$			
Off Time Constant	$10\ \mu\text{s} + ((25\ \text{k}\Omega) \times C_{AV})$			$10\ \mu\text{s} + ((25\ \text{k}\Omega) \times C_{AV})$			$10\ \mu\text{s} + ((25\ \text{k}\Omega) \times C_{AV})$			
POWER SUPPLY										
Operating Voltage Range	$\pm 3.0$			$\pm 3.0$			$\pm 3.0$			V
Quiescent Current	2.2			2.2			2.2			mA
Standby Current	350			350			350			$\mu\text{A}$
TRANSISTOR COUNT	107			107			107			

## NOTES

<sup>1</sup>Accuracy specified 0–7 V rms dc with AD637 connected as shown in Figure 2.

<sup>2</sup>Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10 mV and 2 V.

<sup>3</sup>Error vs. crest factor is specified as additional error for 1 V rms.

<sup>4</sup>Input voltages are expressed in volts rms. % are in % of reading.

<sup>5</sup>With external 2 k $\Omega$  pull-down resistor tied to  $-V_S$ .

Specifications shown in **bold** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

# AD637

## ABSOLUTE MAXIMUM RATINGS

ESD Rating	500 V
Supply Voltage	$\pm 18$ V dc
Internal Quiescent Power Dissipation	108 mW
Output Short Circuit Duration	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering 10 secs)	$300^{\circ}\text{C}$
Rated Operating Temperature Range	
AD637J, K	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
AD637A, B	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
AD637S, 5962-8963701CA	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD637AR	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	SOIC	R-16
AD637BR	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	SOIC	R-16
AD637AQ	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Cerdip	Q-14
AD637BQ	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Cerdip	Q-14
AD637JD	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Side Brazed Ceramic DIP	D-14
AD637JD/+	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Side Brazed Ceramic DIP	D-14
AD637KD	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Side Brazed Ceramic DIP	D-14
AD637KD/+	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Side Brazed Ceramic DIP	D-14
AD637JQ	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Cerdip	Q-14
AD637KQ	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Cerdip	Q-14
AD637JR	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	SOIC	R-16
AD637JR-REEL	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	SOIC	R-16
AD637JR-REEL7	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	SOIC	R-16
AD637KR	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	SOIC	R-16
AD637SD	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Side Brazed Ceramic DIP	D-14
AD637SD/883B	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Side Brazed Ceramic DIP	D-14
AD637SQ/883B	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Cerdip	Q-14
AD637SCHIPS	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Die	
5962-8963701CA*	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Cerdip	Q-14

\*A standard microcircuit drawing is available.

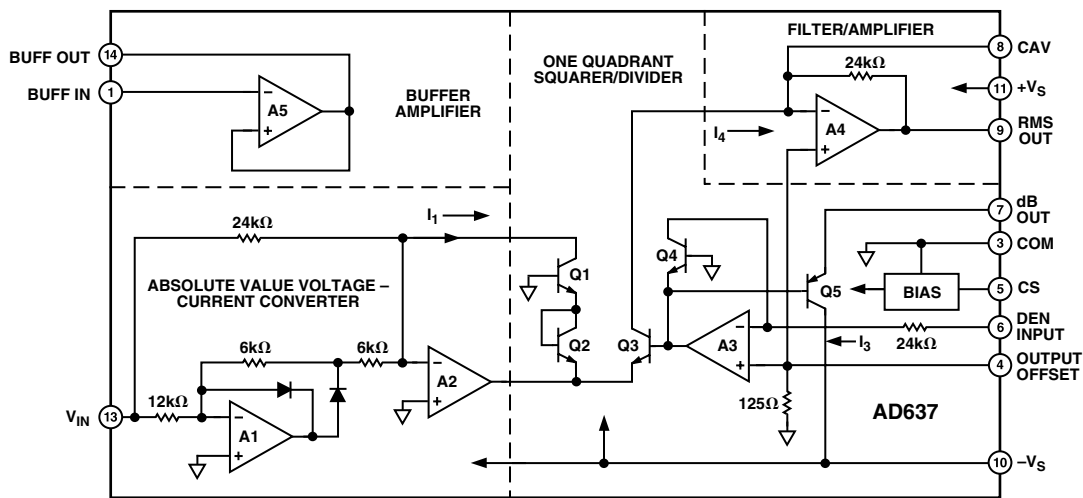


Figure 1. Simplified Schematic

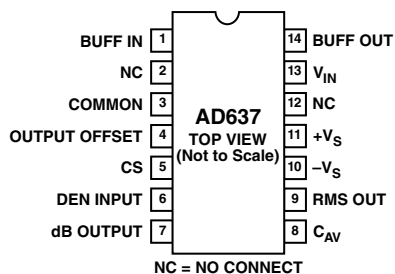
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD637 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

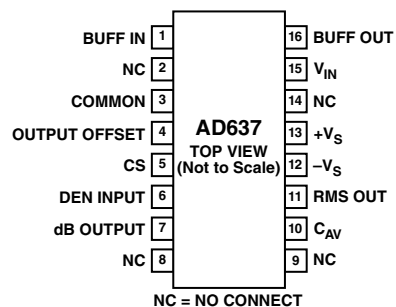


## PIN CONFIGURATIONS

### 14-Lead DIP



### 16-Lead SOIC



## PIN FUNCTION DESCRIPTIONS

### 14-Lead DIP

Pin No.	Mnemonic	Description
1	BUFF IN	Buffer Input
2, 12	NC	No Connection
3	COMMON	Analog Common
4	OUTPUT OFFSET	Output Offset
5	CS	Chip Select
6	DEN INPUT	Denominator Input
7	dB OUTPUT	dB Output
8	C <sub>AV</sub>	Averaging Capacitor Connection
9	RMS OUT	rms Output
10	-V <sub>S</sub>	Negative Supply Rail
11	+V <sub>S</sub>	Positive Supply Rail
13	V <sub>IN</sub>	Signal Input
14	BUFF OUT	Buffer Output

### 16-Lead SOIC

Pin No.	Mnemonic	Description
1	BUFF IN	Buffer Input
2, 8, 9, 14	NC	No Connection
3	COMMON	Analog Common
4	OUTPUT OFFSET	Output Offset
5	CS	Chip Select
6	DEN INPUT	Denominator Input
7	dB OUTPUT	dB Output
10	C <sub>AV</sub>	Averaging Capacitor Connection
11	RMS OUT	rms Output
12	-V <sub>S</sub>	Negative Supply Rail
13	+V <sub>S</sub>	Positive Supply Rail
15	V <sub>IN</sub>	Signal Input
16	BUFF OUT	Buffer Output

# AD637

## FUNCTIONAL DESCRIPTION

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation

$$V_{rms} = Avg \left[ \frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 1 is a simplified schematic of the AD637, subdivided into four major sections: absolute value circuit (active rectifier), square/divider, filter circuit, and buffer amplifier. The input voltage  $V_{IN}$ , which can be ac or dc, is converted to a unipolar current  $I_1$  by the active rectifier A1, A2.  $I_1$  drives one input of the squarer/divider, which has the transfer function

$$I_4 = \frac{I_1^2}{I_3}$$

The output current of the squarer/divider  $I_4$  drives A4, which forms a low-pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal, then A4's output will be proportional to the average of  $I_4$ . The output of this filter amplifier is used by A3 to provide the denominator current  $I_3$ , which equals Avg.  $I_4$  and is returned to the squarer/divider to complete the implicit rms computation

$$I_4 = Avg \left[ \frac{I_1^2}{I_4} \right] = I_1 \text{ rms}$$

and

$$V_{OUT} = V_{IN} \text{ rms}$$

If the averaging capacitor is omitted, the AD637 will compute the absolute value of the input signal. A nominal 5 pF capacitor should be used to ensure stability. The circuit operates identically to that of the rms configuration except that  $I_3$  is now equal to  $I_4$ , giving

$$I_4 = \frac{I_1^2}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage,  $V_{REF}$ , to Pin 6. The circuit operates identically to the rms case except that  $I_3$  is now proportional to  $V_{REF}$ . Thus:

$$I_4 = Avg \frac{I_1^2}{I_3}$$

and

$$V_O = \frac{V_{IN}^2}{V_{DEN}}$$

This is the mean square of the input signal.

## STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 2, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 will compute the true rms of any input signal. An averaging error, the magnitude of which will be dependent on the value of the averaging capacitor, will be present at low frequencies. For example, if the filter capacitor,  $C_{AV}$ , is 4  $\mu\text{F}$ , this error will be 0.1% at 10 Hz and increases to 1% at 3 Hz. If it is desired to measure only ac signals, the AD637 can be ac coupled through the addition of a nonpolar capacitor in series with the input as shown in Figure 2.

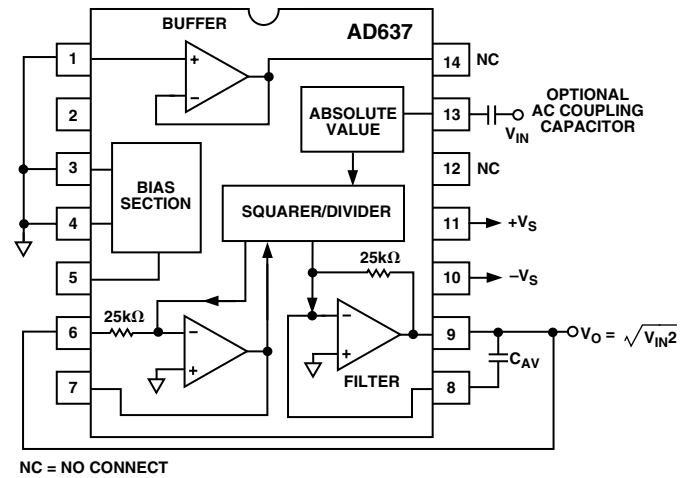


Figure 2. Standard RMS Connection

The performance of the AD637 is tolerant of minor variations in the power supply voltages; however, if the supplies being used exhibit a considerable amount of high frequency ripple it is advisable to bypass both supplies to ground through a 0.1  $\mu\text{F}$  ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 3. The output signal can be used buffered or nonbuffered depending on the characteristics of the load. If no buffer is needed, tie the buffer input (Pin 1) to common. The output of the AD637 is capable of driving 5 mA into a 2 k $\Omega$  load without degrading the accuracy of the device.

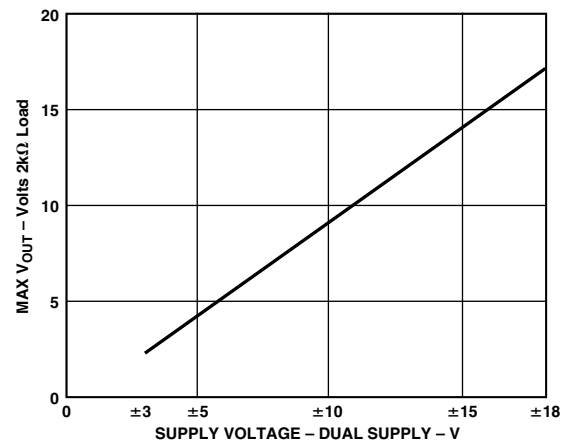


Figure 3. AD637 Max  $V_{OUT}$  vs. Supply Voltage

## CHIP SELECT

The AD637 includes a chip select feature that allows the user to decrease the quiescent current of the device from 2.2 mA to 350  $\mu$ A. This is done by driving the CS, Pin 5, to below 0.2 V dc. Under these conditions, the output will go into a high impedance state. In addition to lowering power consumption, this feature permits bussing the outputs of a number of AD637s to form a wide bandwidth rms multiplexer. If the chip select is not being used, Pin 5 should be tied high.

## OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions to allow the user to trim out both output offset and scale factor errors. These trims will result in significant reduction in the maximum total error as shown in Figure 4. This remaining error is due to a nontrimmable input offset in the absolute value circuit and the irreducible nonlinearity of the device.

The trimming procedure on the AD637 is as follows:

1. Ground the input signal,  $V_{IN}$ , and adjust R1 to give 0 V output from Pin 9. Alternatively R1 can be adjusted to give the correct output with the lowest expected value of  $V_{IN}$ .
2. Connect the desired full-scale input to  $V_{IN}$ , using either a dc or a calibrated ac signal, and trim R3 to give the correct output at Pin 9, i.e., 1 V dc should give 1.000 V dc output. Of course, a 2 V peak-to-peak sine wave should give 0.707 V dc output. Remaining errors are due to the nonlinearity.

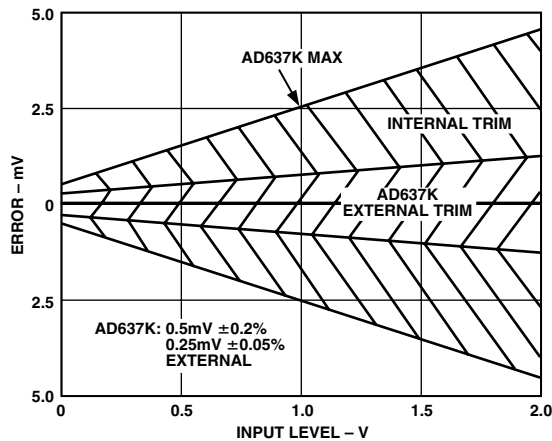


Figure 4. Max Total Error vs. Input Level AD637K Internal and External Trims

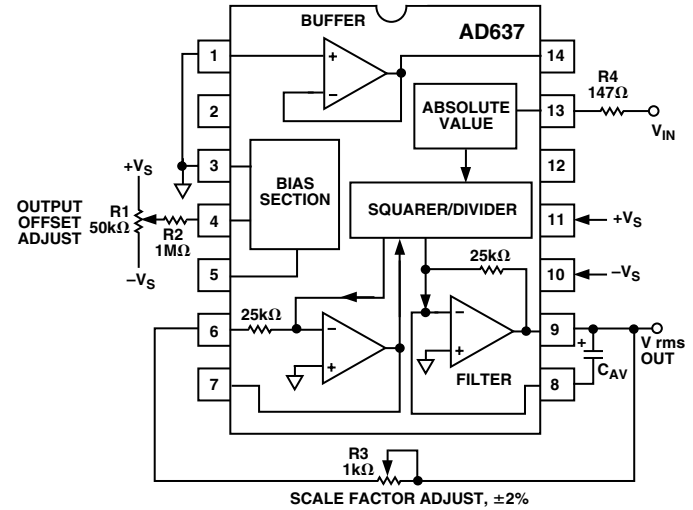


Figure 5. Optional External Gain and Offset Trims

## CHOOSING THE AVERAGING TIME CONSTANT

The AD637 will compute the true rms value of both dc and ac input signals. At dc the output will track the absolute value of the input exactly; with ac signals the AD637's output will approach the true rms value of the input. The deviation from the ideal rms value is due to an averaging error. The averaging error is comprised of an ac and dc component. Both components are functions of input signal frequency  $f$  and the averaging time constant  $\tau$  ( $\tau$ : 25 ms/ $\mu$ F of averaging capacitance). As shown in Figure 6, the averaging error is defined as the peak value of the ac component, ripple, plus the value of the dc error.

The peak value of the ac ripple component of the averaging error is defined approximately by the relationship:

$$\frac{50}{6.3 \tau f} \text{ in \% of reading where } (t > 1/f)$$

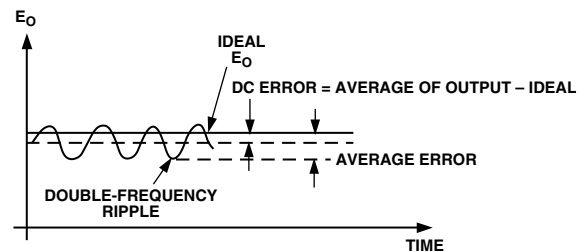


Figure 6. Typical Output Waveform for a Sinusoidal Input

This ripple can add a significant amount of uncertainty to the accuracy of the measurement being made. The uncertainty can be significantly reduced through the use of a post filtering network or by increasing the value of the averaging capacitor.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the equation:

$$\frac{1}{0.16 + 6.4 \tau^2 f^2} \text{ in \% of reading}$$

Since the averaging time constant, set by  $C_{AV}$ , directly sets the time that the rms converter "holds" the input signal during computation, the magnitude of the dc error is determined only by  $C_{AV}$  and will not be affected by post filtering.

# AD637

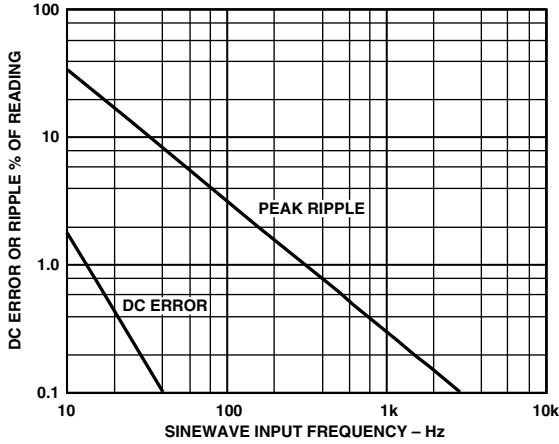


Figure 7. Comparison of Percent DC Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard RMS Connection with a  $1 \times \mu\text{F}$   $C_{AV}$

The ac ripple component of averaging error can be greatly reduced by increasing the value of the averaging capacitor. There are two major disadvantages to this: first, the value of the averaging capacitor will become extremely large, and second, the settling time of the AD637 increases in direct proportion to the value of the averaging capacitor ( $T_s = 115 \text{ ms}/\mu\text{F}$  of averaging capacitance). A preferable method of reducing the ripple is through the use of the post filter network, shown in Figure 8. This network can be used in either a one or two pole configuration. For most applications the single pole filter will give the best overall compromise between ripple and settling time.

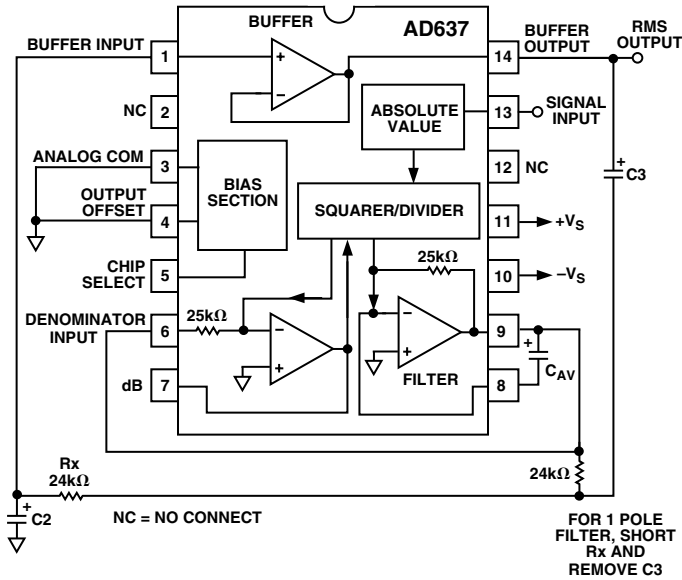


Figure 8. Two Pole Sallen-Key Filter

Figure 9a shows values of  $C_{AV}$  and the corresponding averaging error as a function of sine-wave frequency for the standard rms connection. The 1% settling time is shown on the right side of the graph.

Figure 9b shows the relationship between averaging error, signal frequency settling time, and averaging capacitor value. This graph is drawn for filter capacitor values of 3.3 times the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50 Hz. As an example, by using a  $1 \mu\text{F}$  averaging capacitor and a  $3.3 \mu\text{F}$  filter capacitor, the ripple for a 60 Hz input signal will be reduced from 5.3% of reading using the averaging capacitor alone to 0.15% using the single pole filter. This gives a factor of thirty reduction in ripple and yet the settling time would only increase by a factor of three. The values of  $C_{AV}$  and  $C_2$ , the filter capacitor, can be calculated for the desired value of averaging error and settling time by using Figure 9b.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table I gives practical component values for various types of 60 Hz input signals. These capacitor values can be directly scaled for frequencies other than 60 Hz; i.e., for 30 Hz double these values, for 120 Hz they are halved.

For applications that are extremely sensitive to ripple, the two pole configuration is suggested. This configuration will minimize capacitor values and settling time while maximizing performance.

Figure 9c can be used to determine the required value of  $C_{AV}$ ,  $C_2$ , and  $C_3$  for the desired level of ripple and settling time.

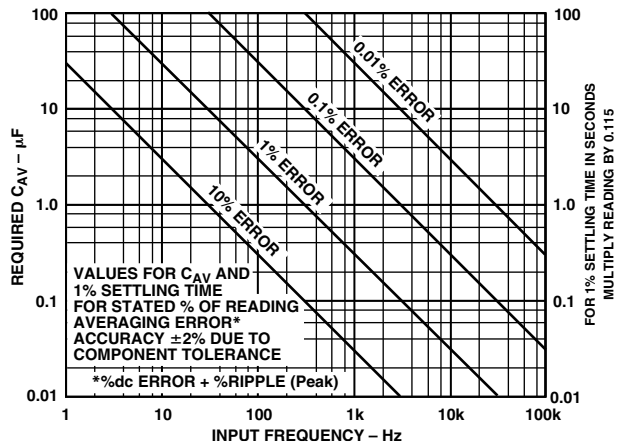


Figure 9a.

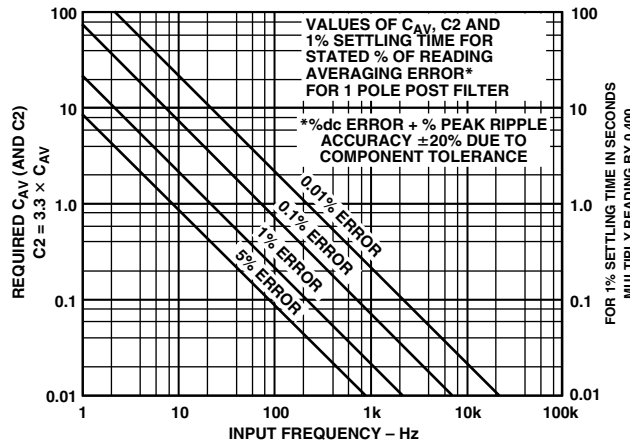


Figure 9b.



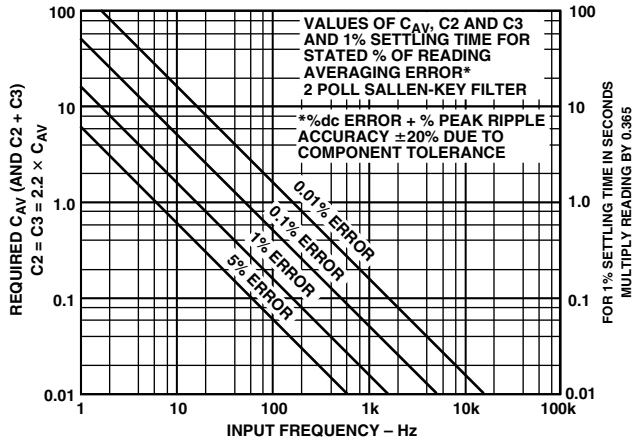


Figure 9c.

Table I. Practical Values of  $C_{AV}$  and  $C2$  for Various Input Waveforms

Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum $R \times C_{AV}$ Time Constant	Recommended $C_{AV}$ and $C2$ Values for 1% Averaging Error@60Hz with $T = 16.6ms$		1% Settling Time
			Recommended Standard Value $C_{AV}$	Recommended Standard Value $C2$	
A Symmetrical Sine Wave 		$1/2T$	$0.47\mu F$	$1.5\mu F$	181ms
B Sine Wave with dc Offset 		$T$	$0.82\mu F$	$2.7\mu F$	325ms
C Pulse Train Waveform 		$10(T - T_2)$	$6.8\mu F$	$22\mu F$	2.67sec
D 		$10(T - 2T_2)$	$5.6\mu F$	$18\mu F$	2.17sec

**FREQUENCY RESPONSE**

The frequency response of the AD637 at various signal levels is shown in Figure 10. The dashed lines show the upper frequency limits for 1%, 10%, and  $\pm 3$  dB of additional error. For example, note that for 1% additional error with a 2 V rms input the highest frequency allowable is 200 kHz. A 200 mV signal can be measured with 1% error at signal frequencies up to 100 kHz.

To take full advantage of the wide bandwidth of the AD637, care must be taken in the selection of the input buffer amplifier. To ensure that the input signal is accurately presented to the converter, the input buffer must have a  $-3$  dB bandwidth that is wider than that of the AD637. A point that should not be overlooked is the importance of slew rate in this application. For example, the minimum slew rate required for a 1 V rms 5 MHz sine-wave input signal is  $44 V/\mu s$ . The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier, as some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD845 is recommended as a precision input buffer.

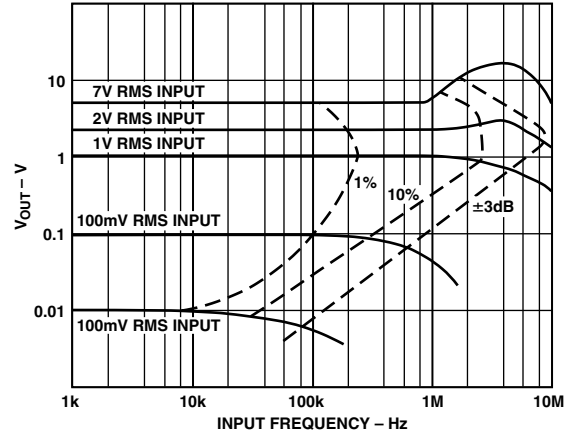


Figure 10. Frequency Response

**AC MEASUREMENT ACCURACY AND CREST FACTOR**

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal ( $CF = V_p/V_{rms}$ ). Most common waveforms, such as sine and triangle waves, have relatively low crest factors ( $\leq 2$ ). Waveforms that resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 ( $CF = 1/\sqrt{\eta}$ ).

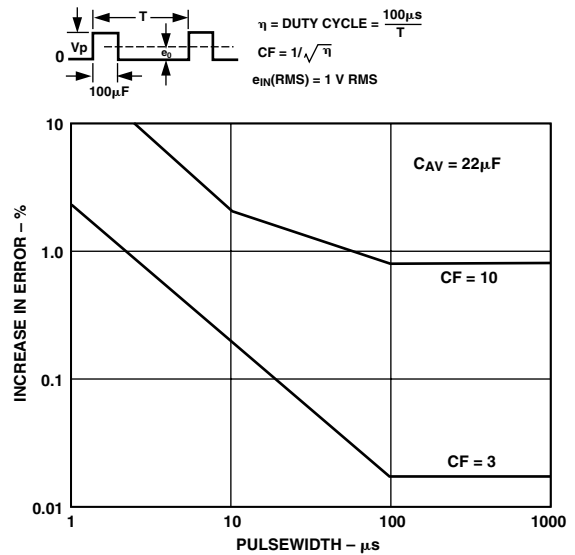


Figure 11. AD637 Error vs. Pulsewidth Rectangular Pulse

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Figure 12 is a curve of additional reading error for the AD637 for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulsewidth 100  $\mu$ s) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 V rms input amplitude.

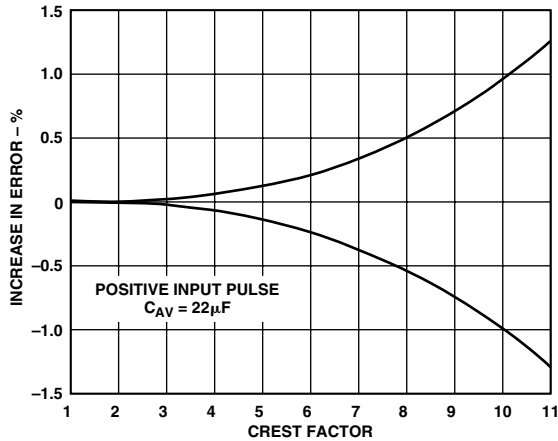


Figure 12. Additional Error vs. Crest Factor

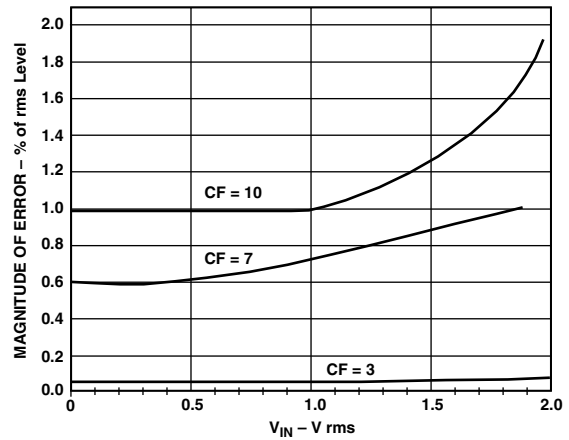


Figure 13. Error vs. RMS Input Level for Three Common Crest Factors

## CONNECTION FOR dB OUTPUT

Another feature of the AD637 is the logarithmic, or decibel, output. The internal circuit that computes dB works well over a 60 dB range. The connection for dB measurement is shown in Figure 14. The user selects the 0 dB level by setting R1 for the proper 0 dB reference current (which is set to exactly cancel the log output current from the squarer/divider circuit at the desired 0 dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the  $+0.33\%/^{\circ}\text{C}$  temperature drift of the dB circuit. The special T.C. resistor R3 is available from Tel Labs in Londonderry, NH (model Q-81) and from Precision Resistor Inc., Hillside, NJ (model PT146).

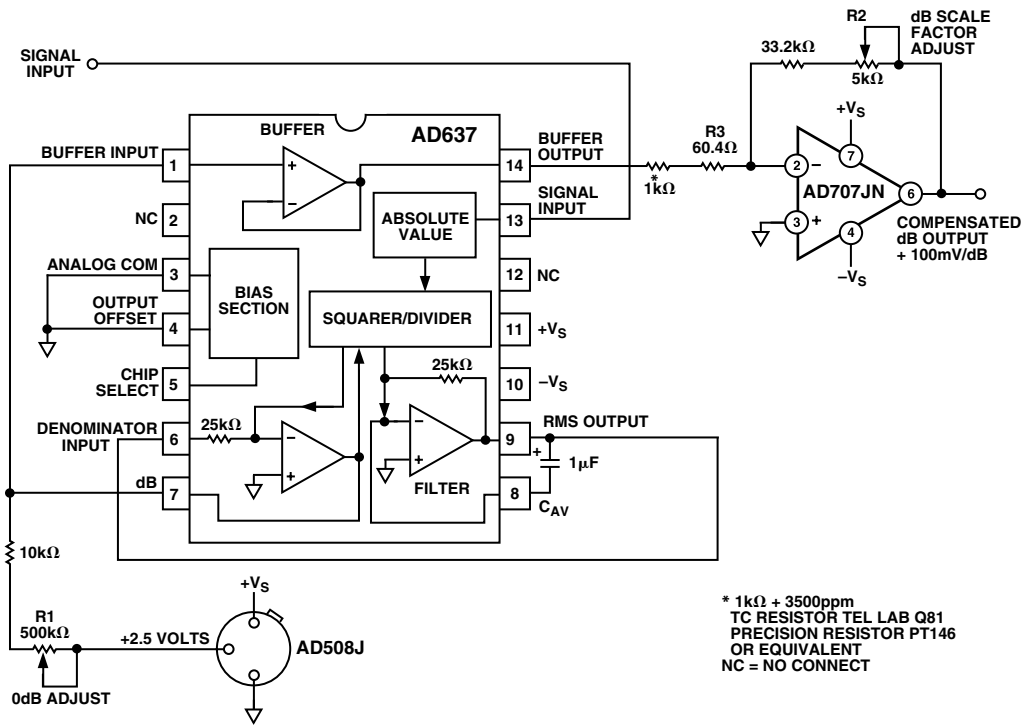


Figure 14. dB Connection



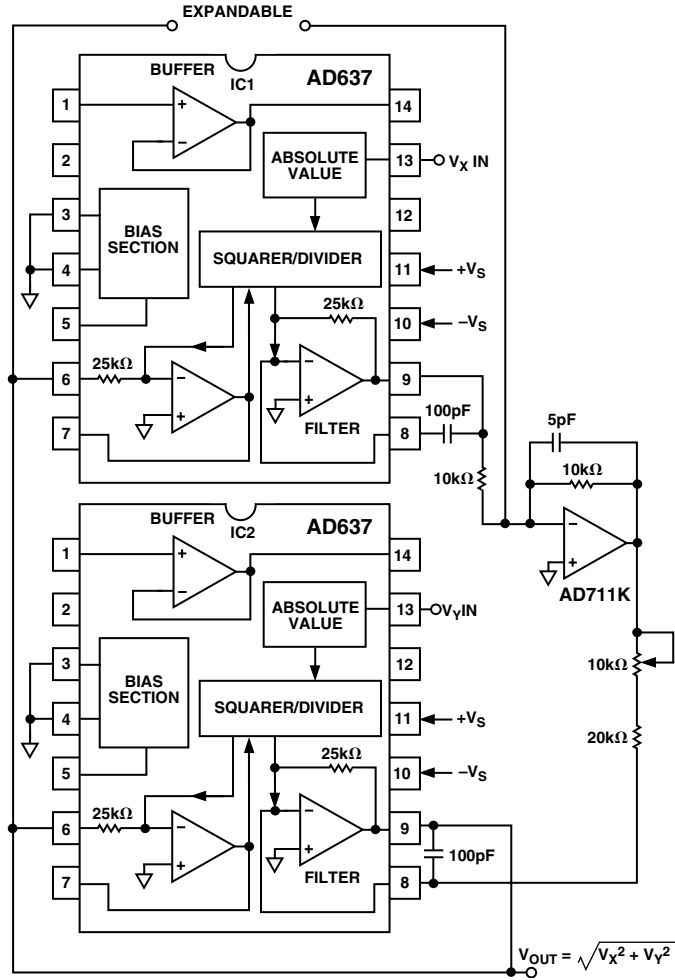
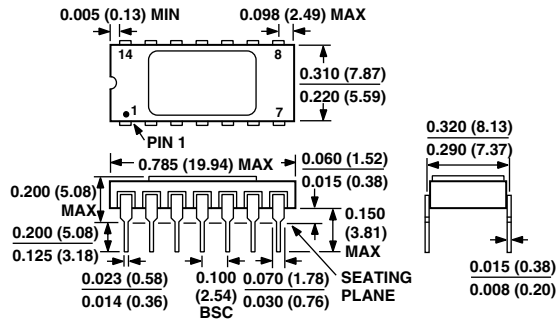


Figure 16. Vector Sum Configuration

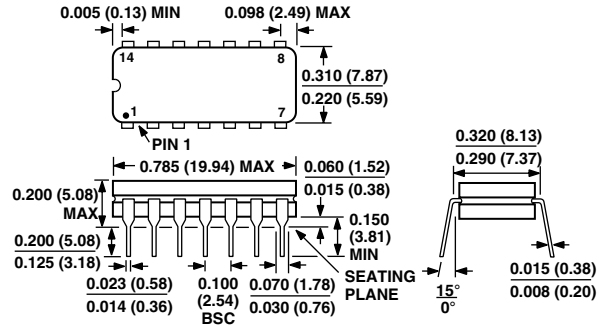
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

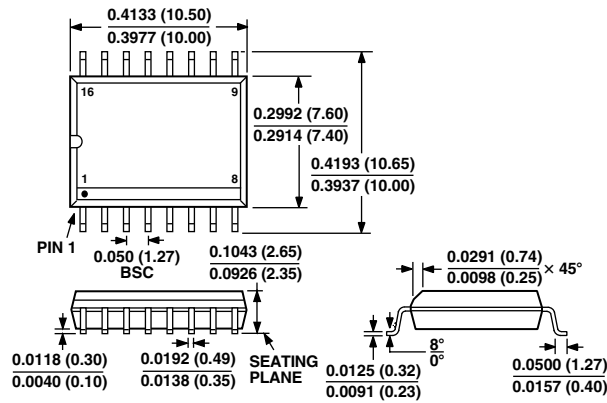
TO-116 Package  
(D-14)



Cerdip Package  
(Q-14)



SOIC Package  
(R-16)



# AD637

## Revision History

Location	Page
Data Sheet changed from REV. E to REV. F.	
Edits to ORDERING GUIDE .....	3



