

Matched N-Channel JFET Pairs

Product Summary

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
2N5911	-1 to -5	-25	5	-1	10
2N5912	-1 to -5	-25	5	-1	15

Features

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 85 dB

Benefits

- Minimum Parasitics Ensuring Maximum High-Frequency Performance
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

Applications

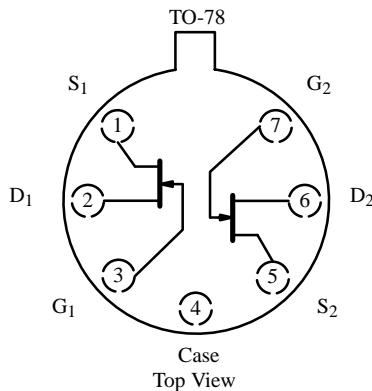
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

Description

The 2N5911/5912 are matched pairs of JFETs mounted in a TO-78 package. This two-chip design reduces parasitics and gives better performance at high frequencies while ensuring extremely tight matching.

The hermetically-sealed TO-78 package is available with full military screening per MIL-S-19500 (see Military Information).

For similar products see the SO-8 packaged SST440/SST441, the TO-71 packaged U440/U441, the low-noise SST/U401 series, and the low-leakage U421/423 data sheets.



Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage	-25 V	Power Dissipation :	Per Side ^a 367 mW
Gate-Gate Voltage	± 80 V		Total ^b 500 mW
Gate Current	50 mA	Notes	
Lead Temperature ($1/16$ " from case for 10 sec.)	300°C	a. Derate 3 mW/ $^{\circ}$ C above 25°C	
Storage Temperature	-65 to 200°C	b. Derate 4 mW/ $^{\circ}$ C above 25°C	
Operating Junction Temperature	-55 to 150°C		

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70255. Applications information may also be obtained via FaxBack, request document #70595.

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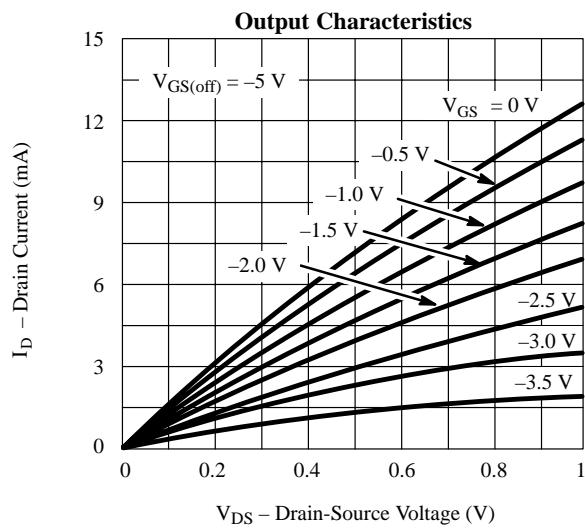
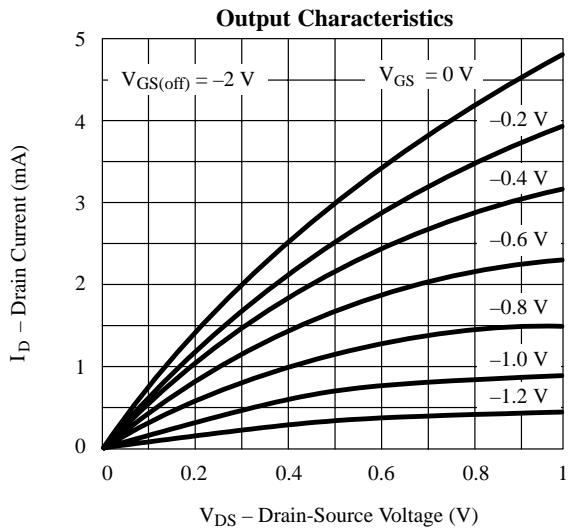
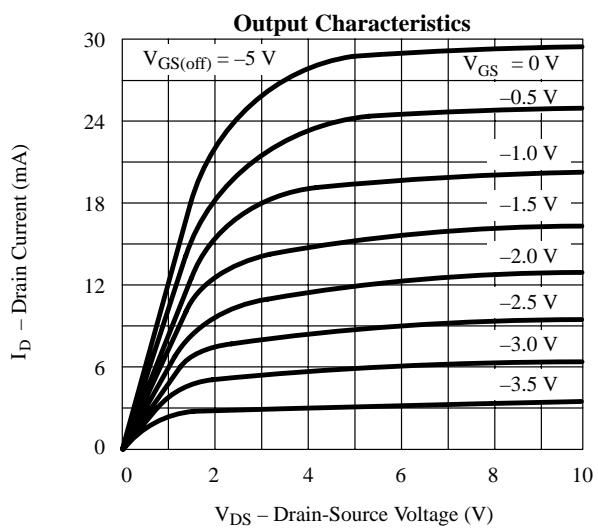
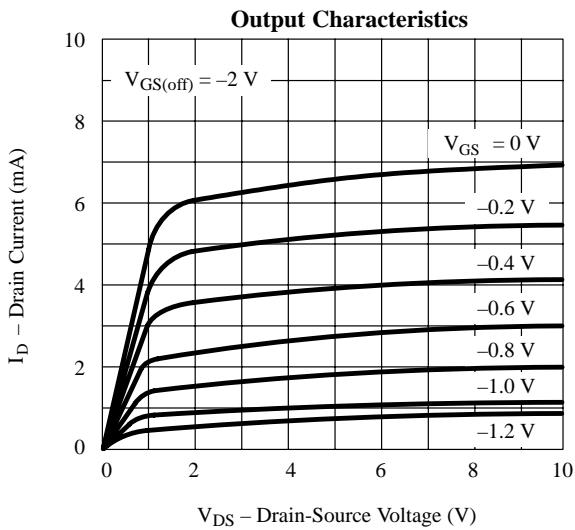
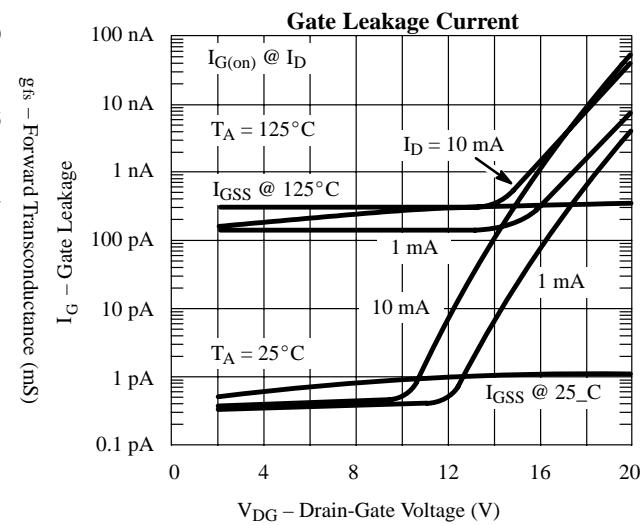
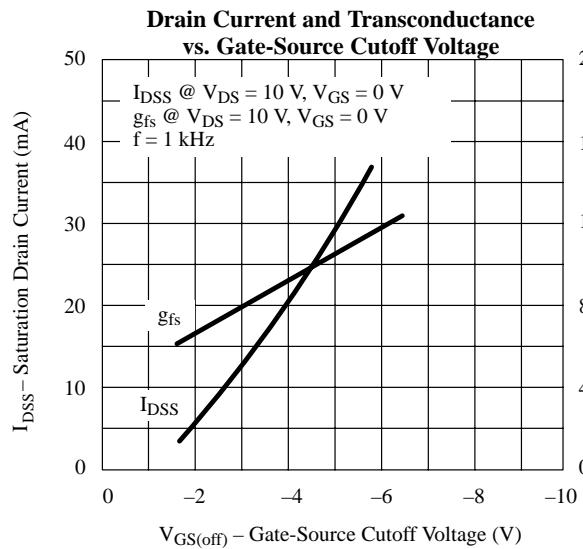
Specifications^a

Parameter	Symbol	Test Conditions	Typ ^b	Limits				Unit
				2N5911		2N5912		
Static								
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 nA	-3.5	-1	-5	-1	-5	
Saturation Drain Current ^c	I _{DSS}	V _{DS} = 10 V, V _{GS} = 0 V	15	7	40	7	40	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -15 V, V _{DS} = 0 V T _A = 150°C	-1 -2		-100 -250		-100 -250	pA nA
Gate Operating Current	I _G	V _{DG} = 10 V, I _D = 5 mA T _A = 125°C	-1 -0.3		-100 -100		-100 -100	pA nA
Gate-Source Voltage	V _{GS}	V _{DG} = 10 V, I _G = 5 mA	-1.5	-0.3	-4	-0.3	-4	V
Gate-Source Forward Voltaged ^d	V _{GS(F)}	I _G = 1 mA, V _{DS} = 0 V	0.7					
Dynamic								
Common-Source Forward Transconductance	g _{fs}	V _{DG} = 10 V, I _D = 5 mA f = 1 kHz	6	5	10	5	10	mS
Common-Source Output Conductance	g _{os}		70		100		100	μS
Common-Source Forward Transconductance	g _{fs}	V _{DG} = 10 V, I _D = 5 mA f = 100 MHz	5.8	5	10	5	10	mS
Common-Source Output Conductance	g _{os}		90		150		150	μS
Common-Source Input Capacitance	C _{iss}	V _{DG} = 10 V, I _D = 5 mA f = 1 MHz	3		5		5	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		1		1.2		1.2	
Equivalent Input Noise Voltage	ē _n	V _{DG} = 10 V, I _D = 5 mA f = 10 kHz R _G = 100 kΩ	4		20		20	nV/√Hz
Noise Figure	NF		0.1		1		1	dB
Matching								
Differential Gate-Source Voltage	V _{GS1} - V _{GS2}	V _{DG} = 10 V, I _D = 5 mA	4		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V _{DG} = 10 V, I _D = 5 mA T _A = -55 to 125°C	15		20		40	μV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 10 V, V _{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 10 V, I _D = 5 mA f = 1 kHz	0.98	0.95	1	0.95	1	
Differential Gate Current	I _{G1} - I _{G2}	V _{DG} = 10 V, I _D = 5 mA, T _A = 125°C	0.005		20		20	nA
Common Mode Rejection Ratio ^d	CMRR	V _{DG} = 5 to 10 V, I _D = 5 mA	85					dB

Notes

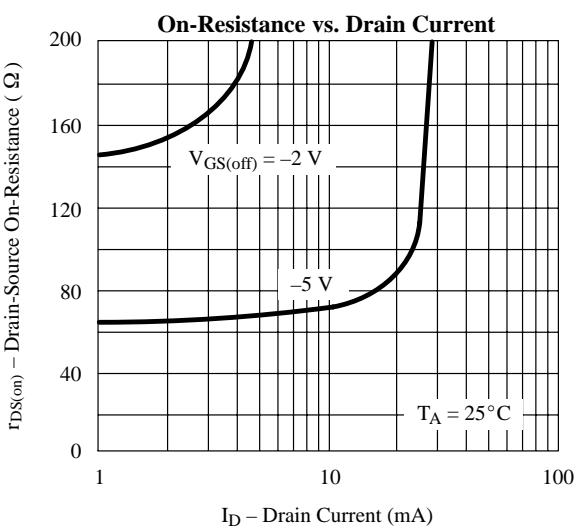
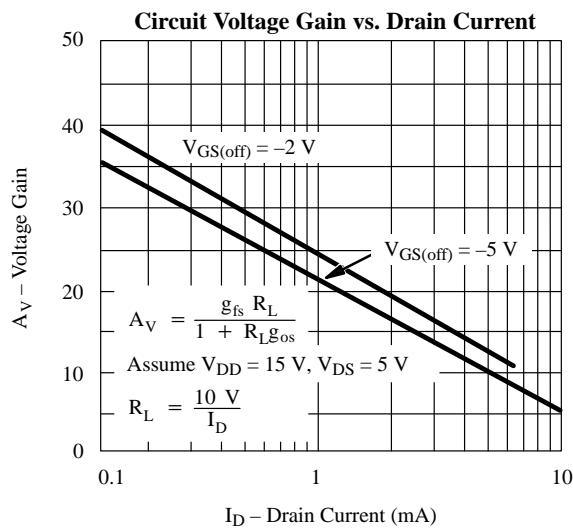
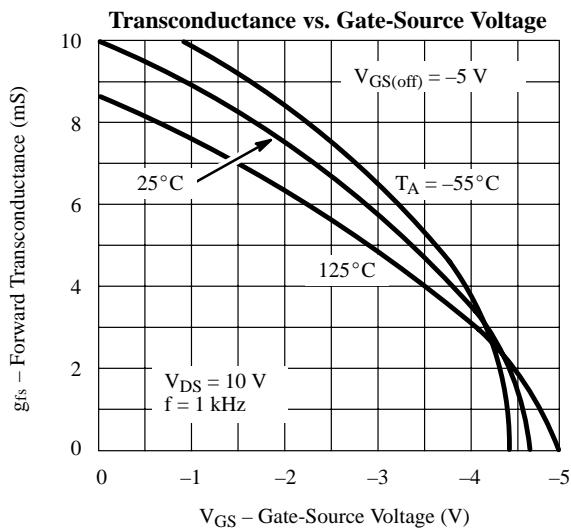
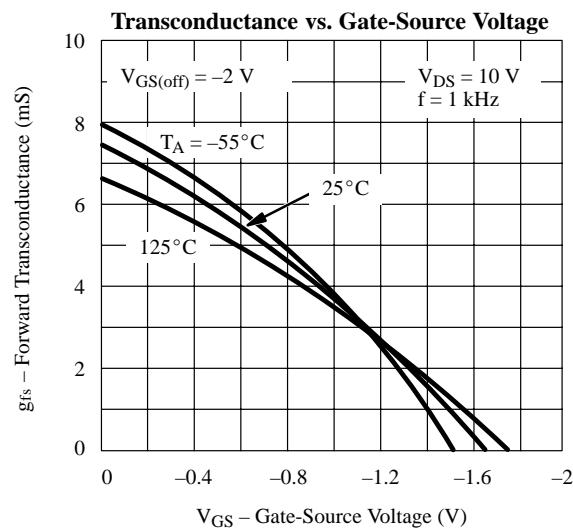
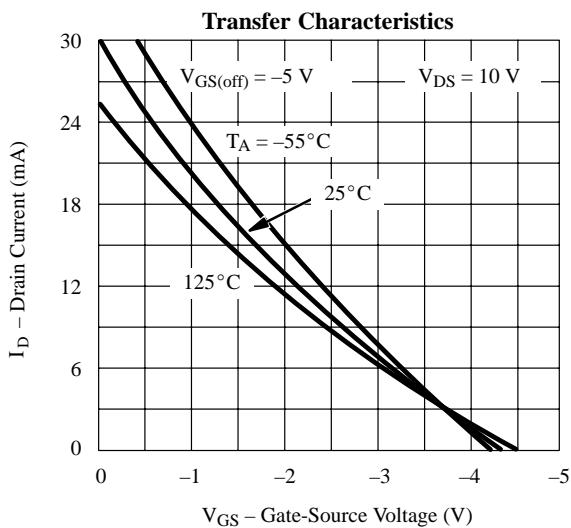
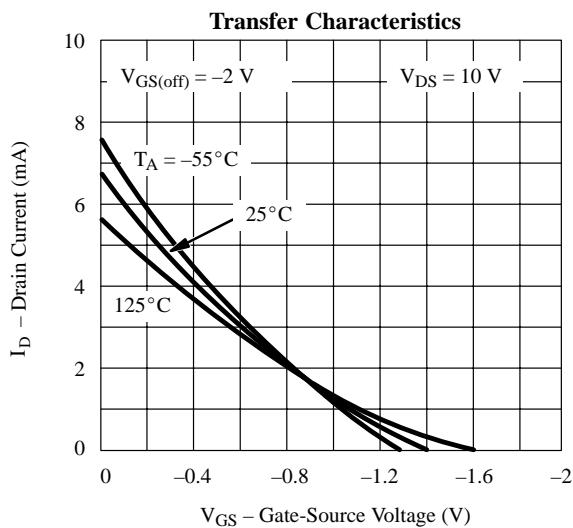
- a. T_A = 25°C unless otherwise noted.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
- d. This parameter not registered with JEDEC.

Typical Characteristics

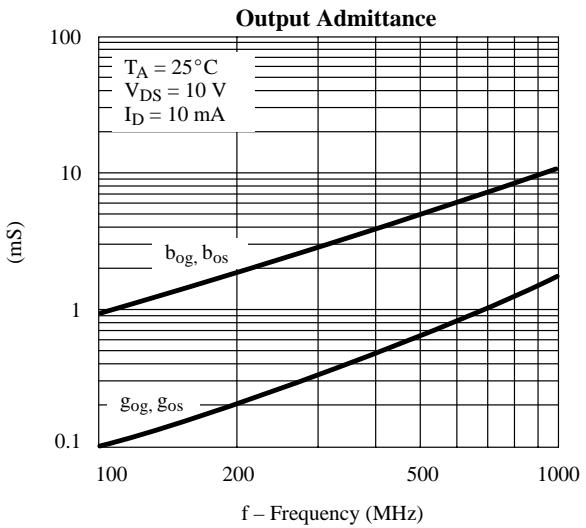
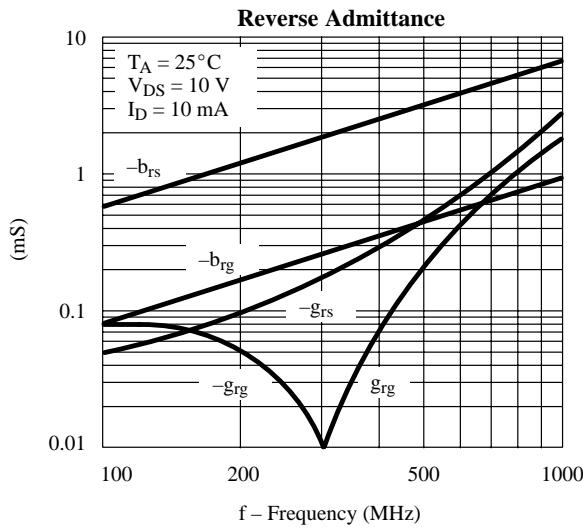
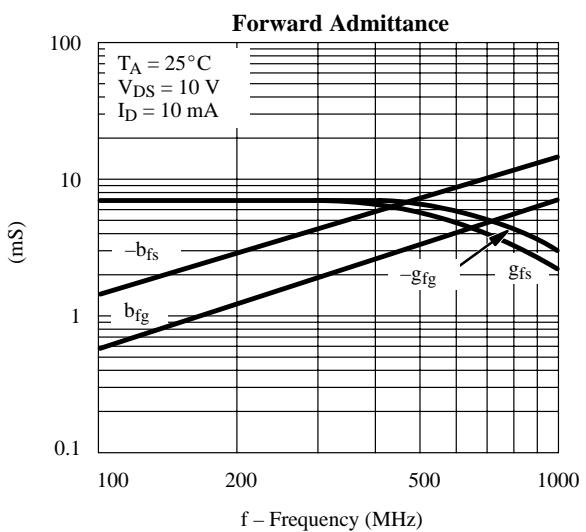
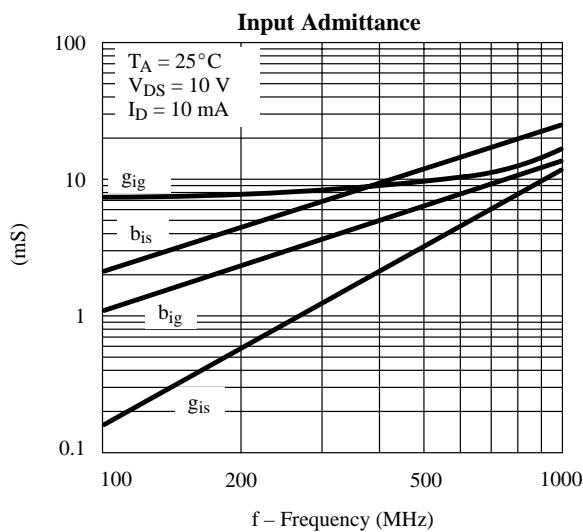
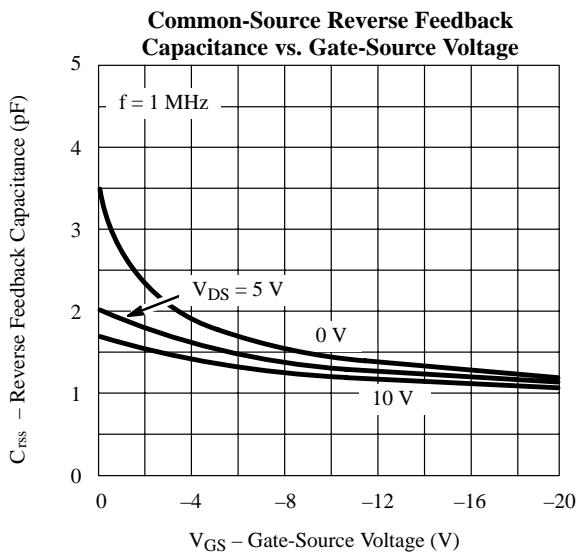
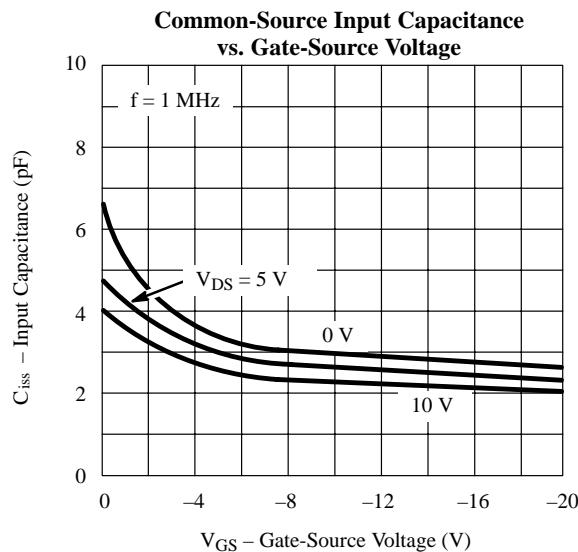


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Typical Characteristics (Cont'd)



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Typical Characteristics (Cont'd)

