

**General Description**

The MTSS PEB 2046 is a monolithic CMOS device which has the ability to connect any of the 256 PCM channels of eight incoming PCM lines to any of the 256 PCM channels of eight output lines.

The input information of a complete frame is stored in the speech memory SM. The incoming 256 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with an 8-kHz repetition rate.

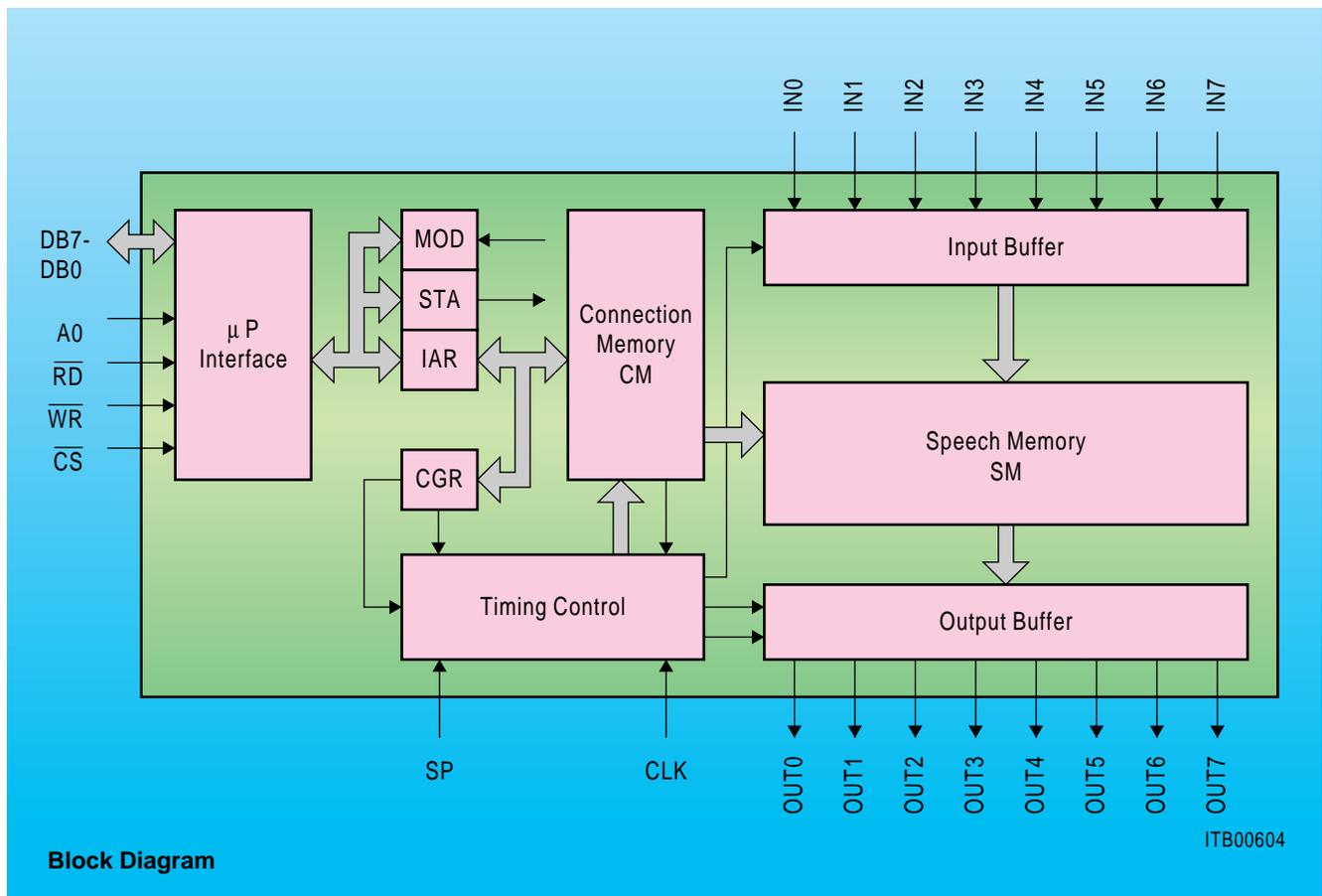
For output, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time-slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Thus the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time-slot and line number. The contents of this CM-address point to a particular input time-slot and line number (now resident in the SM).

Type	Package
PEB 2046-N	P-LCC-44-1 (SMD)
PEB 2046-P	P-DIP-40-1

**Features**

- Time/space switch for 2.048-kbit/s PCM systems
- Switching of up to 256 incoming PCM channels to up to 256 outgoing PCM channels
- Eight input and eight output PCM lines
- Configurable for a 4096- and 8192-kHz device clock
- Tristate function for further expansion and tandem operation
- 8-bit  $\mu$ P-interface
- Single +5-V power supply
- Advanced low power CMOS technology



**Block Diagram**