PRELIMINARY | Data Sheet | October 5, 2004 | FN9180.0

Li-ion/Li Polymer Battery Charger Accepting Two Power Sources

The ISL6293 is a fully integrated low-cost single-cell Li-ion or Li-polymer battery charger. The charger accepts two power inputs, normally one from a USB (Universal Serial Bus) port and another one from a desktop cradle. The ISL6293 is an ideal charger for smart handheld devices that need to communicate with a personal computer via USB.

The ISL6293 features 28V and 7V maximum voltages for the cradle and the USB inputs respectively. The 28V rating allows low-cost adapters be safely used. When both inputs are powered, the cradle input is used to charge the battery. The charge current is independently programmable for both inputs with two small resistors. One additional USBP pin allows the selection of high-power or low-power port for the USB input. The charger is self-protected against over temperature. If the die temperature rises above 100°C, a thermal foldback function reduces the charge current automatically to prevent further temperature rise. The charger preconditions the battery with low current when the battery voltage is below 2.6V. The charger has two indication pins. The PPR (power present) pin outputs an open-drain logic LOW when either the cradle or the USB input power is attached. The CHG (charge) pin is also an open-drain output that indicates a logic LOW when the charge current is above a minimum current level. When the charge current is below the minimum current, the charger remains in operation but the CHG pin indicates a logic HIGH signal. For simplicity, the charger does not have re-charge or timer functions.

Ordering Information

PART #	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6293-2CR	-40 to 85	10 Ld 3x3 DFN	L10.3x3
ISL6293-2CRZ (Note)	-40 to 85	10 Ld 3x3 DFN (Pb-free)	L10.3x3
ISL6293-2CR-T	10 Ld 3x3 DFN Tape and Reel		
ISL6293-2CRZ-T (Note)	10 Ld 3x3 DFN Tape and Reel (Pb-free)		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Features

- Complete Charger for Single-Cell Li-ion/Polymer Batteries
- **Accept Two Power Sources**
- **Low Component Count**
- Integrated Pass Element
- Integrated Charge-Current Sensor with 10% Accuracy
- No External Blocking Diode Required
- **Charge Current Thermal Foldback for Thermal Protection**
- **28V Maximum Voltage for the Cradle Input**
- Charge Indication
- Adapter Presence Indication
- Less than 1µA Leakage Current off the Battery when No Input Power Attached
- Ambient Temperature Range: -40°C to 85°C
- Thermally-Enhanced 3x3 DFN Package
- Pb-free Available

Applications

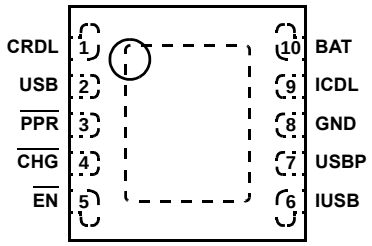
- Smart Handheld Devices
- Cell Phones, PDAs, MP3 Players
- Digital Still Cameras
- Handheld Test Equipment

Related Literature

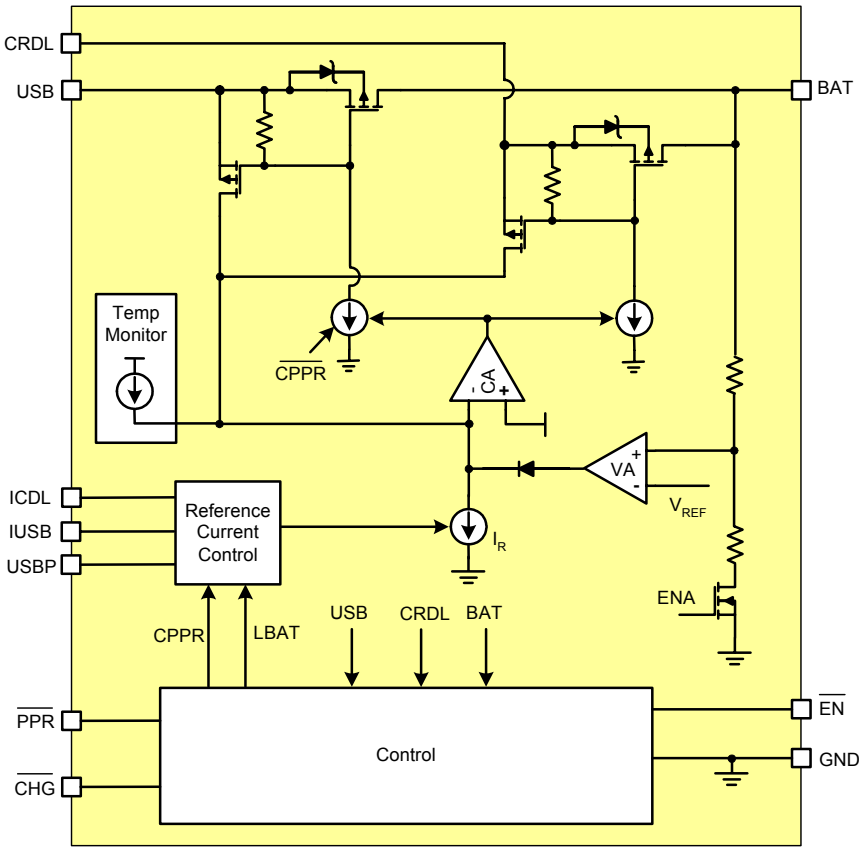
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Pinout

ISL6293-2 (DFN)
TOP VIEW

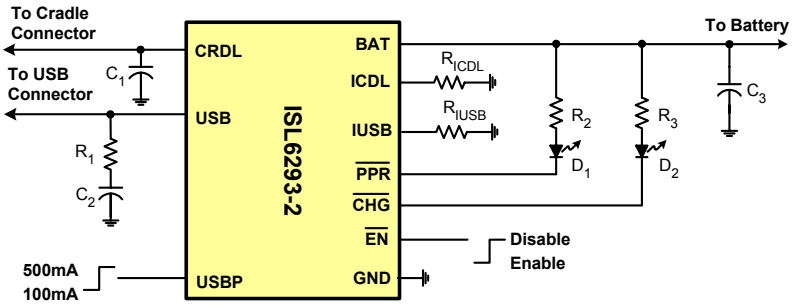


Block Diagram



Typical Applications

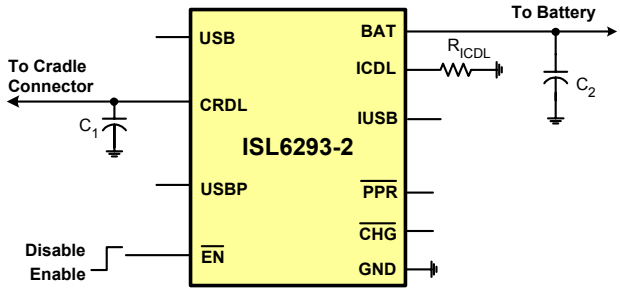
A Simple Charger Accepting Power from Both a USB Port and a Desktop Cradle



COMPONENT SELECTION

R_{ICDL}	1.82kΩ for 0.8A cradle charge current
R_{IUSB}	80kΩ for 100mA/500mA USB charge current
R_2, R_3	350Ω
C_1, C_2, C_3	1µF ceramic capacitor
R_1	1Ω
D_1, D_2	LEDs

A Simple Charger with Programmable Charge Current and Wide Input Voltage Range



COMPONENT SELECTION

R_{ICDL}	1.82kΩ for 0.8A cradle charge current
C_1, C_2	1µF ceramic capacitor

R_{IUSB} is not required when the USB input of ISL6293-2 is left floating in the design for a single input charger.

Absolute Maximum Ratings

Supply Voltage (USB) . . . . . -0.3V to 7V
Supply Voltage (CRDL) . . . . . -0.3V to 28V
Signal Input Voltage (EN, USBP, ICDL, IUSB, BAT) . . . . -0.3V to 7V
Open-Drain Pull-Up Voltage (PPR, CHG) . . . . . -0.3V to 7V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to 85°C
Supply Voltage (USB Pin) . . . . . 4.3V to 5.5V
Supply Voltage (CRDL Pin) . . . . . 4.3V to 24V
Typical Cradle Charge Current . . . . . 300mA to 1A
Typical USB Charge Current . . . . . 350mA to 450mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x3 DFN Package (Notes 1, 2)	46	4

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical Values Are Tested at USB = CRDL = 5V and ambient temperature is at 25°C, Unless Otherwise Noted. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising USB/CRDL Threshold			3.4	3.7	4.0	V
Falling USB/CRDL Threshold			3.2	3.5	3.8	V
VIN-BAT OFFSET VOLTAGE						
Rising Edge	V_{OS}	V_{BAT} = 4.0V, use CHG pin to indicate the comparator output (Note 3)	-	TBD	TBD	mV
Falling Edge	V_{OS}		TBD	TBD	-	mV
STANDBY CURRENT						
BAT Pin Sink Current	$I_{STANDBY}$	EN = HIGH or both inputs are floating	-	-	1.0	µA
CRDL Pin Supply Current	I_{CRDL}	EN = HIGH	-	150	-	µA
USB Pin Supply Current	I_{USB}		-	150	250	µA
CRDL/USB Pin Supply Current		EN = LOW or floating	-	0.55	-	mA
VOLTAGE REGULATION						
Output Voltage (Note 4)	V_{CH}	Load = 0mA	4.158	4.2	4.242	V
CRDL PMOS On Resistance		V_{BAT} = 3.8V, $I_{CHARGER}$ = 0.5A	-	700	-	mΩ
USB PMOS On Resistance		V_{BAT} = 3.8V, $I_{CHARGER}$ = 0.35A	-	700	-	mΩ
CHARGE CURRENT (Note 5)						
ICDL Pin Output Voltage	V_{ICDL}	V_{BAT} = 3.8V	1.17	1.20	1.23	V
IUSB Pin Output Voltage	V_{IUSB}		0.776	0.8	0.824	V
CRDL Input Constant Charge Current	I_{CHARGE}	R_{ICDL} = 1.82kΩ, V_{BAT} = 3.8V, V_{CRDL} = 5V Valid for -10°C to 85°C	720	800	880	mA
CRDL Input Trickle Charge Current	$I_{TRICKLE}$	R_{ICDL} = 1.82kΩ, V_{BAT} = 2.4V, V_{CRDL} = 5V Given as a % of the CRDL I_{CHARGE}	5.0	8.5	11.0	%
USB Input Constant Charge Current	I_{CHARGE}	USBP = HIGH, R_{IUSB} = 80kΩ, V_{BAT} = 3.8V	380	440	500	mA
USB Input Trickle Charge Current (Note 4)	$I_{TRICKLE}$	USBP = HIGH, R_{IUSB} = 80kΩ, V_{BAT} = 2.4V Given as a % of the USB HIGH I_{CHARGE}	8.0	10.0	12.0	%
USB Input Constant Charge Current	I_{CHARGE}	USBP = LOW, R_{IUSB} = 80kΩ, V_{BAT} = 3.8V	68	84	100	mA

Electrical Specifications Typical Values Are Tested at USB = CRDL = 5V and ambient temperature is at 25°C, Unless Otherwise Noted. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Conditions. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
USB Input Trickle Charge Current	$I_{TRICKLE}$	USBP = LOW, R_{IUSB} = 80kΩ, V_{BAT} = 2.4V Given as a % of the USB LOW I_{CHARGE}	45.0	50.0	55.0	%
END-OF-CHARGE CURRENT THRESHOLD						
Powered From USB Pin	I_{EOC}	USBP = HIGH, USB = 5V, R_{IUSB} = 80kΩ Given as a % of the USB HIGH I_{CHARGE}	8.0	10.5	13.0	%
Powered From USB Pin	I_{EOC}	USBP = LOW, USB = 5V, R_{IUSB} = 80kΩ Given as a % of the USB LOW I_{CHARGE}	17.0	21.0	25.0	%
Powered From CRDL Pin	I_{EOC}	R_{ICDL} = 1.82kΩ, V_{CRDL} = 5V Given as a % of the CRDL I_{CHARGE}	5.5	8.5	11.0	%
PRECONDITIONING CHARGE THRESHOLD						
Preconditioning Charge Threshold Voltage	V_{MIN}		2.5	2.6	2.7	V
INTERNAL TEMPERATURE MONITORING						
Current Foldback Threshold (Note 6)	T_{FOLD}		85	100	115	°C
LOGIC INPUT AND OUTPUT						
USBP Pin Logic Input High			2.0	-	-	V
USBP Pin Logic Input Low			-	-	0.4	V
USBP Pin Internal Pull Down Resistance			-	1000	-	kΩ
EN Pin Logic Input High			1.2	-	-	V
EN Pin Logic Input Low			-	-	0.4	V
EN Pin Internal Pull Down Resistance			-	1000	-	kΩ
CHG/PPR Sink Current		Pin Voltage = 0.8V	15	-	-	mA

NOTES:

3. The 4.0V V_{BAT} is selected so that the CHG output can be used as the indication for the offset comparator output indication. If the V_{BAT} is lower than the POR threshold, no output pin can be used for indication.
4. The maximum and minimum limits are guaranteed over -40°C to 70°C ambient temperature range.
5. The charge current may be reduced by the thermal foldback function, depending on the heatsinking condition of the test setup.
6. The threshold value at which the charger output is reduced to near zero. Guaranteed by design, not tested.

Functional Pin Description

CRDL (Pin 1)

Cradle input. This pin is usually connected to a cradle power input. The maximum input voltage is 28V. The charge current from this pin is programmable with the ICDL pin up to 1A. When this pin is connected to a power source, no charge current is drawn from the USB pin. A 1µF or larger value ceramic capacitor is recommended for decoupling.

USB (Pin 2)

USB input. This pin is usually connected to a USB port power connector. Other sources that are lower than 5.5V are also acceptable. The charge current from the USB pin is selectable between 100mA and 500mA maximum with the USBP pin when the R_{IUSB} = 80kΩ. A 1µF or larger value ceramic capacitor is recommended for decoupling. It is also recommended to have a 1Ω resistor in series with the decoupling capacitor to prevent an over-shoot voltage when a USB cable is plugged in.

PPR (Pin 3)

Power presence indication. This is an open-drain output pin that outputs a logic LOW when either the USB input voltage or the CRDL input voltage is above its POR level, regardless if the charger is enabled or disabled. This pin provides a wake-up signal to a microprocessor when either the cradle or the USB power is connected.

CHG (Pin 4)

Charge indication pin. When the charge current from the cradle input during the constant current mode falls to below 8% of the programmed reference current by the ICDL pin or the charge current from the USB input is below 10% of the programmed charge current, the open-drain MOSFET is turned off. The pin will be pulled to logic HIGH by the pull-up resistor to indicate the End Of Charge.

EN (Pin 5)

Enable logic input. Connect to LOW or leave floating to enable the charger.

IUSB (Pin 6)

The IUSB pin programs the USB charge current. This pin is regulated to 0.8V. The current flowing out of this pin is mirrored to the USB charge current control reference. When the USBP pin is connected to logic HIGH, the typical USB charge current can be found as:

$$I_{USB} = 45000 \cdot \frac{V_{REF}}{R_{IUSB}} = 45000 \times \frac{0.8V}{R_{IUSB}} (A)$$

The R_{IUSB} has a programming range of 80kΩ to 103kΩ, such that the USB current has a typical value ranges from 350mA to 450mA.

When the USBP pin is driven to logic LOW, the charge current is approximately 1/5 of the above value.

USBP (Pin 7)

USB port selection logic input. When this pin is left floating or driven to logic LOW, the USB port is regarded as a low-power port, such that the charge current is 84mA. When this pin is driven to logic HIGH, the USB port is considered a high-power port, and the charge current is 450mA. The ratio of the charge current when this pin is HIGH or LOW is fixed at approximately 5:1.

GND (Pin 8)

System ground.

ICDL (Pin 9)

The ICDL pin has two functions. The first function is to program the cradle charge current during the constant-current mode. The voltage of this pin is 1.20V during the constant-current mode of the cradle charger. The constant-current mode current is programmed by the following equation:

$$I_{CDL} = \frac{1.20V}{R_{ICDL}} \cdot ratio \quad (A)$$

where R_{ICDL} is the resistor connected to the ICDL pin (see the Typical Application). The ratio is given by the following table and curve.

TABLE 1. RATIO vs R_{ICDL}

R_{ICDL} (kΩ)	1.5	2.2	3.0	3.9	4.6
Ratio	1291	1216	1155	1122	1088

It is recommended that the charge current be programmed in the range of 300mA to 1A.

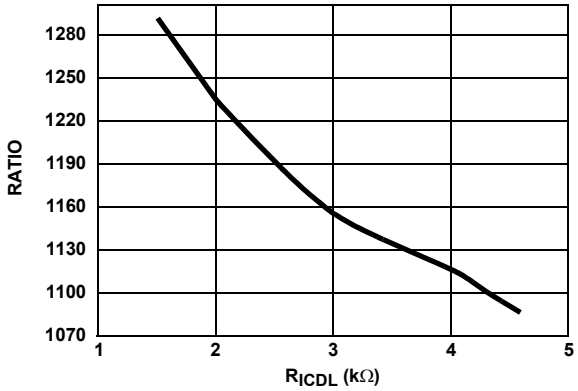


FIGURE 1. THE RATIO USED IN THE CHARGE CURRENT CALCULATION vs R_{ICDL}

The second function of the ICDL pin is to monitor the actual charge current. The voltage of this pin, V_{ICDL}, is proportional to the actual charge current, I_{CHG}, in either the USB or the cradle charger. When the cradle charger or the USB charger is working with USBP connected to logic HIGH, the ICDL pin voltage is given by the following equation.

$$V_{ICDL} = \frac{1.20V}{I_{CDL}} \cdot I_{CHG} = \frac{R_{ICDL} \cdot I_{CHG}}{ratio}$$

where the ratio has the same value given in Table 1.

The cradle charge current should be programmed equal or higher than the USB current; otherwise, the ICDL pin voltage will be higher than 1.20V during the constant current mode when the USB charger is working. The charger still works properly but the accuracy of the current monitoring voltage degrades and saturates at approximately 2.1V.

When the USB charger is working with the USBP pin connected to logic LOW, the ICDL pin voltage is approximately five times of the above equation.

BAT (Pin 10)

Charger output pin. Connect this pin to the battery pack or the battery cell. A 1µF or larger value ceramic capacitor is recommended for decoupling. The charger relies on the battery for stability so a battery should always be connected to the BAT pin.

Description

The ISL6293 is designed for a single-cell Li-ion or Li-polymer battery charging circuit that accepts both a USB port and a desktop cradle as its power source. The charge current from each power source is independently programmable but only one of the two sources charges the battery. The following describes the operation of the charger.

Input Auto Selection

The charger selects only one power source to charge the battery. When the CRDL input is higher than both the POR threshold and the battery voltage, CRDL is the power source. When this condition is not true, then the USB input is selected as the power source. If the CRDL input happens to have a voltage below the battery voltage but the USB input has a voltage higher than the battery voltage, then the USB input is used to charge the battery. The control circuit always breaks both internal power devices before switching in one power source to avoid any simultaneous conduction of both power MOSFETs.

When the BAT pin voltage is below 1.7V, the charger selects the CRDL input as the power source. Hence, if the USB input is powered, the charger will not charge the battery.

USB Charge Current

When the USB port is the power source, the charge current is programmed by the logic input USBP pin. When the USBP is driven to logic LOW, the charge current is set to 90mA (when R_{IUSB} is 80kΩ). When the USBP is driven to logic HIGH, the charge current is set to 450mA (when R_{IUSB} is 80kΩ). The USBP is equivalent to a logic LOW when left floating. Typically the P-channel MOSFET for the USB input has an $r_{DS(ON)}$ of 700mΩ at room temperature. With a 500mA charge current, the typical head room is 350mV. If the input voltage drops to a level that the voltage different between the USB pin and the BAT pin is less than 350mV, the $r_{DS(ON)}$ becomes a limiting factor of the charge current; and the charge current will reduce to a lower level in this case.

Cradle Charge Current

The cradle charge current is programmed with the external resistor connected between the ICDL pin and the GND pin. The current can be calculated with the equation given in the ICDL pin description. The typical P-channel MOSFET for the CRDL input is 700mΩ at room temperature. The actual charge current will be limited by several factors, for example, the programmed ICDL, the thermal limit, and the $r_{DS(ON)}$.

Floating Charge Voltage

The floating voltage during the constant voltage mode is 4.2V. The floating voltage has 1% accuracy over the ambient temperature range of -40°C to 70°C. No leakage current from any of the two power MOSFETs will cause the battery voltage to drift to a higher level.

Trickle Charge Current

When the battery voltage is below the minimum battery voltage V_{MIN} given in the electrical specification, the charger operates in a trickle/preconditioning mode. If power comes from the cradle, the trickle mode current is

$$I_{TRICKLE} = \frac{1.20V}{R_{ICDL}} \cdot 100 \quad (A)$$

The trickle current is 45mA if the power comes from the USB port with R_{IUSB} = 80kΩ.

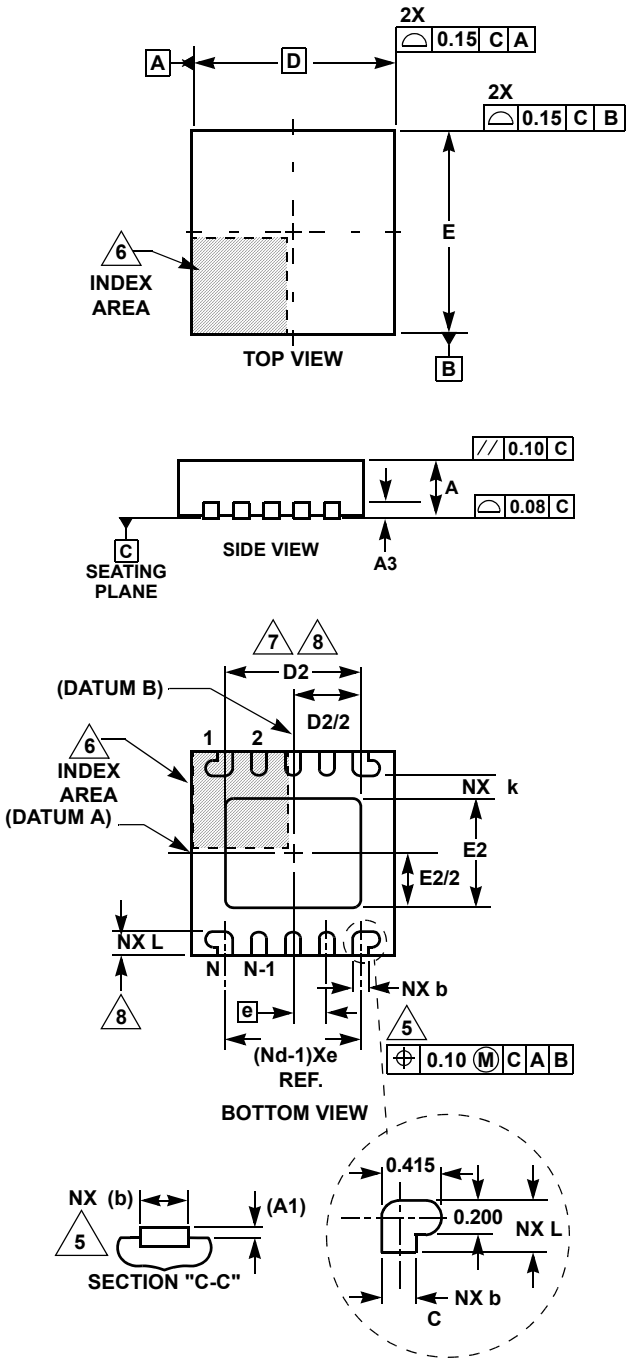
End-of-Charge Indication

The CHG pin outputs a logic HIGH by turning off the internal open-drain MOSFET when the charge current falls below 8% of the constant current mode current for the cradle charger or 10% for the USB charger. The charger, however, does not turn off as long as an input power source is attached.

Power Presence Indication

When either the USB or the cradle input voltage is above the POR level, the PPR pin outputs a logic LOW signal to indicate the presence of input power.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

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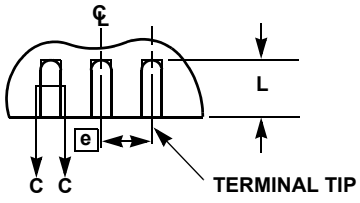
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE