FMS9874

Graphics Digitizer

3x8-Bit, 108Ms/s Triple Video A/D Converter with Clamps

Features

- 3-channels
- 108 Ms/s conversion rate
- Programmable Clamps
- 500ps PLL clock jitter
- Adjustable Gain and offset
- Internal Reference Voltage
- I[2]C/SMBus compatible Serial Port
- 100-pin package

Applications

- Flat panel displays and projectors
- RGB Graphics Processing

Description

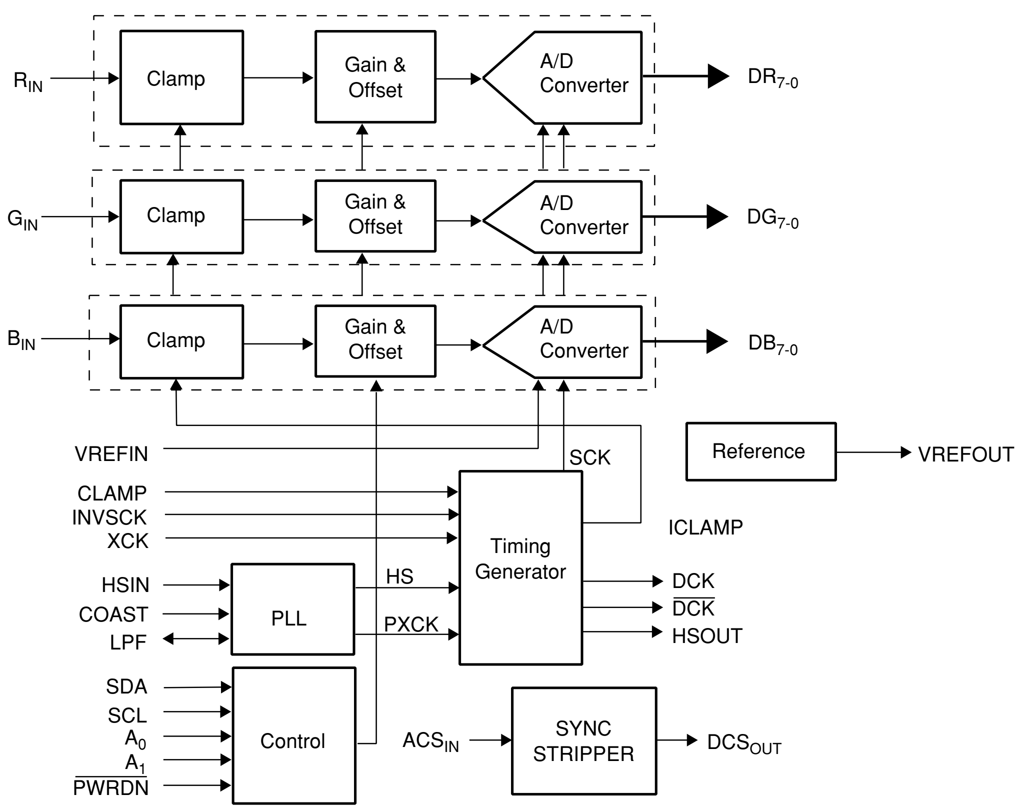
As a fully integrated analog interface, the FMS9874 can directly digitize RGB graphics with resolutions up to 1024 x 768/85Hz and 1280 x 1024/60Hz; or using alternate pixel sampling, 1600 x 1200/75Hz. ADC sampling clock can be derived from either an external source or incoming horizontal sync signal using the internal PLL. Output data is 24-bit RGB. Setup and control is via registers, accessible through an SMBus/I[2]C compatible serial port.

Input amplitude range is 500–1000mV with either DC or AC coupling. Lower reference of AC coupled inputs is established with input clamps that are either internally generated or externally provided.

Common to the three channels are clamp pulses, a bandgap reference voltage and clocks derived from a PLL or an external source. Digital data levels are 2.5–3.3 volt CMOS compliant.

Power can be derived from a single +3.3 Volt power supply. Package is a 100-lead MQFP. Performance specifications are guaranteed over 0°C to 70°C range.

Block Diagram



Architectural Overview

Three separate digitizer channels are controlled by common timing signals derived from the Timing Generator. A/D clock signals can be derived from either a PLL or an external clock XCK. With the PLL selected, A/D clocks track the incoming horizontal sync signal connected to the HSIN input. Setup is controlled by registers that are accessible through the serial interface.

Conversion Channels

Typical RGB graphics signals, R_{IN}, G_{IN}, B_{IN} are ground referenced with 700mV amplitude. If a sync signal is embedded then the usual format is sync on green with the sync tip at ground, the black level elevated to 300mV and peak green at 1000mV.

AC coupled video signals must be level shifted to establish the lower level of the conversion range by clamping to the black level of the back porch (see Figure 1). Clamp pulses are derived from internal Timing and Control logic or from the external CLAMP input.

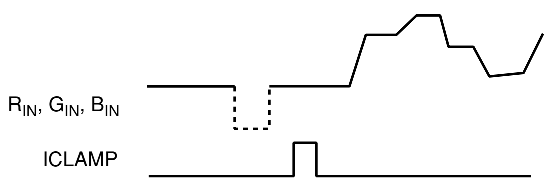


Figure 1. Clamping to the back-porch

Gain and Offset

Gain and Offset registers serve two functions: adjustment of contrast and brightness by setting RGB values in tandem; matching the gain and offsets between channels, by setting RGB values individually to obtain the same output levels.

A/D conversion range can be matched to the amplitude of the incoming video signal by programming Gain Registers GR, GG and GB, which vary sensitivity (LSB/volt) over a 2:1 range. Incoming video signal amplitudes varying from 0.5 to 1.0 volt can be accommodated.

Input offset voltage of each converter is programmable in 1 LSB steps through the 6-bit OSR, OSG and OSB registers. Range of adjustment is equivalent to –31 to +32 LSB.

A/D Converter

Each A/D converter digitizes the analog input into 8-bit data words. Latency is 5–$5^1/_2$ clock cycles, depending upon the state of CHINV.

V_{REFIN} is the source of reference voltage for the three A/D converters. V_{REFIN} can be connected to either the internal bandgap voltage, V_{REFOUT} or an external voltage.

Output Data Configuration

Output data number format for each channel is binary: 00 corresponds to the lowest input; FF corresponds to the highest input.

Timing and Control

Timing and Control logic encompasses the Timing Generator, PLL and Serial Interface.

Timing Generator

All internal clock and synchronization signals are generated by the Timing Generator. Master Clock source is either the PLL or the external clock input, XCK. Bit XCKSEL selects the Master Clock source. Two clocks are generated.

Sampling clock, SCK is supplied to all three A/D converters. Phase of SCK can be adjusted in 32 11.25 degree phase increments using the 5-bit PHASE register.

DCK is the output data clock. DCK and $\overline{DCK}$ are supplied as outputs for synchronizing data transfer from the digitizer outputs.

Horizontal sync applied to the input, HS_{IN} is propagated by the Timing and Control to the HS_{OUT} output with a delay that aligns leading and trailing edges with the output data.

Phase Locked Loop

With a horizontal sync signal connected to the HSIN input pin, the PLL generates a high frequency internal clock signal, PXCK that is fed to the Timing and Control logic. Frequency of PXCK is set by the register programmable PLL divide ratio, PLLN.

COAST is an input that disables the PLL lock to the horizontal sync input, HSIN. If HSIN is to be disregarded for a period such as the vertical sync interval, COAST allows the VCO frequency to be maintained. Missing horizontal sync pulses during the vertical interval can cause tearing at the top of a picture, if COAST is not used.

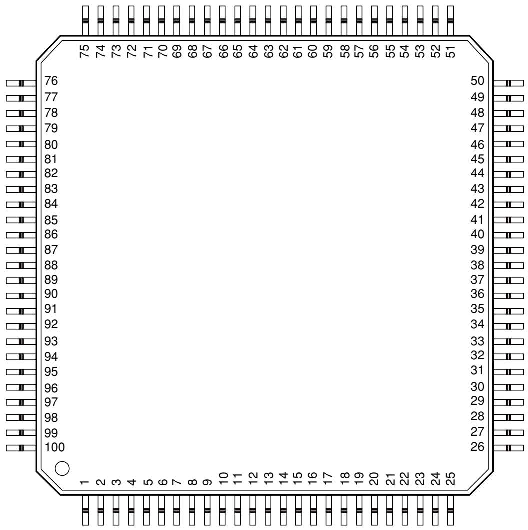
Two pixels per clock mode is set by programming the PLL to half the pixel rate. By toggling the INVCK pin between frames, even and odd pixels can be read on alternate frames.

Serial Interface

Registers are accessed through an I^2C/SMBus compatible serial port. Four serial addresses are pin selectable.

Pin Assignments

100-Lead MQFP (KG)



No.	Name	No.	Name	No.	Name	No.	Name
1	GND	26	GND	51	DB_7	76	DR_7
2	R_{IN}	27	GND	52	DB_6	77	DR_6
3	V_{DDA}	28	HSIN	53	DB_5	78	DR_5
4	GND	29	COAST	54	DB_4	79	DR_4
5	V_{DDA}	30	GND	55	DB_3	80	DR_3
6	GND	31	V_{DDP}	56	DB_2	81	DR_2
7	ACS_{IN}	32	XCK	57	DB_1	82	DR_1
8	G_{IN}	33	LPF	58	DB_0	83	DR_0
9	V_{DDA}	34	NC	59	GND	84	GND
10	GND	35	GND	60	V_{DDO}	85	V_{DDO}
11	V_{DDA}	36	V_{DDP}	61	GND	86	DCK
12	GND	37	GND	62	V_{DDO}	87	$\overline{DCK}$
13	B_{IN}	38	V_{DDP}	63	DG_7	88	HS_{OUT}
14	V_{DDA}	39	GND	64	DG_6	89	DCS_{OUT}
15	GND	40	GND	65	DG_5	90	GND
16	V_{DDA}	41	GND	66	DG_4	91	V_{DDO}
17	GND	42	NC	67	DG_3	92	GND
18	INVSCK	43	NC	68	DG_2	93	GND
19	CLAMP	44	NC	69	DG_1	94	GND
20	SDA	45	NC	70	DG_0	95	V_{DDA}
21	SCL	46	NC	71	GND	96	$\overline{PWRDN}$
22	A_0	47	NC	72	V_{DDO}	97	V_{REFOUT}
23	A_1	48	NC	73	NC	98	V_{REFIN}
24	V_{DDP}	49	GND	74	NC	99	V_{DDA}
25	V_{DDP}	50	V_{DDO}	75	NC	100	V_{DDA}

Pin Descriptions

Pin Name	Pin No.	Type/Value	Pin Function Description
Converter Channels			
R_{IN}, G_{IN}, B_{IN}	2, 8, 13	Input	**Analog Inputs.**
DR_{7-0}	76–83	Output	**Red Channel A Data Output.**
DG_{7-0}	63–70	Output	**Green Channel A Data Output.**
DB_{7-0}	51–58	Output	**Blue Channel A Data Output.**
Timing Generator			
CLAMP	19	Input	**External Clamp Input.**
INVSCK	18	Input	**Invert Sampling Clock.** Inverts SCK, the internal clock sampling the analog inputs. Supports Alternate Pixel Sampling mode for capture pixel rates up to 216Ms/s.
XCK	32	Input	**External Clock input.** Enabled if register bit, XCKSEL = H. Replaces PXCK clock generated by PLL. If unused, connect to ground through a 10kΩ resistor.
DCK	86	Output	**Output Data Clock.** Clock for strobing output data to external logic.
$\overline{DCK}$	87	Output	**Output Data Clock Inverted.** Inverted clock for strobing output data to external logic.
HSOUT	88	Output	**Horizontal Sync Output.** Reconstructed HSYNC delayed by FMS9874 latency and synchronized with DCK. Leading edge is synchronized to start of data output. Polarity is always active HIGH.
Phase Locked Loop			
HSIN	28	Schmitt	**Horizontal Sync input.** Schmitt trigger threshold is 1.5V. A 5V source should be clamped at 3.3V or current limited to prevent overdriving ESD protection diodes.
COAST	29	Input	**PLL Coast.** Maintain frequency of PLL output clock PXCK, disregarding HSIN. If horizontal sync is missing during the vertical sync interval, PXCK clock frequency can be maintained by asserting COAST.
LPF	33	Passive	**PLL Low Pass Filter.** Connect recommended PLL filter to LPF pin. (see Figure 13.)
Sync Stripper			
ACS_{IN}	7		**Analog Composite Sync Input.** Input to sync stripper with 150mV threshold.
DCS_{OUT}	89		**Digital Composite Sync Output.** Output from sync stripper.
Control			
SDA	20	Bi-directional	**Serial Port Data.** Bi-directional data.
SCL	21	Input	**Serial Port Clock.** Clock input.
A_0	22	Input	**Address bit 0.** Lower bit of serial port address.
A_1	23	Input	**Address bit 1.** Upper bit of serial port address.
$\overline{PWRDN}$	96	Input	**Power Down/Output Control.** Powers down the FMS9874 and tri-states the outputs.

Pin Descriptions

Pin Name	Pin No.	Pin Function Description
Power and Ground		
V_{DDA}	3, 5, 9, 11, 14, 16, 95, 99, 100	**ADC Supply Voltages.** Provide a quiet noise free voltage.
V_{DDP}	24, 25, 31, 36, 38	**PLL Supply Voltage.** Most sensitive supply voltage. Provide a very quiet noise free voltage.
V_{DDO}	50, 60, 62, 72, 85, 91	**Digital Output Supply Voltage.** Decouple judiciously to avoid propagation of switching noise.
GND	1, 4, 6, 10, 12, 15, 17, 26, 27, 30, 35, 37, 39, 40, 41, 49, 59, 61, 71, 84, 90, 92, 93, 94	**Ground.** Returns for all power supplies. Connect ground pins to a solid ground plane.
V_{REFIN}	98	**Voltage Reference Input.** Common reference input to RGB converters. Connect to VREFOUT, if internal reference is used.
V_{REFOUT}	97	**Voltage Reference Output.** Internal band-gap reference output. Tie to ground through a 0.1μF capacitor.

Addressable Memory

Register Map

Name	Address	Function	Default (hex)
$PLLN_{11-4}$	00	**PLL divide ratio, MSBs.** PLLN + 1 = total number of pixels per horizontal line.	69 (1693)
$PLLN_{3-0}$	01	**PLL divide ratio, LSBs.** PLLN + 1 = total number of pixels per horizontal line. $PLLN_{3-0}$ stored in the four upper register bits 7-4. [$PLLN_{3–0}$ | X | X | X | X]	D0 (1693)
GR_{7-0}	02	**Gain, red channel.** Adjustable from 70 to 140%.	80
GG_{7-0}	03	**Gain, green channel.** Adjustable from 70 to 140%.	80
GB_{7-0}	04	**Gain, blue channel.** Adjustable from 70 to 140%.	80
OSR_{5-0}	05	**Offset, red channel.** OSR_{5-0} stored in the six upper register bits 7-2.Default value is decimal 32. [$OSR_{5–0}$ | X | X]	80
OSG_{5-0}	06	**Offset, green channel.** OSR_{5-0} stored in the six upper register bits 7-2. Default value is decimal 32. [$OSG_{5–0}$ | X | X]	80
OSB_{5-0}	07	**Offset, blue channel.** OSR_{5-0} stored in the six upper register bits 7-2. Default value is decimal 32. [$OSB_{5–0}$ | X | X]	80
CD_{7-0}	08	**Clamp delay.** Delay in pixels from trailing edge of horizontal sync.	80
CW_{7-0}	09	**Clamp width.** Width of clamp pulse in pixels.	80
CONFIG 1	0A	**Configuration Register No. 1**	F4
$PHASE_{7-0}$	0B	**Sampling clock phase.** $PHASE_{4-0}$ stored in upper register bits 7-3. PHASE sets the sampling clock phase in 11.25° increments. Default value is decimal 16. [$PHASE_{4–0}$ | X | X | X]	10

Name	Address	Function	Default (hex)
PLLCTRL	0C	**PLL Control**	24
CONFIG 2	0D	**Configuration Register No. 2**	00
	0E	**Reserved**	0X
	0F	**Reserved**	00

Register Definitions

Configuration Register 1 (0A)

Bit no.	Name	Type	Description
0			
1	XCKSEL	R/W	**External Clock Select.** Select internal clock source. **0:** Internal PLL **1:** XCK input.
2	XCLAMPOL	R/W	**External Clamp Polarity.** Select clamp polarity. **0:** Active L. **1:** Active H.
3	XCLAMP	R/W	**External Clamp Select.** Select clamp source. **0:** Internally generated by PLL referenced to HSIN. **1:** External CLAMP input.
4	COASTPOL	R/W	**Coast Polarity.** Select COAST input polarity. **0:** Active L. **1:** Active H.
5	HSPOL	R/W	**HSIN Polarity.** Select horizontal sync input polarity. PLL is locked to selected edge: **0:** Falling edge. **1:** Rising edge.
6	—	R/W	**0:** Default must be 0.
7	—	R/W	**0:** Default must be 0.

PLL Configuration Register (0C)

Bit no.	Name	Type	Description
1-0	—		
4-2	$IPUMP_{2\text{-}0}$	R/W	**Charge Pump Current.** Selects Charge Pump current (µA). (see Table 5. Charge Pump Current Codes) **000:** 50 **001:** 100 **010:** 150 **011:** 250 **100:** 350 **101:** 500 **110:** 750 **111:** 1500
6-5	$FVCO_{1\text{-}0}$	R/W	**VCO Frequency Range.** Selects VCO frequency range (MHz). **00:** 20–90 **01:** 20–90 **10:** 80–108 **11:** —
7	—	R/W	**Reserved.** **0:** Run. **1:** (reserved).

Configuration Register 2 (0D)

Bit no.	Name	Type	Description
0	—	—	**Reserved.** Set to 0.
3-1	REV	R	**Revision Number.** Die revision number.
4	OUTPHASE	W	**Output Data Phase.** In the alternate pixel mode, selects either odd (1, 3, 5, …) or even (2, 4, 6 ….) samples following the HSYNC leading edge to be emitted from output data ports. **0:** Even samples **1:** Odd samples
7-5	-	R/W	**Reserved.** Set to 00.

Functional Description

There are two major sections within the FMS9874 Digitizer:

1. Analog-to-digital Converter Channels, one for each channel, RGB and the voltage reference.
2. Timing and Control comprising the PLL, Timing Generator, Sync Stripper and Serial Interface.

A/D Converter Channels

Each of the three RGB channels consists of:

1. A clamp to set the lower reference level of an AC coupled input.
2. Gain and offset stages to tune the converter to input signal levels.
3. An Analog-to-Digital Converter to digitize the analog input.

Analog Inputs

Input signal range is 500 to 1000mV to support conversion of single-ended signals with a typical amplitude of 700mV p-p. With the clamp active, each input accommodates a negative 300mV excursion.

Inputs are optimized for a source resistance of 37.5 to 75Ω. To reduce noise sensitivity, the ultra-wide 500MHz input bandwidth may be reduced by adding a small series inductor prior to the 75Ω terminating resistor. See Applications Section.

Clamps

If the incoming signals are not ground referenced, a clamp must be used to set the incoming video range relative to ground. Prior to each A/D converter, each channel includes a clamp that allows a capacitively coupled input to be referenced to the A/D converter bottom reference voltage when the clamp pulse is active. Source of the clamp signal is determined by the XCLAMP bit.

Internal clamp timing is generated by the Timing and Control Block. Position and width of the internal clamp pulse, ICLAMP are programmable through registers CD and CW. External clamp input is selected by register bit XCLAMP and the external clamp polarity selected through register bit XCLAMPOL. To disable the clamp for DC coupled inputs, set XCLAMP = 1 with either of these conditions:

1. XCLAMPOL = 0 with input CLAMP = H.
2. XCLAMPOL = 1 with input CLAMP = L.

Best performance will be achieved with the clamp set active for most of the black signal level interval between the trailing edge of horizontal sync and the start of active video. Insufficient clamping can cause brightness changes at the top of the image and slow recovery from large changes in Average Picture Level (APL). Recommended value of CD is 0x10 to 0x20 for most standard video sources.

Analog-to-Digital Converter

Figure 2 is a block diagram of the ADC core with gain and offset functions. $G_{7\text{-}0}$, $OS_{5\text{-}0}$, RGB_{IN} and $PD_{7\text{-}0}$ generically refer to the gain and offset register values, analog input and parallel data output of any RGB channel.

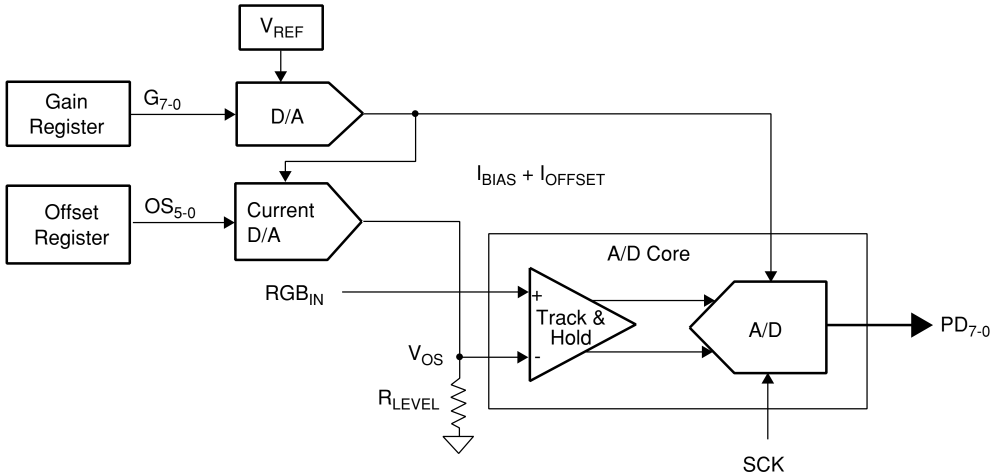


Figure 2. A/D Converter Architecture

Core of the ADC block is a high speed A/D encoder with differential inputs. Within the A/D converter core are the following elements:

1. Differential track and hold.
2. Differential analog-to-digital converter.

Setting the gain register value G_{7-0} (GR_{7-0}, GG_{7-0}, GB_{7-0}), establishes the gain D/A converter voltage which is the A/D reference voltage. Increasing video gain reduces the contrast of the picture since the number of output codes is reduced. Conversion range is defined by the gain setting according to Table 1.

Table 1. Gain Calibration

G_{7-0}	Conversion Range (mV)
0	500
66_h	700
FF_h	1000

A/D Converter sensitivity is:

$$S = \frac{255}{500} \bullet \frac{255}{255 + G_{7-0}} \text{LSB/mV}$$

Offset is set through the Single-Ended to Differential Amplifier which translates the ground referenced input to a differential voltage centered around A/D common mode bias voltage.

The 6-bit Offset D/A converter injects a current into R_{LEVEL} with two components:

1. I_{BIAS} to establish the A/D common mode voltage.
2. I_{OFFSET} to set the offset from the common mode level.

Voltage offset from the common mode voltage at the inverting input of the Track and Hold is:

$$V_{OS} = (OS_{5-0} - 31) \bullet \frac{255 + G_{7-0}}{255} \bullet \frac{500}{255}$$

D/A converter gain tracks A/D gain with 1 LSB of offset corresponding to 1LSB of gain. Increasing the offset of a video signal increases brightness of the picture. Data output from the A/D converter is:

$$D_{7-0} = S \bullet V_{IN} - (OS_{5-0} - 31)$$

Impact of the offset values OSR_{5-0}, OSG_{5-0}, and OSB_{5-0} is shown in Table 2.

Table 2. Offset Calibration

OS_{5-0}	Equivalent Offset (bits)
0	-31_d
$1F_h$	0
FF_h	32_d

Sampling Clock PHASE Adjustment

Picture quality is strongly impacted by the $PHASE_{4-0}$ value. If PHASE is not set correctly, any section of an image consisting of vertical lines may exhibit tearing.

Figure 3 shows how an analog input, $R_{IN}G_{IN}B_{IN}$ is sampled by the rising edge of SCK after a delay PHASE from the rising edge of either PXCK or XCK. SCK can be delayed up to 32 steps in 11.25° increments by adjusting the register value, $PHASE_{4-0}$.

Output data, DCK and $\overline{DCK}$ are delayed in tandem with SCK relative to PXCK or XCK. There is a 5-6$^{1}/_{2}$ clock latency between the data sample S_n and the corresponding data out DA_{7-0}.

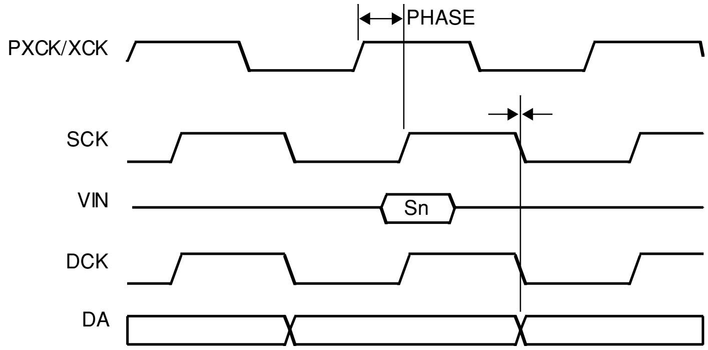


Figure 3. Internal Sampling Clock, SCK Timing

Ideally, incoming pixels would be trapezoidal with fast rise-times and the sampling edge of the A/D clock, SCK would be positioned along the level section of the incoming pixel waveform as shown in Figure 4. There is a narrow zone of uncertainly where sampling during pixel rise time would cause an error in the value of the A/D data output, D_{7-0}, which is shown as a value, 0-255.

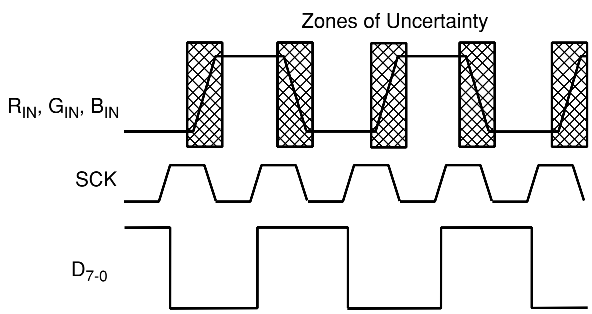


Figure 4. Ideal Pixel Sampling

In practice, high-resolution pixels have long rise-times. As shown in Figure 5, there are narrow zones of serendipity when the pixel amplitude is level. Samples are valid in these zones.

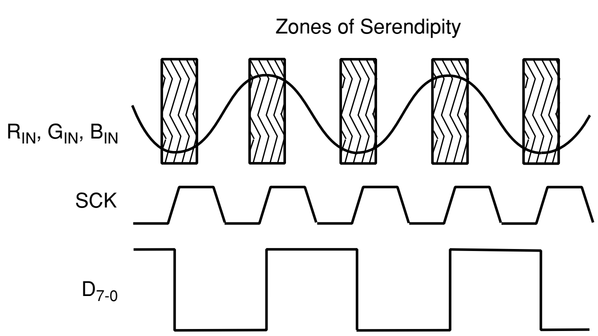


Figure 5. Acceptable Pixel Sampling

Referring to Figure 6, when the sample clock, SCK has some jitter, if the sampling edge occurs anywhere within the zone of uncertainty where the pixel rise time is steep, there will be amplitude modulation of the digitized data, D_{7-0}, due to the sampling clock jitter. To avoid corruption of the image, setting the value $PHASE_{7-0}$ is critical. $PHASE_{4-0}$ should be trimmed to position the sampling edge of SCK within the zone of serendipity.

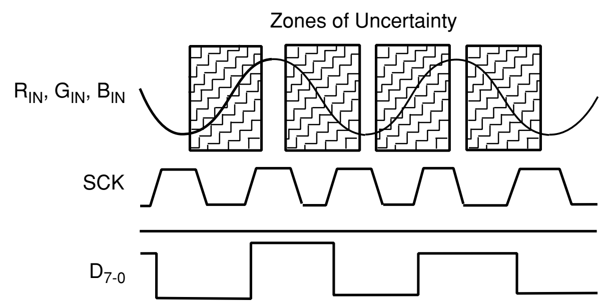


Figure 6. Improper Pixel Sampling

Voltage References

An on-chip voltage reference is generated from a bandgap source. V_{REFOUT} is the buffered output of this source that can be connected to V_{REFIN} to supply a voltage reference that is common to the three converter channels.

V_{REFIN}, with a nominal voltage of 1.25V, is the source of the differential reference voltages for each A/D converter. Reference voltages supplied to the differential inputs of the comparators in the A/D converters are derived from V_{REFIN}.

Digital Data Outputs

Input horizontal sync HSIN and outgoing data, D[7..0] are resynchronized to the delayed sample clock, SCK. Output timing characteristics are defined in Figure 4. Latency of the first pixel, N varies according to the mode:

1. Normal.
2. Alternate pixel sampling.

Levels are 3.3 volt CMOS with the output supply variable between 2.5 and 3.3 V. $\overline{PWRDN}$ = L sets the outputs high-impedance. $\overline{PWRDN}$ = H enables the outputs.

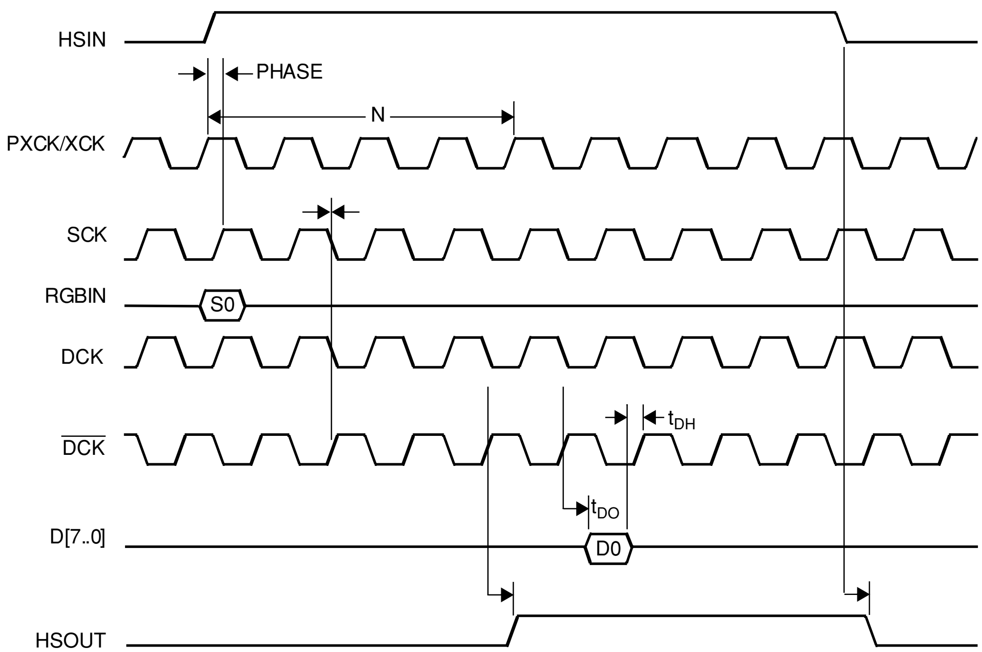


Figure 7. Output Timing

Figures 8 through 10 depict data output timing relative to the sampling clock and inputs for all modes. Timing is referenced to the leading edge of HSIN when the first sample is taken at the rising edge of SCK. Register bit OUTPHASE, determines if odd or even samples are directed to the data ports.

Note the timing of the HSOUT waveform:

1. HSOUT is always active HIGH.
2. Only the leading edge of HSOUT is active or selected by the HSPOL register bit.
3. HSOUT is aligned with DCK.
4. Trailing edge is linked to HSIN.
5. If MSIN does not terminate before mid-line, HSOUT is forced low. A 50% duty cycle indicates that HSPOL is incorrectly set.

HS is the internal sync pulse generated from HSYNC. SCK is the internal A/D converter sampling clock.

Output data transitions are synchronized with the falling edge of DCK. Output data should be strobed on the rising edge of DCK. A 5 to 5.5 clock cycle delay must be flushed before valid data is available.

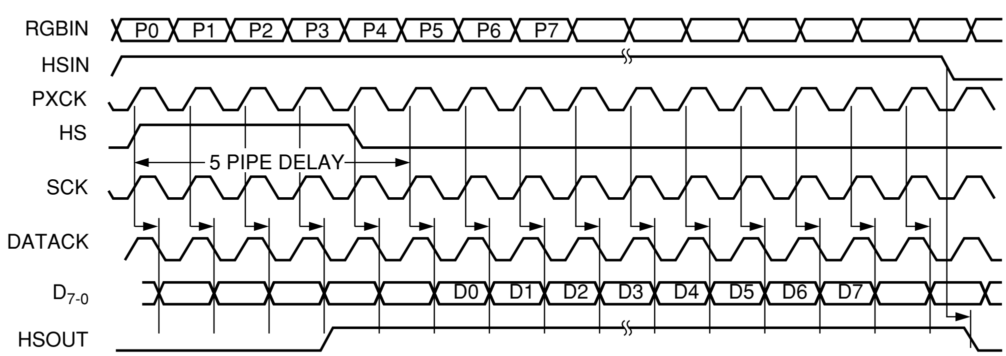


Figure 8. Normal Mode

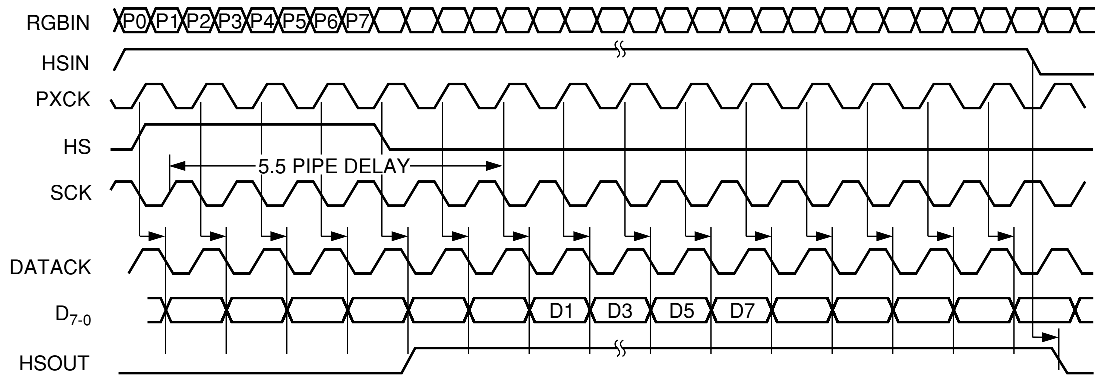


Figure 9. Alternate Pixel Sampling Mode, (Even Pixels)

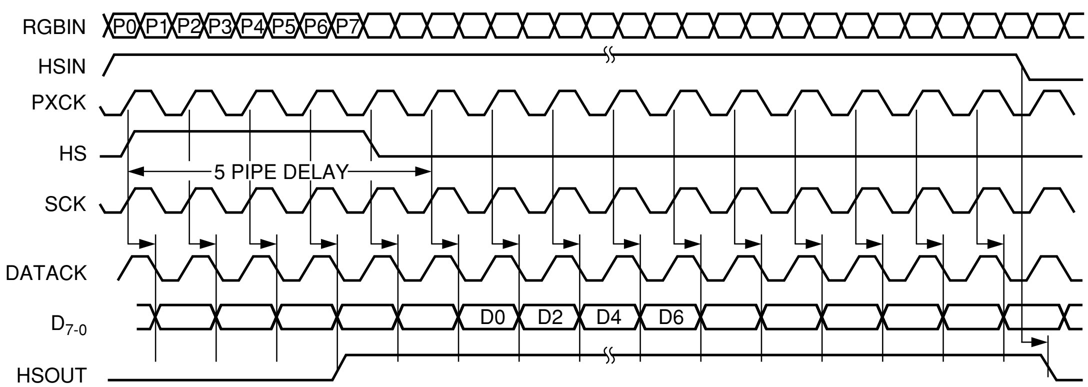


Figure 10. Alternate Pixel Sampling Mode, (Odd Pixels)

Alternate Pixel Sampling Mode

A logic H on the CKINV pin inverts the sampling phase of SCK. In the Alternate Pixel Sampling Mode:

1. The PLL is run at half rate. SCK, DCK and $\overline{DCK}$ are half rate.
2. CKINV is toggled between frames.

O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E
O	E	O	E	O	E	O	E	O	E	O	E

Figure 11. Odd and Even Pixels in a Frame

On one frame, even pixels are sampled. On the other, odd pixels are sampled.

Alternate Pixel Sampling is similar to interlacing used in broadcast video, except that the columns of pixels are interlaced instead of lines.

O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1
O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1	O1	E1

Figure 12. Odd Pixels from Frame 1

```
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
```

Figure 13. Even Pixels from Frame 2

```
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
O1 E2 O1 E2 O1 E2 O1 E2 O1 E2 O1 E2
```

Figure 14. Subsequent Output Combining Frames 2 and 3

```
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
O3 E2 O3 E2 O3 E2 O3 E2 O3 E2 O3 E2
```

Figure 15. Combined Frames 2 and 3

Timing and Control

Timing and Control logic encompasses the PLL, Timing Generator and Sync Stripper.

Phase Locked Loop

Two clock types originate in the PLL:

1. Data clocks DCK and $\overline{DCK}$.
2. Internal sampling clock SCK.

DCK and $\overline{DCK}$ are used to strobe data from the FMS9874 to following digital circuits. SCK is the ADC sample clock which has adjustable phase controlled through the PHASE register. DCK and $\overline{DCK}$ are phase aligned with SCK.

Reference for the PLL is the horizontal sync input, HSIN with polarity selected by the HSPOL bit.

Frequency of the HS_{IN} input is multiplied by the value PLLN + 1 derived from the $PLLN_{11-4}$ and $PLLN_{3-0}$ registers. PLLN + 1 should equal the number of pixels per horizontal line including active and blanked sections. Typically blanking is 20–30% of active pixels. Divide ratios from 2–4095 are supported. SCK, DCK and $\overline{DCK}$ run at a rate PLLN + 1 times the HS_{IN} frequency.

The PLL consists of a phase comparator, charge pump VCO and ÷N counter, with the charge pump connected through the LPF pin to an external filter. These elements must be programmed to match the incoming video source to be captured.

Values of IPUMP and FVCO for Standard VESA timing parameters are shown in Table 3. Timing of many computer video outputs does not comply with VESA recommendations. PLLN should be optimized to avoid vertical noise bars on the displayed image.

Modes marked 2X are 2X-oversampled modes where the number of samples per horizontal line is doubled. To select this mode, the Phase-locked Loop Divide Ratio value must changed from PLL_{1x} to:

$$PLL_{2x} = 2 \bullet (PLL_{1x} + 1) - 1$$

Values of IPUMP and FVCO are set through the PLL Configuration Register (0x0C). Recommended external filter components are shown in Figure 16. RF quality ±10% ceramic capacitors with X7R dielectric are recommended.

Table 3. Recommended IPUMP and FVCO values for Standard Display Formats[1]

Standard	Resolution	Refresh Rate	Horizontal Frequency	Sample Rate	$FVCO_{1-0}$	$IPUMP_{2-0}$
VGA	640 X 480	60 Hz	31.5 kHz	25.175 MHz	01	100
		72 Hz	37.7 kHz	31.500 MHz	01	100
		75 Hz	37.5 kHz	31.500 MHz	01	100
		85 Hz	43.3 kHz	36.000 MHz	01	100
2X	640 X 480	60 Hz	31.5 kHz	50 MHz	01	100
		67 Hz	35 kHz	62.5 MHz	01	100
		72 Hz	37.7 kHz	63 MHz	01	100
		75 Hz	37.5 kHz	63 MHz	01	100
	720 X 400	70 Hz	31.5 kHz	56.6 MHz	01	100
SVGA	800 X 600	56 Hz	35.1 kHz	36.000 MHz	01	111
		60 Hz	37.9 kHz	40.000 MHz	01	111
		72 Hz	48.1 kHz	50.000 MHz	01	111
		75 Hz	46.9 kHz	49.500 MHz	01	111
		85 Hz	53.7 kHz	56.250 MHz	01	

Table 3. Recommended IPUMP and FVCO values for Standard Display Formats[1] (continued)

Standard	Resolution	Refresh Rate	Horizontal Frequency	Sample Rate	$FVCO_{1-0}$	$IPUMP_{2-0}$
XGA	1024 X 768	60 Hz	48.4 kHz	65.000 MHz	01	111
		70 Hz	56.5 kHz	75.000 MHz	01	111
		75 Hz	60.0 kHz	78.750 MHz	10	111
		80 Hz	64.0 kHz	85.500 MHz		
		85 Hz	68.3 kHz	94.500 MHz		
SXGA	1280 X 1024	60 Hz	64.0 kHz	108.000 MHz	10	111

Notes:
1. VESA Monitor Timing Standards and Guidelines, September 17, 1998 and others.

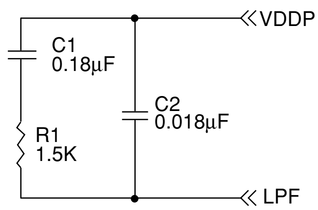


Figure 16. Schematic, PLL Filter.

Loop performance is established by setting:

1. VCO frequency range through $FVCO_{1-0}$. (see Table 4)
2. Charge Pump Current through $IPUMP_{2-0}$. (see Table 5)
3. External loop filter component values.

Table 4. VCO Frequency Bands

$FVCO_{2-0}$	Frequency Range (MHz)	KVCO (MHz/V)
00	20–90	60
01		
10	75–108	90
11	—	—

Table 5. Charge Pump Current Levels

$IPUMP_{2-0}$	Current (µA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

Setting $SPHASE_{4-0}$ selects the sampling phase of SCK relative to PXCK in 32 steps of 11.25°. Phase of the output data, DCK and $\overline{DCK}$ is slaved to the SCK phase.

COAST = H disables PLL lock to HSIN, while the VCO frequency is retained. VCO frequency remains stable over several lines without updates from HSIN. COAST can be connected directly to the vertical sync signal or supplied by the graphics controller.

RMS Clock jitter is less than 3% of pixel period in all operating modes. At lower frequencies below 40MHz, the jitter rises but can be reduced by over-sampling at a 2X clock rate. See Performance section for jitter specifications and plots.

COAST

COAST = H disables PLL lock to HSIN, while the VCO frequency is retained. VCO frequency remains stable over several lines without updates from HSIN. COAST can be connected directly to the vertical sync signal or supplied by the graphics controller.

Operation of COAST is depicted in Figure 17. HSOUT polarity is always positive. When COAST = L, HSOUT tracks HSIN (shown with postive polarity in Figure 1):

1. HSOUT rising edge tracks HSIN delayed by a few pixels.
2. HSOUT falling edge tracks the trailing edge of HSIN with no delay.

When COAST = H, the PLL flywheels, disregarding the incoming HSIN references, while the HSOUT waveform depends upon the state of HSIN.

1. If HSIN = H:
   - a.) HSOUT rising edge remains locked to the PLL.
   - b.) HSOUT trailing edge falls after 50% of the HSOUT period has expired.
2. HSIN transitions:
   - a.) HSOUT rising edge remains locked to the PLL.
   - b.) HSOUT falling edge is terminated by the trailing edge of HSIN.
3. If HSIN = L, then HSOUT = L

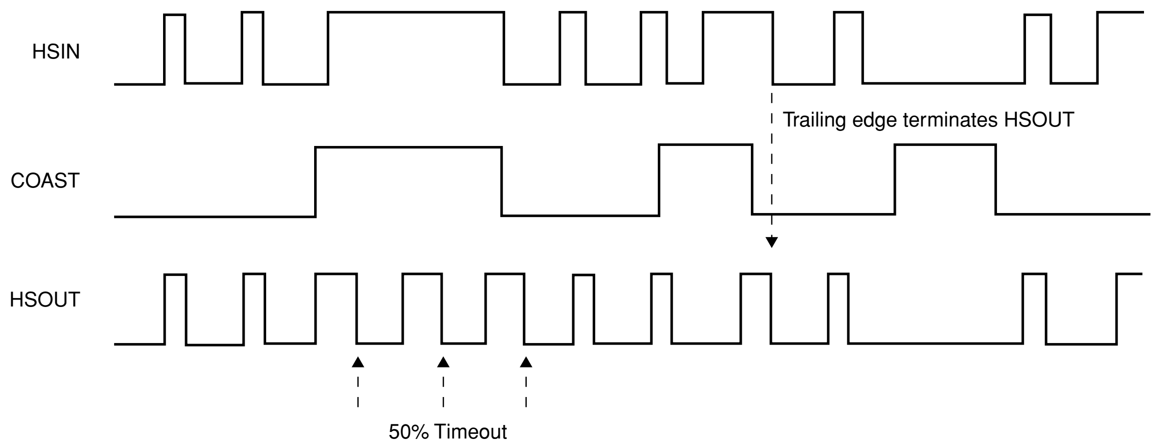


Figure 17.

Timing Generator

Timing and Control logic generates:

1. Internal sampling clock, SCK.
2. Output data clocks, DCK and $\overline{DCK}$.
3. Output horizontal sync, HS_{OUT}.
4. Internal clamp pulse, ICLAMP.

With HSPOL set correctly, ICLAMP delay follows the trailing edge of horizontal sync in (HSIN). Delay is set by the CD register. Width of ICLAMP is set by the CW register. Range of CD and CW values is 1–255 pixels.

Sync Stripper

Some video signals include embedded composite sync rather than separate horizontal and vertical sync signals, typically sync on green. Composite sync is extracted from Composite Video at the ACS_{IN} pin.

When the ACS_{IN} signal falls below a 150mV ground referenced threshold, sync is detected. Composite Sync Output, DCS_{OUT} reflects the ACS_{IN} sync timing with non-inverted CMOS digital levels.

Power Down

$\overline{PWRDN}$ = L minimizes FMS9874 power consumption. Data outputs become high impedance. Clocks generation is stopped. Register contents are maintained. Sync stripping and the internal voltage reference function.

Serial Interface

Register access is via a 2-wire I^2C/SMBus compatible interface. As a slave device, the 7-bit address is selected by the A_{1-0} pins (see Table 6). Serial port pins SDA and SCL communicate with the host SMBus/I^2C controller which act as a master.

Since the serial control port is design to interface with 3.3V logic, the pins must be protected by series connected 150Ω resistors if SDA and SCL signals originate from 5V logic. (See Applications Section)

Table 6. Serial Interface Address Codes

A_{1-0}	7-Bit Address
00	4C
01	4D
10	4E
11	4F

Two signals comprise the bus: clock (SCL) and bi-directional data (SDA). When receiving and transmitting data through the serial interface, the FMS9874 acts as a slave, responding only to commands by the I^2C/SMBus master.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA may change only when SCL = L. An SDA transition while SCL = H is interpreted as a start or stop signal.

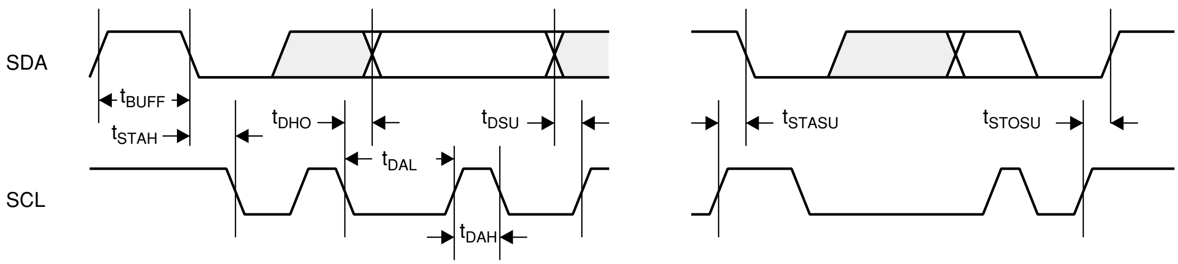


Figure 18. Serial Bus: Read/Write Timing

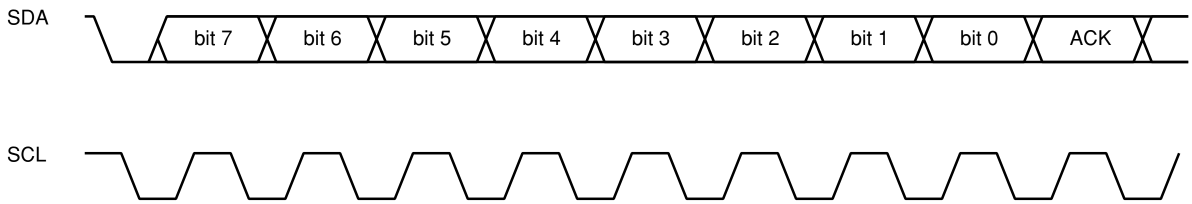


Figure 19. SerialBus: Typical Byte Transfer

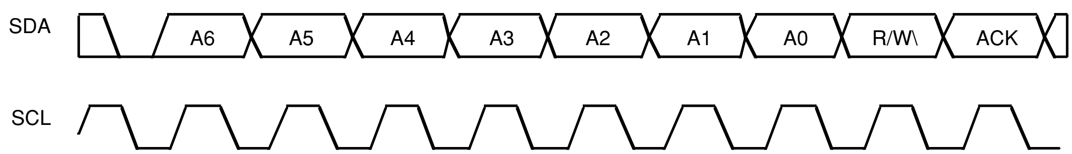


Figure 20. Serial Bus: Slave Address with Read/$\overline{\text{Write}}$ Bit

There are five steps within an I^2C/SMBus cycle:

1. Start signal
2. Slave address byte
3. Pointer register address byte
4. Data byte to read or write
5. Stop signal

When the Serial Bus interface is inactive, SCL = H and SDA = H. Communications are initiated by sending a start signal (Figure 14, left waveform) that is a HIGH-to-LOW transition on SDA while SCL is HIGH. A start signal alerts all slaved devices that a data transfer sequence is imminent.

After a start signal, the first eight bits of data comprise a seven bit slave address followed a single R/W bit (Read = H, Write = L) to set the direction of data transfer: read from; or write to the slave device. If the transmitted slave address matches the address of the FMS9874 which set by the state of the ADD pin, the FMS9874 acknowledges by pulling SDA LOW on the 9th SCL pulse (see Figure 16). If the addresses do not match, the FMS9874 does not acknowledge.

For each byte of data read or written, the MSB is the first bit of the sequence.

Data Transfer via Serial Interface

If a slave device, such as the FMS9874 does not acknowledge the master device during a write sequence, SDA remains HIGH so the master can generate a stop signal. During a read sequence, if the master device does not acknowledge by bringing SDA = L, the FMS9874 interprets SDA = H as "end of data." SDA remains HIGH so the master can generate a stop signal.

To write data to a specific FMS9874 control register, three bytes are sent:

1. Write the slave address byte with bit $R/\overline{W}$ = L.
2. Write the pointer byte.
3. Write to the control register indexed by the pointer.

After each byte is written, the pointer auto-increments to allow multiple data byte transfers within one write cycle.

Data is read from the control registers of the FMS9874 in a similar manner, except that two data transfer operations are required:

1. Write the slave address byte with bit $R/\overline{W}$ = L.
2. Write the pointer byte.
3. Write the slave address byte with bit $R/\overline{W}$ = H
4. Read the control register indexed by the pointer.

After each byte is read, the pointer auto-increments to allow multiple data byte transfers within one read cycle.

Preceding each slave write, there must be a start cycle. Following the pointer byte there should be a stop cycle. After the last read, there must be a stop cycle comprising a LOW-to-HIGH transition of SDA while SCL is HIGH. (see Figure 18, right waveform)

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Examples below show how serial bus cycles can be linked together for multiple register read and write access cycles. For sequential register accesses, each ACK handshake initiates further SCL clock cycles from the master to transfer the next data byte.

Write to one register

1. Start signal
2. Slave Address byte ($R/\overline{W}$ bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Stop signal

Write to four consecutive registers

1. Start signal
2. Slave Address byte ($R/\overline{W}$ bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Data byte to (base address + 1)
6. Data byte to (base address + 2)
7. Data byte to (base address + 3)
8. Stop signal

Read from one register

1. Start signal
2. Slave Address byte ($R/\overline{W}$ bit = LOW)
3. Pointer byte (= base address)
4. Stop signal (optional)
5. Start signal
6. Slave Address byte ($R/\overline{W}$ bit = HIGH)
7. Data byte from base address
8. Stop signal

Read from four registers

1. Start signal
2. Slave Address byte ($R/\overline{W}$ bit = LOW)
3. Pointer byte (= base address)
4. Stop signal (optional)
5. Start signal
6. Slave Address byte ($R/\overline{W}$ bit = HIGH)
7. Data byte from base address
8. Data byte from (base address + 1)
9. Data byte from (base address + 2)
10. Data byte from (base address + 3)
11. Stop signal

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{CC} (Measured to GND)	-0.5		4	V
Digital Inputs				
Applied voltage (Measured to GND)[2]	-0.3		V_{DDA}	V
Forced current [3, 4]	-5.0		5.0	mA
Analog Inputs				
Applied Voltage (Measured to GND)[2]	-0.5		V_{DDA}	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
Applied voltage (Measured to GND)[2]	-0.5			V
Forced current [3, 4]	-6.0		6.0	mA
Forced current [3, 4]	-8.0		8.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DDA}	ADC Power Supply Voltage	3.0	3.3	3.6	V
V_{DDP}	PLL Power Supply Voltage	3.0	3.3	3.6	V
V_{DDO}	Output Power Supply Voltage	2.2	3.3	3.6	V
T_A	Ambient Temperature, Still Air	0		70	°C
	A/D analog input range, min.			500	mV p-p
	A/D analog input range, max.	1000			mV p-p

Electrical Characteristics[1]

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
I_{DDA}	Supply current, ADC	Operating, 25°C		211		mA
I_{DDD}	Supply current[2], Digital Output	Operating, 25°C		47		mA
I_{DDP}	Supply current, PLL	Operating, 25°C		30		mA
P_D	Power dissipation	0 to 70°C		800		mW
I_{PD}	Power-down current	0 to 70°C		23		mA
P_{DD}	Powered-down disspation	0 to 70°C		10		mW
Digital Inputs/Outputs						
C_I	Input Capacitance	25°C		3		pF
I_{IH}	Input Current, HIGH	0 to 70°C	-1			µA
I_{IL}	Input Current, LOW	0 to 70°C			+1	µA
V_{IH}	Input Voltage, HIGH	0 to 70°C	2.5			V
V_{IL}	Input Voltage, LOW	0 to 70°C			0.8	V
I_{OHD}	Output Current, HIGH, data	0 to 70°C		4		mA
I_{OHC}	Output Current, HIGH, clock	0 to 70°C		8		mA
I_{OLD}	Output Current, LOW, data	0 to 70°C		4		mA
I_{OLC}	Output Current, LOW, clock	0 to 70°C		8		mA
V_{OH}	Output Voltage, HIGH	I_{OH} = max., 0 to 70°C	V_{DDO}–0.1			V
V_{OL}	Output Voltage, LOW (V_{DD3})	I_{OL} = max., 0 to 70°C			0.1	V
Serial Bus I/O						
V_{SMIH}	Input Voltage, HIGH	0 to 70°C	2.5			V
V_{SMIL}	Input Voltage, LOW	0 to 70°C			0.8	V
V_{SMOL}	Output Voltage, LOW	I_{SMOL} = max.			0.1	V
I_{SMOH}	Output Current, HIGH	0 to 70°C				µA
I_{SMOL}	Output Current, HIGH	0 to 70°C				mA
Analog Inputs						
I_B	Input bias current	0 to 70°C			1	µA
E_{OS}	Input Offset Voltage	0 to 70°C		7	50	mV
Reference Output						
	Output Voltage	0 to 70°C	1.20	1.25	1.30	V
	Temperature Coefficient	0 to 70°C		±50		ppm/°C

Notes:

1. Unless otherwise stated, 0 to 70°C
2. DCK, $\overline{DCK}$ load = 15 pF; data load = 5 pF.

Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Unit
Analog-to-Digital Converters						
	Conversion rate	0 to 70°C	10		108	Ms/s
t_{SKEW}	Data to clock skew	0 to 70°C	-0.5		2.0	ns
Timing Generator						
	HSIN input frequency	0 to 70°C	15		110	kHz
	Maximum PLL clock rate	0 to 70°C	108			MHz
	Minimum PLL clock rate	0 to 70°C			20	MHz
	PLL Jitter[1]	25°C	1.8			µs p-p
	Sampling phase tempco	0 to 70°C		15		ps/°C
Serial Bus Interface						
tDAL	SCL Pulse Width, LOW	0 to 70°C		4.7		µs
tDAH	SCL Pulse Width, HIGH	0 to 70°C		4.0		µs
tSTAH	SDA Start Hold Time	0 to 70°C		4.0		µs
tSTASU	SCL to SDA Setup Time (Stop)	0 to 70°C		4.7		µs
tSTOSU	SCL to SDA Setup Time (Start)	0 to 70°C		4.0		µs
tBUFF	SDA Stop Hold Time Setup	0 to 70°C		4.7		µs
tDSU	SDA to SCL Data Setup Time	0 to 70°C		250		ns
tDHO	SDA to SCL Data Hold Time	0 to 70°C		0		ns

Notes:

1. FVCO = 10, IPUMP = 110, PLLN = 1375_{10}.

System Performace Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
Analog to Digital Converter						
E_{LI}	Integral Linearity Error	25°C	-1.4	±0.8	1.4	LSB
		0 to 70°C	-2.5		2.5	LSB
E_{LD}	Differential Linearity Error	25°C	-1.0	±0.5	1.15	LSB
		0 to 70°C	-1.0		1.25	LSB
	Missing Codes	0 to 70°C			0	
	Input full scale matching	0 to 70°C		5		%FS
	Offset adjustment range	0 to 70°C		25		%FS
	Gain tempco	25°C		280		ppm/°C
B_W	Analog bandwidth, full power	25°C		500		MHz
	Transient response	25°C		2		ns
t_{OV}	Over-voltage recovery time	25°C		1.5		ns
SNR	SNR without harmonics			45		dB

System Performace Characteristics (continued)

Parameter			Conditions	Min	Typ[1]	Max	Unit
Phase Locked Loop							
t_{PP}	Peak-to-peak PLL Jitter @ MHz	25.175	25°C		7.1		ns
		31.5			6.9		
		36			6.5		
		40			4.6		
		49.5			2.8		
		56.25			2.4		
		66			2.2		
		78.75			2.1		
		108			1.8		
t_{RMS}	RMS PLL Jitter @ MHz	25.175	25°C		900		ps
		31.5			700		
		36			600		
		40			600		
		49.5			400		
		56.25			300		
		66			300		
		78.75			250		
		108			250		
Thermal							
θ_{JC}	Resistance, junction-to-case						°C/W
θ_{JA}	Resistance, junction-to-ambient				44		°C/W

Notes:
1. External pixel clock.

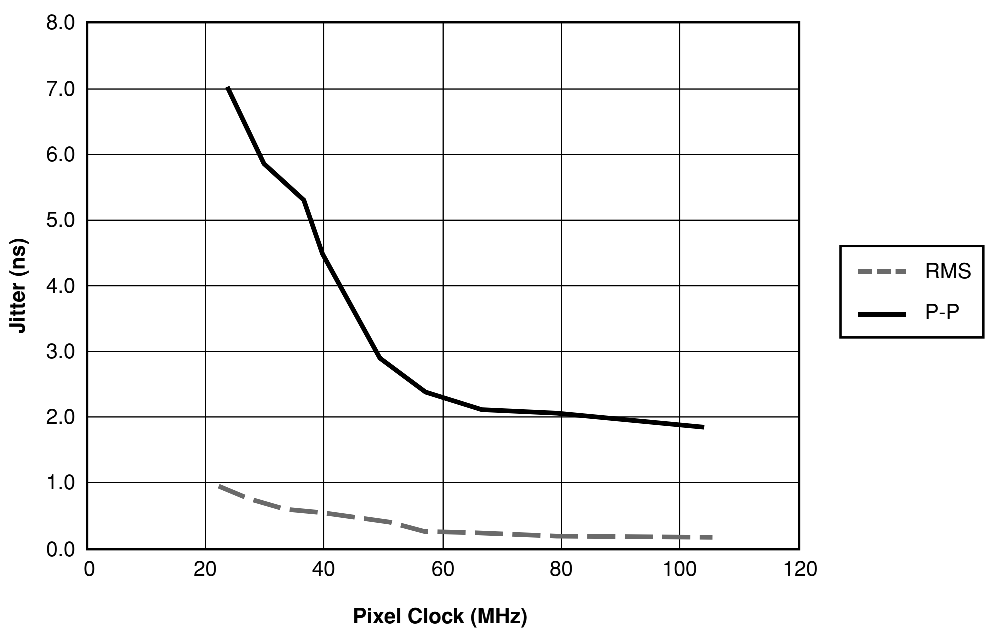


Figure 21. Pixel Clock Jitter vs. Frequency

Applications Information

To minimize component count, use of the following on-chip circuits is recommended:

1. ADC sampling clock.
2. Clamp.
3. Voltage reference

Optimum PLL Configuration Register (address 0x0C) settings for typical graphics modes are listed in Table 3. Unless otherwise indicated, all modes are compliant with VESA specifications. For unlisted modes, values should be adjusted to optimize performance.

By adjusting the values in the gain (GR, GG, GB) and offset (OSR, OSG, OSB) registers, the input conversion range can be matched to the incoming analog signals.

AC Coupled Digitizer

Shown in Figure 22 is an implementation of a video digitizer with AC coupled RGB inputs. Horizontal sync input, HS is passed through a voltage divider which attenuates the 5.0 V logic HIGH excursion to the 3.3 V HIGH input level of the FMS9874. Vertical sync is also attenuated to make the VSOUT level compatible with 3.3 V pixel processing following the FMS9874.

Output data is three channel 24-bit pixels with a maximum rate of 140Ms/s. Data is clocked out on the negative edge of DCK. HSOUT defines the active video along a line, while incoming vertical sync, VSIN is propagated as VSOUT to the output data to synchronize handling of digitized frames of output data.

Control is through the serial port with 150Ω resistors inserted to allow interfacing with 5V logic. If the serial bus is operates with 3.3V levels, these resistors are unnecessary.

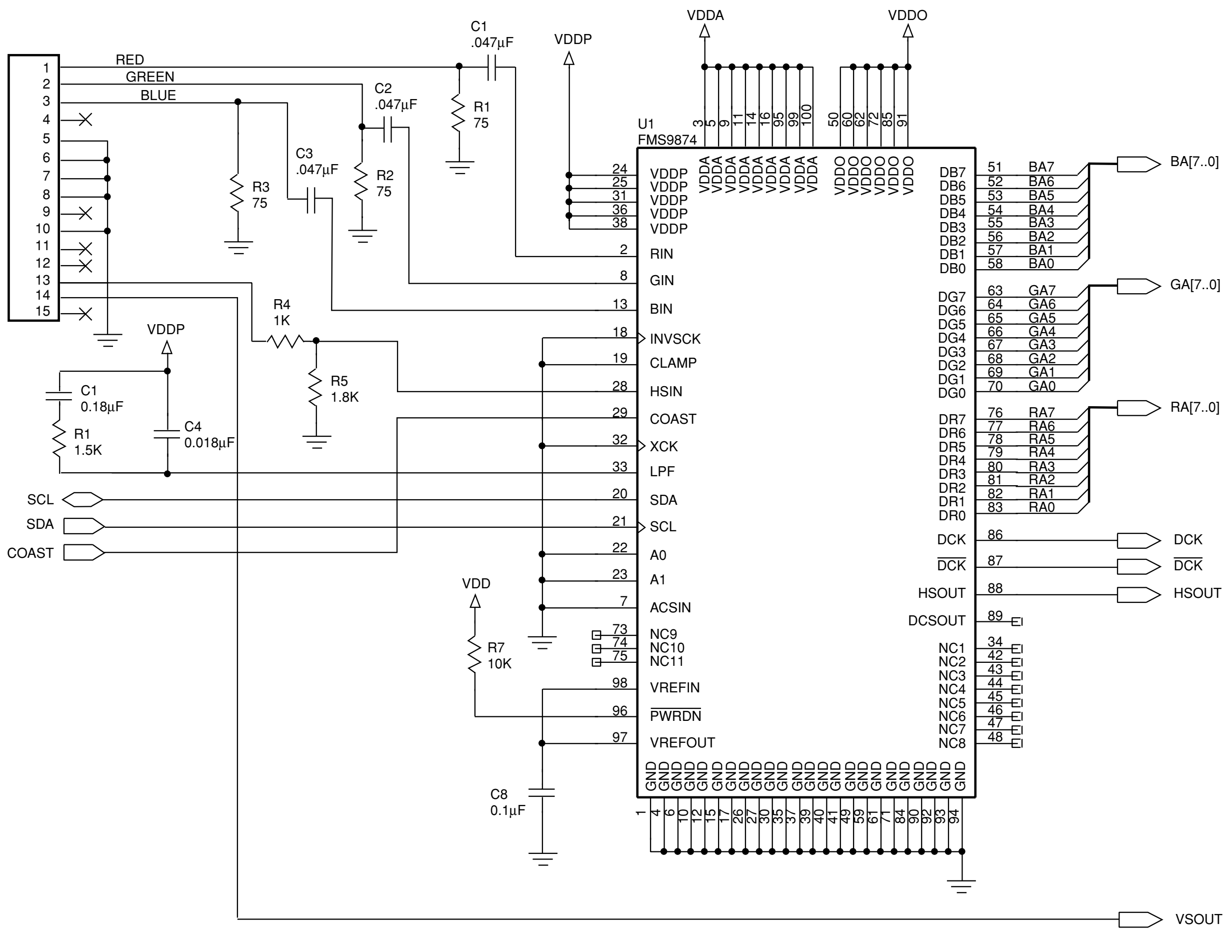


Figure 22. Schematic, VGA Digitizer, AC Coupled RGB

Printed Wiring Board Design Guidelines

Recommended strategy is to mount the FMS9874 over a ground plane with carefully routed analog inputs and digital outputs. All connections should be treated as transmission lines to ensure that reflections due to mismatches are minimized and ground return currents do not interfere with critical signals.

Analog Inputs

Recommendations:

1. Keep analog trace lengths short to minimize crosstalk.
2. Terminate analog inputs with 75Ω resistors, placed close to the FMS9874 analog inputs, R_{IN}, G_{IN} and B_{IN}. By matching transmission line impedances, reflections will be minimized.
3. Layout traces as 75Ω transmission lines.
4. Avoid running analog traces near digital traces. Due to the wide input bandwidth (500MHz) digital noise can easily leak into analog inputs.
5. If necessary, limit bandwidth by adding a ferrite bead in series with each RGB input as shown in Figure 23. A Fair-Rite #2508051217Z0 is recommended. Further bandwidth reduction using a shunt 10pF capacitor may reduce snow (intensity noise) caused by HF noise riding on the RGB input. Mismatches, reflections and noise may cause ringing or distortion of the incoming video signals.
6. Locate the PLL filter clear of other signals.
7. Bypass the reference with a 0.1μF capacitor to ground.

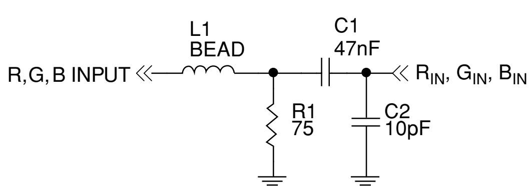


Figure 23. RGB Input Filter Option

Digital I/O

Recommendations:

1. Route digital I/O signals clear of analog inputs.
2. Terminate clock lines to reduce reflections. Treat clock lines as transmission lines.
3. Scale the HSIN input to 3.3V, using a resistor network or a series 1 kΩ resistor.
4. Limit Serial Port inputs SDA and SDL with 150Ω resistors connected directly to the pins.
5. If necessary terminate the HSIN input with 330/220Ω.
6. If necessary, to reduce reflections, EMI or spikes add a 50–200Ω resistor at each data output pin.
7. To minimize noise within the FMS9884A, restrict the capacitive load at the digital outputs to < 10pF.

Power and Ground

A schematic of the recommended power distribution is shown in Figure 24. Note that:

1. Analog and digital circuits are layed out over a common solid ground plane.
2. Each FMS9874 pin is decoupled with a 0.1μF capacitor.
3. A group of pins may be de-coupled through a common capacitor if no pin is more than 5 mm from the capacitor.
4. A separate regulated supply is used for the phase-locked loop power supply, V_{DDP}.
5. Capacitors are attached to each PLL pin or pin-pair.

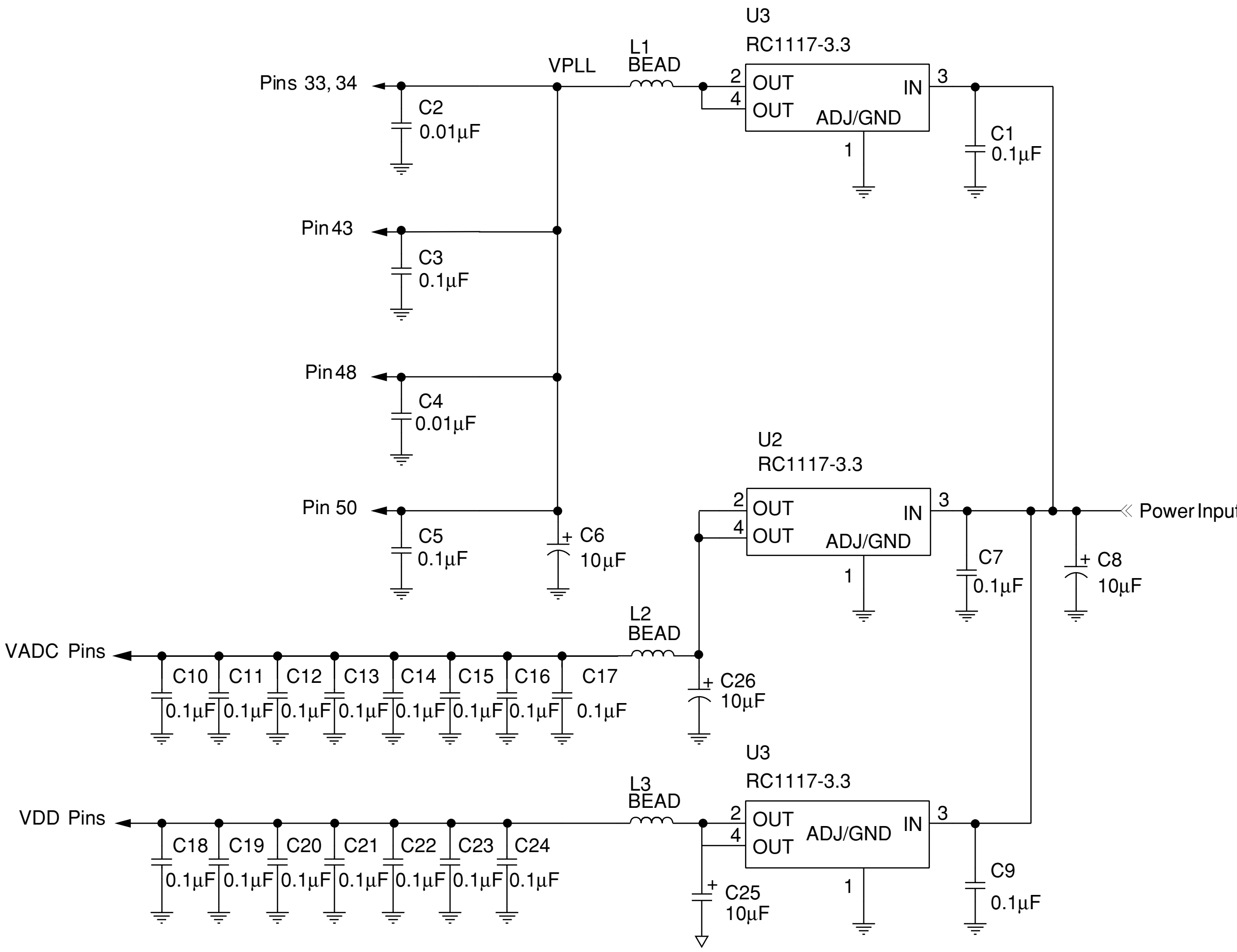


Figure 24. Recommended Power Distribution

Physical placement of PLL power supply decoupling components is critical. Bearing in mind the following suggestions:

1. All components should be placed in close proximity to the FMS9874 pins.
2. Routing through vias should be avoided, if possible.
3. Each V_{DDP}/GND pin pair: 24&25/26, 31/30, 36/35, and 38/37 should be decoupled with a 100–1000p/10µF pair of capacitors (see Figure 24). If board space is limited, use as many capacitor pairs as possible.
4. Use Fair-rite 274 301 9447 bead.

Firmware

Best performance can be achieved by correctly setting the FMS9874 registers. Here are some recommendations:

1. Set the value of PLLN equal to the number of pixels to be sampled minus one. With this setting, the number of samples per horizontal line equals the number of pixels. If PLLN + 1 does not equal the number of pixels, there will be irregular intensities on text and an interference pattern on a vertical grill pattern.
2. Calibrate Offset and Gain by first setting each input to 0mV. Then adjust OSR, OSG, and OSB to set each RGB data output D_{7-0} = 0x00. Next with 700mV input, adjust GR, GG and GB so that each RGB data output D_{7-0} = (same value), typically 240 decimal.
3. Clamp registers, CD and CW, should be programmed to maximize the period of the clamp during the backporch, while not encroaching into the sync or active video periods.
4. PHASE must be trimmed to minimize onscreen snow (intensity noise) when a vertical grill pattern is displayed.
5. FVCO must be set to encompass the incoming frequency range.
6. IPUMP must be set to minimize intensity noise.

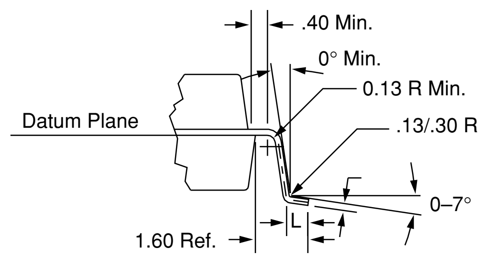
Mechanical Dimensions

100-Lead MQFP (KG) Package

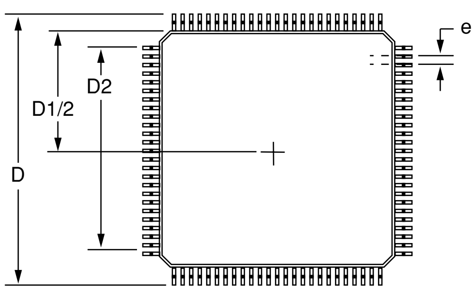
Symbol	Millimeters			Notes
	Min.	Typ.	Max	
A	—	2.82	3.00	
A1	—	0.15	—	
A2	2.62	2.67	2.77	3, 5
D	17.20 BSC			
D1	14.00 BSC			
D2	12.00 BSC			
L	0.73	0.88	1.03	4
N	100			
e	0.50 BSC			
b	0.17	—	0.27	

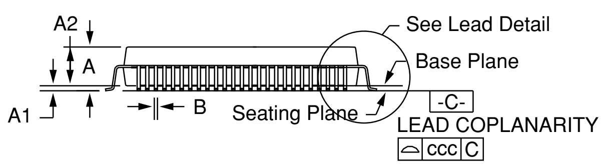
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1994.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254mm per side.
3. "N" is the number of terminals, 25 per side.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm in excess of the "b" dimension at the maximum material condition.



Lead Detail





Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
FMS9874KGC100	0°C to 70°C	Commercial	100 Lead MQFP	9874KGC100

11/10/00 0.0m 003
Stock#DS30009874