a

Current-Output Serial-Input, 16-/14-Bit DAC

Preliminary Technical Data — AD5543/AD5553

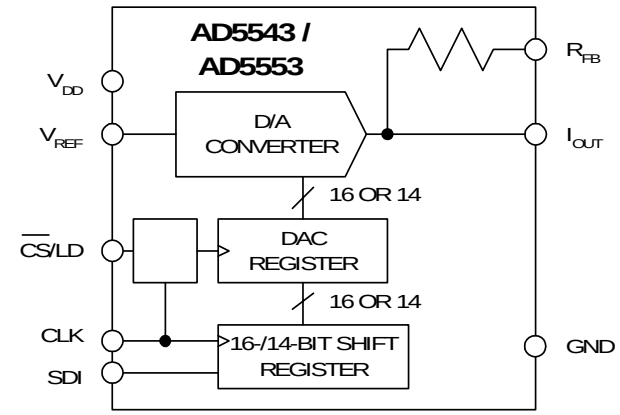
FEATURES

16-bit Resolution AD5543
14-btt Resolution AD5553
±1 LSB DNL
±1, ±2 or ±4 LSB INL
2mA Full Scale Current ± 20%, with V_{REF}=10V
0.5µs Settling Time
4Q Multiplying Reference-input
3-Wire Interface
Ultra Compact uSOIC-8 Package

APPLICATIONS

Automatic Test Equipment
Instrumentation
Digitally Controlled Calibration
Industrial Control PLCs

FUNCTIONAL DIAGRAMS



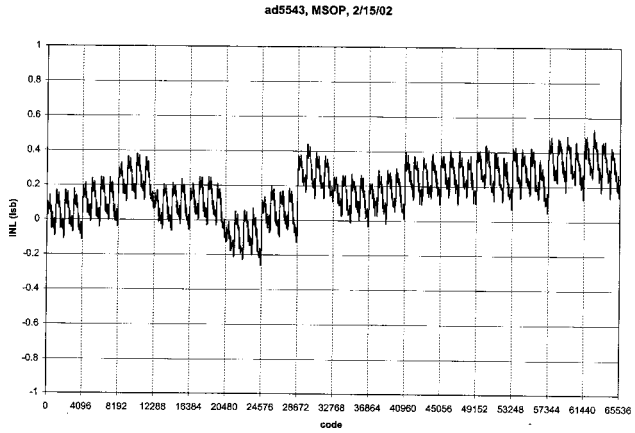


Figure 1. Integral Nonlinearity Error Plot

GENERAL DESCRIPTION

The AD5543, 16-bit, current-output, digital-to-analog converter is designed to operate from a single +5 volt supply.

The applied external reference input voltage VREF determines the full-scale output-current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I to V precision amplifier.

A serial-data interface offers high-speed, three-wire micro controller compatible inputs using serial-data-in (SDI), clock (CLK), and ($\overline{CS}$/LD).

The AD5543/AD5553 are packaged in the space saving SO-8, and the ultra compact (3x4.7mm) uSOIC-8.

ORDERING GUIDE

MODEL	INL (LSB)	RES (LSB)	TEMP RANGE	Package Description	Package Option
AD5543CR	±1	16	-40 / +85°C	SO-8	R-8
AD5543BR	±2	16	-40 / +85°C	SO-8	R-8
AD5543BRM	±2	16	-40 / +85°C	uSOIC-8	RM-8
AD5553CRM	±1	14	-40 / +85°C	uSOIC-8	RM-8

The AD5543 contains xxxx transistors.
The die size measures 53 mil X 73 mil, 3,879 sqmil.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD5543/AD5553

ELECTRICAL CHARACTERISTICS at V_{DD} = 5V±10%, V_{SS} = 0V, I_{OUT} = Virtual GND, GND=0V, V_{REF} = 10V, T_A = Full Operating temperature Range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
STATIC PERFORMANCE[1]				
Resolution	N	1 LSB = $V_{REF}/2^{16}$ = 153µV when V_{REF} = 10V AD5543	16	Bits
Resolution	N	1 LSB = $V_{REF}/2^{14}$ = 610µV when V_{REF} = 10V AD5553	14	Bits
Relative Accuracy	INL	Grade: AD5543C, AD5553C	±1	LSB max
Relative Accuracy	INL	Grade: AD5543B	±2	LSB max
Differential Nonlinearity	DNL	Monotonic	±1	LSB max
Output Leakage Current	I_{OUT}	Data = 0000_H, T_A = 25°C	10	nA max
Output Leakage Current	I_{OUT}	Data = 0000_H, T_A = T_A MAX	20	nA max
Full-Scale Gain Error	G_{FSE}	Data = $FFFF_H$	±1/±4	mV typ/max
Full-Scale Tempco[2]	TCV_{FS}		1	ppm/°C typ
REFERENCE INPUT				
V_{REF} Range	V_{REF}		-15/+15	V min/max
Input Resistance	R_{REF}		5	k ohm typ[4]
Input Capacitance[2]	C_{REF}		5	pF typ
ANALOG OUTPUT				
Output Current	I_{OUT}	Data = $FFFF_H$	2	mA typ
Output Capacitance[2]	C_{OUT}	Code Dependent	200	pF typ
LOGIC INPUTS & OUTPUT				
Logic Input Low Voltage	V_{IL}		0.8	V max
Logic Input High Voltage	V_{IH}		2.4	V min
Input Leakage Current	I_{IL}		10	µA max
Input Capacitance[2]	C_{IL}		10	pF max
INTERFACE TIMING [2, 3]				
Clock Input Frequency	f_{CLK}		40	MHz
Clock Width High	t_{CH}		10	ns min
Clock Width Low	t_{CL}		10	ns min
CS to Clock Set Up	t_{CSS}		0	ns min
Clock to CS Hold	t_{CSH}		10	ns min
Data Setup	t_{DS}		5	ns min
Data Hold	t_{DH}		10	ns min
SUPPLY CHARACTERISTICS				
Power Supply Range	$V_{DD\ RANGE}$		4.5/5.5	V min/max
Positive Supply Current	I_{DD}	Logic Inputs = 0V	10	µA max
Power Dissipation	P_{DISS}	Logic Inputs = 0V	0.055	mW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	%/% max

NOTES:

1. All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP177 I-to-V converter amplifier. The AD5543 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C
2. These parameters are guaranteed by design and not subject to production testing.
3. All input control signals are specified with $t_R = t_F$ = 2.5ns (10% to 90% of +3V) and timed from a voltage level of 1.5V.
4. All AC Characteristic tests are performed in a closed loop system using an OP42 I-to-V converter amplifier.

ELECTRICAL CHARACTERISTICS at V_{DD} = 5V±10%, I_{OUT} = Virtual GND, GND=0V, V_{REF} = 10V, T_A = Full Operating Temperature Range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
AC CHARACTERISTICS				
Output Voltage Settling Time	t_S	To ±0.1% of Full Scale, Data = 0000_H to $FFFF_H$ to 0000_H	0.5	µs typ
Reference Multiplying BW	BW	V_{REF} = $5V_{P-P}$, Data = $FFFF_H$	4	MHz typ
DAC Glitch Impulse	Q	V_{REF} = 0V, Data 0000_H to 8000_H to 0000_H	7	nV-s typ
Feed Through Error	V_{OUT}/V_{REF}	Data = 0000_H, V_{REF} = 100mVrms, same channel	-65	dB
Digital Feed Through	Q	$\overline{CS}$ = 1, and f_{CLK} = 1MHz	7	nV-s typ
Total Harmonic Distortion	THD	V_{REF} = $5V_{P-P}$, Data = $FFFF_H$, f=1KHz	–73	dB typ
Output Spot Noise Voltage	e_N	f = 1kHz, BW = 1Hz	4	nV/ rt Hz

NOTES:

1. All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP177 I-to-V converter amplifier. The AD5543 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C
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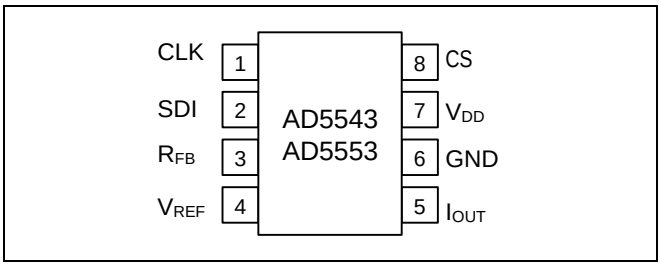
ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... –0.3V, +8V
V_{REF} to GND .....–18V, 18V
Logic Inputs to GND..... –0.3V, +8V
$V(I_{OUT})$ to GND .....–0.3V, V_{DD} + 0.3V
Input Current to Any Pin except Supplies..... ±50mA
Package Power Dissipation ..... $(T_{J\ MAX} – T_A)/ THETA_{JA}$
Thermal Resistance $THETA_{JA}$
8-lead Surface Mount (SO-8)..... 100°C/W
Maximum Junction Temperature ($T_{J\ MAX}$) ..... 150°C
Operating Temperature Range
Models A, B, C .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature:
R-8, RM-8 (Vapor Phase, 60 secs)..... +215°C
R-8, RM-8 (Infrared, 15 secs) ..... +220°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



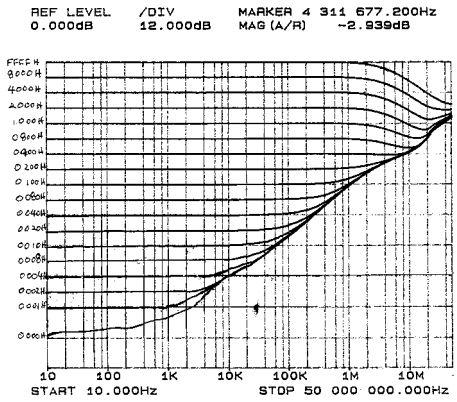


Figure 2. Reference Multiplying Bandwidth

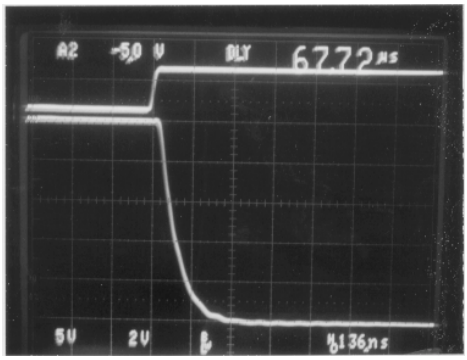


Figure 3. Settling time

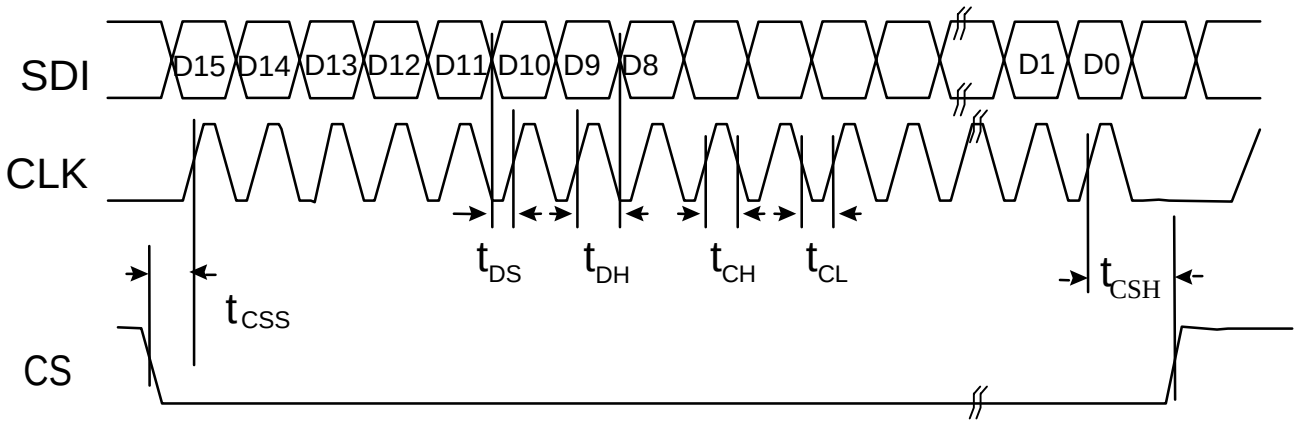


Figure 2. Timing Diagram

Table 1. Control-Logic Truth Table

CLK	$\overline{CS}$	Serial Shift Register Function	DAC Register
X	H	No Effect	Latched
↑+	L	Shift-Register-Data advanced one bit	Latched
X	H	No Effect	Latched
X	↑+	Shift-Register-Data transferred to DAC Register	New Data loaded from Serial Register

Notes:
1. ↑+ positive logic transition; X Don't Care

Table 2. AD5543 Serial Input Register Data Format; Data is loaded in the MSB-First Format.

	MSB															LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 3. AD5553 Serial Input Register Data Format; Data is loaded in the MSB-First Format.

	MSB													LSB
Bit Position	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A full 16-bit data word can be loaded into the DAC serial input register, but only the last 14-bits entered will be transferred to the DAC register when $\overline{CS}$ returns to logic high.

PIN DESCRIPTION

PIN#	Name	Function
1	CLK	Clock input, positive-edge triggered clocks data into shift register.
2	SDI	Serial Register Input, data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	R_{FB}	Internal matching Feedback Resistor. Connect to external opamp output.
4	V_{REF}	DAC reference input pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
5	I_{OUT}	DAC current-output. Connects to inverting terminal of external precision I to V opamp
6	GND	Analog & Digital Ground.
7	V_{DD}	Positive power supply input. Specified range of operation +5V ±10%.
8	$\overline{CS}$	Chip Select, active low digital input. Transfers shift-register data to DAC register on rising edge. See truth table for operation.

CIRCUIT OPERATION

The AD5543/AD5553 contains a 16-/14-bit, current-output, digital-to-analog converter, a serial input register, and a DAC register. Both parts use a 3-wire serial data interface.

D/A Converter Section

The DAC architecture uses a current-steering R-2R ladder design. Figure 3 shows the typical equivalent DAC. The DAC contains a matching feedback resistor for use with an external I to V converter amplifier. The R_{FB} pin is connected to the output of the external amplifier. The I_{OUT} terminal is connected to the inverting input of the external amplifier. These DACs are designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches ON and OFF. Note that a matching switch is used in series with the internal 5K-ohm feedback resistor. If users are attempting to measure the value of R_{FB}, power must be applied to V_{DD} in order to achieve continuity. The V_{REF} input voltage and the digital data (D) loaded into the corresponding DAC register according to equation [1 &2] determines the DAC output voltage:

$V_{OUT} = -V_{REF} * D / 65{,}536$ Equation 1

$V_{OUT} = -V_{REF} * D / 16{,}384$ Equation 2

Note that the output full-scale polarity is opposite to the V_{REF} polarity for DC reference voltages.

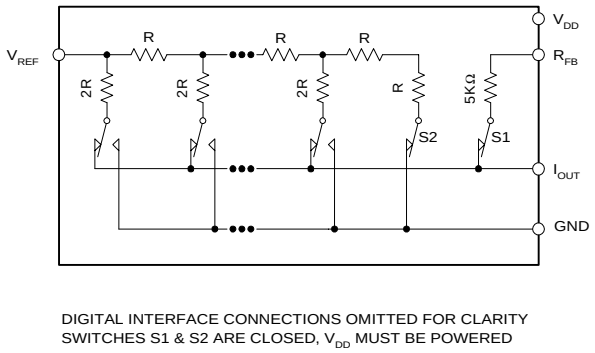


Figure 3. Equivalent R-2R DAC Circuit

These DACs are also designed to accommodate AC reference input signals. The AD5543 will accommodate input reference voltages in the range of -12 to +12 volts. The reference voltage inputs exhibit a constant nominal input-resistance value of 5K ohms, ±30%. The DAC output (I_{OUT}) is code-dependent producing various output resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the AD5543 on the amplifiers inverting input node. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. In order to maintain good analog performance, power supply bypassing of 0.01uF in parallel with 1uF is recommended. Under these conditions clean power supply voltages (low ripple, avoid switching supplies) appropriate for the application should be used. It is best to derive the AD5543's +5V supply from the systems analog supply voltages. (Don't use the digital 5V supply). See figure 4.

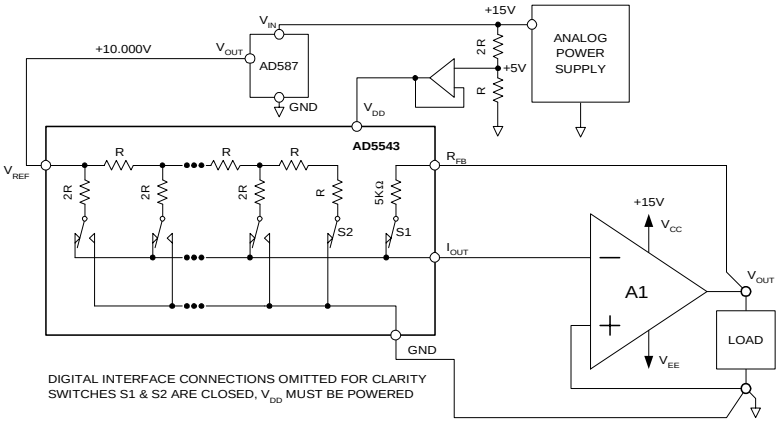


Figure 4. Recommended System Connections

SERIAL DATA INTERFACE

The AD5543 uses a 3-wire ($\overline{CS}$/LD, SDI, CLK) serial data interface. New serial data is clocked into the serial input register in a 16-bit data-word format. The MSB bit is loaded first. Table 2 defines the 16 data-word bits. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the INTERFACE TIMING SPECIFICATIONS. Only the last 16-bits clocked into the serial register will be interrogated when the $\overline{CS}$ pin is strobed to transfer the serial register data to the DAC register. Since most micro controllers' output serial data in 8-bit bytes, two right justified data bytes can be written to the AD5543. After loading the serial register the rising edge of $\overline{CS}$ transfers the serial register data to the DAC register, during this strobe the CLK should not be toggled.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection Zeners connected to ground (GND) and V_{DD} as shown in figure 7.

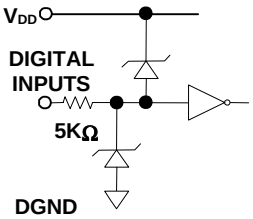


Figure 7. Equivalent ESD Protection Circuits

APPLICATIONS

The AD5543 is inherently a 2-Quadrant multiplying D/A converter. That is, it can be easily set up for Unipolar output operation. The full-scale output polarity is the inverse of the reference-input voltage.

In some applications it may be necessary to generate the full 4-Quadrant multiplying capability or a bipolar output swing. This is easily accomplished using an additional external amplifier (A2) configured as a summing amplifier, see figure 8. In this circuit the second amplifier (A2) provides a gain of 2 which increases the output span magnitude to 20 volts. Biasing the external amplifier with a 10V offset from the reference voltage results in a full 4-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero (V_{OUT} = -10V) to midscale (V_{OUT} = 0V) to full-scale (V_{OUT} = +10V).

$$V_{OUT} = (D / 32768 - 1) * V_{REF} \qquad \text{Equation 3}$$

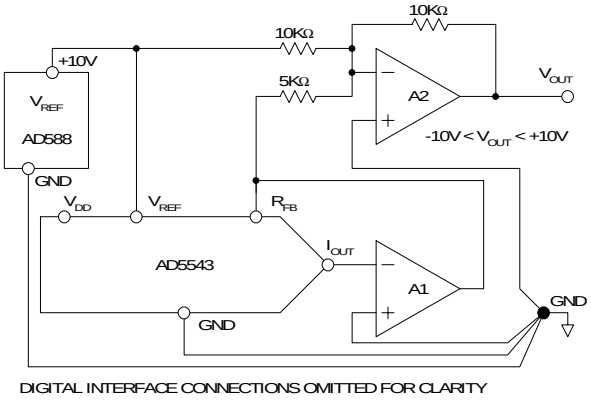


Figure 8. Four-Quadrant Multiplying Application Circuit

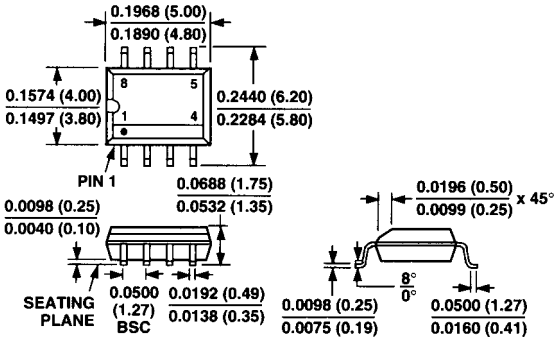
PCB Layout Recommendations

A star ground approach should be used as shown in figure 8. The PCB metal traces between V_{REF} and R_{FB} should match in order to minimize gain error.

Mechanical Outline Dimensions

Dimensions shown in inches and (mm).

8-Lead SOIC (SO-8)



8-Lead microSOIC (RM-8)