NEC

MOS FIELD EFFECT TRANSISTOR
2SK2355, 2SK2355-Z/2SK2356, 2SK2356-Z

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2355, 2SK2355-Z/2SK2356, 2SK2356-Z is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-Resistance
  2SK2355: $R_{DS(on)}$ = 1.4 Ω (V_{GS} = 10 V, I_D = 2.5 A)
  2SK2356: $R_{DS(on)}$ = 1.5 Ω (V_{GS} = 10 V, I_D = 2.5 A)
- Low C_{iss} C_{iss} = 670 pF TYP.
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

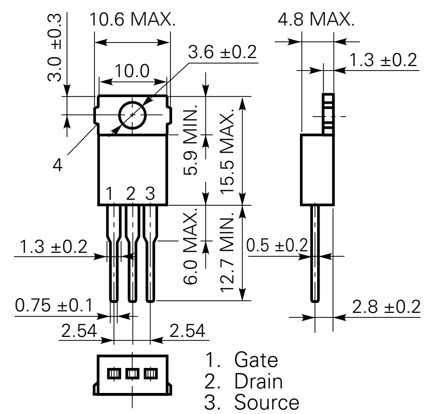
Drain to Source Voltage (2SK2355/2356)	V_{DSS}	450/500	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±5.0	A
Drain Current (pulse)*	$I_{D(pulse)}$	±20	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	50	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current**	I_{AS}	5.0	A
Single Avalanche Energy**	E_{AS}	17.4	mJ

* PW ≤ 10 μs, Duty Cycle ≤ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

PACKAGE DIMENSIONS

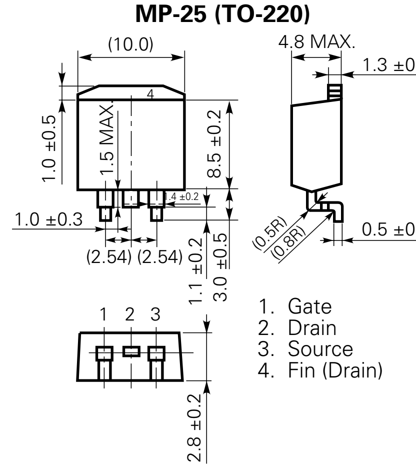
(in millimeter)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

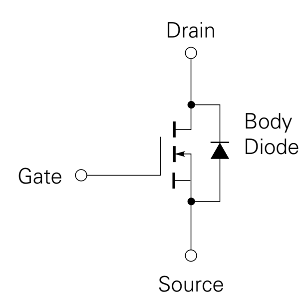
JEDEC: TO-220AB

MP-25 (TO-220)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

MP-25Z (TO-220 SURFACE MOUNT TYPE)



The information in this document is subject to change without notice.

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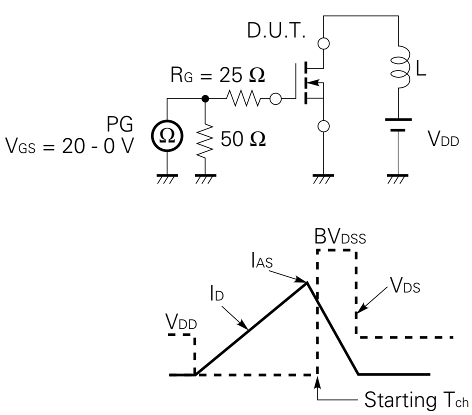
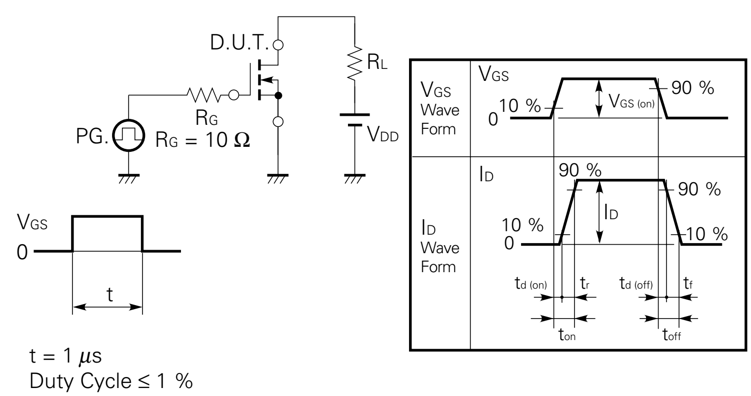
ELECTRICAL CHARACTERISTICS (T_A = 25 ˚C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-Resistance	$R_{DS(on)}$		0.9	1.4	mΩ	V_{GS} = 10 V	2SK2355
			1.0	1.5		I_D = 2.5 A	2SK2356
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA	
Forward Transfer Admittance	$\mid y_{fs} \mid$	1.0			S	V_{DS} = 10 V, I_D = 2.5 A	
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = V_{DSS}, V_{GS} = 0	
Gate to Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±30 V, V_{DS} = 0	
Input Capacitance	C_{iss}		670		pF	V_{DS} = 10 V	
Output Capacitance	C_{oss}		140		pF	V_{GS} = 0	
Reverse Transfer Capacitance	C_{rss}		18		pF	f = 1 MHz	
Turn-On Delay Time	$t_{d(on)}$		11		ns	I_D = 2.5 A	
Rise Time	t_r		8		ns	V_{GS} = 10 V	
Turn-Off Delay Time	$t_{d(off)}$		40		ns	V_{DD} = 150 V	
Fall Time	t_f		8		ns	R_G = 10 Ω R_L = 60 Ω	
Total Gate Charge	Q_G		20		nC	I_D = 5.0 A	
Gate to Source Charge	Q_{GS}		4.5		nC	V_{DD} = 400 V	
Gate to Drain Charge	Q_{GD}		9		nC	V_{GS} = 10 V	
Body Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 5.0 A, V_{GS} = 0	
Reverse Recovery Time	t_{rr}		270		ns	I_F = 5.0 A, V_{GS} = 0	
Reverse Recovery Charge	Q_{rr}		1.0		nC	di/dt = 50 A/μs	

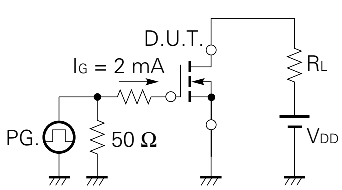
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time



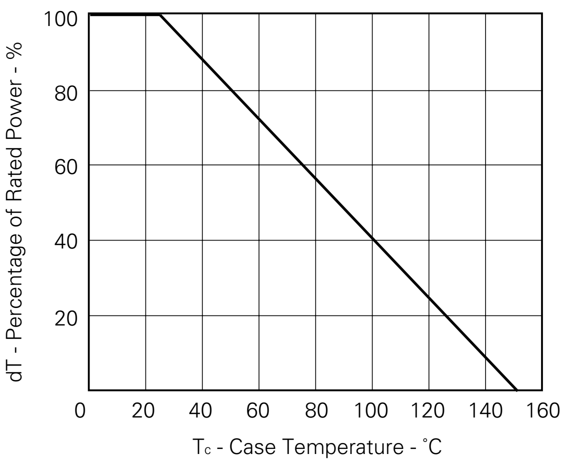
Test Circuit 3 Gate Charge



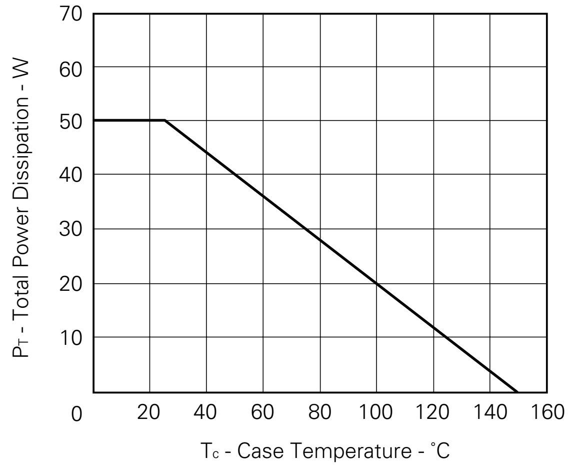
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (T_A = 25 °C)

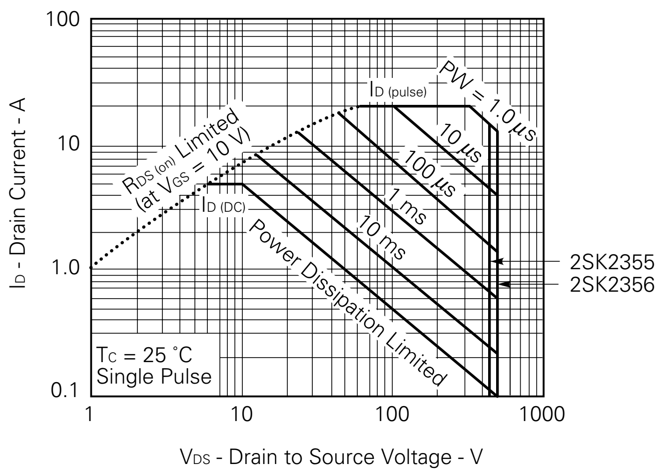
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



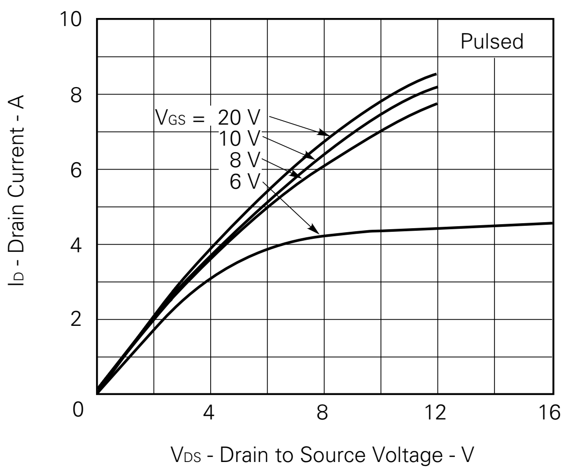
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



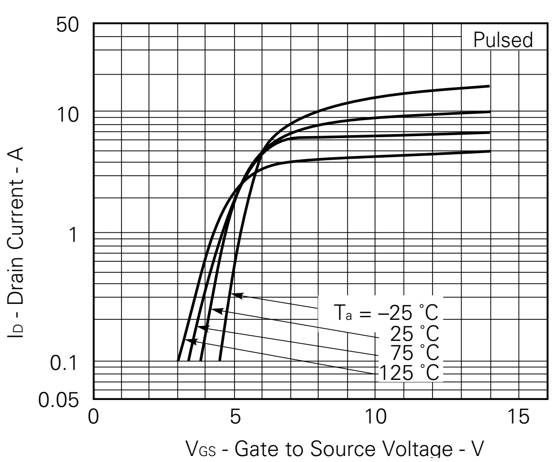
FORWARD BIAS SAFE OPERATING AREA



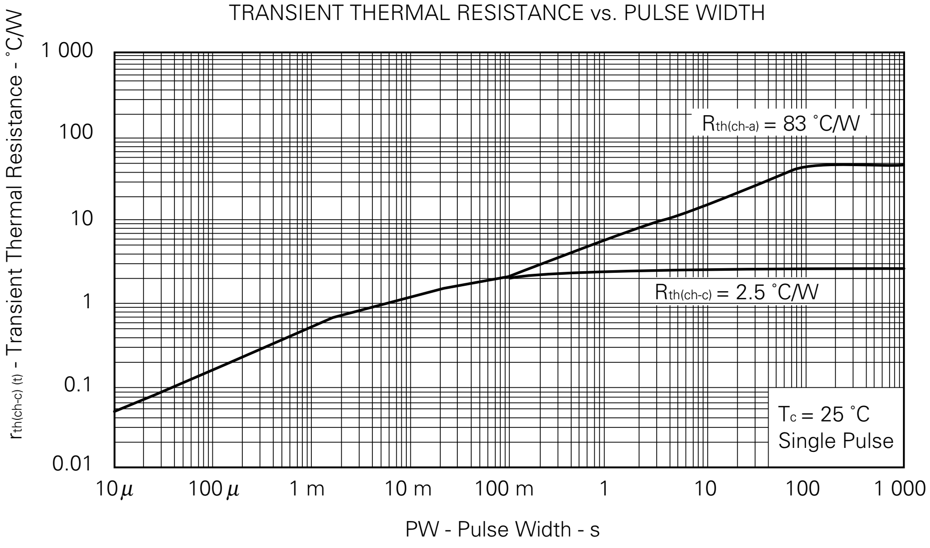
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



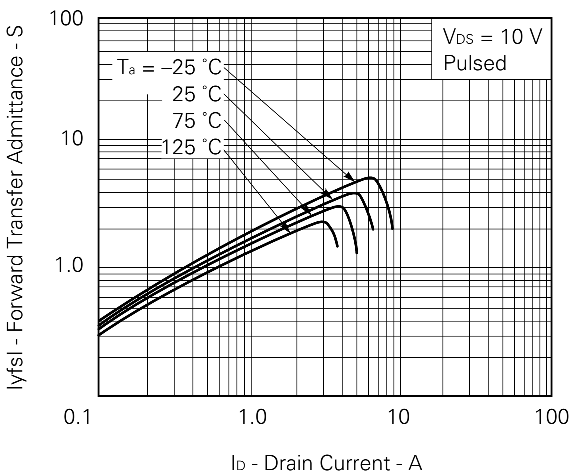
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



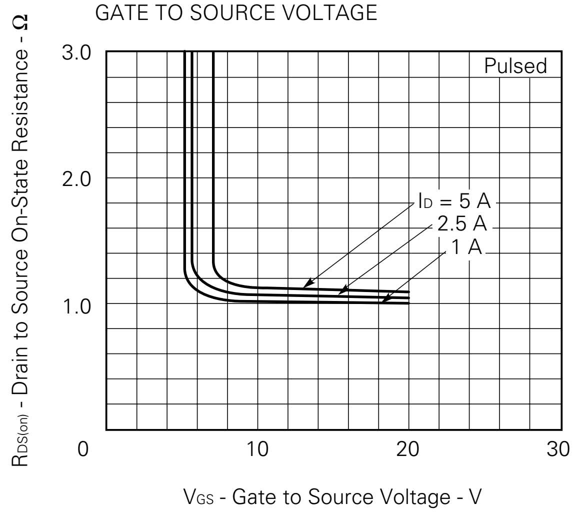
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



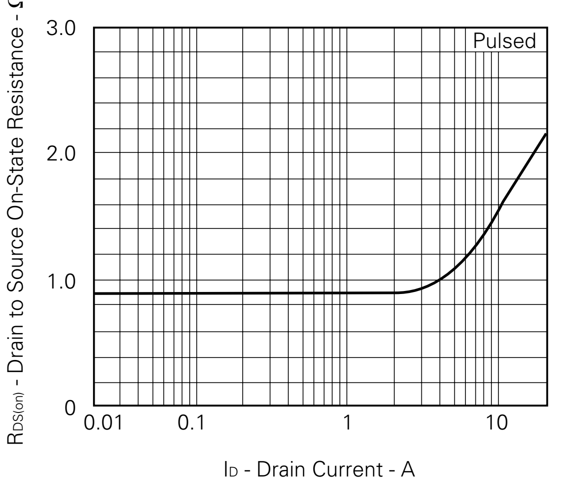
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



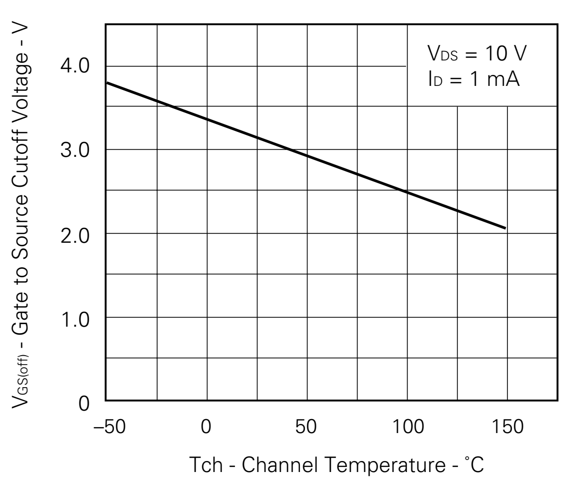
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



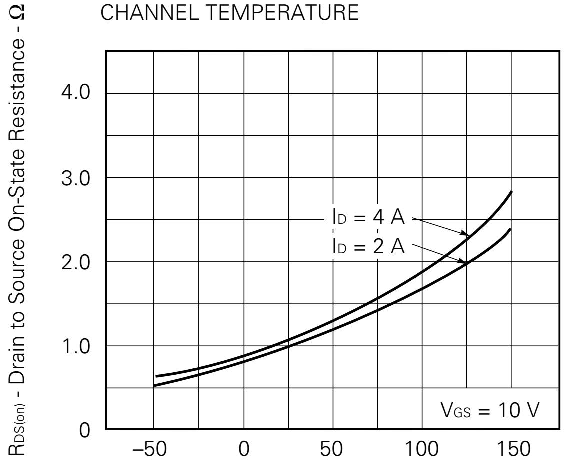
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



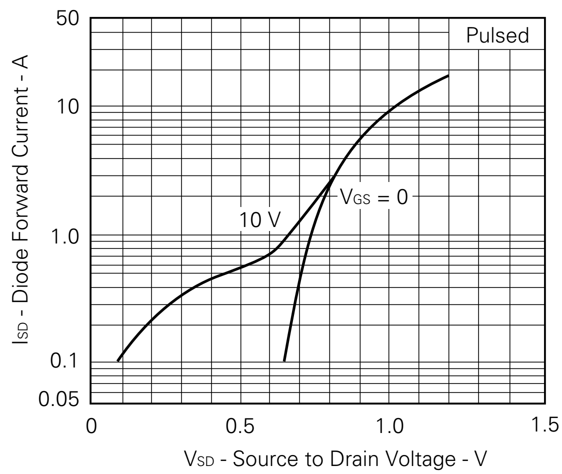
GATE TO SOURCE CUTOFF VOLTAGE vs.
CHANNEL TEMPERATURE



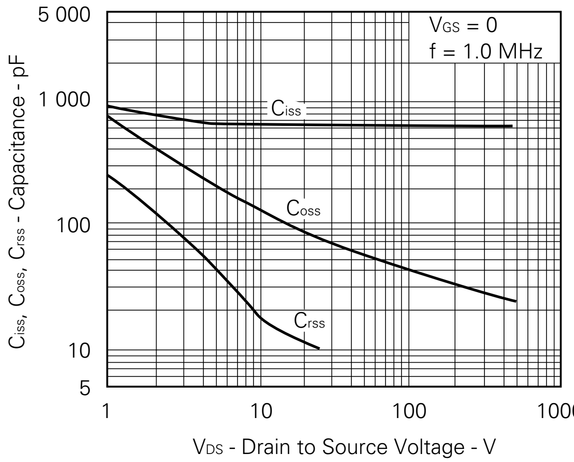
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



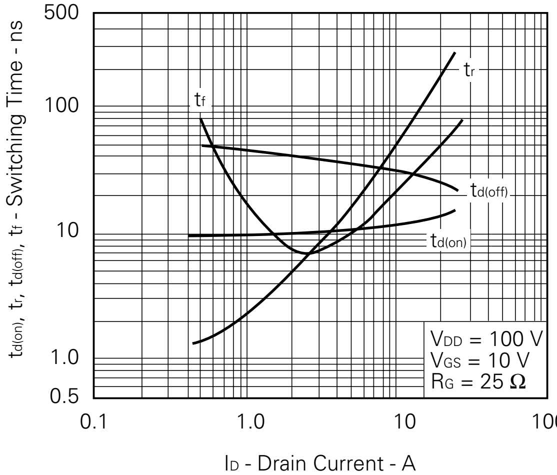
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



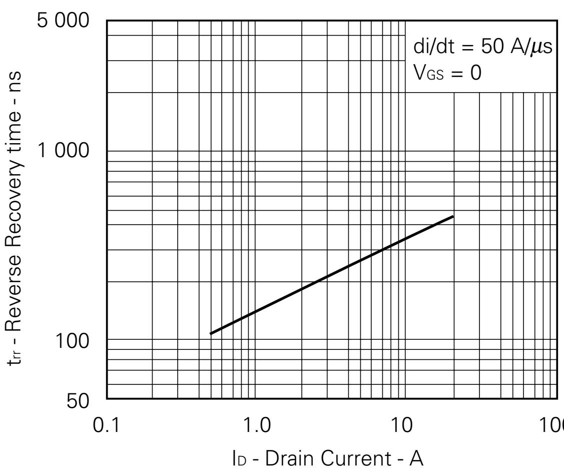
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



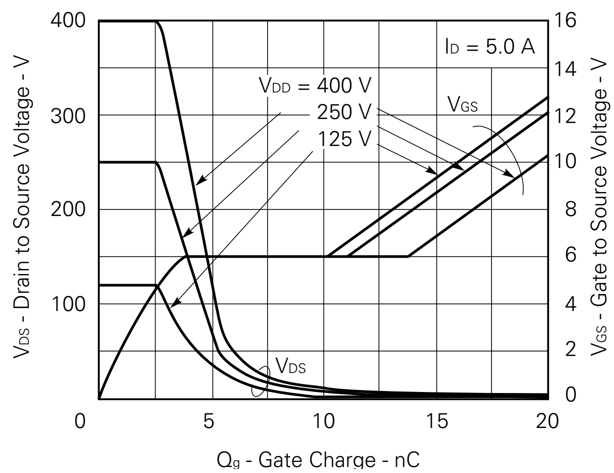
SWITCHING CHARACTERISTICS



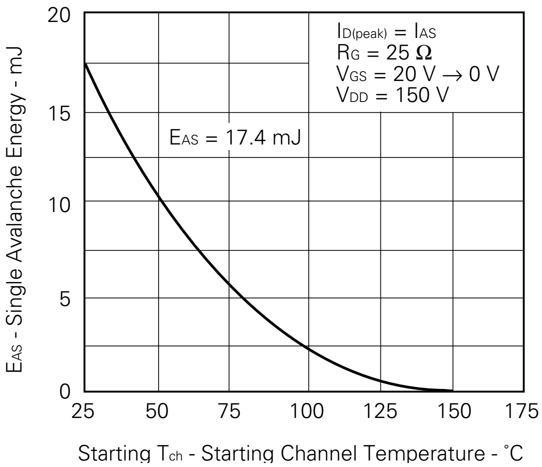
REVERSE RECOVERY TIME vs. DRAIN CURRENT



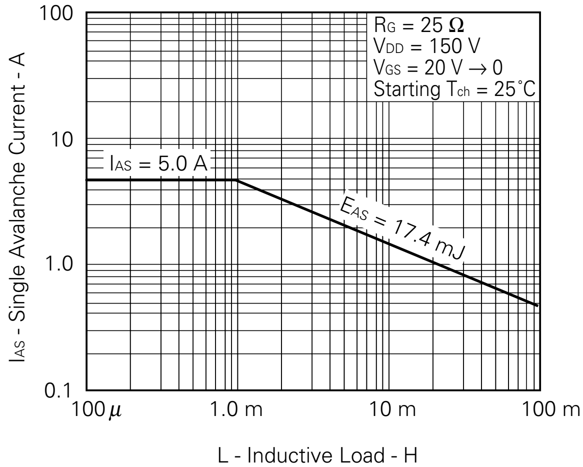
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE ENERGY vs
STARTING CHANNEL TEMPERATURE



SINGLE AVALANCHE CURRENT vs
INDUCTIVE LOAD



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]