

MOS FIELD EFFECT TRANSISTOR 2SK2355, 2SK2355-Z/2SK2356, 2SK2356-Z

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2355, 2SK2355-Z/2SK2356, 2SK2356-Z is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

• Low On-Resistance

2SK2355: $R_{DS(on)} = 1.4 \Omega \text{ (VGS} = 10 V, ID = 2.5 A)}$

2SK2356: $R_{DS(on)} = 1.5 \Omega$ (Vgs = 10 V, ID = 2.5 A)

• Low Ciss Ciss = 670 pF TYP.

· High Avalanche Capability Ratings

QUALITY GRADE

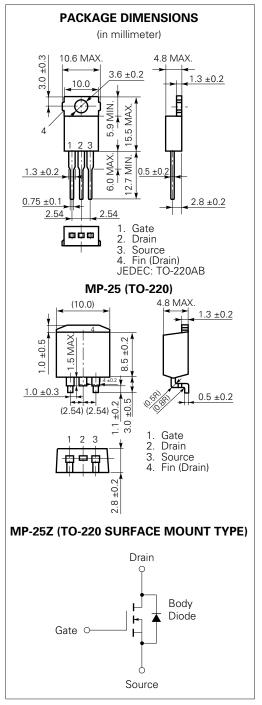
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage (2SK2355/2356)	VDSS	450/500	V
Gate to Source Voltage	Vgss	±30	V
Drain Current (DC)	$I_{D(DC)}$	±5.0	Α
Drain Current (pulse)*	I _{D(pulse}) ±20	Α
Total Power Dissipation ($T_c = 25$ °C)	P _{T1}	50	W
Total Power Dissipation (Ta = 25 °C)	P_{T2}	1.5	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T _{stg} ·	–55 to +150	°C
Single Avalanche Current**	las	5.0	Α
Single Avalanche Energy**	Eas	17.4	mJ

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0



The information in this document is subject to change without notice.

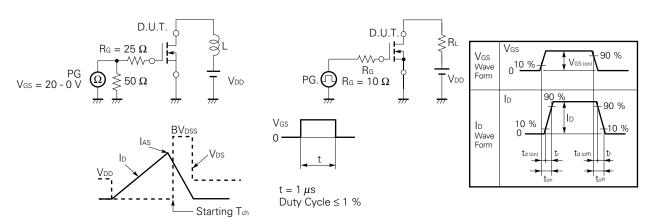


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

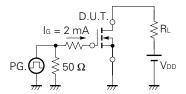
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-Resistance	RDS(on)		0.9	1.4	mΩ	Vgs = 10 V	2SK2355
			1.0	1.5		ID = 2.5 A	2SK2356
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	٧	V _{DS} = 10 V, I _D = 1 mA	
Forward Transfer Admittance	yfs	1.0			S	V _{DS} = 10 V, I _D = 2.5 A	
Drain Leakage Current	Ipss			100	μΑ	V _{DS} = V _{DSS} , V _{GS} = 0	
Gate to Source Leakage Current	Igss			±100	nA	Vgs = ±30 V, Vps = 0	
Input Capacitance	Ciss		670		pF	V _{DS} = 10 V	
Output Capacitance	Coss		140		pF	V _G S = 0	
Reverse Transfer Capacitance	Crss		18		pF	f = 1 MHz	
Turn-On Delay Time	td(on)		11		ns	ID = 2.5 A	
Rise Time	tr		8		ns	Vgs = 10 V	
Turn-Off Delay Time	td(off)		40		ns	V _{DD} = 150 V	
Fall Time	tf		8		ns	$R_G = 10 \Omega R$	= 60 Ω
Total Gate Charge	QG		20		nC	ID = 5.0 A	
Gate to Source Charge	Qgs		4.5		nC	$V_{DD} = 400 \text{ V}$	
Gate to Drain Charge	QgD		9		nC	V _G S = 10 V	
Body Diode Forward Voltage	V _F (S-D)		1.0		V	IF = 5.0 A, Vo	ss = 0
Reverse Recovery Time	trr		270		ns	IF = 5.0 A, Vo	ss = 0
Reverse Recovery Charge	Qrr		1.0		nC	$di/dt = 50 A/\mu s$	

Test Circuit 1 Avalanche Capability

Test Circuit 2 Switching Time

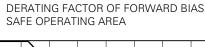


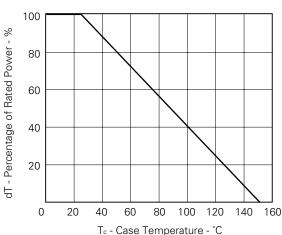
Test Circuit 3 Gate Charge



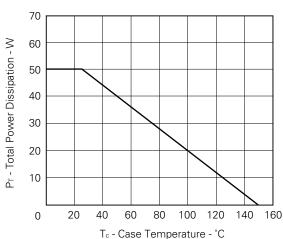
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (TA = 25 °C)

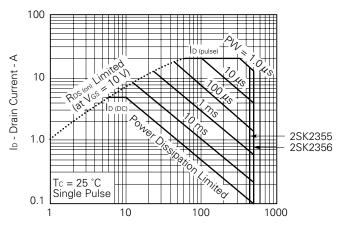




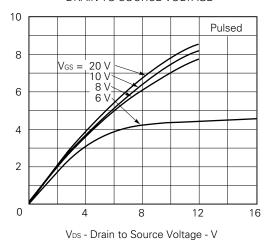
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

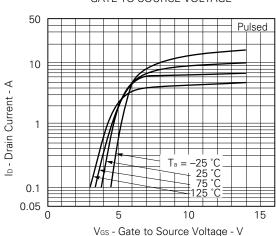


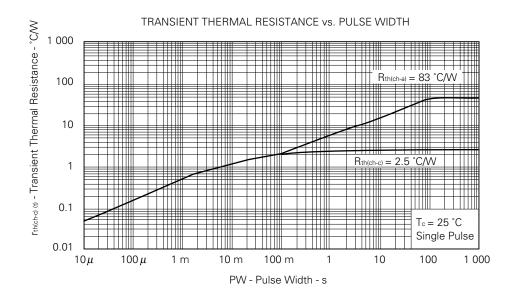
Drain Current - A

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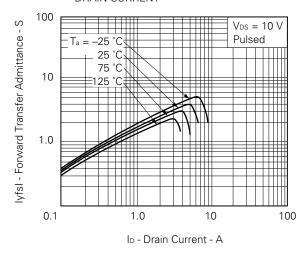
V_{DS} - Drain to Source Voltage - V

DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE





FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



RESISTANCE vs. DRAIN CURRENT

3.0

Pulsed

Pulsed

1.0

0 0.01

0 0.01

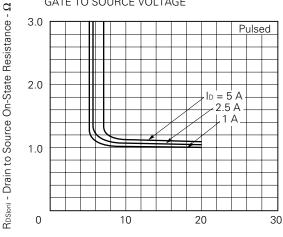
1 1

10

ID - Drain Current - A

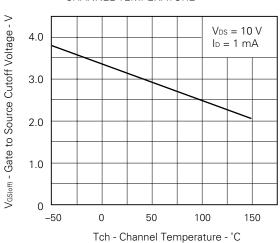
DRAIN TO SOURCE ON-STATE

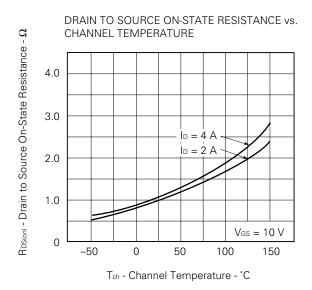
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

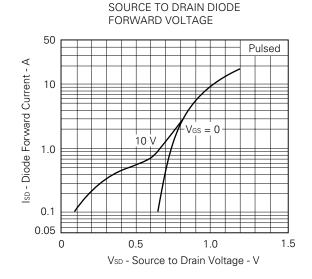


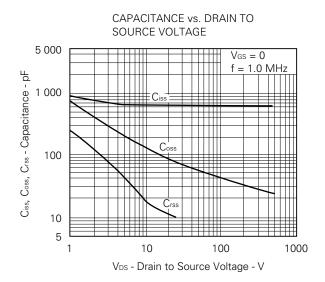
 $\ensuremath{\mathsf{V}}_\text{GS}$ - Gate to Source Voltage - $\ensuremath{\mathsf{V}}$

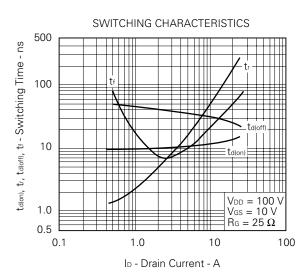
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

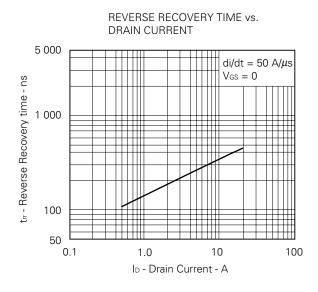


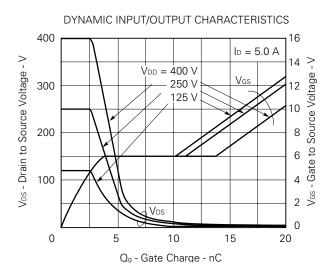






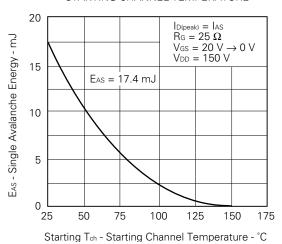




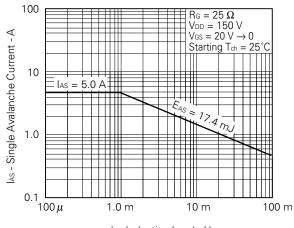




SINGLE AVALANCHE ENERGY vs STARTING CHANNEL TEMPERATURE



SINGLE AVALANCHE CURRENT vs INDUCTIVE LOAD





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



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