agere

Product Brief August 2003

WaveLAN[™] WL60040 Multimode Wireless LAN Media Access Controller (MAC)

1 Features

- Full implementation of the *IEEE*[®] 802.11 WMAC protocol including the following:
 - *IEEE* 802.11a, *IEEE* 802.11g, and *IEEE* 802.11h
 standards, supporting all mandatory and optional
 CCK and OFDM data rates up to 54 Mbits/s.
 IEEE 802.11b standard data rates.
- Full IEEE 802.11 standard is implemented on chip: —Downloadable firmware architecture leads to simple driver solutions.
- Supports 802.11i security encryption algorithms without impacting device throughput:
 - -Advanced Encryption Standard (AES) hardware accelerator operating in Counter Mode (CCM).
 - High-performance hardware acceleration encryption engine supporting Wired Equivalent Privacy (WEP) and 128 RC4.
 - —Temporal Key Integrity Protocol (TKIP) per Wi-Fi[®] Protected Access (WPA) hardware accelerator and draft 802.11i standard.
- Host interface support of the following:
 - -PCI v2.3 bus mastering 32-bit, 33 MHz transfers with PCI power management.
 - MiniPCI Specification v1.0.
 - CardBus bus mastering 32-bit, 33 MHz transfers v8.0.
 - —USB v1.1.
 - PC Card interface supports full 16-bit implementation per PCMCIA release 7.1.
 Compact Flash CF+ v.1.4.
- On-chip 64k x 16-bit static RAM supports full IEEE 802.11 client functionality without external memory.
- Flexible modem data interface options:
 Multiple baseband processor interfaces (bit, nibble, and byte modes).
- Modem data and modem management interfaces provide a direct connection to the *WaveLAN* WL64040 baseband.
- Supports SPI SEEPROM and ²C[®] SEEPROM interfaces.



- Flexible external memory expansion (access point applications):
 - Programmable wait-states for slow external memory.
 - -Multiple memory organization up to 4 Mbytes.
- Supports *Bluetooth[™]* coexistence through a simple two-wire interface.
- Multiple queue management supports 802.11e compliant quality of service (QoS).
- Device is capable of low-power operation:
 —Active mode 35 mA, 8 mA doze, <1 mA sleep.
- Small package footprint: 196-pin FSBGA 12 mm x 12 mm.
- Operation at 3.0 V to 3.6 V single supply.
- Operation ambient temperature: -40 °C to +85 °C.
- Supports IEEE 1149.1 boundary-scan standard.

2 Wireless LAN Applications

- High data-rate multimode applications.
- Client cards for notebooks, desktop PCs, and PDAs.
- Modules with WLAN functionality.
- Enterprise and home infrastructure devices.
- High-speed bridges and point-to-multipoint systems.
- Home entertainment and multimedia systems.

3 Description

The WL60040 MAC is designed to form a complete *IEEE* 802.11a/*IEEE* 802.11b/*IEEE* 802.11g chip set, along with the WL64040 baseband, WL54040 transceiver, and the WL54240 dual-band PA. Using a wide variety of host interfaces, the WL60040 supports the MAC and data buffer management functions and is fully compliant with the *IEEE* 802.11a, *IEEE* 802.11b, and *IEEE* 802.11g WLAN standards.

The WL60040 supports high data rates up to 54 Mbits/s while remaining cost-effective. It includes PCI/MiniPCI, CardBus/PCMCIA, PC Card, and Compact Flash support. The device features 1 Mbit of internal memory (RAM It supports the *IEEE* 802.11b and *IEEE* 802.11a standardized data rates and the drafted *IEEE* 802.11g mandatory and optional data rates up to 54 Mbits/s.

The WL60040 offers a rich set of exposed interfaces intended to provide flexibility to the system designer in multiple host interface applications. The WL60040 system architecture maps directly to that of the current WL60010 MAC. The major modifications are bus mastering and the addition of a hardware assist engine to support the *IEEE* 802.11i compliant AES and TKIP security enhancements. Figure 1 details the system architecture and major interfaces.



Figure 1. WLAN System Block Diagram Showing Major Interfaces

The WL60040 directly interfaces with the Agere family of baseband processors, offering a complete end-to-end chip set solution for wireless LAN products. Protocol and PHY support are implemented in firmware to allow custom protocol and *IEEE* 802.11 PHY transceivers.

The WL60040 has been designed to provide maximum performance with minimum power consumption. The FSBGA package provides optimal PC board layout to all of the aforementioned user interfaces. Firmware implements the full *IEEE* 802.11 wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF. Low-level protocol functions such as RTS/CTS and acknowledgement, fragmentation, defragmentation, and automatic beacon monitoring are handled without host intervention. Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multithreaded I/O drivers. Additional firmware functions specific to access point applications are also available.

A block diagram detailing the WL60040 device architecture and major interfaces is provided in Figure 2.

3 Description (continued)



Figure 2. WL60040 Block Diagram

4 Package Information

The WL60040 is packaged in a 196 FSBGA package of 12 mm x 12 mm, height^{*} 1.45 mm. Only 184 balls may be used for power/ground and signals. The other 12 balls (see Table 7) are not used and should be left unconnected.



Figure 3. Pin Layout of 196 FSBGA Used for WL60040, Bottom View

^{*} Height before the solder balls collapse.

5 Pin Information

The WL60040 signals are grouped by function in Table 1 through Table 5. In addition to the standard (default) pin definitions for each mode, some of the pins are multipurpose and can be programmed to other functions by setting the appropriate bits in device control registers. In the tables below, the pin name column shows the primary function pin name with alternative functions, if applicable, also shown. Signals ending with _B are active-low.

AD31 (D10) K8 Multiplexed address/data for PCI and CardBus. AD30 (D9) J13 Secondary function is used in PC Card mode (selected by BUSSEL). A0—A9 AD28 (D8) M8 re address, D0—D15 are data. AD27 (D0) P11 Pull-ups and pull-downs are only active in PC Card mode. They are switched off in any other mode (PCI, CardBus, or USB). AD22 (A4) L9 Pull-ups and pull-downs are only active in PC Card mode. They are switched off in any other mode (PCI, CardBus, or USB). AD22 (A4) L9 Pull-ups and pull-downs are only active in PC Card mode. They are switched off in any other mode (PCI, CardBus, or USB). AD21 (A6) N8 Pull-ups and pull-downs are only active in PC Card mode. They are switched off in any other mode (PCI, CardBus, or USB). AD22 (A4) L9 AD21 (A6) N8 AD21 (A6) N8 AD21 (D6) P14 AD13 (IORP_B) L11 AD14 (A7) M9 AD11 (OE B) J9 AD11 (OE B) M9 AD03	PCI/CardBus Pin Name*	Alt. Funct.	Pin #	Description
A030 AD29 AD28 (D8) (D9) MB J13 N9 are address, D0–D15 are data. AD27 AD27 AD27 (D0) MB Secondary function is used in PC Card mode (selected by BUSSEL). A0–A9 are address, D0–D15 are data. AD26 AD27 AD26 (A0) LT Initial-downs are only active in PC Card mode. They are switched off in any other mode (PCI, CardBus, or USB). AD22 AD22 (A4) L10 AD24 (A2) Initial-downs are only active in PC Card mode. They are switched off in any other mode (PCI, CardBus, or USB). AD22 AD22 (A4) L10 AD24 (A5) L8 AD20 (A6) N8 AD19 - AD11 AD18 (A7) MP P14 AD13 (IORD_B) L12 AD14 AD14 (CE2_B) M14 AD11 (OEB, J9 AD11 (OEE B) AD11 AD03 (IORD_B) L12 AD12 - M14 AD11 AD03 (IORD_B) J11 AD04 (D12) M14 AD07 (D7) AD04 (D12) K11 AD03 (D3) K10 AD14 AD04 (D12) Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE2_B C_BE1_B (A8) L13 AD02 (D1) Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE2_B C_BE1_B (A8) H14 C_BE1_B Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE2_B C_BE1_B - M4 AD14 Party (even) across AD and C, BE signals. Driven by master for address and write phases. FRAME_B	AD31	(D10)	K8	Multiplexed address/data for PCI and CardBus.
AD29 (D1) N9 are address, D0—D15 are data. AD27 (D0) P11 Pull-ups and pull-downs are only active in PC Card mode. They are switched off AD26 (A1) L10 Pull-ups and pull-downs are only active in PC Card mode. They are switched off AD26 (A1) L10 Pull-ups and pull-downs are only active in PC Card mode. They are switched off AD23 (A3) P9 Pull-ups and pull-downs are only active in PC Card mode. They are switched off AD23 (A3) P9 Pull-ups and pull-downs are only active in PC Card mode. They are switched off AD24 (A2) J10 Addition and public downs are only active in PC Card mode. They are switched off AD24 (A2) J10 Addition and public downs are only active in PC Card mode. They are switched off AD25 (A4) L9 Addition and public downs are only active and active and active and public downs are only active and public downs are only active and public downs are only active and acti	AD30	(D9)	J13	Secondary function is used in PC Card mode (selected by BUSSEL) A0—A9
AD28 (D8) M8 Pull-ups and pull-downs are only active in PC Card mode. They are switched off AD26 (A0) L7 in any other mode (PCI, CardBus, or USB). AD23 (A3) P9 AD22 (A4) L9 AD22 (A4) L9 AD21 (A5) L8 AD20 (A6) N8 AD19 M11 AD18 (A7) K9 AD14 (A9) P14 AD15 (IOWR B) P13 AD14 (A9) P14 AD13 M14 AD14 (CEZ B) J11 AD06 (D15) K14 AD07 T07 J12 AD06 (D15) K14 AD07 D11 K12 AD08 (D5) L13 AD04 (D12) K11 AD03 (D5) L13 C_BE2_B H14 C_BE2_B <t< td=""><td>AD29</td><td>(D1)</td><td>N9</td><td>are address. D0—D15 are data.</td></t<>	AD29	(D1)	N9	are address. D0—D15 are data.
AD27 (D0) P11 Point-gs and pur-downs are only active in PC Calcinitide. They are switched on in any other mode (PCI, CardBus, or USB). AD26 (A1) L10 AD23 (A3) P9 AD21 (A5) L8 AD20 (A6) N8 AD21 (A5) L8 AD21 (A5) L8 AD21 (A5) L8 AD21 (A6) N8 AD18 (A7) K9 AD16 L11 AD16 H1 AD16 H1 AD17 M14 AD14 (A9) P14 AD11 (CE2_B) J11 AD02 (D7) J12 AD03 (D5) L13 AD04 (D12) K11 AD00 (D3) K10 C	AD28	(D8)	M8	Dull upp and null downs are only active in DC Card made. They are switched off
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AD23 (A2) P0 AD23 (A3) P9 AD21 (A4) L9 AD21 (A5) L8 AD20 (A6) N8 AD19 - M11 AD18 (A7) K9 AD17 - M9 AD16 (IOWR_B) P13 AD15 (IOWR_B) L12 AD13 (IORD_B) L12 AD14 (A9) P14 AD15 (IOWR_B) J1 AD10 (CE2_B) J11 AD05 (D1) K14 AD06 (D1) N13 AD06 (D1) N12 AD06 (D1) N14 AD03 (D5) L13 AD04 (D12) K11 AD03 (D5) L13 AD04 (D1) K12 AD01 (D4) N11 AD00 (D3) K10 C_BE3_B (CE1_B) H11 PAR - K4	AD25	(A1) (A2)	L10	
AD22 (A4) L9 AD21 (A5) L8 AD20 (A6) N8 AD19 M11 AD18 (A7) K9 AD17 M9 AD16 L11 AD15 (IOWR_B) P13 AD14 (A9) P14 AD12 M14 AD11 (CE_B) J9 AD12 M14 AD11 (CE_2B) J11 AD05 (D6) M12 AD06 (D13) N13 AD05 (D6) M12 AD04 (D12) K12 AD01 D4) N11 AD00 (D3) K10 C_BE3_B (REG_B) L4 C_BE1_B (A8) H13 C_BE0_B (C11) K12 AD00 (D3) K10 PAR N4 Parti	AD24 AD23	(A2) (A3)		
AD21 (A6) L3 AD20 (A6) N8 AD19 - M11 AD18 (A7) K9 AD17 - M9 AD16 - L11 AD15 (IOWR-B) P13 AD14 (A9) P14 AD13 (IORD_B) L12 M14 AD11 (OEB) J9 AD11 (OE2B) J9 AD11 (OE2B) J9 AD06 (D13) N13 AD06 (D13) N13 AD03 (D5) L13 AD04 (D12) K11 AD03 (D5) L13 AD04 (D14) N11 AD00 (D3) K10 AD01 (D4) N11 AD02 (D11) K12 AD01 (D4) N11 AD02 (D13) N13 G_BE2_B - H14	AD23 AD22	(A3) (A4)	19	
AD20 (A6) N8 AD19 M11 AD18 (A7) K9 AD17 M9 AD16 L11 AD15 (IOWR_B) P13 AD14 (A9) P14 AD12 M14 AD11 (OE_B) J9 AD10 (CE2_B) J11 AD09 M10 AD08 (D15) K14 AD06 (D13) N13 AD05 D6) M12 AD04 (D2) K11 AD03 (D5) L13 AD03 (D3) K10 C_BE2_B H14 C_BE2_B (CE1_B) H14 C_BE2_B (A8) H13 C_BE2_B (CE1_B) H14 C_BE3_B (CE1_B) H14 C_BE2_B K5 Frame is driven by master to indicate start and duration of a transaction	AD21	(A5)	18	
AD19 Curve M11 AD18 (A7) K9 AD17 - M9 AD16 - L11 AD13 (IORD_B) P13 AD14 (A9) P14 AD13 (IORD_B) L12 AD11 (OE_B) J9 AD10 (CE2_B) J11 AD09 - M10 AD09 - M10 AD00 (D15) K14 AD01 (DE2_B) J11 AD03 (D5) L13 AD04 (D12) K11 AD03 (D5) L13 AD04 (D2) K11 AD03 (D5) L13 AD00 (D3) K10 C_BE3_B (REG_B) L4 C_BE1_B (A8) H13 C_BE1_B (A8) H13 C_BE1_B - K5 Frame is driven by master to indicate start and duration of a transaction. <td>AD20</td> <td>(A6)</td> <td>N8</td> <td></td>	AD20	(A6)	N8	
AD18 AD17 (A7) K9 M9 M9 M9 M016 AD15 AD14 L11 M019 M016 AD14 AD13 (IOWR_B) (IOWR_B) AD10 P13 M014 AD13 (IOWR_B) M019 AD10 L12 M019 CE_B) AD10 AD14 M14 AD11 AD10 (CE2_B) J11 J9 AD10 AD08 (D15) K14 AD07 AD06 (D13) N13 AD03 AD06 (D13) N13 AD01 AD06 (D11) K12 AD04 AD01 (D4) N11 AD03 AD02 (D11) K12 AD04 AD03 (D5) L13 AD01 C_BE2_B H14 C_BE1_B Cell_B) C_BE2_B N4 Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases. FRAME_B K5 Frame is driven by master to indicate start and duration of a transaction. IRDY_B <	AD19		M11	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	AD18	(A7)	K9	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	AD17	``	M9	
AD15 (IOWR, B) P13 AD14 (A9) P14 AD13 (IORD_B) L12 AD12 — M14 AD11 (OEB) J9 AD10 (CE2_B) J11 AD09 — M10 AD08 (D15) K14 AD07 (D7) J12 AD06 (D13) N13 AD05 (D6) M12 AD04 (D12) K11 AD03 (D5) L13 AD04 (D4) N11 AD03 (D5) L13 AD04 (D4) N11 AD03 (D4) N11 AD00 (D3) K10 C_BE3_B — H14 C_BE3_B (CE1_B) H11 PAR — N4 Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases. FRAME_B — K5 Frame is driven by master to indicate start and duration of a transaction. IRDY_B — M7 Initi	AD16	—	L11	
AD14 (A9) P14 AD13 (IORD_B) L12 AD11 (OE_B) J9 AD10 (CE2B) J9 AD09 — M10 AD09 — M10 AD08 (D15) K14 AD07 (D7) J12 AD06 (D13) N13 AD06 (D12) K11 AD03 (D5) L13 AD04 (D12) K11 AD03 (D5) L13 AD04 (D4) N11 AD03 (D4) N11 AD04 (D4) N11 AD03 (D5) L13 AD04 (D4) N11 AD00 (D3) K10 C_BE3_B (REG_B) L4 Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE1_B (A8) H13 Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases. FRAME_B — K5 Frame is driven by master to indicate start and duration of a transaction.	AD15	(IOWR_B)	P13	
AD13 AD12(IORD_B) M14 AD11L12 M14 M14 AD11L12 (OE_B)J9 J9 J9 J9 AD00AD10 AD09 AD09 AD08(CE2_B)J11 M10 M10 AD08J11 (CE2_B)AD09 AD06 (D13)K14 M12 AD06M10 M12 M12 AD06AD06 AD03 (D5)L13 K12 AD03 (D5)L13 K12 AD03 (D5)AD03 AD02 (D5)L13 K12 AD00 (D3)K10C_BE3_B C_BE1_B C_BE1_B(REG_B) (CE1_B)L4 H11PAR PAR-N4 M2PAR FRAME_B-K5 M7FRAME_B C_BE3_B-K5 M7FRAME_B C_BE3_B-M7 M12 Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.FRAME_B TRDY_B-H12 M7Target ready. Indicates that the target is ready to complete the data phase.TRDY_B C_BE3_B C_BE3_B C_BE3_B-M4 M412Stop. Indicates that the target is ready to complete the data phase.TRDY_B C_BE3_B C_BE3_B C_BE3_B C_BE3_B-M4 M4Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE3_B C_BE3_B C_BE3_B C_BE3_B-H14 M4Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE3_B C_BE3_B C_BE3_B-H14 M4Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE3_B -H14 H44Command/byte enable. Target does not drive C_BE. Pins can be input only. <td>AD14</td> <td>(A9)</td> <td>P14</td> <td></td>	AD14	(A9)	P14	
AD12 AD11 $-$ M14 M14AD11 AD09(CE2_B)J9 J9AD00 AD08(D15)K14 K14 AD07AD06 AD08(D15)K14 K14 AD07AD06 AD08(D13)N13 N13 AD05AD06 AD08(D12)K11 K12 AD04AD03 AD03(D5)L13 K10AD04 C_BE3_B C_BE1_B(CE4_B)L4 H14C_BE3_B C_BE1_B(REG_B) (CE1_B)L4 H11PAR PAR-N4 N1 N1PAR PAR-K5FRAME_B FRAME_B-K5FRAME_B STOP_B-M7 H12TRDY_B C_BE3_B C_BE3_B-M4 Stop. Indicates that the target is ready to complete the data phase.TRDY_B C_BE3_B C_BE3_B-M4 Stop. Indicates that the target is ready to complete the data phase.TRDY_B C_BE3_B C_BE3_B C_BE3_B -M4 Stop. Indicates that the target is ready to complete the data phase.TRDY_B 	AD13	(IORD_B)	L12	
AD11 AD09 AD08 (CE2_B)J1 J11 M10 M108 AD08 (D15)J11 M10 M10 M208 (D15)J11 M10 M10 M208 (D13)AD06 AD06 (D13)(D13) M12 M203 (D5)N13 L13 L13 AD04 (D2)N13 M12 K11 K12 AD03 (D5)AD04 AD03 (D5)(D12) L13 K10K11 K12 AD03 (D5)AD03 AD02 (D11)K12 K12 AD01 (D4)N11 K12 K11 AD02 (D3)C_B83_B C_BE2_B (CE1_B)L4 H11Command/byte enable. Target does not drive C_BE. Pins can be input only.C_B83_B C_BE0_B (CE1_B)Command/byte enable. Target does not drive C_BE. Pins can be input only.PAR PAR-N4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B IRDY_B-K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B C_BE3_B CCE_B-H12Target ready. Indicates that the target is ready to complete the data phase.TRDY_B-M4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE1_B C_BE1_B C_BE1_BL4 (A8) H114Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE3_B C_BE1_B C_BE1_BCommand/byte enable. Target does not drive C_BE. Pins can be input only.	AD12		M14	
AD10 AD09 AD08(CE2_B) (D15)J11 M10 M10AD08 AD08 AD07(D15)K14 K14 AD07AD06 AD05 (D13)(D13)N13 N13 AD05AD06 AD04 (D12)K11 K12 AD02 AD01(D11)K12 AD02 AD01(D11)K12 K11 AD02AD01 C_BE3_B C_BE1_B C_BE0_BL4 (A8)Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE3_B C_BE1_B (A8)(CE1_B)H14 H11PAR-N4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by master for read phases.FRAME_B-K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B-M12 Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_B-H12 H12Target ready. Indicates that the target is ready to complete the data phase.STOP_B-M4Stop. Indicates that the target is ready to complete the data phase.STOP_B-M4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE1_B C_BE1_B(A8) (A8) H113Command/byte enable. Target does not drive C_BE. Pins can be input only.	AD11	(OE_B)	J9	
AD09 AD08—MI0 (D15)AD08(D15)K14 AD07AD06(D13)N13 N12 AD06AD06(D13)N13 N12 AD04AD04(D12)K11 K12 AD03AD02(D11)K12 K12 AD01AD00(D3)K10C_BE3_B(REG_B)L4 H14 C_BE1_BCommand/byte enable. Target does not drive C_BE. Pins can be input only.C_BE2_B—H14 H14Command/byte enable. Target does not drive C_BE. Pins can be input only.PAR—N4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B—K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B—H12Target ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_B—H12Target ready. Indicates that the target is ready to complete the data phase.STOP_B—M4Stop. Indicates that the target to stop the current transaction.C_BE3_B C_BE1_B C_BE1_B(A8) (A8)H13Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE1_B C_BE1_B(A8) (A8)H13Command/byte enable. Target does not drive C_BE. Pins can be input only.	AD10	(CEZ_B)	JII M10	
AD00(D17)N14 J12AD06(D13)N13 N13AD05(D6)M12 M12 	AD09	(D15)	IVI 10	
ADO6(D1)N12AD06(D3)N13AD05(D6)M12AD04(D12)K11AD03(D5)L13AD02(D11)K12AD01(D4)N11AD00(D3)K10C_BE3_B(REG_B)L4C_BE3_B(CE1_B)H14C_BE0_B(CE1_B)H11PAR-N4PAR-N4PAR-K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B-M7Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.STOP_B-M4Stop_B(REG_B)L4C_BE3_B(REG_B)L4C_BE3_B-M4Stop_IB-H12Target ready. Indicates that the target is ready to complete the data phase.STOP_B-M4Stop_Indicates that the target request to stop the current transaction.C_BE3_B(REG_B)L4C_BE3_B(A8)H13C_BE3_B(A8)H13C_BE3_B(C81_B)H14C_BE3_B(A8)H13C_BE3_B(C81_B)H14C_BE3_B(C81_B)H14C_BE3_B(C81_B)H14C_BE3_B(C81_B)H14C_BE3_B(A8)H13C_BE3_B(C81_B)H14C_BE3_B(C81_B)H14C_BE3_B(A8)H		(D13) (D7)	.112	
AD05 AD03(D6) (D12)M12 K11 	AD06	(D13)	N13	
AD04 AD03(D12) (D5)K11 L13 L13 AD02AD03 AD02(D5)L13 (D11)AD02 AD01(D11)K12 AD01(D4)AD01 	AD05	(D6)	M12	
AD03 AD02 (D11)(D5) (D11)L13 K12 K10AD01 AD00 (D3)(D4) (D4)N11 K10C_BE3_B C_BE2_B C_BE0_B(REG_B) (CE1_B)L4 H11Command/byte enable. Target does not drive C_BE. Pins can be input only.PAR PAR PAR-N4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B IRDY_B-K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B C_BE3_B C_BE3_B-H12Target ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_B C_BE3_B C_BE3_B C_BE3_B C_BE3_B C_BE3_B C_BE3_B-M4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE3_B C_BE3_B C_BE3_B L4 H13Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE3_B -H14 H13Command/byte enable. Target does not drive C_BE. Pins can be input only.	AD04	(D12)	K11	
AD02 AD01 (D4)(D11) (D4)K12 N11 K10C_BE3_B C_BE2_B C_BE0_B(REG_B) - H14 (CE1_B)L4 H13 CCommand/byte enable. Target does not drive C_BE. Pins can be input only.PAR PAR- - H11N4Command/byte enable. Target does not drive C_BE. Pins can be input only.PAR PAR- - N4N4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B IRDY_B-K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B C_BE3_B C_BE3_B C_BE1_B-H12Target ready. Indicates that the initiator (master) is ready to complete the data phase.STOP_B C_BE3_B C_BE3_B C_BE1_B-M4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE1_B C_BE1_B C_BE1_B(REG_B) (A8) H13L4 H13Command/byte enable. Target does not drive C_BE. Pins can be input only.	AD03	(D5)	L13	
AD01 AD00(D4) (D3)N11 K10C_BE3_B C_BE2_B C_BE1_B (A8)(REG_B) H13L4 Command/byte enable. Target does not drive C_BE. Pins can be input only.PAR PAR-H14 (A8)Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B IRDY_B-K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B STOP_B-H12Target ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_B C_BE3_B C_BE3_B C_BE1_B-M4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE1_B C_BE1_B(REG_B) H14L4 COmmand/byte enable. Target does not drive C_BE. Pins can be input only.	AD02	(D11)	K12	
AD00(D3)K10C_BE3_B C_BE2_B(REG_B) - (A8)L4 H14Command/byte enable. Target does not drive C_BE. Pins can be input only.PAR (A8)H13 H11Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B N4K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B N4M7Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_BH12Target ready. Indicates that the target is ready to complete the data phase.STOP_BM4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE2_B(REG_B) - (A8)L4 H13Command/byte enable. Target does not drive C_BE. Pins can be input only.	AD01	(D4)	N11	
C_BE3_B C_BE2_B C_BE1_B C_BE0_B(REG_B) - (A8) (CE1_B)L4 H14 H13 H11Command/byte enable. Target does not drive C_BE. Pins can be input only.PARN4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_BK5Frame is driven by master to indicate start and duration of a transaction.IRDY_BM7Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_BM4Stop. Indicates that the target is ready to complete the data phase.STOP_BM4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE1_B(REG_B) (A8)L4 H14Command/byte enable. Target does not drive C_BE. Pins can be input only.C_BE1_B C_BE1_B(A8)H14Command/byte enable. Target does not drive C_BE. Pins can be input only.	AD00	(D3)	K10	
C_BE2_B C_BE1_B C_BE0_B—H14 (A8) (CE1_B)H11PAR—N4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B—K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B—M7Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_B—H12Target ready. Indicates that the target is ready to complete the data phase.STOP_B—M4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE1_B C_BE1_B(A8)H13C_BE1_B C_BE1_B(A8)H13	C_BE3_B	(REG_B)	L4	Command/byte enable. Target does not drive C_BE. Pins can be input only.
C_BE1_B C_BE0_B(A8) (CE1_B)H13 H11PAR-N4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_B-K5Frame is driven by master to indicate start and duration of a transaction.IRDY_B-M7Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_B-H12Target ready. Indicates that the target is ready to complete the data phase.STOP_B-M4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE2_B C_BE1_B(REG_B) (A8)L4 H13 H11Command/byte enable. Target does not drive C_BE. Pins can be input only.	C_BE2_B	—	H14	
C_BE0_B (CE1_B) H11 PAR - N4 Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases. FRAME_B - K5 Frame is driven by master to indicate start and duration of a transaction. IRDY_B - M7 Initiator ready. Indicates that the initiator (master) is ready to complete the data phase. TRDY_B - H12 Target ready. Indicates that the target is ready to complete the data phase. STOP_B - M4 Stop. Indicates that the target request to stop the current transaction. C_BE3_B (REG_B) L4 Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE1_B (A8) H13 H14	C_BE1_B	(A8)	H13	
PARN4Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.FRAME_BK5Frame is driven by master to indicate start and duration of a transaction.IRDY_BM7Initiator ready. Indicates that the initiator (master) is ready to complete the data phase.TRDY_BH12Target ready. Indicates that the target is ready to complete the data phase.STOP_BM4Stop. Indicates that the target request to stop the current transaction.C_BE3_B C_BE1_B C_BE1_B(REG_B) (A8)L4 H13Command/byte enable. Target does not drive C_BE. Pins can be input only.	C_BE0_B	(CE1_B)	H11	
FRAME_B — K5 Frame is driven by master to indicate start and duration of a transaction. IRDY_B — M7 Initiator ready. Indicates that the initiator (master) is ready to complete the data phase. TRDY_B — H12 Target ready. Indicates that the target is ready to complete the data phase. STOP_B — M4 Stop. Indicates that the target request to stop the current transaction. C_BE3_B (REG_B) L4 Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE1_B (A8) H13 H14	PAR	—	N4	Parity (even) across AD and C_BE signals. Driven by master for address and write phases; driven by target for read phases.
IRDY_B — M7 Initiator ready. Indicates that the initiator (master) is ready to complete the data phase. TRDY_B — H12 Target ready. Indicates that the target is ready to complete the data phase. STOP_B — M4 Stop. Indicates that the target request to stop the current transaction. C_BE3_B (REG_B) L4 Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE1_B (A8) H13 H14	FRAME_B	_	K5	Frame is driven by master to indicate start and duration of a transaction.
TRDY_B H12 Target ready. Indicates that the target is ready to complete the data phase. STOP_B M4 Stop. Indicates that the target request to stop the current transaction. C_BE3_B (REG_B) L4 C_BE2_B H14 C_BE1_B (A8) H11 H11	IRDY_B	—	M7	Initiator ready. Indicates that the initiator (master) is ready to complete the data
STOP_B M4 Stop. Indicates that the target request to stop the current transaction. C_BE3_B (REG_B) L4 C_BE2_B H14 C_BE1_B (A8) H13 H14	ם עומד		LI12	phase.
C_BE3_B (REG_B) L4 Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE2_B — H14 C_BE1_B (A8) H13 C_BE0_B (CE1_B) H11			N/4	Stop. Indicates that the target request to stop the surrent transaction
C_BE3_B (REG_B) L4 Command/byte enable. Target does not drive C_BE. Pins can be input only. C_BE2_B — H14 C_BE1_B (A8) H13 C_BE0_B (CE1_B) H11	STUP_B		IVI4	
	C_BE3_B C_BE2_B C_BE1_B C_BE0_B	(REG_B) — (A8) (CE1_B)	L4 H14 H13 H11	Command/byte enable. Target does not drive C_BE. Pins can be input only.

Table 1. Host Interface Pins

* All of these interface pins have 5 V tolerant pads.

Table 1	Host	Interface	Pins	(continued)
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PCI/CardBus Pin Name	Alt. Funct.	Pin #	Description
DEVSEL_B	—	N7	Device select. Indicates that the target has decoded the address.
PERR_B	_	P2	Parity error. For reporting parity errors during PCI transactions except special cycle.
SERR_B	(WAIT_B)	P4	System error, open drain. Used for reporting address parity errors and data parity errors on the special cycle command or any other system error where the result will be catastrophic.
PCICLK	—	М3	PCI clock: provides timing for all transactions. 0 MHz—33 MHz.
RST_B	(RESET)	K6	RST_B is used to bring registers, sequencers, and signals into a consistent state. In PC Card mode, this is RESET: same function but active-high.
IDSEL	_	M5	Initialization device select. Used as chip select during configuration transactions. Used as external power-on reset input in PC Card mode. This pin should be pulled high in Cardbus operation mode.
INT_B	(IREQ_B/READY)	M6	Interrupt output, open drain. (De)assertion is asynchronous to PCICLK.
CLKRUN_B	(IOIS16_B)	P6	Clock run. Signal to control the PCI clock.
PME_B	(STSCHG_B) (STSCHG)	N5	Power management enable. Used to request a change in the device or system power state. For PC Card, this pin is STSCHG_B. For CardBus, this pin is STSCHG.
GNT#	WE_B	L6	Bus grant signal: only needed for PCI/CardBus master. In non-PC Card mode, this pin serves as an external power-on reset input. In PC Card mode, this pin has WE_B functionality.
_	D2	L5	Reserved future use for CardBus. D2 for PC Card.
—	D14	N3	Reserved future use for CardBus. D14 for PC Card.
REQ#	INPACK_B	N6	Bus request signal: only needed for PCI/CardBus master. INPACK_B is needed for PC Card.
PCIVIO	_	P7	PCI signaling select signal: when this pin is 5 V, 5 V signaling is used, else 3.3 V signaling.
			PCI cards: connected to pciVIO on the PCI connector.
			CardBus/Mini PCI: connected to the 3.3 V power rail.
			PC Card: connected to the 3.3 V power rail.
USBPOS USBNEG	USBPOS USBNEG	L3 M1	USB data signals: connected to terminals DM and DP of the cell.

* All of these interface pins except USBPOS and USBNEG have 5 V tolerant pads.

Table 2. External Memory Interface Pins

Name and Function		Pin #	Description
Mem	Misc		
MA21 MA20 MA19 MA18 MA17 MA16 MA15 MA14 MA13 MA12 MA11 MA10 MA09 MA08 MA07 MA06 MA05 MA04 MA03 MA02 MA01	OSLP BKCS_B XCSB_B XCSA_B	E7 G5 G1 D11 C11 D10 A11 E11 C12 E14 C14 K4 A14 C10 B11 A12 C8 A4 C5 D5 C4	Memory address lines, multiplexed with oscillator sleep, chip selects, and port logic.
MD15 MD14 MD13 MD12 MD11 MD10 MD09 MD08	VauxPwr 16bdev HOSC HIFISA Stridle Mem16 NvDs RomDs	A2 E2 F2 F4 D4 F12 E5	Memory data 15.
MD07 MD06 MD05 MD04 MD03 MD02 MD01 MD00	_	A6 D6 B7 C6 D7 C7 B8	Memory data, low byte.
MWE_B MHBS_B MLBS_B	MWEL_B MWEH_B MA00	B10 A13 J2	Memory write/read enable signals for single 16 bits. Alternative signals for dual 8 bits or single 8 bits external RAM.
MOE_B		E1	Memory output enable.
RAMCS_B		A1	RAM chip select.
NVCS_B	BootCS_B	G2	Boot ROM/nonvolatile chip select.

Table 3. Modem Interface Pins

Name and Function		Pin #	Description		
Modem	Misc	I/O Port			
TXC	TRXC	—	C2	Transmit clock input for WL64040. Transmit/receive clock for MDI nibble and byte mode.	
TXD RXD RXC	TXRX0 TXRX1 TXRX5	_	D12 F9 C3	Transmit data, receive data. For OFDM, these pins are used as transmit or receive data (half duplex).	
XBUSY	TXR	K(4)	H2	Transmit busy function; alt: transmit ready.	
BTBusy	TXRX4	J(7)	D13	Bluetooth busy signal; Bit 4, MDI byte mode.	
TXRX2	—	—	K1	Bit 2, MDI nibble, or byte mode.	
BSEL LED	TXRX6	K(2)	H3	Band select LED function; Alt: K-port, octal mode pins.	
RadioEn	TXRX7	K(3)	H1	Radio disable switch; Alt: K-port, octal mode pins.	
PDA	UWDET	K(5)	F10	PHY data available.	
MBUSY	—	K(6)	E10	Medium busy.	
EDET	—	K(7)	G12	Energy detect.	
TXE	—	L(0)	E12	Transmit enable.	
PHYSLP_B	RXE	L(1)	G11	PHY sleep; Alt: receive enable.	
PHYRES	—	L(2)	F11	PHY Reset, FW-controlled through L(2).	
WLANBusy	SLOT	L(3)	G10	WLAN busy signal; Alt: slot synchronization, FW-controlled through L(3).	
PStat	—	L(4)	K2	Phy status, FW-controlled through L(4).	
SCK	—	J(0)	C13	Serial clock MMI.	
SDIO	—	J(1) SCL	H10	Serial data out MMI. SCL for I^2C , FW-controlled through J(1).	
SDI	SDDIR	J(2) SDS5	F5	Serial data in MMI/ SDDIR output. Device select5, FW-controlled per J(2) port.	
SDS0	PHYCS_B	J(3)	B14	Device select0, typically from MMI state machine. PHY memory chip select.	
SDS1	—	J(4)	E9	Device select1, typically from MMI state machine.	
SDS2	—	J(5) SDA	E6	Device select2, SDA for I^2C , FW-controlled through J(5).	
PSwitch	SDS3	J(6)	K3	Modem power switch/device select3. FW-controlled per J(6) port, shared with debug information.	
TXRX3		_	F3	Bit 3, MDI nibble, or byte mode.	

Table 4. Test Interface and Indicator Pins

Name	Pin #	Description
TEST_B	A8	Test mode select. This pin is also used to disable the pull-ups/pull-downs (for IDDQ test). Must be externally connected to VDD.
SCAN_B	G3	Selects between scan (shift) and capture mode: 0 = scan, 1 = capture.
BSCANEN	E13	Boundary-scan compliance pin: 0 selects debug functionality on BSCAN pins TDI, TDO, TMS, TRST_B and TCK. 1 selects BSCAN functionality on the mentioned pins.
TDI	J4	Boundary-scan data in.
TDO	H5	Boundary-scan data out.
TMS	J3	Boundary-scan mode select.
TRST_B	E8	Boundary-scan reset.
ТСК	D3	Boundary-scan clock.
MCLKOUT	E4	MCLK clock output.

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Table 5. Power and Ground Pins

Pin Name	Pin #	Description
VDD_USB	N1	3.3 V for USB transceiver.
VSS_USB	M2	Ground for USB transceiver.
VDD_32KHZ	A9	3.3 V for 32 kHz oscillator.
VSS_32KHZ	B9	Ground for 32 kHz oscillator.
VDD_PLL	G13	3.3 V for PLL.
VSS_PLL	G14	Ground for PLL.
VDD3 VDD4 VDD5 VDD7 VDD8 VDD10 VDD14 VDD18	K13 N2 N14 P12 P8 P3 J14	3.3 V for PCI.
VDD1 VDD2 VDD6 VDD9 VDD11 VDD12 VDD13 VDD15 VDD16 VDD17	A3 B12 A7 F1 B1 B2 B3 F13 B13 F14	3.3 V for other I/O logic.
VSS1 VSS2 VSS6 VSS8 VSS9 VSS11 VSS13 VSS14	M13 L14 P5 N10 K7 P1 H9 P10	Ground for PCI.
VSS3 VSS4 VSS5 VSS7 VSS10 VSS12 VSS15 VSS16 VSS17 VSS18	B4 B5 L1 A10 D1 D14 G9 D2 A5 L2	Ground for other I/O logic.

Table 6. Miscellaneous Pins

Pin Name	Pin #	Description				
CKIN	C1	Clock input.				
XTALA32K XTALB32K*	D9 C9	32 kHz crystal oscillator inputs.				
BTBusy	D13	Bluetooth busy signal; Bit 4, MDI byte mode.				
WLANBusy	G10	VLAN busy signal; Alt: slot synchronization, FW-controlled through L(3).				
LED1 [†]	D8	LED1, FW-controlled per K(1) port.				
LED0	J5	LED0, FW-controlled per K(0) port.				
INTPPOREN	G4	Jsed to select between external power-on reset (0) or internally generated power-on reset.				
BUSSEL1 [‡]	J1	Host Bus Interface select signals:				
BUSSEL0	H4	BS[1] BS[0] Mode 0 0 16-bit: PC-Card 0 1 USB 1 0 CardBus 1 1 PCI				

* An external 32 kHz signal can also be provided on this pin.

+ LED[1:0] pins characteristics defined as: ISOURCE = 9.4 mA; ISINK = 6.5 mA.

‡ BUSSEL[1:0] signals do not have 5 V tolerant pads.

Table 7. Unused Pins

Pin Name	Pin #	Description
VSSNC1, VSSNC2 VSSNC3, VSSNC4 VSSNC5, VSSNC6 VSSNC7, VSSNC8 VSSNC9, VSSNC10 VSSNC11, VSSNC12	F6, F7 F8, G6 G7, G8 H6, H7 H8, J6 J7, J8	No connections.*

* These pins are not connected to anything internally within the chip and should be left unconnected within the board design.

6 Electrical Characteristics

Table 8. Operating Conditions

Category	Value
Power Supply Range	3.0 V—3.6 V
Suspend Current (typ): USB Mode	< 0.5 mA
Sleep Current (typ): CardBus/miniPCI Mode PCMCIA Mode	10 mA 2.5 mA
Ambient Temperature	Min = -40 °C/Max = 85 °C USB: Min = 0 °C/Max = 85 °C

Note: Junction temperature is determined by power dissipation and thermal resistance of the package.

6 Electrical Characteristics (continued)

Table 9. Active Power Dissipation

Mode	CardBus/mPCI	USB	PC Card	Unit
IEEE 802.11b	132	99	83	mW
<i>IEEE</i> 802.11a/b/g	149	116	99	mW

Table 10. Recommended Operating Condition Limits

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage with Respect to Ground	Vdd	2.7	3.6	V
Input Voltages	VIN	Vss – 0.3	VDD + 0.3	V
Junction Temperature	TJ	-40	125	°C

Table 11. Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage with Respect to Ground	Vdd		≤4.2	V
Input Voltages	Vin	Vss – 0.3	VDD + 0.3	V
Junction Temperature	TJ	-40	125	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

7 Ordering Information

Part Number	Temperature Range °C	Package	Packing	MOQ	Comcode
WL600402LY-DB	-40 to +85	FSBGA196	Tray	756	700054556

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ASIA: EUROPE:	Agere Systems Hong Kong Ltd., Suites 3201 & 3210-12, 32/F, Tower 2, The Gateway, Harbour City, Kowloon Tel. (852) 3129-2000, FAX (852) 3129-2020 CHINA: (86) 21-5047-1212 (Shanghai), (86) 755-25881122 (Shenzhen) JAPAN: (81) 3-5421-1600 (Tokyo), KOREA: (82) 2-767-1850 (Seoul), SINGAPORE: (65) 6778-8833, TAIWAN: (886) 2-2725-5858 (Taipei) Tel. (44) 1344 296 400

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August 2003 PB03-164WLAN