

DN8648FBP

32-bit Shift Register Latch Driver IC

■ Overview

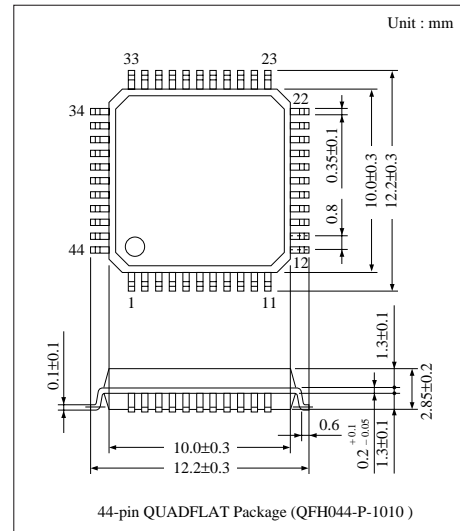
The DN8648FBP is an IC which incorporates a 32-bit shift register and a latch driver to meet high-speed operation low power consumption and high-density printout of the thermal printers for the work processors, and so on. It employs the Bi-CMOS process in which the serial-in and serial-out/parallel-out functions are incorporated, the 32-step shift register block and latch block are composed of CMOS, and the 32-step parallel driver block is bipolar.

■ Features

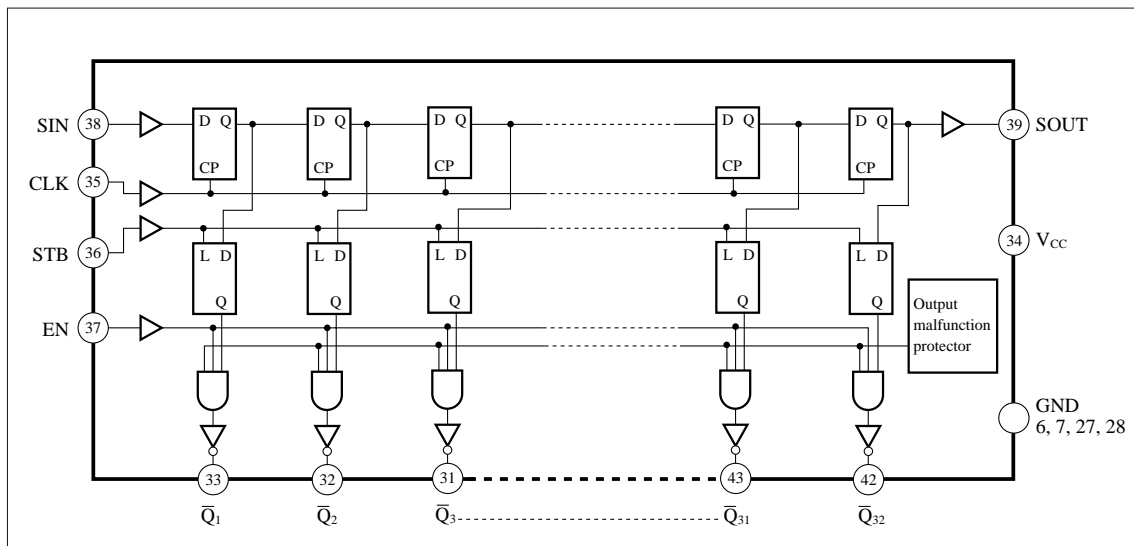
- Serial-in and serial-out/parallel-out
- Cascade connection allowed
- Built-in output malfunctioning preventive circuit
- Low current consumption at standby $I_{CC} \leq 100\mu A$
- High-breakdown, large current drive type output steps
Breakdown voltage : 30V
Output current : 120mA (per pin)
- Surface mountable 44-pin flat package (pin pitch : 0.8mm)

■ Applications

- Driving of the thermal heads
- Driving of the relays, LEDs, solenoids, etc.



■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	0 to 7	V
Output voltage	V _O	0 to 30	V
Output current	I _O	120 (Per one circuit)	mA
Power dissipation	P _D	1.8 *	W
Operating ambient temperature	T _{opr}	- 20 to + 75	°C
Storage temperature	T _{stg}	- 55 to + 125	°C

* When mounting onto the PCB, power dissipation is reduced at a rate of 15mW/°C from Ta= 25°C.

■ Recommended Operating Range (Ta=25°C)

Parameter	Symbol	Range	
Operating supply voltage	V _{CC}	4 to 6V	
Output voltage	V _O	below 30V	
Output current	I _O	below 100mA * ¹	
Clock frequency	f _{CLK}	below 10MHz * ²	
Input pulse width	CLK	t _w	over 40ns
	STB		over 40ns
Setup time	SIN	t _{su}	over 30ns
	STB		over 40ns
Hold time	SIN	t _h	over 20ns
	STB		over 0ns
Clock pulse rise time	t _r	below 500ns	
Clock pulse fall time	t _f	below 500ns	

*¹ An allowable value changes depends on the number of simultaneously turned-on circuits and the duty. Use with power dissipation taken into full account.

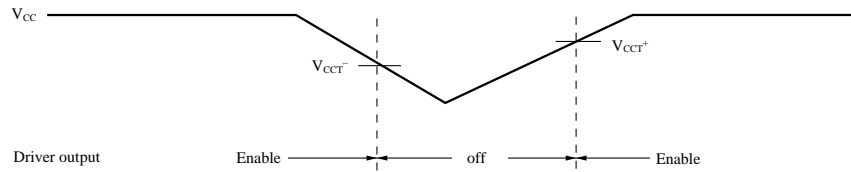
*² Input duty : 40 to 60%

■ Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Input voltage	V _{IH}	V _{CC} = 4 to 6V	0.7V _{CC}	—	V _{CC}	V
	V _{IL}		0	—	0.3V _{CC}	V
Input current	I _{IH}	V _{IH} = 5V	—	—	25	μA
	I _{IL}	V _{IL} = 0V	—	—	- 25	μA
Output voltage (SOUT)	V _{OH}	I _O = -1μA	4.9	—	—	V
	V _{OL}	I _O =1μA	—	—	0.1	V
Output current (SOUT)	I _{OH}	V _{OH} = 4.5V	- 4	—	—	mA
	I _{OL}	V _{OL} = 0.4V	4	—	—	mA
Output saturation voltage (Q̄n)	V _{CE(sat) 1}	I _{OL} =100mA	—	—	0.4	V
	V _{CE(sat) 2}	I _{OL} = 80mA	—	—	0.35	V
Output leakage current	I _{OLK1}	V _O = 30V (output OFF)	—	—	50	μA
	I _{OLK2}	V _O =15V (output OFF)	—	—	25	μA
Supply current	I _{CC1}	Total driver output OFF	—	—	100	μA
	I _{CC2}	Driver output 1 circuit ON	—	—	5	mA
Output malfunctioning preventive Circuit operating voltage	V _{CCT+}	*	2.9	—	3.9	V
	V _{CCT-}	*	2.6	—	3.6	V

* V_{CC}=5V unless otherwise specified

* Output malfunctioning preventive circuit operating voltage timing chart



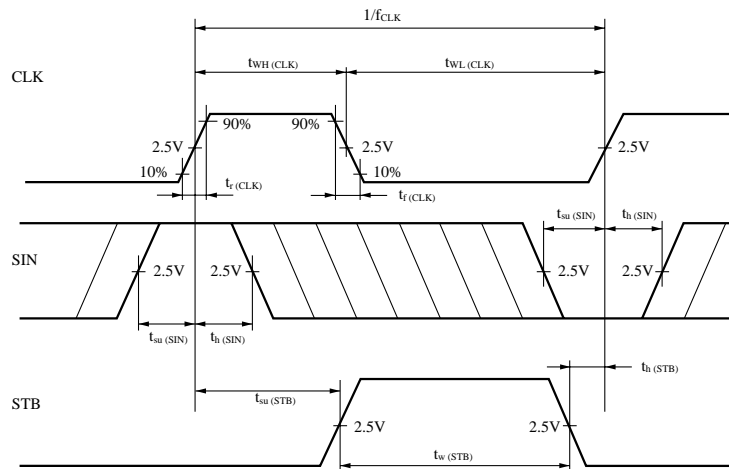
■ Switching Characteristics (Ta = 25°C)

Parameter	Symbol	Input	Output	Condition	min	typ	max	Unit
Maximum clock frequency	f_{max}	CLK			10	—	—	MHz
Propagation delay time	t_{PLH}	CLK	SOUT	$V_{CC} = 5V$ $C_L = 15pF$	—	—	100	ns
	t_{PHL}				—	—	100	ns
	t_{PLH}	CLK	$\bar{Q}n$	$V_{CC} = 5V$ $R_L = 100\Omega$ $C_L = 15pF$	—	—	2	μs
	t_{PHL}				—	—	0.5	μs
	t_{PLH}	EN	$\bar{Q}n$	$C_L = 15pF$	—	—	2	μs
	t_{PHL}				—	—	0.5	μs

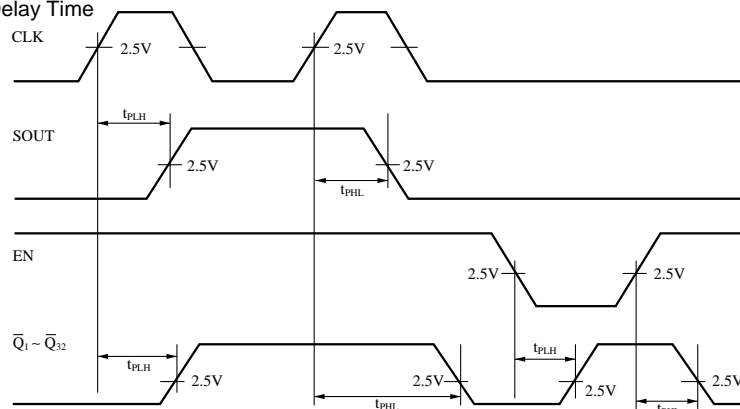
■ Supplementary Descriptions

• Timing Chart

1. Input Timing



2. Propagation Delay Time



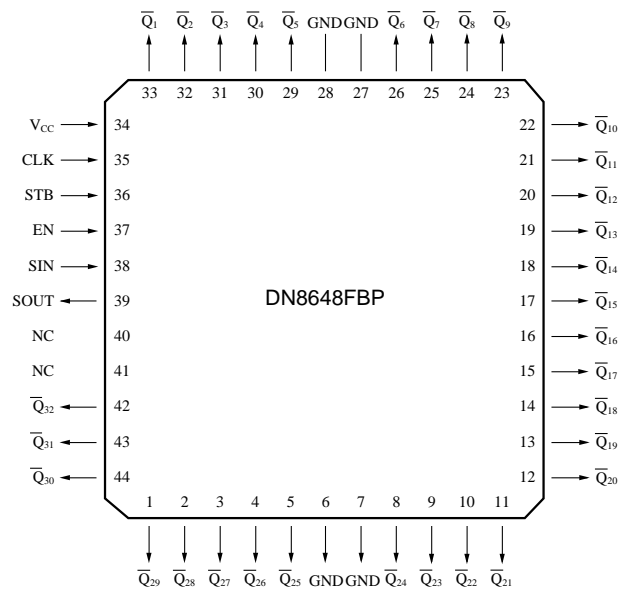
■ Supplementary Descriptions (cont.)

• Function Table

Input				Driver output		SOUT
CLK	EN	STB	SIN	\bar{Q}_1	\bar{Q}_n	
↑	L	×	×	H	H	Q'_{31}
↓	L	×	×	H	H	nc
↑	H	L	×	nc	nc	Q'_{31}
↑	H	H	L	H	\bar{Q}_{n-1}	Q'_{31}
↑	H	H	H	L	\bar{Q}_{n-1}	Q'_{31}
↓	H	H	×	nc	nc	nc

Note) H = High level, L = Low level, × = Either "H" or "L" will do, ↑ = Transition from "H" to "L",
 ↓ = Transition from "H" to "L", nc = No change, Q'_{31} = Status of the 31st shift register

• Pin Assignments



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