

4-, 5-, 6-Channel, Muxed Input Line Inversion LCD Gamma Buffers

ADD8504/ADD8505/ADD8506

FEATURES

- Single-supply operation: 3.3 V to 6.5 V**
- Rail-to-rail input, rail-to-rail output**
- High output current: 380 mA**
- Low supply current: 3.9 mA**
- Stable with 1 nF loads**
- Wide temperature range: -40°C to +105°C**
- 16-, 20-, and 24-lead, Pb-free, TSSOP packages**

APPLICATIONS

- LCD line inversion gamma references**
- Car navigation panels**
- Personal media player panels**

GENERAL DESCRIPTION

The ADD8504, ADD8505, and ADD8506 are 4-, 5-, and 6-channel LCD gamma reference buffers designed to drive column driver gamma inputs in line inversion panels. Each buffer channel has an A/B input to select between two gamma voltage curves. These buffer channels drive the resistor ladders of LCD column drivers for gamma correction. The ADD8504/ADD8505/ADD8506 outputs have high slew rates and output drives that increase the stability of the reference ladder resulting in optimal gray scale and visual performance.

The ADD8504/ADD8505/ADD8506 are specified over the -40°C to +105°C temperature range. They are available, respectively, in 16-, 20-, and 24-lead thin shrink small outline (TSSOP), surface-mount, Pb-free packages.

PIN CONFIGURATION DIAGRAMS

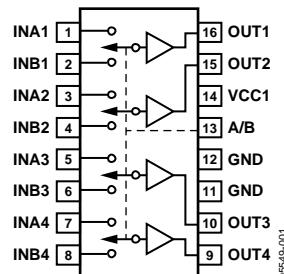


Figure 1. ADD8504: 4-Channel Buffer

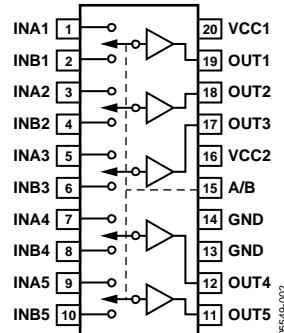


Figure 2. ADD8505: 5-Channel Buffer

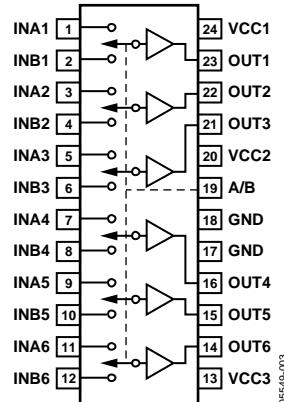


Figure 3. ADD8506: 6-Channel Buffer

Rev. B

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ADD8504/ADD8505/ADD8506

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REVISION HISTORY

1/06—Rev. A to Rev. B

| | |
|--|---|
| Added Pin Configurations and Function Descriptions Section | 5 |
| Added Table 5..... | 8 |

10/05—Rev. 0 to Rev. A

| | |
|---|---|
| Added ADD8504 and ADD8505.....Universal Changes to Specifications Section | 3 |
| Updated Outline Dimensions | 7 |
| Changes to Ordering Guide | 7 |

9/05—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted. V_{IN} denotes buffer input voltage; I_{LOAD} denotes load current; R_L denotes load resistance; C_L denotes load capacitance.

Table 1.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---------------------------------|-----------|--|-------|------|-----|------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $0 \text{ V} \leq V_{IN} \leq 5 \text{ V}$ | | 20 | | mV |
| Input Common-Mode Voltage Range | V_{CM} | | 0 | 5 | | V |
| Input Bias Current | I_B | $V_{IN} = 2.5 \text{ V}$ | | 2 | 50 | nA |
| Voltage Gain | A_{VO} | | 0.985 | | | V/V |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $I_{LOAD} = +20 \text{ mA}$ | 4.75 | | | V |
| Output Voltage Low | V_{OL} | $I_{LOAD} = -20 \text{ mA}$ | | 0.2 | | V |
| Output Resistance | R_{OUT} | $-20 \text{ mA} \leq I_{LOAD} \leq +20 \text{ mA}; 0.5 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ | | 0.20 | | Ω |
| Output Short-Circuit Current | I_{SC} | | 120 | 380 | | mA |
| POWER SUPPLY | | | | | | |
| Supply Current ADD8504 | I_{SY} | $V_{IN} = 2.5 \text{ V}$ | | 2.7 | 3.8 | mA |
| ADD8505 | | | | 3.0 | 4.4 | mA |
| ADD8506 | | | | 3.9 | 5.1 | mA |
| Supply Voltage Range | V_{CC} | | 3.3 | 6.5 | | V |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $C_L = 15 \text{ pF}$ $R_L = 250 \Omega$ | 7.0 | | | $\text{V}/\mu\text{s}$ |
| Settling Time | t_S | $C_L = 200 \text{ pF}, R_L = 10 \text{ k}\Omega$ | 6.2 | | | $\text{V}/\mu\text{s}$ |
| LOGIC INPUT CHARACTERISTICS | | | | | | |
| Input Current Low | I_{IL} | $V_{IN} = 0.0 \text{ V}$ | | 100 | | nA |
| Input Current High | I_{IH} | $V_{IN} = 5.0 \text{ V}$ | | 100 | | nA |
| Input Voltage Low | V_{IL} | $V_{CC} = 5.0 \text{ V}, -40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | | 0.8 | | V |
| Input Voltage Low | V_{IL} | $V_{CC} = 3.3 \text{ V}, -40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | | 0.7 | | V |
| Input Voltage High | V_{IH} | $V_{CC} = 5.0 \text{ V}, -40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | 1.7 | | | V |
| Input Voltage High | V_{IH} | $V_{CC} = 3.3 \text{ V}, -40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | 1.4 | | | V |

ADD8504/ADD8505/ADD8506

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|--------------------------------------|------------------------|
| Supply Voltage | 7 V |
| Input Voltage | GND to V _{CC} |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3. Thermal Package Characteristics

| Model | Package Type | θ _{JA} ¹ | θ _{JC} ² | Unit |
|-------------|-----------------------|------------------------------|------------------------------|------|
| ADD8504WRUZ | 16-Lead Pb-Free TSSOP | 150 | 28 | °C/W |
| ADD8505WRUZ | 20-Lead Pb-Free TSSOP | 143 | 45 | °C/W |
| ADD8506WRUZ | 24-Lead Pb-Free TSSOP | 128 | 45 | °C/W |

¹ θ_{JA} is specified for natural convection on a two-layer board.

² θ_{JC} is specified for natural convection on a two-layer board.

ESD PERFORMANCE

Table 4.

| Model | HBM ¹ | MM ² | FICDM ³ |
|-------------|------------------|-----------------|--------------------|
| ADD8504WRUZ | 4.0 kV | 400 V | 1.0 kV |
| ADD8505WRUZ | 3.5 kV | 200 V | 1.0 kV |
| ADD8506WRUZ | 3.5 kV | 200 V | 1.0 kV |

¹ Human body model.

² Machine model.

³ Field induced charge device model.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

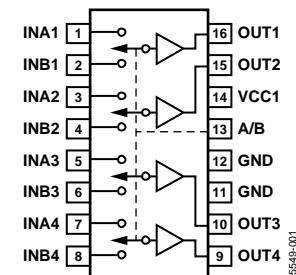
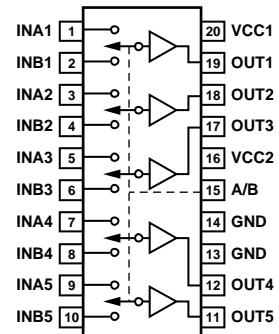
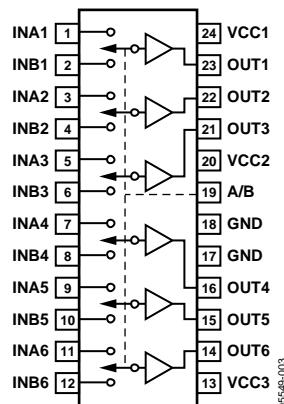


Table 5. Pin Function Descriptions

| ADD8506 Pin No. | ADD8505 Pin No. | ADD8504 Pin No. | Mnemonic | Function | Description |
|--------------------|--------------------|--------------------|----------|----------|--|
| 1 | 1 | 1 | INA1 | Input | Channel 1 Buffer Input A. |
| 2 | 2 | 2 | INB1 | Input | Channel 1 Buffer Input B. |
| 3 | 3 | 3 | INA2 | Input | Channel 2 Buffer Input A. |
| 4 | 4 | 4 | INB2 | Input | Channel 2 Buffer Input B. |
| 5 | 5 | 5 | INA3 | Input | Channel 3 Buffer Input A. |
| 6 | 6 | 6 | INB3 | Input | Channel 3 Buffer Input B. |
| 7 | 7 | 7 | INA4 | Input | Channel 4 Buffer Input A. |
| 8 | 8 | 8 | INB4 | Input | Channel 4 Buffer Input B. |
| 9 | 9 | N/A | INA5 | Input | Channel 5 Buffer Input A. |
| 10 | 10 | N/A | INB5 | Input | Channel 5 Buffer Input B. |
| 11 | N/A | N/A | INA6 | Input | Channel 6 Buffer Input A. |
| 12 | N/A | N/A | INB6 | Input | Channel 6 Buffer Input B. |
| 13 | N/A | N/A | VCC3 | Power In | Power Supply Input. Short to VCC1 and VCC2. Typically connected to +5 V. |
| 14 | N/A | N/A | OUT6 | Output | Channel 6 Buffer Output. |
| 15 | 11 | N/A | OUT5 | Output | Channel 5 Buffer Output. |
| 16 | 12 | 9 | OUT4 | Output | Channel 4 Buffer Output. |
| 17, 18 | 13, 14 | 11, 12 | GND | Ground | Ground. |
| 19 | 15 | 13 | A/B | Input | Switch Control. Logic high selects Input A; logic low selects Input B. |
| 20 | 16 | N/A | VCC2 | Power In | Power Supply Input. Short to VCC1 and VCC3. Typically connected to +5 V. |
| 21 | 17 | 10 | OUT3 | Output | Channel 3 Buffer Output. |
| 22 | 18 | 15 | OUT2 | Output | Channel 2 Buffer Output. |
| 23 | 19 | 16 | OUT1 | Output | Channel 1 Buffer Output. |
| 24 | 20 | 14 | VCC1 | Power In | Power Supply Input. Short to VCC2 and VCC3. Typically connected to +5 V. |

ADD8504/ADD8505/ADD8506

TYPICAL PERFORMANCE CHARACTERISTICS

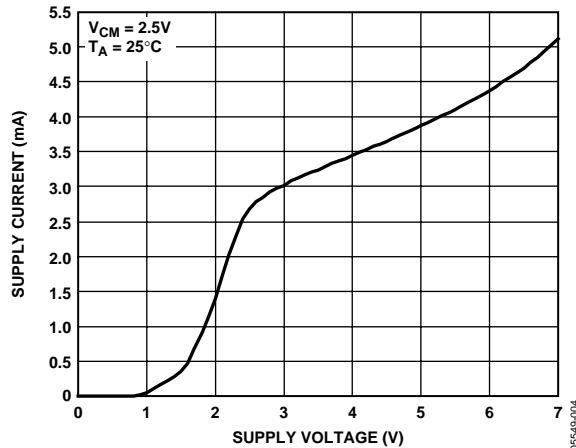


Figure 7. Supply Current vs. Supply Voltage

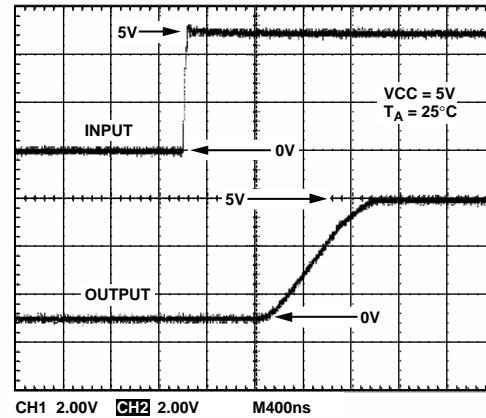


Figure 10. Transient Response—Rising

05549-007

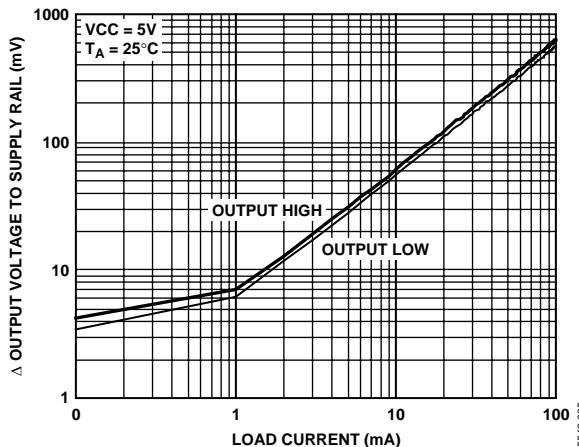


Figure 8. Δ Output Voltage to Supply Rail vs. Load Current

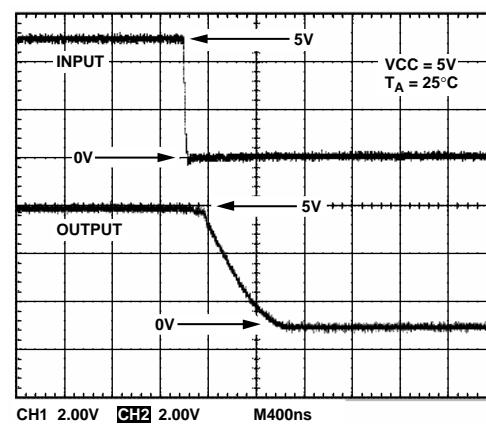


Figure 11. Transient Response—Falling

05549-008

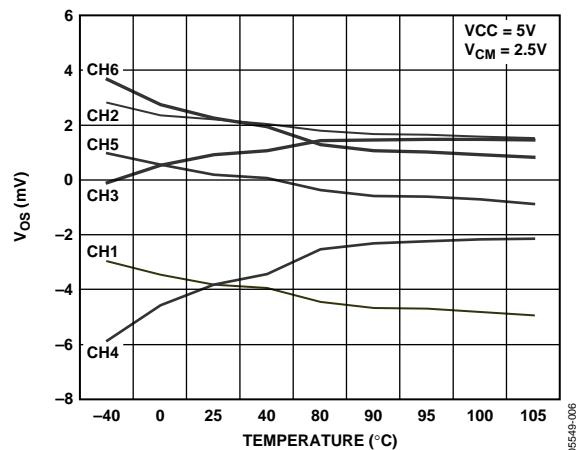


Figure 9. Offset Voltage vs. Temperature

APPLICATIONS

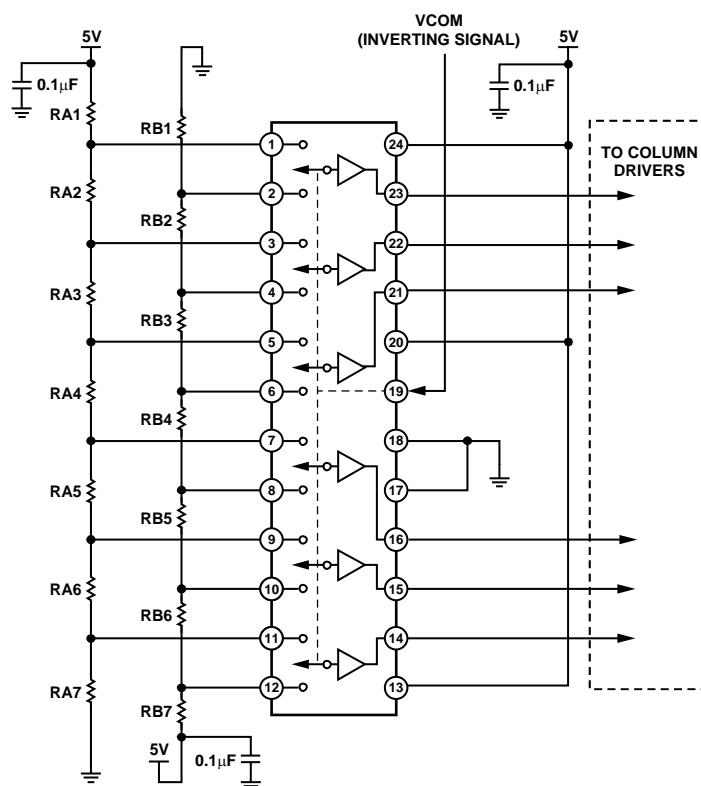
The ADD8504/ADD8505/ADD8506 have CMOS buffers with A/B inputs to select between two different reference voltages set up by an external resistor ladder. Input bias currents are orders of magnitude less than competitive parts. This allows the use of a very large resistor ladder to save supply current.

The buffer outputs are designed to drive resistive or capacitive loads. Therefore, to attain the best display performance, do not use resistors in series with these outputs. Outputs have high slew rates and 6 μ s settling times. Each output delivers a minimum of 120 mA, ensuring a fast response to varying loads.

Power supply pins on the ADD8505 and ADD8506 have multiple ground (GND) and supply (VCC) connections. Because of the high peak currents that these buffers deliver, it is recommended that all GND and VCC pins be connected and suitably bypassed.

Table 6. MUX Function

| A/B Select | Input |
|------------|-------|
| Logic High | INAx |
| Logic Low | INBx |



NOTES

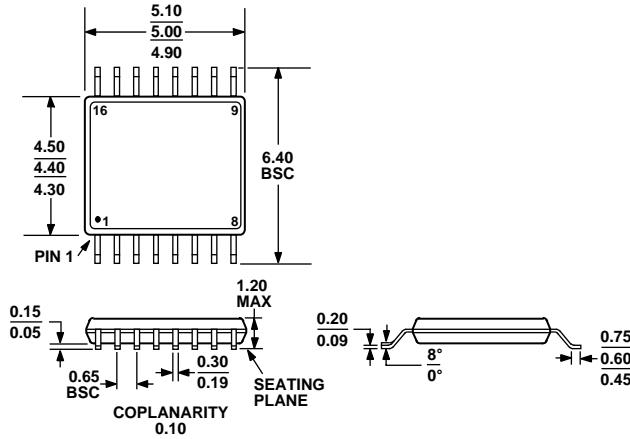
1. RA_x RESISTORS ARE USED TO SET POSITIVE INVERSION GAMMA VOLTAGES.
2. RB_x RESISTORS ARE USED TO SET NEGATIVE INVERSION GAMMA VOLTAGES.

05549-009

Figure 12. Typical Application

ADD8504/ADD8505/ADD8506

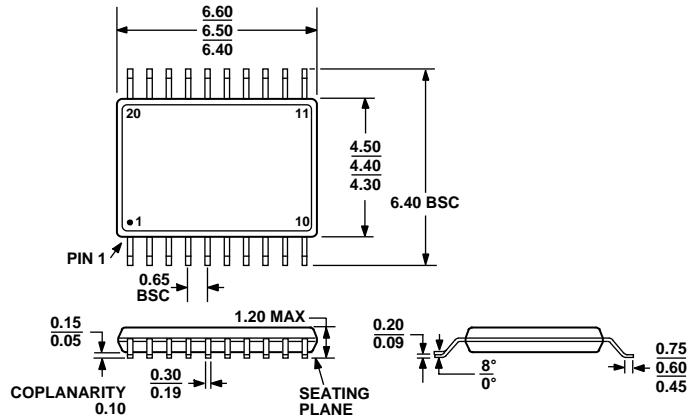
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 13. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

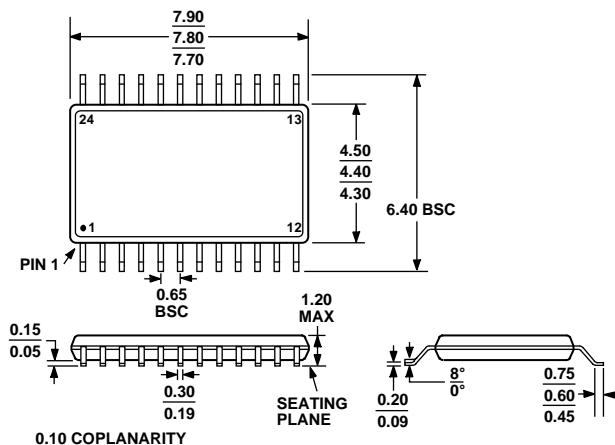
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 14. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 15. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Ordering Quantity |
|--------------------------------|-------------------|---|----------------|-------------------|
| ADD8504WRUZ ¹ | -40°C to +105°C | 16-Lead Thin Shrink Small Outline Package [TSSOP], Tube | RU-16 | 96 |
| ADD8504WRUZ-REEL7 ¹ | -40°C to +105°C | 16-Lead Thin Shrink Small Outline Package [TSSOP], 7" Reel | RU-16 | 1,000 |
| ADD8504WRUZ-REEL ¹ | -40°C to +105°C | 16-Lead Thin Shrink Small Outline Package [TSSOP], 13" Reel | RU-16 | 2,500 |
| ADD8505WRUZ ¹ | -40°C to +105°C | 20-Lead Thin Shrink Small Outline Package [TSSOP], Tube | RU-20 | 96 |
| ADD8505WRUZ-REEL7 ¹ | -40°C to +105°C | 20-Lead Thin Shrink Small Outline Package [TSSOP], 7" Reel | RU-20 | 1,000 |
| ADD8505WRUZ-REEL ¹ | -40°C to +105°C | 20-Lead Thin Shrink Small Outline Package [TSSOP], 13" Reel | RU-20 | 2,500 |
| ADD8506WRUZ ¹ | -40°C to +105°C | 24-Lead Thin Shrink Small Outline Package [TSSOP], Tube | RU-24 | 96 |
| ADD8506WRUZ-REEL7 ¹ | -40°C to +105°C | 24-Lead Thin Shrink Small Outline Package [TSSOP], 7" Reel | RU-24 | 1,000 |
| ADD8506WRUZ-REEL ¹ | -40°C to +105°C | 24-Lead Thin Shrink Small Outline Package [TSSOP], 13" Reel | RU-24 | 2,500 |

¹Z = Pb-free part.