ZARLINK SEMICONDUCTOR

ZL40813/14/18

13.5GHz Fixed Modulus Dividers

Data Sheet

January 2003

Features

- Very High Operating Speed
- Low Phase Noise (Typically better than -146dBc/Hz at 10kHz offset)
- 5V Single Supply Operation
- Low Power Dissipation: 500mW (Typ)
- Surface Mount Plastic Package with Exposed Pad (See Application Notes)

Prescaler Modulus

- ZL40813 - Divide by 8
- ZL40814 - Divide by 16
- ZL40818 - Divide by 4

Applications

- 10.5 to 13.5GHz PLL applications
- LMDS
- Instrumentation
- Satellite Communications
- Fibre Optic Communications; OC48, OC192
- Ultra Low Jitter Clock Systems

Ordering Information

ZL40813/DCE (tubes)	8 pin SOIC
ZL40813/DCF (tape and reel)	8 pin SOIC
ZL40814/DCE (tubes)	8 pin SOIC
ZL40814/DCF (tape and reel)	8 pin SOIC
ZL40818/DCE (tubes)	8 pin SOIC
ZL40818/DCF (tape and reel)	8 pin SOIC

-40°C to +85°C

Description

The ZL40813, 14 and 18 are 5V supply, very high speed low power prescalers for professional applications with a fixed modulus of 8, 16, or 4 respectively. The dividing elements are dynamic D type flip flops and allow operation from 10.5GHz to 13.5GHz with a sinewave input (Note these prescalers are not suitable for D.C. operation). The output stage has internal 50 ohm pull up giving a 1v p-p output. See application notes for more details.

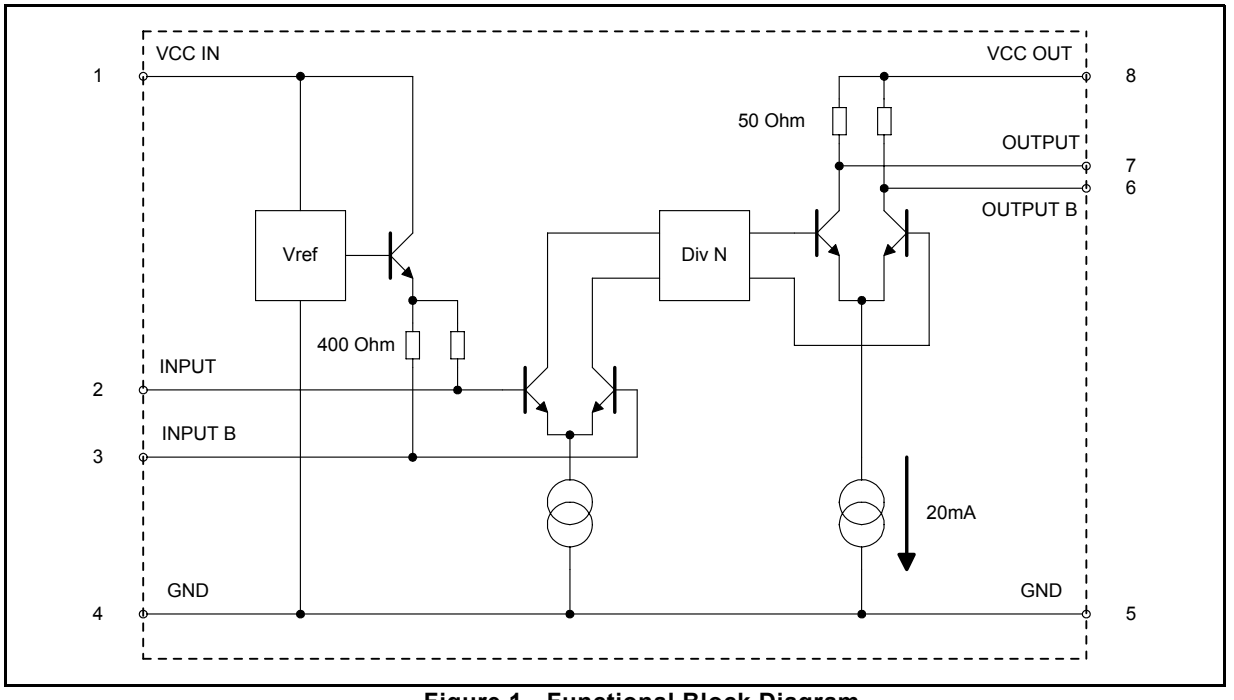


Figure 1 - Functional Block Diagram

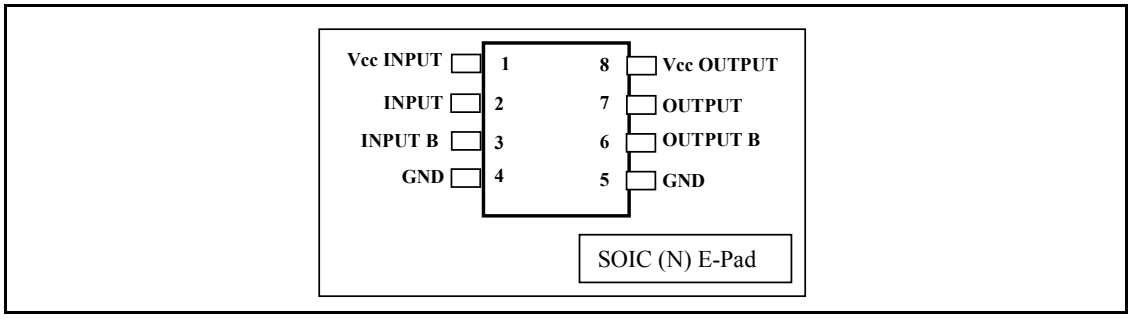


Figure 2 - Pin Connections - Top View

1.0 Application Configuration

Figure 3 shows a recommended application configuration. This example shows the devices set up for single-ended input and differential output operation.

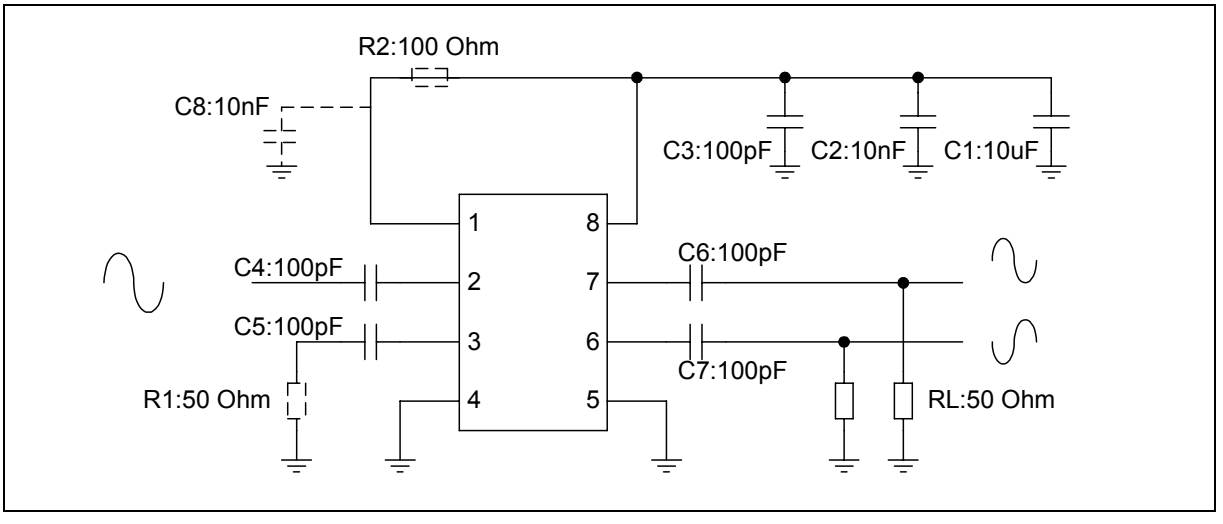


Figure 3 - Recommended circuit configuration.

The above circuit diagram shows some components in dotted lines. These are optional in many applications.

1. C1 (10 µF) and C2 (10 nF) power supply decoupling capacitors may be available on the board already.
2. R2 (100 Ohm) and C8 (10 nF) can be included if further power supply decoupling is required for the first stage biasing circuit. This may optimise the noise and jitter performance. The values are suggestions and may have to be modified if the existing supplies are particularly noisy.
3. R1 (50 Ohm), in series with C5 (100 pF), may reduce feedthrough of the input signal to the output.

2.0 Evaluation Boards From Zarlink Semiconductor

Zarlink Semiconductor provide a prescaler evaluation board. These are primarily for those interested in performing their own assessment of the operation of the prescalers. The boards are supplied unpopulated and may be assembled for single ended or differential input and output operation. Once assembled, all that is required is an RF source and a DC supply for operation. The inputs and outputs are connected via side launch SMA connectors.

Absolute Maximum Ratings

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	Vcc		6.5	V
2	Prescalar Input Voltage		2.5	(vdd_IO+5%)	Vp-p
3	ESD protection (Static Discharge)		2k		V
4	Storage Temperature	T_{ST}	-65	+150	ºC
5	Maximum Junction Temp.	$T_J$max		+125	ºC
6	Thermal Characteristics	TH_{JA}	58.6		ºC/W multi-layer PCB

AC/DC Electrical Characteristics (Tamb = 25C, Vcc = 5V) †

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	1		0.35		mA	Input stage bias current‡
Supply current	8	58	93	130	mA	ZL40813 Div8
Supply current	8	61	96	134	mA	ZL40814 Div16
Supply current	8	61	100	134	mA	ZL40818 Div4

† These characteristics are guaranteed by either production test or design.

‡ Pin 1 is the Vcc pin for the 1st stage bias current. In some applications e.g. if the power supply is noisy, it may be advantageous to add further supply decoupling to this pin (i.e. an additional R, C filter, see diagram of the recommended circuit configuration Figure 3,).

Input and Output Characteristics †

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Input frequency	2,3	8.5		14.5	GHz	RMS sinewave‡
Input sensitivity	2,3		-2	2	dBm	fin = 10.5GHz to 13.5Ghz
Input overload	2,3	10	14		dBm	fin = 10.5GHz to 13.5Ghz
Output voltage	6,7		1		Vp-p	Differential Into 50ohm pullup resistors
Output power	6,7	-6	-1		dBm	fin = 10.5GHz to 13.5GHz
Phase Noise (10kHz offset)	6,7		-140		dBc/Hz	fin = 10GHz, pwr ip = 0dBm See graphs, Figure 7 to Figure 9
O/P Duty Cycle	6,7	45	50	55	%	Differential output

† These characteristics are guaranteed by either production test or design.

† Input sensitivity and output power values assume 50 Ohm source and load impedances.

‡ The device characterisation test method incremented the amplitude over the entire range of frequency and ensures that there are no "holes" in the characteristic.

For details of the test set-up, refer to the Application Note for RF Prescalers.

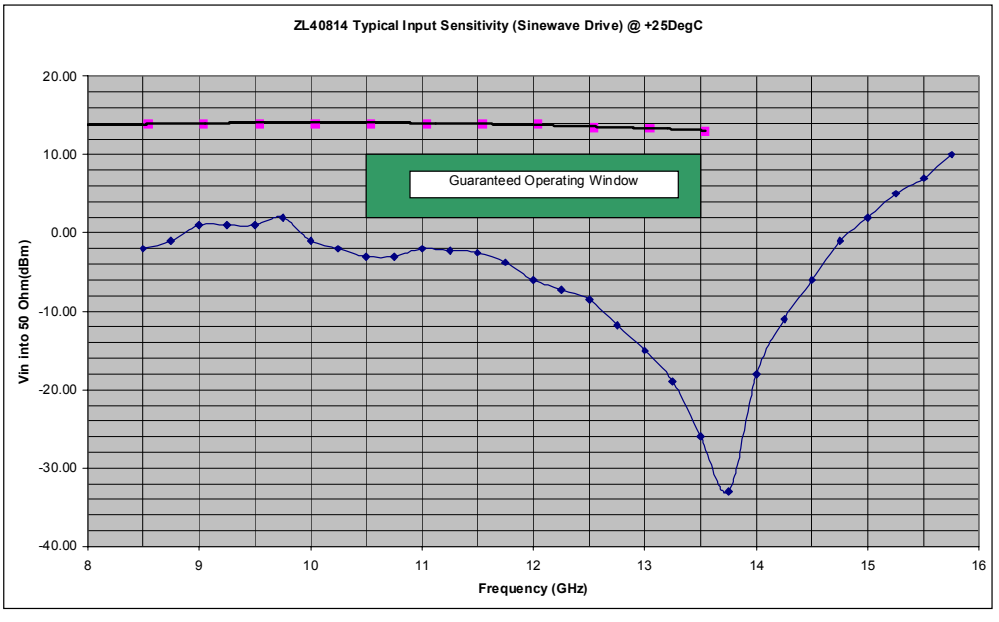


Figure 4 - Graph of Input Sensitivity @ +25 Deg C

Electrical Characteristics (Vcc = 5V ±5%, Tamb = -40 to +85C)

The following characteristics are guaranteed by design and characterisation over the range of operating conditions unless otherwise stated:

(Input Frequency range 9 to 13.5GHz rms Sinewave)

Supply Current Table

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	1		0.35		mA	Input stage bias current †
Supply current	8	51	93	144	mA	ZL40813
Supply current	8	54	96	148	mA	ZL40814
Supply current	8	54	100	148	mA	ZL40818

† Pin 1 is the Vcc pin for the 1st stage bias current. In some applications e.g. if the power supply is noisy, it may be advantageous to add further supply decoupling to this pin (i.e. an additional R, C filter, see diagram of the recommended circuit configuration, Figure 9).

Input and Output Characteristics Table

Input sensitivity and output power values assume 50 Ohm source and load impedances

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Input sensitivity	2,3		-2	2	dBm	fin = 10.5 to 12.5 GHz
Input sensitivity	2,3	10	14		dBm	fin = 10.5 to 13.5 GHz
Output voltage	6,7		1		Vp-p	Differential Into 50ohm pullup resistors
Output power	6,7	-6	0	5	dBm	Single-ended output, fin = 9GHz to 13GHz, pwr ip= -10dBm . See graphs, Figure 7 to Figure 9.
O/P Duty Cycle	6,7	45	50	55	%	
Trise and Tfall	6,7		110		ps	

For details of the test set-up, refer to the Application Note for RF Prescalers.

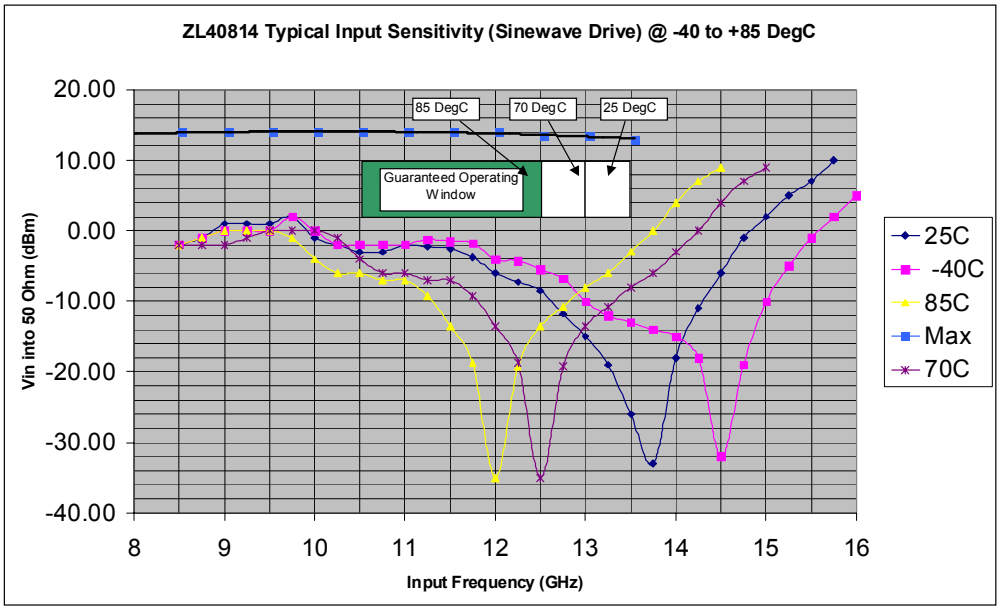


Figure 5 - Graph of Input Sensitivity @ -40, +25, +70 and +85 Deg C.

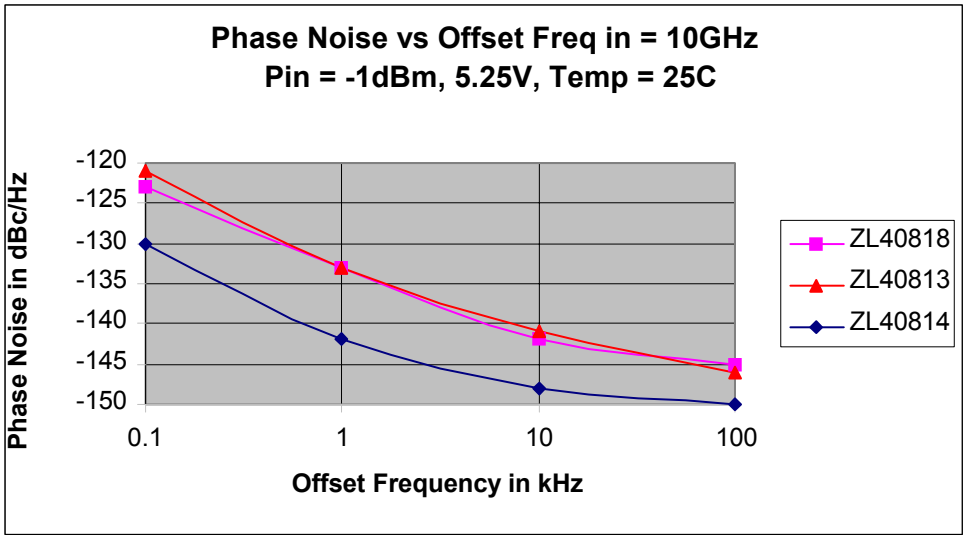


Figure 6 - 13.5GHz Prescalers; Phase Noise vs Offset Frequency

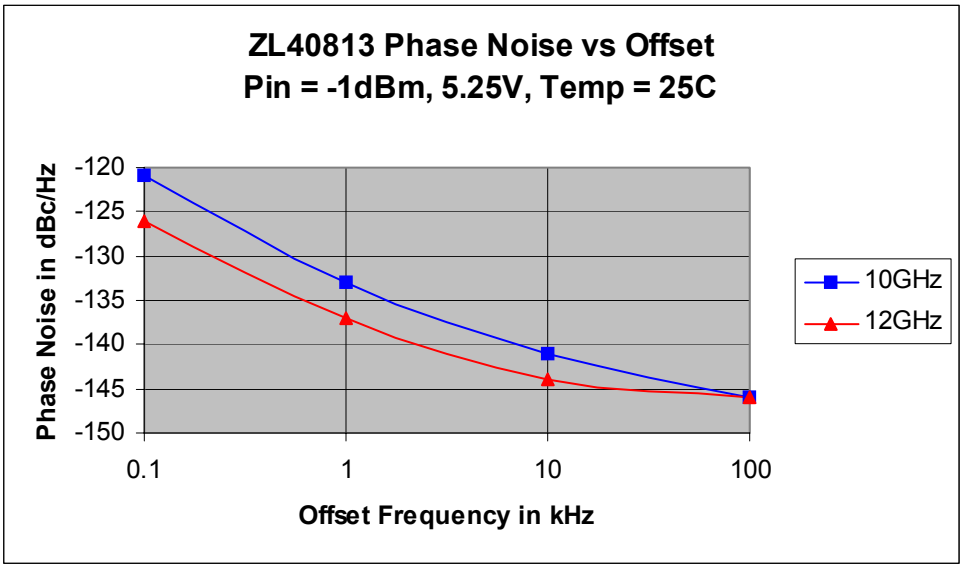


Figure 7 - ZL40813; Phase Noise vs Offset Frequency

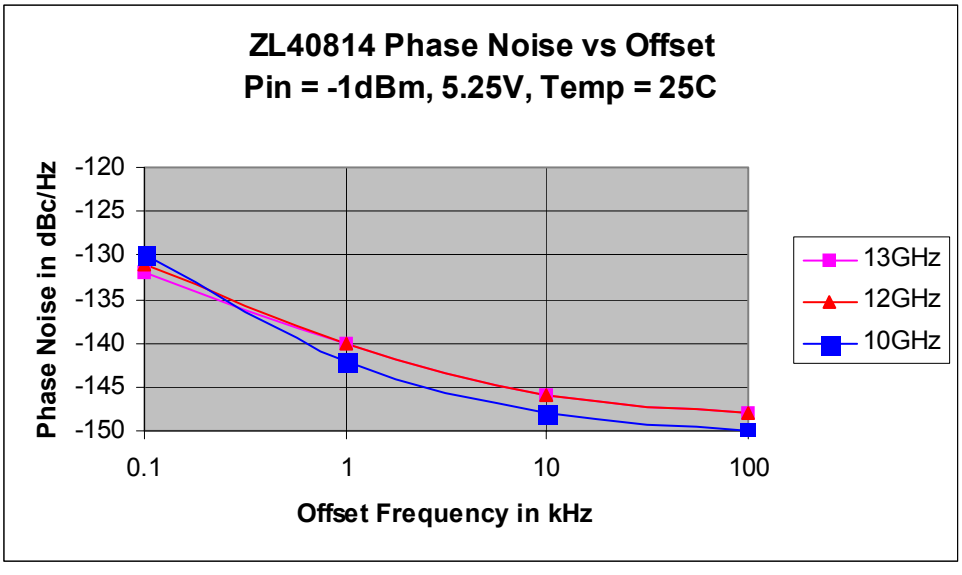


Figure 8 - ZL40814; Phase Noise vs Offset Frequency

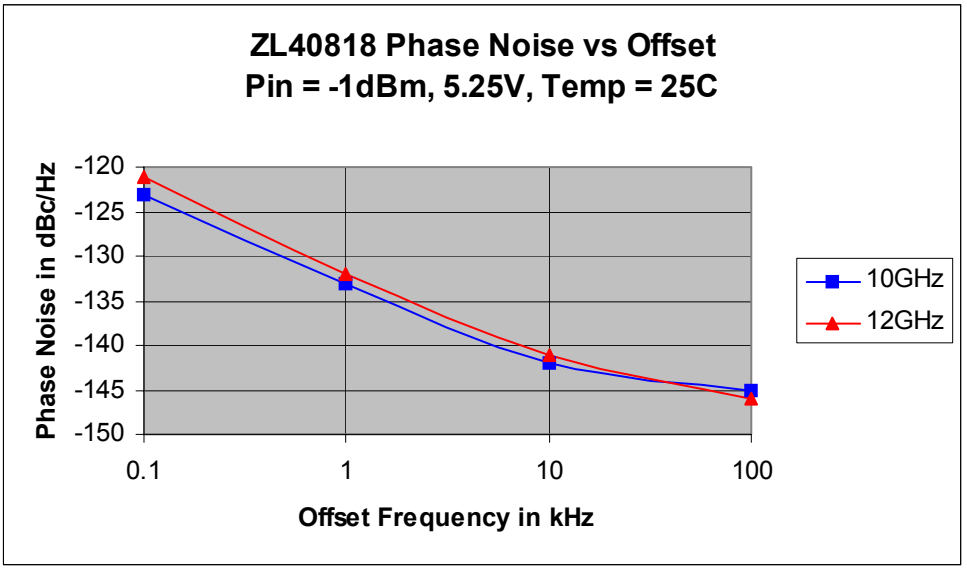


Figure 9 - ZL40818; Phase Noise vs Offset Frequency

3.0 Single Ended Output Power.

The following graphs show how the output power varies with supply.

Differential power will be 3dB greater.

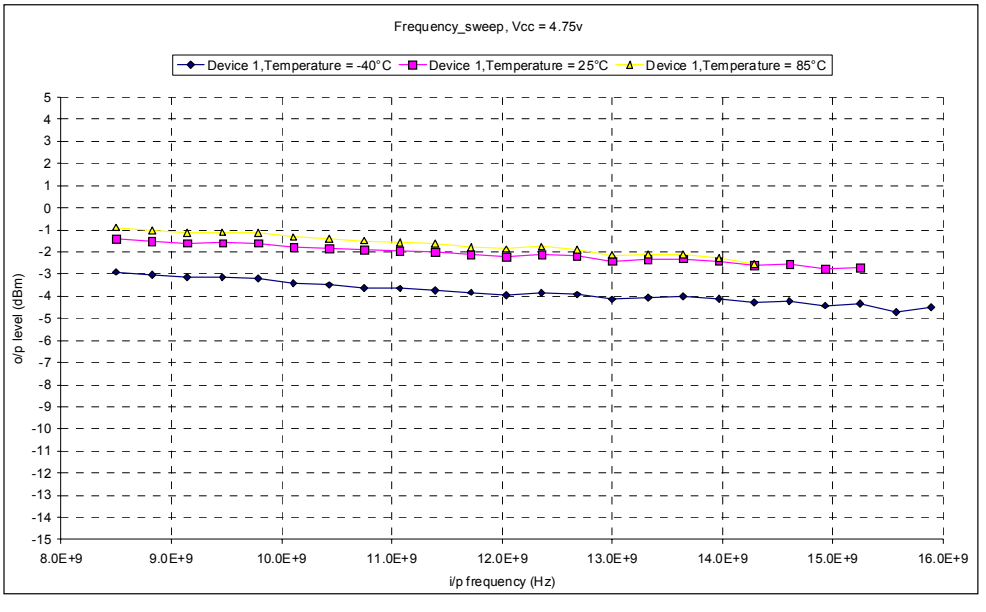


Figure 10 - ZL40813 (div by 8) Pout vs Input Frequency (Vcc = 4.75V)

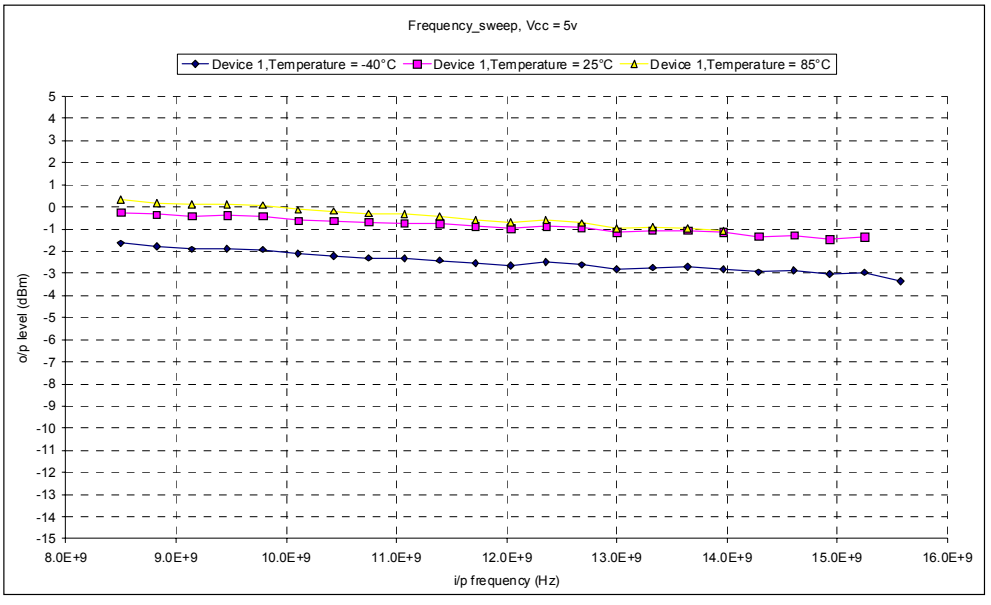


Figure 11 - ZL40813 (div by 8) Pout vs Input Frequency (Vcc = 5.0V)

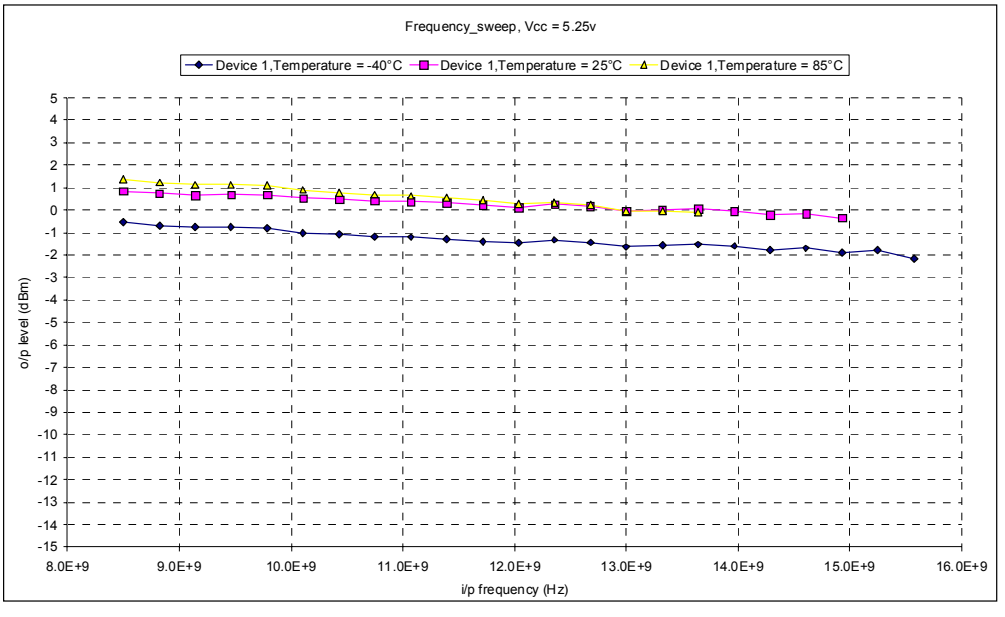


Figure 12 - ZL40813 (div by 8) Pout vs Input Frequency (Vcc = 5.25V)

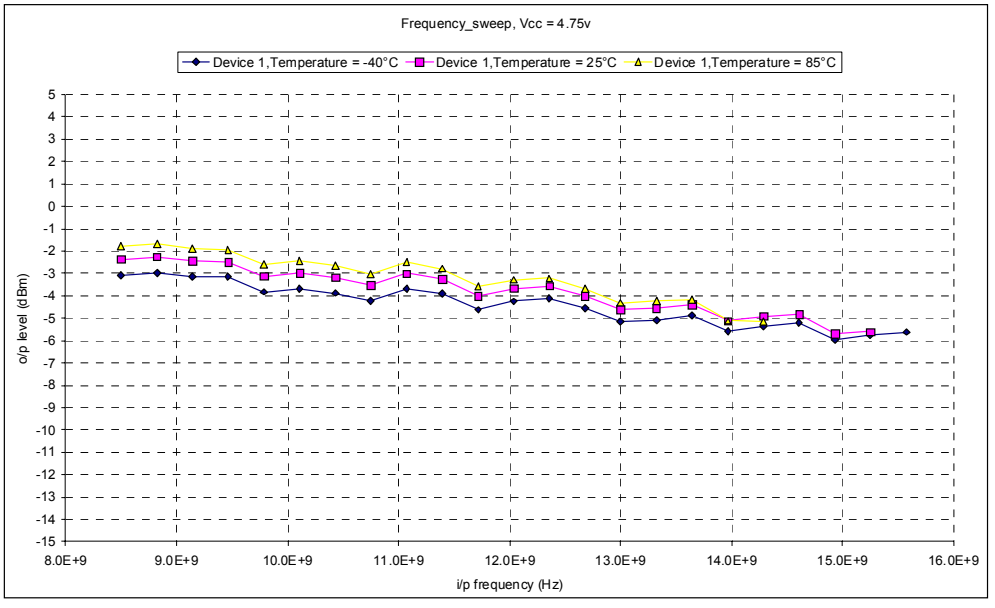


Figure 13 - ZL40818 (div by 4) Pout vs Input Frequency (Vcc = 4.75V)

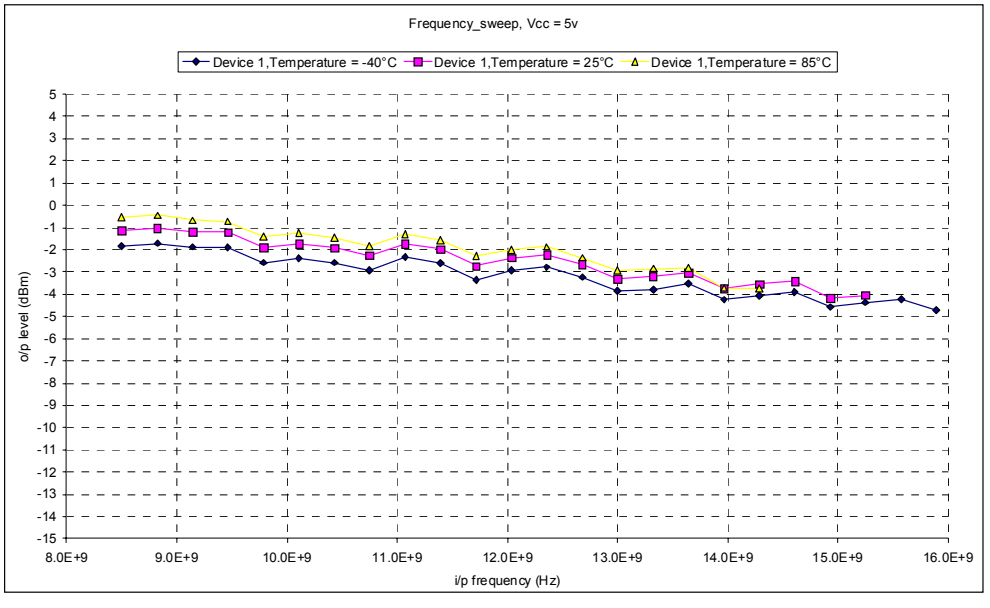


Figure 14 - ZL40818 (Div by 4) Pout vs Input Frequency (Vcc = 5.0V)

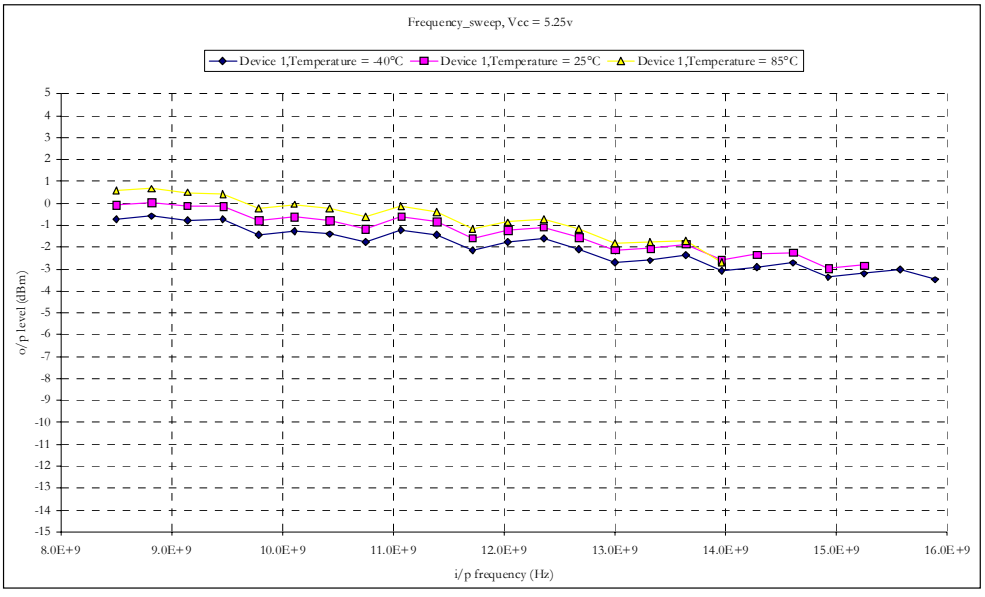


Figure 15 - ZL40818 (Div by 4) Pout vs Input Frequency (Vcc = 5.25V)

4.0 Oscillographs of the divider output waveforms

The following oscillographs show that the low-level feedthrough of the input waveform can be further reduced by summing the two output pins of the device differentially, refer to Figure 16 and Figure 17.

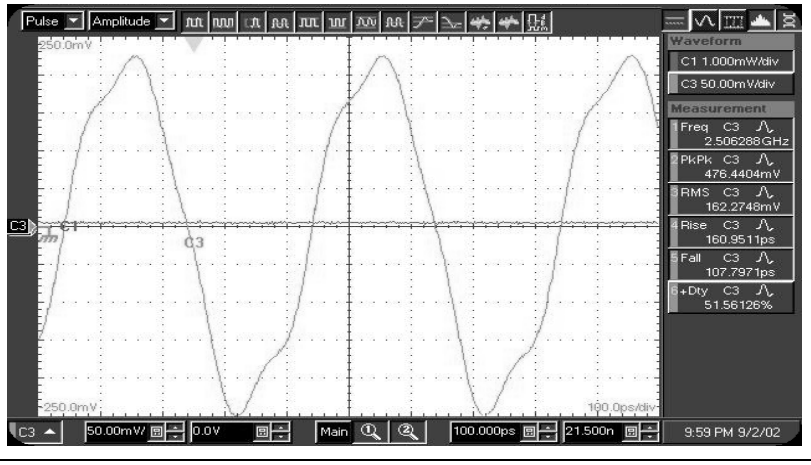


Figure 16 - Single-ended output waveform, showing some feedthrough of the input waveform. VCC = 5V, Vin = 2dBm, Fin = 10GHz.

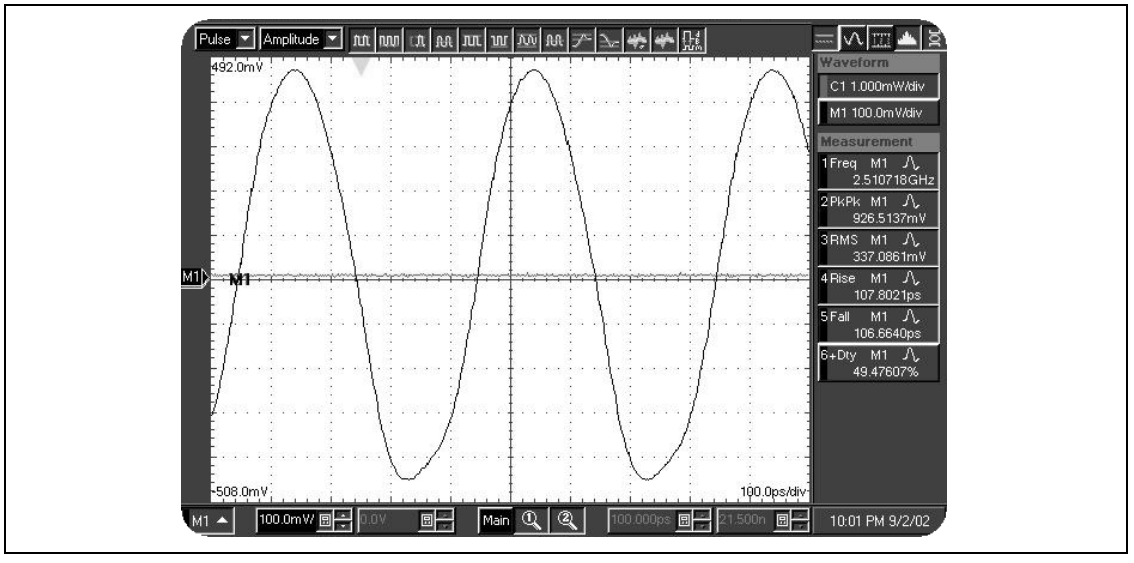


Figure 17 - Differential output waveform, showing reduced feedthrough of the input waveform

VCC = 5V, Vin = 2dBm, Fin = 10GHz.

5.0 Application Notes

5.1 Application Circuit

Figure 3 illustrates the recommended Single Ended Application Circuit. This represents the circuit used to complete characterisation. The tabulated Electrical performance is guaranteed using this application circuit.

A blank application board is available.

5.1.1 Circuit Options

The application circuit includes some optional components that may be required to improve tolerance of system noise present in the application.

Dummy R source may be added to the inverting input to provide a better matched source impedance at the input. This will improve the rejection of common mode noise present within the system.

Dummy R load may be added to the inverting output to provide better matched load at the output. This will reduce the radiated EMI at the output and reduce the Output Noise present on the supply rail.

Rfilter can be inserted between the Vcc in and the Vcc_out to provide additional filtering to the input Vcc. The input Vcc powers the input bias reference only and can be a sensitive point to system noise. The nominal input current at Vcc_IN s 0.35mA. An alternative would be to use an inductive choke.

C1 is additional Supply Filtering and should be added with Rfilter. The IC includes 10pF of on Chip Supply Filtering.

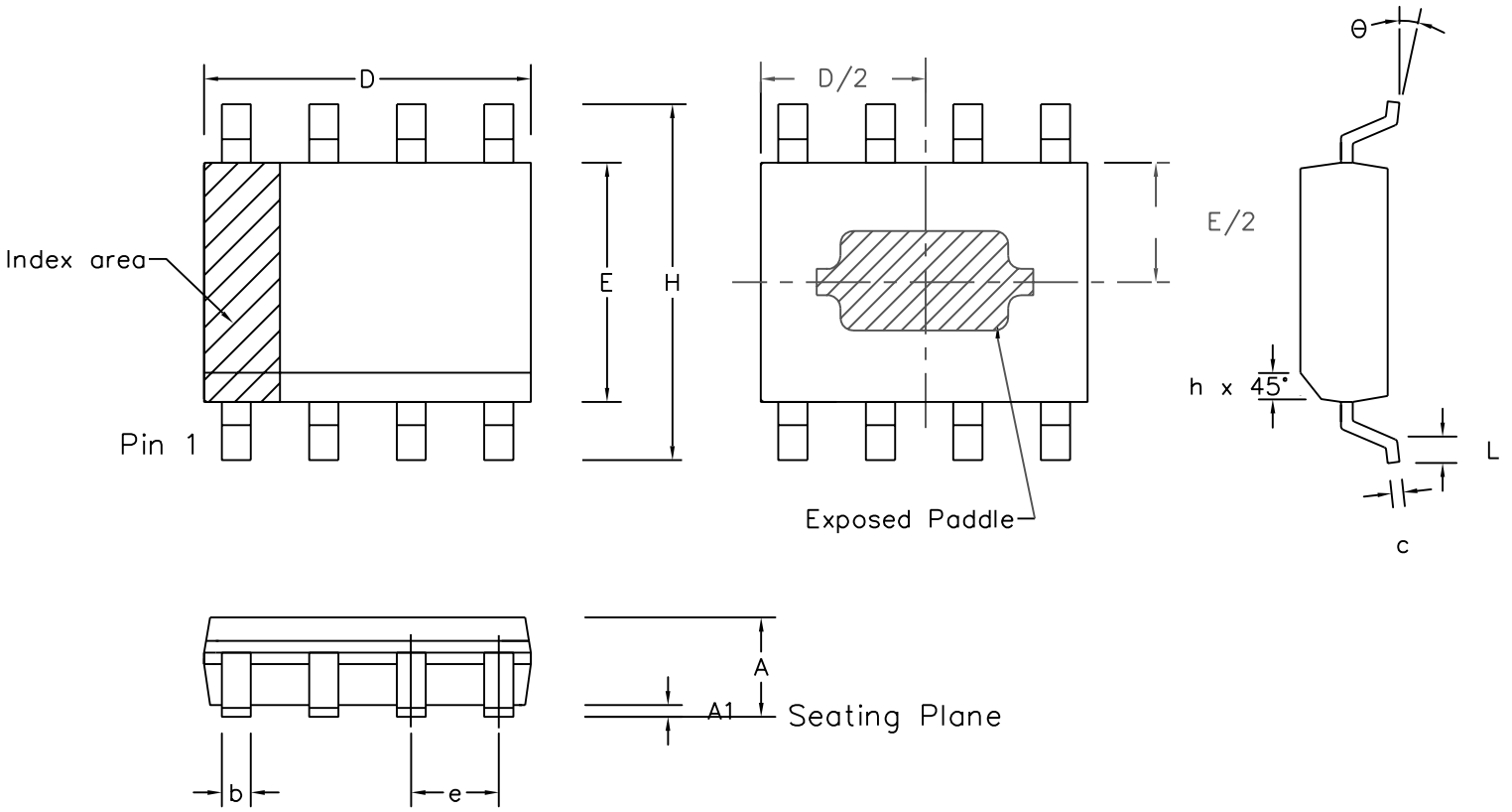
5.2 Single Ended or Differential Load

Figure 16 and Figure 17 illustrate the output waveform when measured differential and single ended with a 10GHz waveform at the input at a level of +2dBm. The single ended output contains some input frequency break through which contributes to the distortion present. This is a common mode signal which is rejected if the output is taken differentially.

Differential operation also provides an additional 3dBV output power.

Differential Operation reduces the radiated EMI in the system and reduces the susceptibility to common mode system noise.

NOTE: It is strongly recommended that these devices are used differentially for all applications.



	Min Inches	Max inches	Min mm	Max mm
A	0.056	0.066	1.43	1.68
A1	0.000	0.004	0.00	0.10
D	0.189	0.196	4.80	4.98
H	0.230	0.244	5.84	6.20
E	0.150	0.157	3.81	3.99
L	0.16	0.35	0.41	0.89
e	0.050 BSC		1.27 BSC	
b	0.0138	0.0192	0.35	0.49
c	0.0075	0.0098	0.19	0.25
θ	0°	8°	0°	8°
h	0.010	0.016	0.25	0.41
	Pin Features		Pin Features	
N	8		8	

Notes:

1. Controlling dimensions are in inches.
2. Dimensions D & E do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
3. Exposed paddle not to scale on drawing
4. Extrusion of the exposed pad in bottom side is 0.20 MM Typical

ISSUE	1				
ACN	212933				
DATE	14Jun02				
APPRD.					

ZARLINK SEMICONDUCTOR

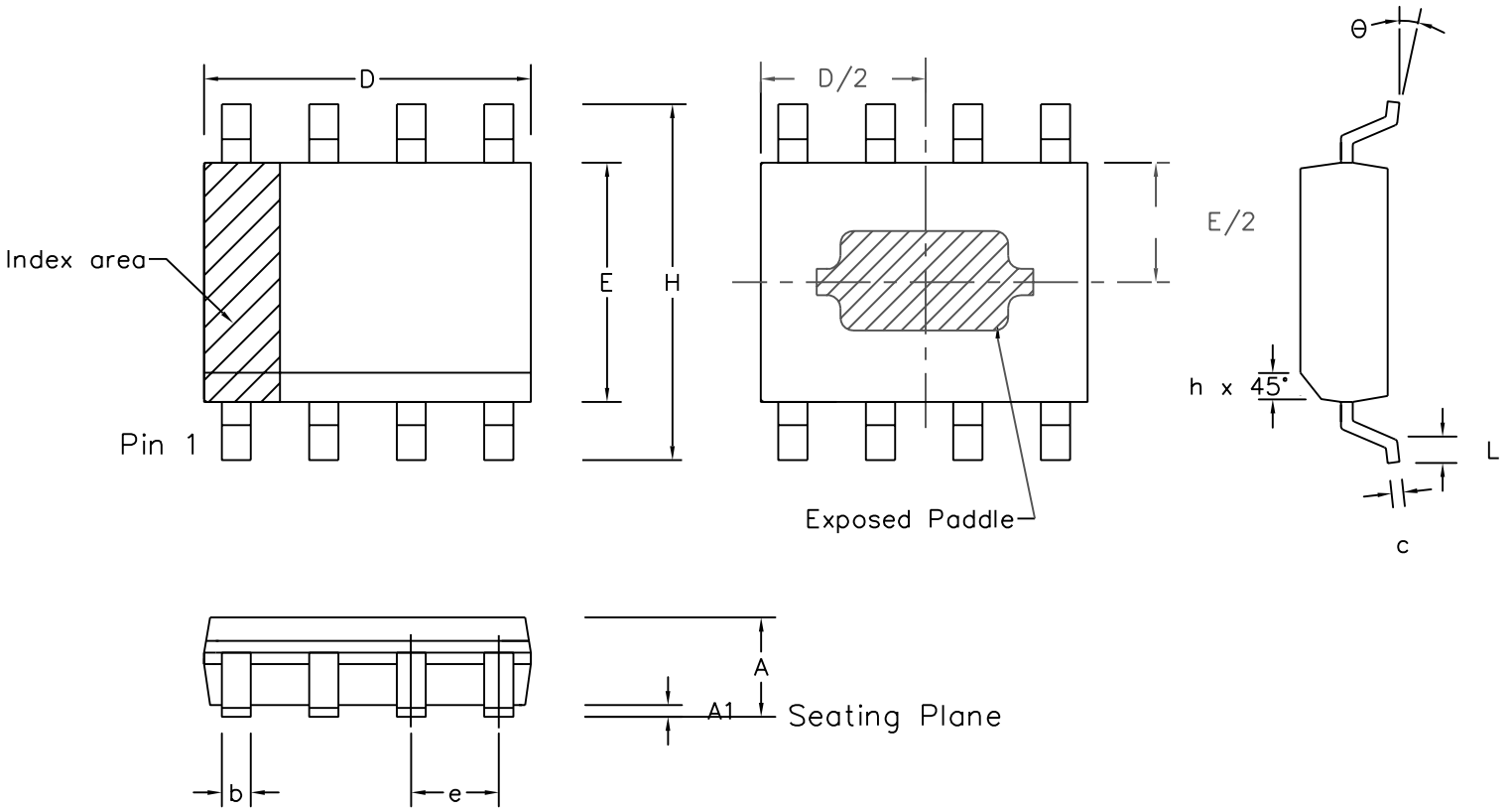
Previous package codes

MH / S

Package Code DC

Package Outline for 8 lead e-pad SOIC (0.150" Body width)

GPD00790



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e	0.050 BSC		1.27 BSC	
b	0.0138	0.0192	0.35	0.49
c	0.0075	0.0098	0.19	0.25
θ	0°	8°	0°	8°
h	0.010	0.016	0.25	0.41
	Pin Features		Pin Features	
N	8		8	

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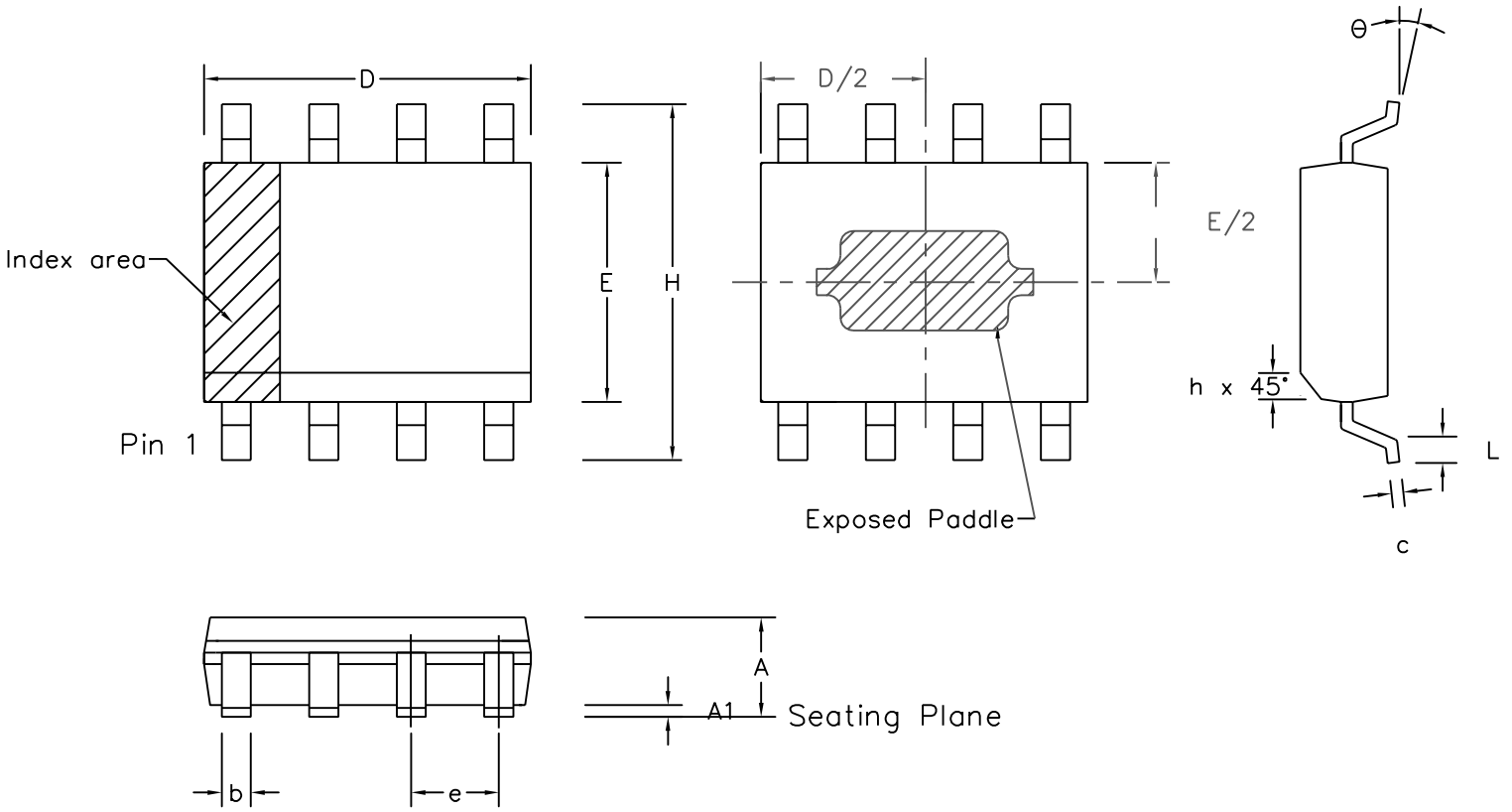

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E	0.150	0.157	3.81	3.99
L	0.16	0.35	0.41	0.89
e	0.050 BSC		1.27 BSC	
b	0.0138	0.0192	0.35	0.49
c	0.0075	0.0098	0.19	0.25
θ	0°	8°	0°	8°
h	0.010	0.016	0.25	0.41
	Pin Features		Pin Features	
N	8		8	

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Package Outline for 8 lead e-pad SOIC (0.150" Body width)

GPD00790

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