19-3398; Rev 0; 7/04

MAX1127 Evaluation Kit

Evaluates: MAX1126/MAX1127

General Description

The MAX1127 evaluation kit (EV kit) is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1126/MAX1127 quad 12-bit analog-to-digital converter (ADC). The MAX1126/MAX1127 accept differential analog input signals. The EV kit generates these signals from user-provided single-ended input sources. The digital outputs produced by the ADC can be easily sampled with a user-provided, high-speed logic analyzer or data-acquisition system. The EV kit also features an on-board deserializer to ease integration with standard logic analysis systems. The EV kit operates from 1.8V and 3.3V power supplies (1.5V for the optional FPGA) and includes circuitry that generates a clock signal from an AC signal provided by the user. The EV kit comes with the MAX1127 installed. Order free samples of the pin-compatible MAX1126 to evaluate this part.

Features

- ♦ **Sample Rate Up to 65Msps (MAX1127)**
- ♦ **Low-Voltage and Power Operation**
- ♦ **Optional On-Board Clock-Shaping Circuitry**
- ♦ **Serial SLVS/LVDS Outputs**
- ♦ **On-Board LVPECL Differential Output Drivers**
- ♦ **On-Board Deserializer**
- ♦ **LVDS Test Mode**
- ♦ **Assembled and Tested**
- ♦ **Also Evaluates the MAX1126**

Part Selection Table

PART	SPEED (Msps)
MAX1126EGK	40
MAX1127EGK	65

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX1127EVKIT	0°C to +70°C	68 QFN

Note: *To evaluate the MAX1126, request a free MAX1126EGK sample with the MAX1127EVKIT.*

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
Central Semiconductor	631-435-1110	631-435-1824	www.centralsemi.com
Diodes Inc	805-446-4800	805-446-4850	www.diodes.com
Panasonic	714-373-7366	714-737-7323	www.panasonic.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Vishay/Vitramon	203-268-6261	203-452-5670	www.vishay.com
Zetex USA	631-543-7100	631-864-7630	www.zetex.com

Note: *Indicate that you are using the MAX1127 when contacting these component suppliers.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C12, C59–C64, C81–C85	23	0.1µF ±20%, X5R 10V ceramic capacitors (0402) TDK C1005X5R1A104M
C13–C20	0	Not installed (0603)
C21–C28	8	39pF ±5%, 50V C0G ceramic capacitors (0402) TDK C1005C0G1H390J
C29–C44, C77–C80, C92, C93	20	1.0µF ±20%, X5R 6.3V ceramic capacitors (0402) TDK C1005X5R0J105M
C45, C46, C47, C55, C86–C89	8	220µF ±20%, 6.3V tantalum capacitors (C case) AVX TPSC227M006R0250
C48, C49, C50, C56	0	Not installed (C case)
C51, C52, C53, C57, C90, C91	6	10µF ±20%, X5R 10V ceramic capacitors (1210) TDK C3225X5R1A106M
C54	1	2.2µF ±20%, X5R 6.3V ceramic capacitor (0603) TDK C1608X5R0J225M
C58, C65-C76	13	0.01µF ±5%, 25V C0G ceramic capacitors (0603) TDK C1608C0G1E103J
C94–C121	28	0.1µF ±20%, X5R 6.3V ceramic capacitors (0201) TDK C0603X5R0J104M
D1	1	Dual Schottky diode (SOT23) Zetex BAS70-04 Central Semiconductor CMPD6263S Vishay BAS70-04 Diodes Inc BAS70-04
D2, D3	2	Green surface-mount LEDs (SS) Panasonic LNJ308G8LRA
J1–J5	5	SMA PC-mount connectors
J6, J7, J12–J15	6	Dual row, 40-pin headers
J8–J11	4	2-pin headers
J16	0	Not installed

DESIGNATION	QTY	DESCRIPTION
JU1–JU9, JU11, JU12, JU15– JU18	15	Jumper, 3-pin headers
JU10	0	Not installed (SIP-3)
JU13	1	Jumper, dual row, 8-pin header
N1	1	Digital logic n-channel MOSFET (SOT23), top mark = 702 Central Semiconductor 2N7002
R1–R16, R22–R25, R82–R93	0	Not installed (0603)
R17–R21, R58–R75	23	49.9Ω ±1% resistors (0603)
R26–R36, R76–R81	0	Not installed (0402)
R37–R44	8	10Ω ±1% resistors (0402)
R45–R50	6	100Ω ±1% resistors (0603)
R51	1	100kΩ potentiometer, 19 turn, 3/8in
R52, R53, R56	3	4.02kΩ ±1% resistors (0603)
R54	1	5kΩ potentiometer, 19 turn, 3/8in
R55	1	2kΩ ±1% resistor (0603)
R57	1	13.0kΩ ±1% resistor (0603)
R94, R95	2	4.7kΩ ±5% resistors (0603)
R96, R97	2	330Ω ±5% resistors (1206)
R98	1	10kΩ ±5% resistor (0603)
SW1	1	Momentary pushbutton switch
T1–T4	4	1:1 800MHz RF transformers Mini-Circuits ADT1-1WT
TP1–TP9	9	Test points (black)
TP10–TP12	0	Not installed
U1	1	Maxim MAX1127EGK (68-pin QFN)
U2	1	Maxim MAX9111ESA (8-pin SO)
U3–U8	6	Maxim MAX9375EUA (8-pin µMAX)
U9	1	Xilinx XC2V80-5FG256C (FGBGA-256) or Xilinx XC2V80-5FG256I (FGBGA-256)
U10	1	Xilinx XC18V01SO20C (20-pin SO)
None	16	Shunts
None	1	MAX1127 PC board

Quick Start

Recommended Equipment

- DC power supplies:

Clock (CVDD)	1.8V, 100mA
Analog (AVDD)	1.8V, 500mA
Digital (OVDD)	1.8V, 150mA
Buffers (VPECL)	3.3V, 350mA

Optional

Deserializer core (VD1.5)	1.5V, 200mA
Deserializer I/O (VD3.3)	3.3V, 200mA

- Signal generator with low-phase noise and low jitter for clock input signal (e.g., HP 8662A, HP 8644B)
- Four signal generators for analog signal inputs (e.g., HP 8662A, HP 8644B)
- Logic analyzer or data-acquisition system (e.g., HP 16500C, TLA621)
- Analog bandpass filters (e.g., Allen Avionics, K&L Microwave) for input signal and clock signal
- Digital voltmeter

Procedure

The MAX1127 EV kit is a fully assembled and tested surface-mount board. Follow the steps below to verify board operation. **Do not turn on power supplies or enable signal generators until all connections are completed:**

1) Verify that shunts are installed in the following locations:

   JU1–JU5 (1-2) → All channels enabled

   JU6 (2-3) → Single termination

   JU7 (2-3) → LVDS outputs

   JU8 (2-3) → Two's-complement output

   JU9 (2-3) → Normal operation

   JU10, JU11, JU12 (2-3) → 48.75MHz to 65MHz clock frequency range

   JU13 (3-4) → Internal reference enabled

   JU15–JU18 (2-3) → Deserializer outputs enabled

2) Connect the clock signal generator to the input of the clock bandpass filter.
3) Connect the output of the clock bandpass filter to the SMA connector labeled J5.
4) Connect the analog input signal generators to the inputs of the desired analog bandpass filters.
5) Connect the output of the analog bandpass filters to the SMA connectors labeled J1 to J4. The analog input signals may also be monitored at J8–J11.

   Note: All four channels may be operated independently or simultaneously.
6) Connect the logic analyzer to either header J6 (SLVS- or LVDS-compatible signals), or J12–J15 (deserialized 3.3V CMOS-compatible signals). See the *Output Bit Locations* section for header connections.
7) Connect a 1.8V, 500mA power supply to AVDD. Connect the ground terminal of this supply to GND.
8) Connect a 1.8V, 150mA power supply to OVDD. Connect the ground terminal of this supply to GND.
9) Connect a 1.8V, 100mA power supply to CVDD. Connect the ground terminal of this supply to GND. **Note:** When using the MAX9111, CVDD must be 3.3V
10) Connect a 3.3V, 350mA power supply to VPECL. Connect the ground terminal of this supply to GND.
11) Connect a 1.5V, 200mA power supply to VD1.5. Connect the ground terminal of this supply to GND.
12) Connect a 3.3V, 200mA power supply to VD3.3. Connect the ground terminal of this supply to GND.
13) Turn on all the power supplies.
14) Enable the signal generators. Set the clock signal generator to output a 48.75MHz to 65MHz signal, with an amplitude of $2.6V_{P-P}$ or higher. Set the analog input signal generators to output the desired frequency with an amplitude ≤ $1V_{P-P}$. All signal generators should be phase locked.
15) Enable the logic analyzer.
16) Collect data using the logic analyzer.

Detailed Description

The MAX1127 EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1126 (40Msps) or MAX1127 (65Msps), 12-bit serial SLVS/LVDS output ADCs. The EV kit comes with the MAX1127, which can be evaluated with a maximum clock frequency (f_{CLK}) of 65MHz.

The MAX1127 accepts differential input signals; however, on-board transformers (T1–T4) convert a readily available single-ended source output to the required differential signal. The input signals of the MAX1127 can be measured using a differential oscilloscope probe at headers J8–J11.

Output level translators (U3–U8) buffer and convert the SLVS/LVDS output signals of the MAX1127 to higher voltage LVPECL signals that can be captured by a wide variety of logic analyzers. The SLVS/LVDS outputs are accessible at header J6. The LVPECL outputs are accessible at header J7.

The EV kit is designed as a four-layer PC board to optimize the performance of the MAX1127. Separate analog, digital, clock, and buffer power planes minimize noise coupling between analog and digital signals; 50Ω coplanar transmission lines are used for analog and clock inputs and 100Ω differential coplanar transmission lines are used for all digital LVDS outputs. All differential outputs are properly terminated with 100Ω termination resistors between true and complementary digital outputs. The trace lengths of the 100Ω differential SLVS/LVDS lines are matched to within a few thousandths of an inch to minimize layout-dependent data skew.

Power Supplies

For best performance, the MAX1127 EV kit requires separate analog, digital, clock, and buffer power supplies. Two 1.8V power supplies are used to power the analog and digital portion of the MAX1127. The clock circuitry is powered by a 1.8V power supply (if using the MAX9111, see the *Optional Clock-Shaping Circuit* section). A separate 3.3V power supply is used to power the output buffers (U3–U8) of the EV kit.

MAX1127 Power-Down

The MAX1127 features several power-management features. In addition to a global device power-down pin, the MAX1127 offers an independent power-down pin for each channel of the ADC. Jumpers JU1–JU5 control the power-management features of the data converter. See Table 1 for shunt positions.

Clock

By default, the MAX1127 EV kit directly connects a user-provided AC-coupled clock signal to the MAX1127 clock input. In this mode, diode D1 limits the amplitude of the clock signal. Overdriving the clock input (J5) can increase the slew rate of the differential signal, thereby reducing clock jitter. The MAX1127 EV kit also features an optional on-board clock-shaping circuit that generates a clock signal with variable duty cycle from an AC-coupled sine-wave signal applied to the clock SMA connector (J5). To use this circuitry, cut the trace on the printed circuit (PC) board at R78 and install 0Ω resistors at R77 and R35. The frequency of the signal should not exceed 65MHz for the MAX1127. The sinusoidal input signal frequency (f_{CLK}) determines the sampling rate of the ADC.

Optional Clock-Shaping Circuit

A differential line receiver (U2) processes the clock-input signal and generates the required CMOS clock signal. When using this circuitry, the voltage at the CVDD pad must be **at least** 3.3V The signal's duty cycle can be adjusted with potentiometer R54. With a 3.3V clock supply voltage (CVDD), a clock signal with a 50% duty cycle (recommended) can be achieved by adjusting R54 until a voltage of 1.32V is produced across test points TP6 and TP7. The clock signal can be observed at TP8.

PLL Frequency-Mode Selection

When driving the MAX1127 EV kit with anything other than the default 65MHz clock signal, the phased-

Table 1. Power-Down Shunt Settings (JU1–JU5)

JUMPER	SHUNT POSITION	POWER-DOWN CONNECTIONS	CHANNEL	DESCRIPTION
JU1 (PD0)	1-2	AVDD	0	Channel 0 disabled
	2-3*	GND		Channel 0 enabled
JU2 (PD1)	1-2	AVDD	1	Channel 1 disabled
	2-3*	GND		Channel 1 enabled
JU3 (PD2)	1-2	AVDD	2	Channel 2 disabled
	2-3*	GND		Channel 2 enabled
JU4 (PD3)	1-2	AVDD	3	Channel 3 disabled
	2-3*	GND		Channel 3 enabled
JU5 (PDALL)	1-2	AVDD	ALL CHANNELS	All channels disabled
	2-3*	GND		All channels enabled

**Default configuration: JU1–JU5 (2-3).*

locked-loop (PLL) circuit of the MAX1127 must be set accordingly. Refer to the MAX1127 data sheet for further details about the operation of the internal PLL. Jumpers JU10, JU11, and JU12 control the PLL mode of the MAX1127. See Table 2 for shunt positions.

Ensure that the desired clock frequency falls between the min/max limits in Table 2.

Table 2. PLL Shunt Settings (JU10-JU12)

	JUMPER		INPUT CLOCK RANGE (MHz)	
	JU11	JU12	MIN	MAX
SHUNT POSITION	2-3*	2-3*	48.750	65.000
	2-3	1-2	32.500	48.750
	1-2	2-3	24.375	32.500
	1-2	1-2	16.000	24.375

**Default configuration: JU10, JU11, JU12 (2-3).*

Input Signal

Although the MAX1127 accepts differential analog input signals, the EV kit only requires a single-ended analog input signal, with an amplitude of less than 1.4VP-P provided by the user. On-board transformers (T1–T4) convert the single-ended analog input signal and generate differential analog signals at the ADC's differential input pins.

Reference Voltage

The MAX1127 EV kit can be configured to use the MAX1127's internal reference, or a stable, low-noise, external reference. Use jumper JU13 to configure the desired reference mode. See Table 3 for shunt settings.

Table 3. Reference Shunt Settings (JU13)

SHUNT POSITION	DESCRIPTION
1-2	Internal reference disabled. Apply an external reference voltage at the REFIO pad.
3-4*	Internal reference enabled.
5-6	**RESERVED. DO NOT USE.**
7-8	

**Default configuration: JU13 (3-4).*

Output Signal

The MAX1127 features four, serial, LVDS-compatible, digital outputs. Each output transmits the converted analog input signals of channels 0 through 3. Two additional outputs (CLKOUT and FRAME) are provided for data synchronization. Refer to the MAX1127 data sheet for more details.

Output Format

The digital output coding can be chosen to be either two's complement or straight offset binary by configuring jumper JU3. See Table 4 for jumper configuration.

Table 4. Output Format Shunt Settings (JU8)

SHUNT POSITION	$\overline{T}$/B PIN	DESCRIPTION
1-2*	AV_{DD}	**Straight offset binary selected.** Digital output in straight offset binary format.
2-3	GND	**Two's complement selected.** Digital output in two's complement format.

**Default configuration: JU8 (1-2).*

Double-Termination Settings

The MAX1127 features trimmed, internal 100Ω termination resistors between the positive (true) and negative (complementary) line of each output (D0–D3, CLK, and FRAME). Use jumper JU6 to switch the resistors into the circuit (double termination), or switch the resistors out of the circuit (single termination). See Table 5 for shunt positions.

Table 5. Double Termination Shunt Settings (JU6)

SHUNT POSITION	DT PIN	DESCRIPTION
1-2	AV_{DD}	**Double termination selected.** Outputs are double terminated.
2-3*	GND	**Single termination selected.** Outputs are single terminated.

**Default configuration: JU6 (2-3).*

SLVS Outputs

The MAX1127 is capable of generating low-voltage differential signaling (LVDS) or scalable low-voltage signaling (SLVS) signals at its outputs. Jumper JU7 controls this feature of the MAX1127. See Table 6 for shunt positions. Regardless of which output signal type is selected, the output buffers (U3–U8) will convert the data to LVPECL logic levels.

Table 6. SLVS Shunt Settings (JU7)

SHUNT POSITION	SLVS/$\overline{\text{LVDS}}$ PIN	DESCRIPTION
1-2	AV_{DD}	SLVS outputs
2-3*	GND	LVDS outputs

**Default configuration: JU7 (2-3).*

LVDS Test Pattern

To debug signal integrity problems, the MAX1127 can generate a factory-default test pattern on all the SLVS/LVDS output channels. Jumper JU9 controls this feature. See Table 7 for shunt positions.

Table 7. LVDS Test Pattern Shunt Settings (JU9)

SHUNT POSITION	LVDSTEST PIN	DESCRIPTION
1-2	AV_{DD}	Test pattern (0000 1011 1101) transmitted, LSB first, on all SLVS/LVDS outputs
2-3*	GND	Normal operation

**Default configuration: JU9 (2-3).*

Output Bit Locations

The digital outputs of the MAX1127 are connected to a 40-pin header (J6). PC board trace length is matched to minimize data skew and improve the overall dynamic performance of the device. Additionally, six drivers (U3–U8) buffer and level translate the digital outputs to LVPECL-compatible signals. The drivers increase the differential voltage swing, and are able to drive large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to the 40-pin header (J7). See Table 8 for bit location of headers J6-J7.

On-Board Deserializer

The MAX1127 EV kit features an on-board deserializer that converts the serial outputs of the MAX1127 to a parallel data stream. The deserializer uses a delay-locked loop (DLL) to synchronize itself with the incoming serial data stream. **After every change of the ADC clock frequency, reset the DLL by pressing SW1**. If LED D3 is not lit, the serial data stream is not synchronized and the output of the deserializer is not valid.

Table 8. Output Bit Locations

SIGNAL		UNBUFFERED (LVDS OR SLVS)	BUFFERED (LVPECL)	DESCRIPTION
CH0	P	J6-5	J7-5	Channel 0
	N	J6-6	J7-6	
CH1	P	J6-11	J7-11	Channel 1
	N	J6-12	J7-12	
CLKOUT	P	J6-17	J7-17	Clock
	N	J6-18	J7-18	
FRAME	P	J6-23	J7-23	Frame
	N	J6-24	J7-24	
CH2	P	J6-29	J7-29	Channel 2
	N	J6-30	J7-30	
CH3	P	J6-35	J7-35	Channel 3
	N	J6-36	J7-36	

P: True
N: Complementary

Channel 0 through channel 3 data is captured on headers J12 through J15. See Table 9 for bit locations.

Table 9. Output Bit Locations (J12–J15)

BIT	POSITION			
	CH0	CH1	CH2	CH3
CLK	J12-38	J13-38	J14-38	J15-38
D11	J12-26	J13-26	J14-26	J15-26
D10	J12-24	J13-24	J14-24	J15-24
D9	J12-22	J13-22	J14-22	J15-22
D8	J12-20	J13-20	J14-20	J15-20
D7	J12-18	J13-18	J14-18	J15-18
D6	J12-16	J13-16	J14-16	J15-16
D5	J12-14	J13-14	J14-14	J15-14
D4	J12-12	J13-12	J14-12	J15-12
D3	J12-10	J13-10	J14-10	J15-10
D2	J12-8	J13-8	J14-8	J15-8
D1	J12-6	J13-6	J14-6	J15-6
D0	J12-4	J13-4	J14-4	J15-4

Note: *Odd-numbered pins are connected to ground. Remaining pins are No Connects.*

Deserializer Output Enables

Jumpers JU15–JU18 control the respective CH0–CH3 output enables of the deserializer. See Table 10 for shunt positions.

Evaluating the MAX1126

The MAX1127 EV kit can also be used to verify the MAX1126 performance. To evaluate the MAX1126, replace the MAX1127 with a free MAX1126EGK sample.

Table 10. Deserializer Output Enables (JU15–JU18)

SHUNT POSITION	DESCRIPTION
1-2	Deserializer output disabled
2-3*	Deserializer output enabled

**Default configuration: JU15–JU18 (2-3).*

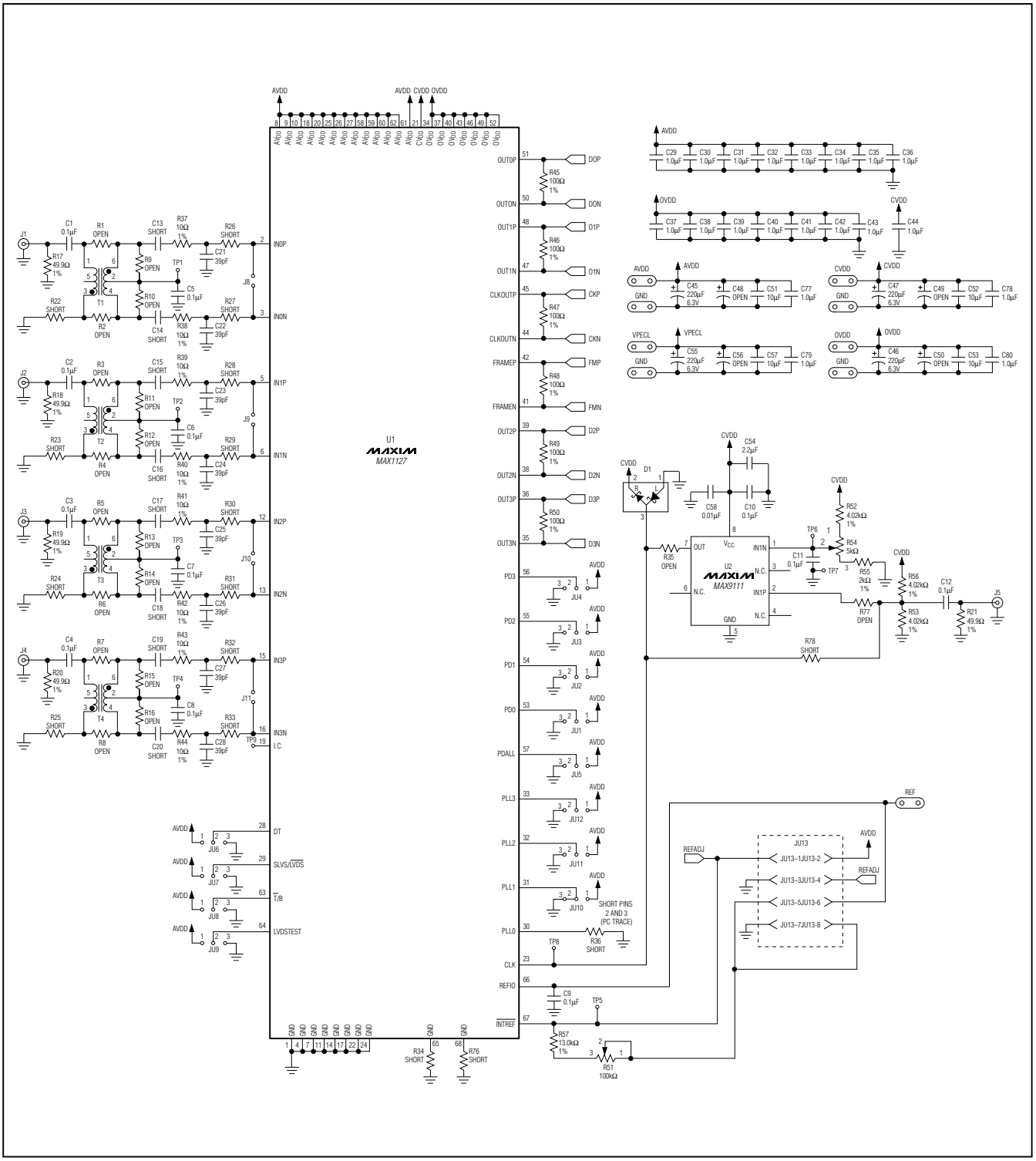

Figure 1. MAX1127 EV Kit Schematic (Sheet 1 of 4)

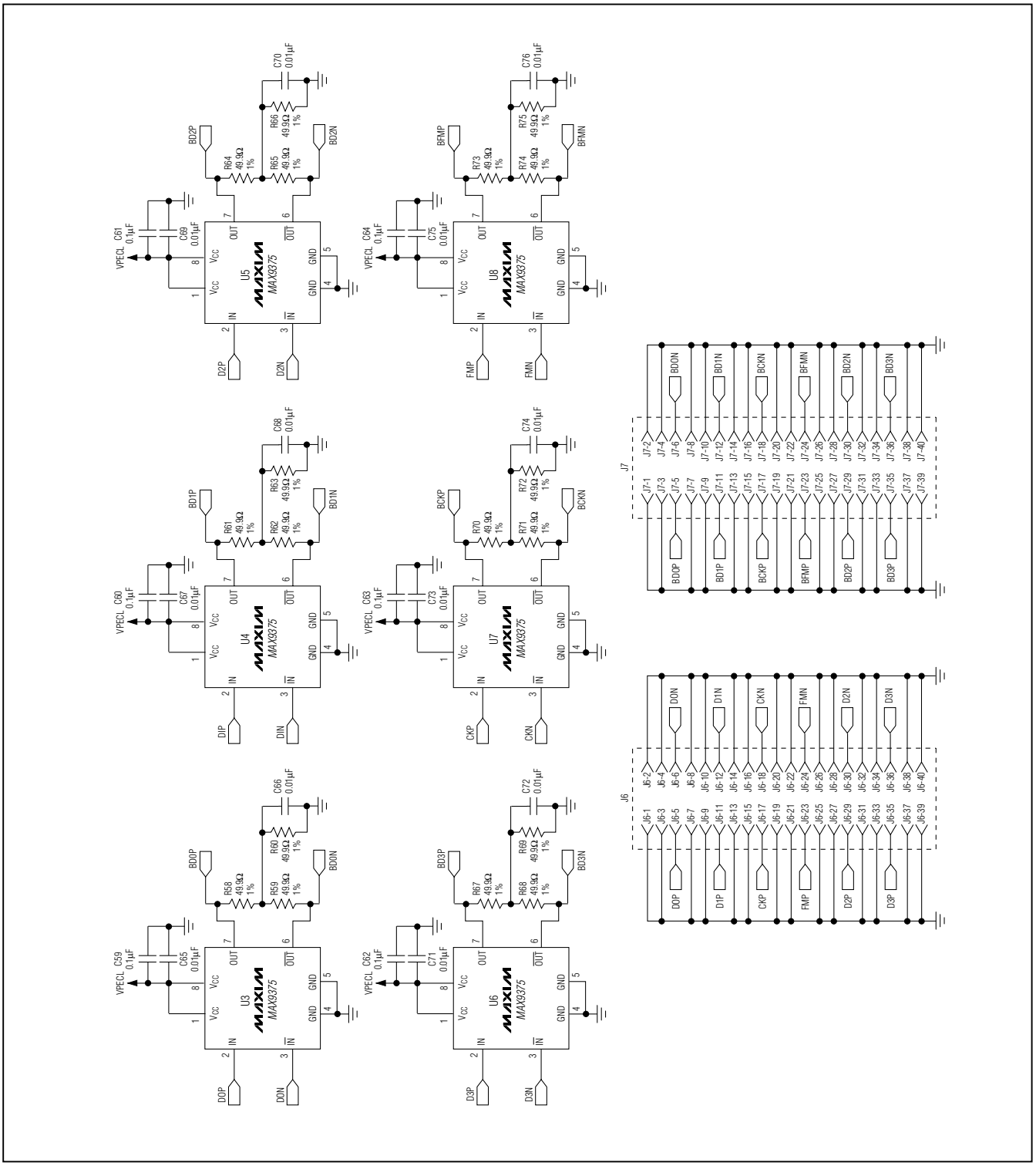

Figure 1. MAX1127 EV Kit Schematic (Sheet 2 of 4)

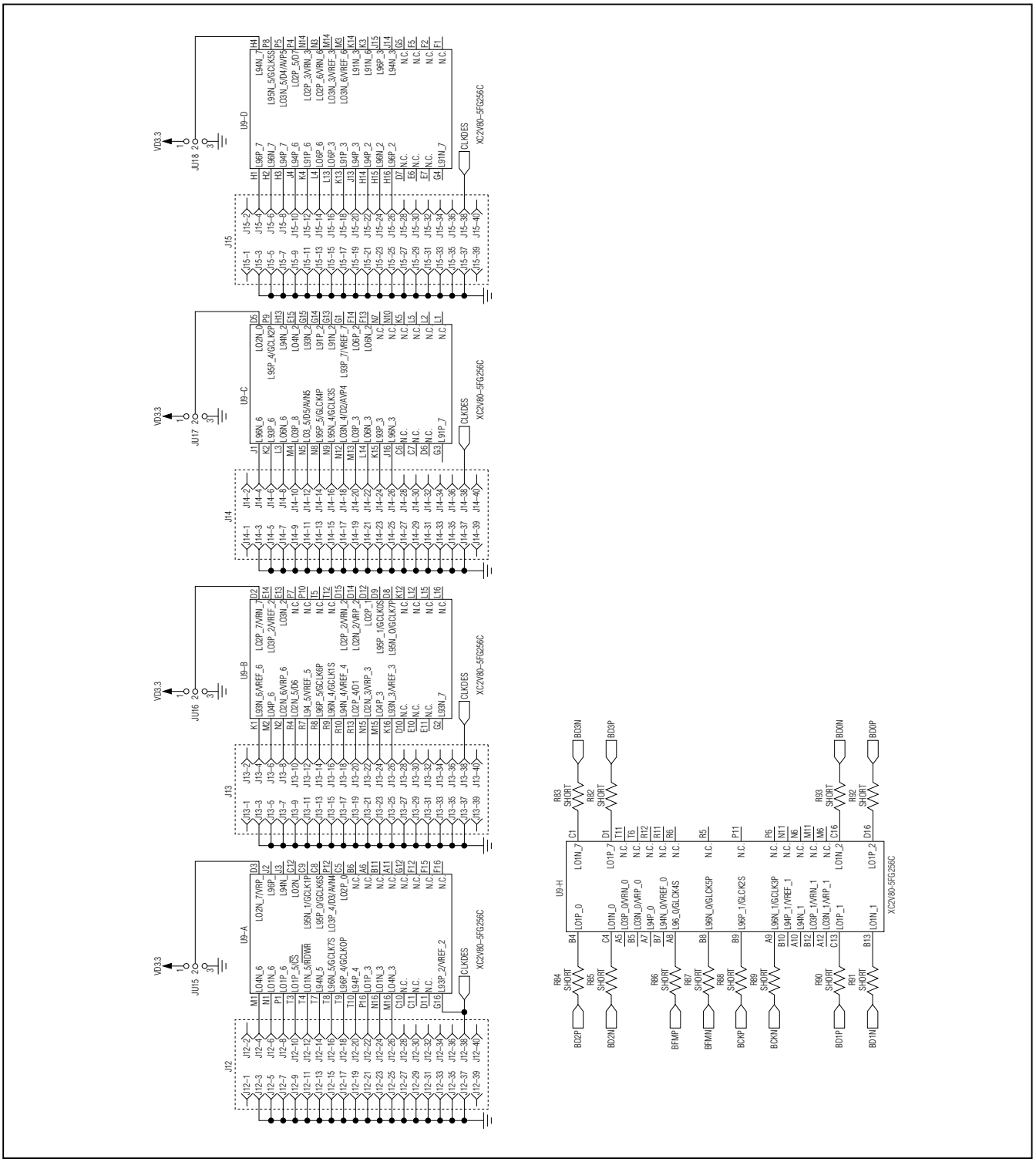

Figure 1. MAX1127 EV Kit Schematic (Sheet 3 of 4)

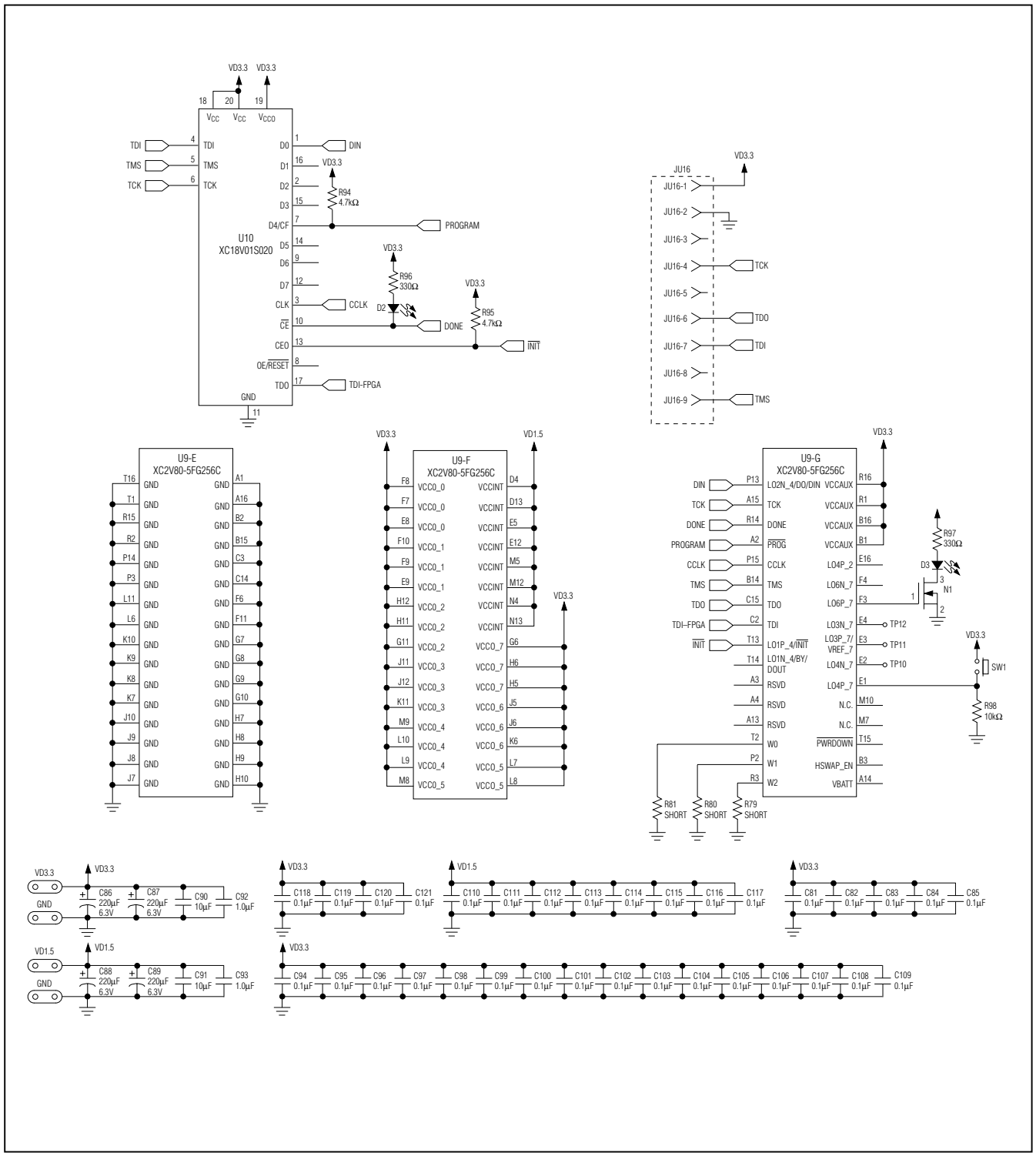

Figure 1. MAX1127 EV Kit Schematic (Sheet 4 of 4)

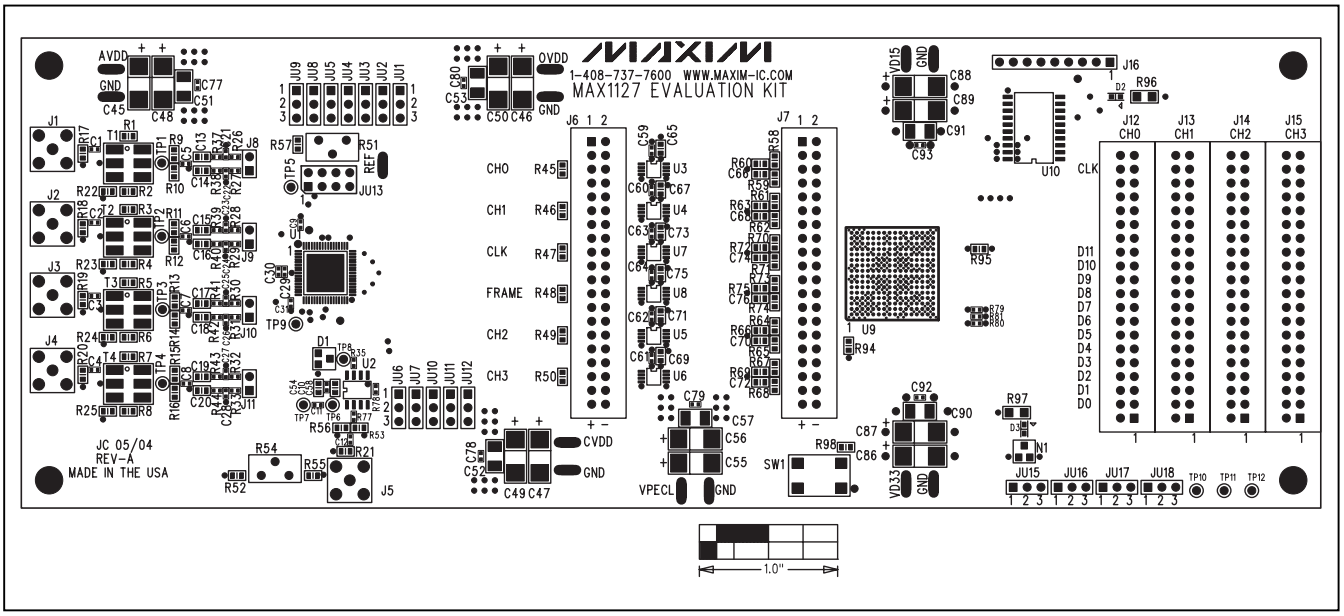

Figure 2. MAX1127 EV Kit Component Placement Guide—Component Side

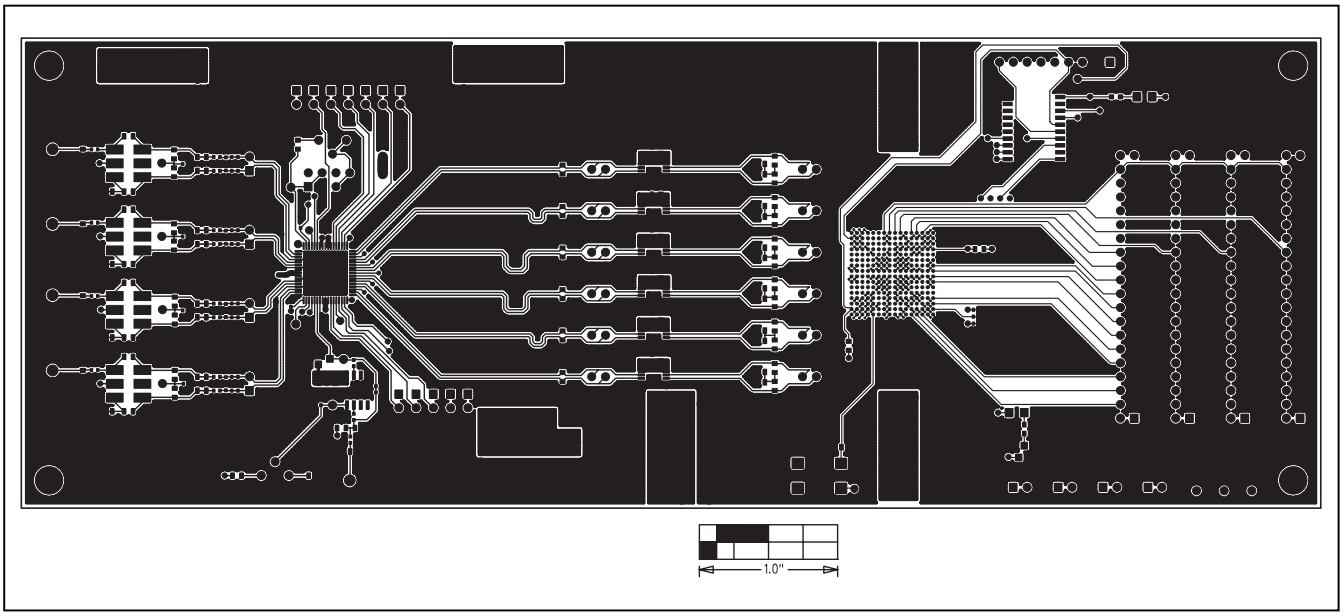

Figure 3. MAX1127 EV Kit PC Board Layout—Component Side

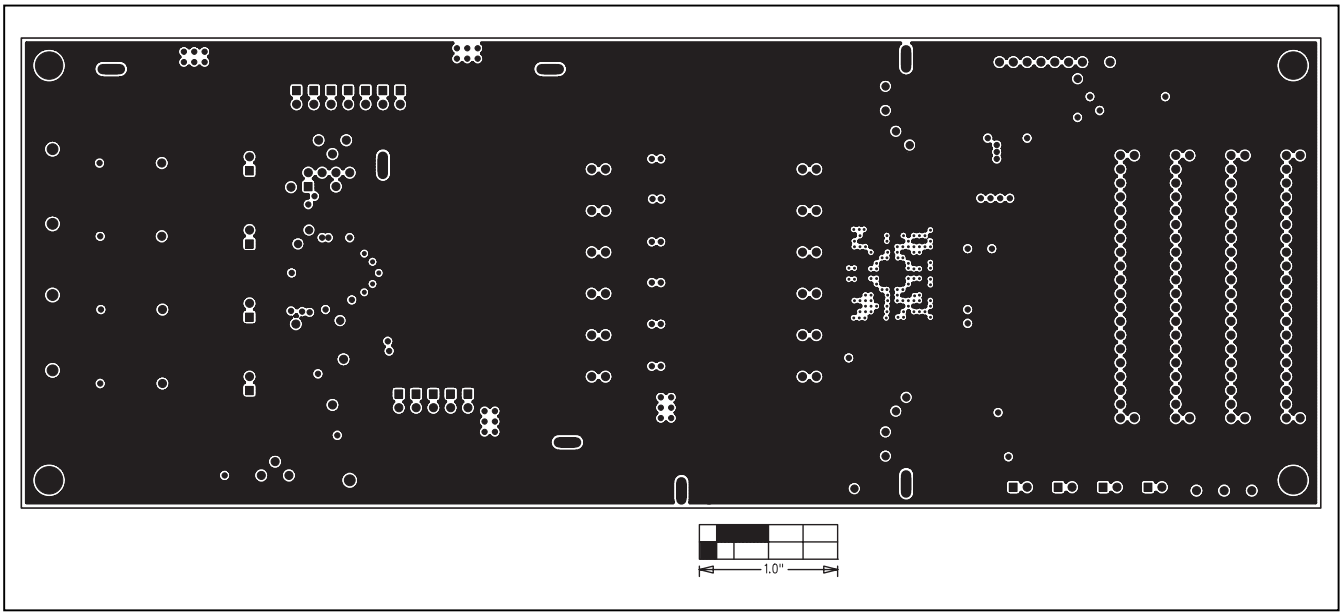

Figure 4. MAX1127 EV Kit PC Board Layout (Inner Layer 2)—Ground Planes

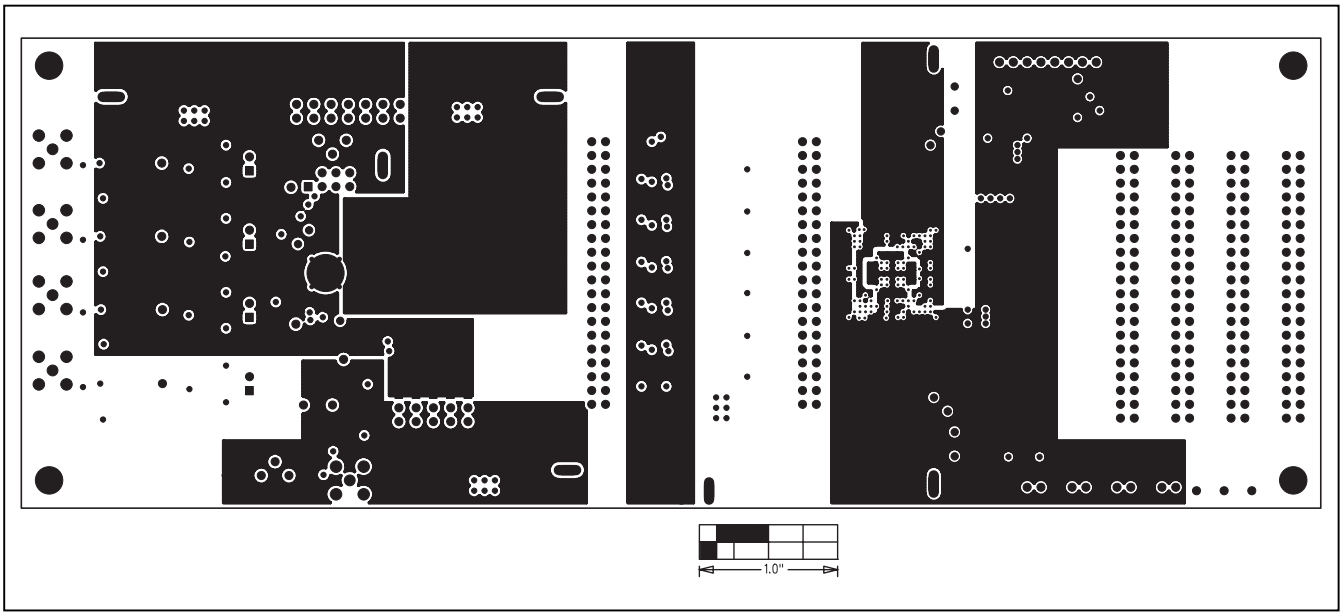

Figure 5. MAX1127 EV Kit PC Board Layout (Inner Layer 3)—Power Planes

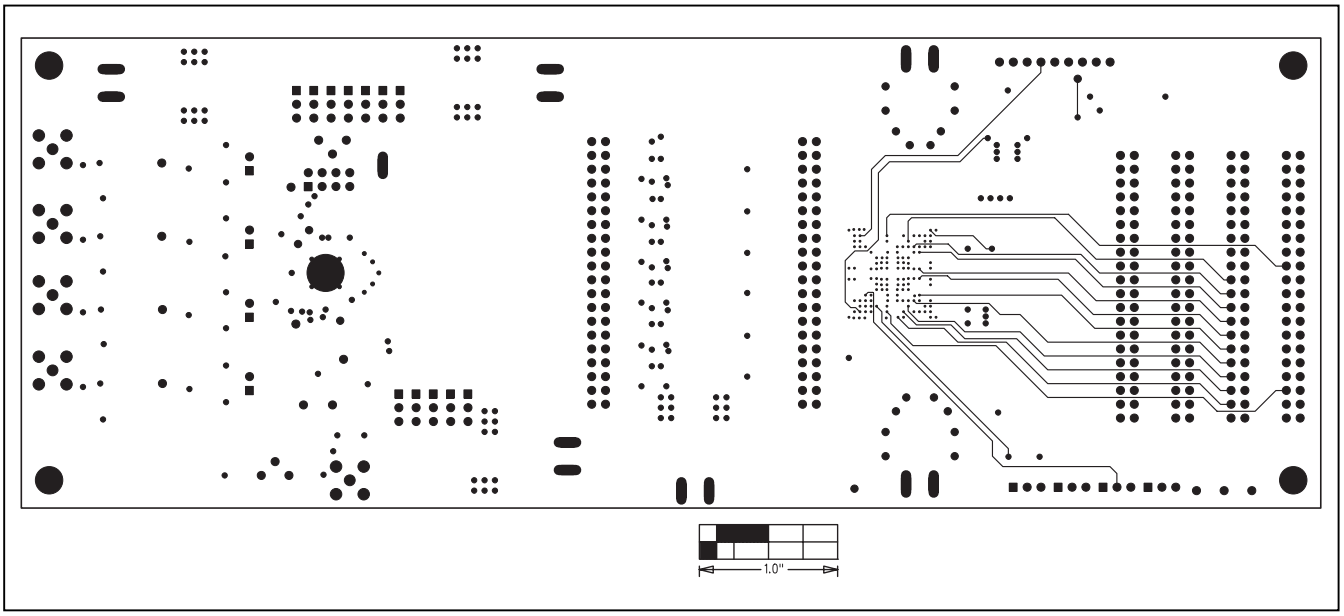

Figure 6. MAX1127 EV Kit PC Board Layout (Inner Layer 4)—Signal Layer

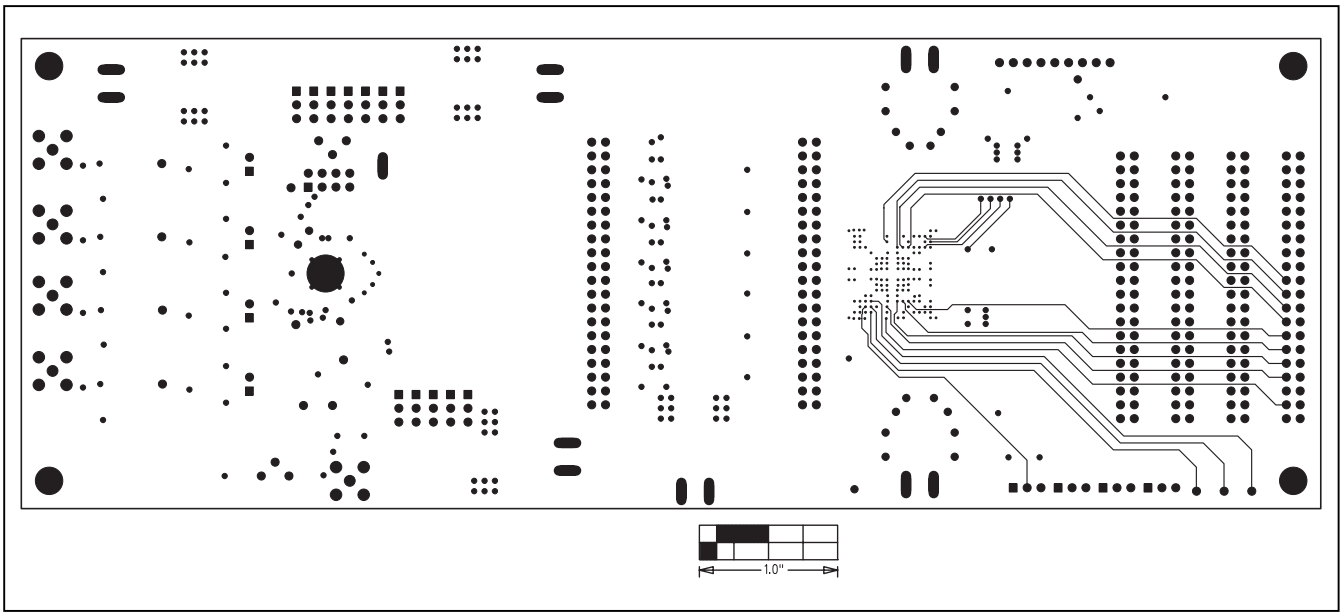

Figure 7. MAX1127 EV Kit PC Board Layout (Inner Layer 5)—Signal Layer

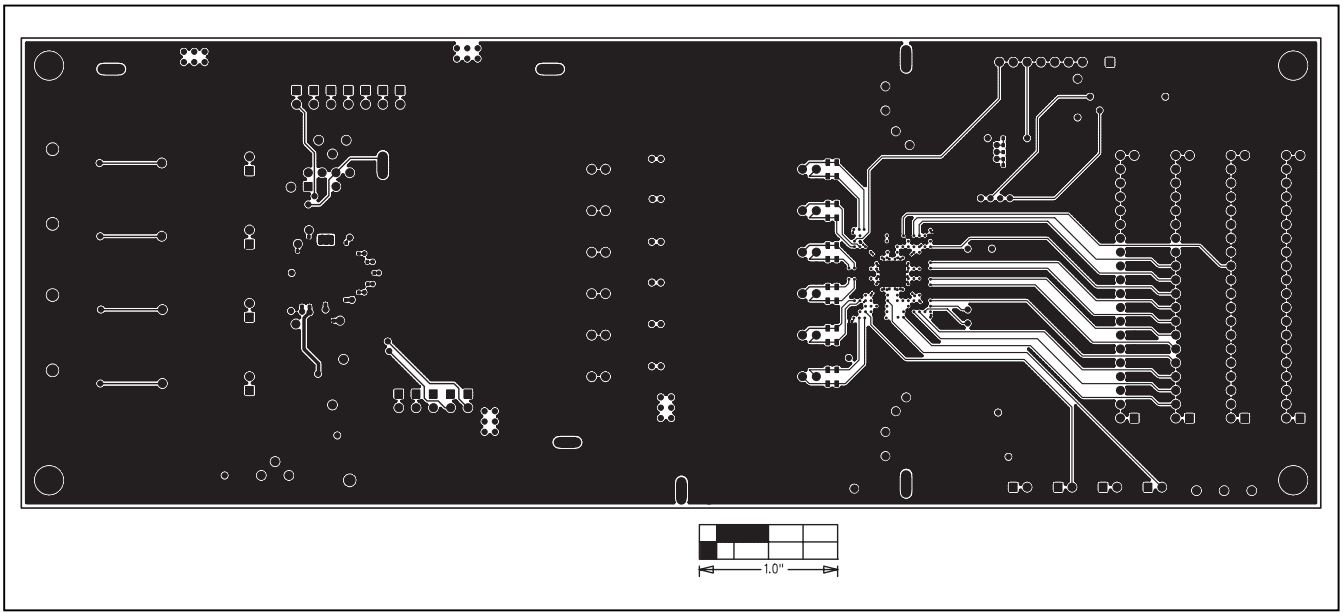

Figure 8. MAX1127 EV Kit PC Board Layout—Solder Side

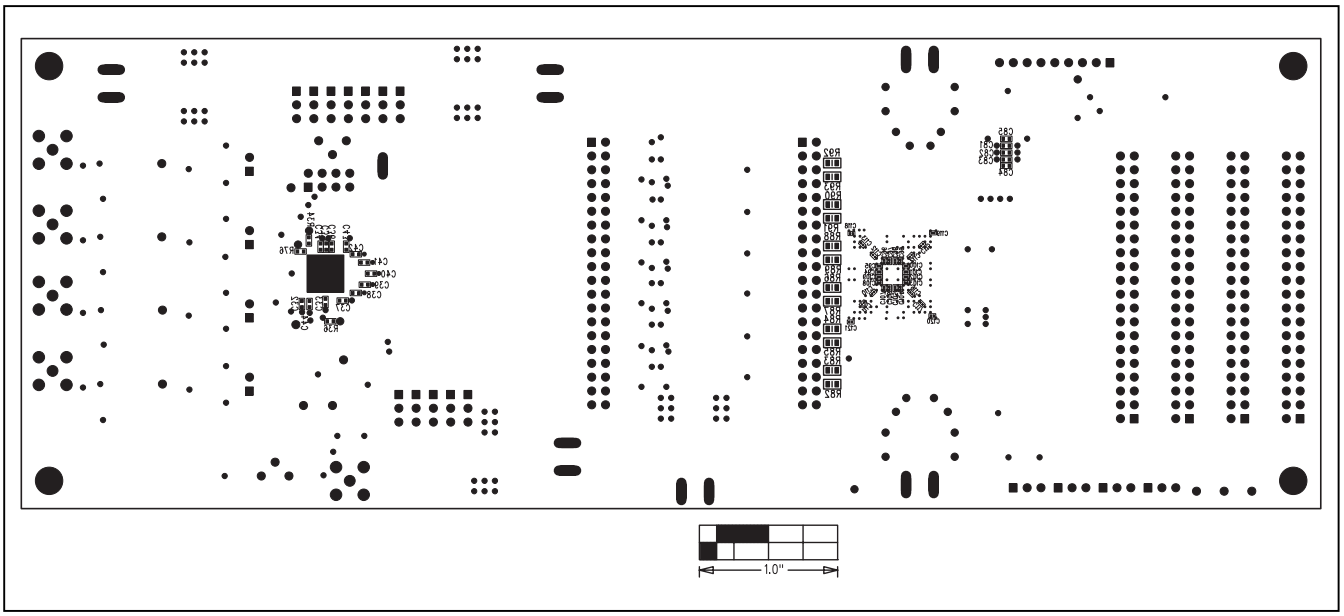

Figure 9. MAX1127 EV Kit Component Placement Guide—Solder Side