Document Title

1 M x 8 bit Low Voltage and Ultra Low Power CMOS Static RAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	January 3,2002	Preliminary

1M x 8 LOW POWER and LOW Vcc CMOS STATIC RAM

Preliminary

FEATURES

- Access times of 55, 70, 100 ns
- CMOS Low power operation:
  I_{CC}=15mA (typical)* operation
  I_{SB2}=2µA (typical)* standby
- Low data retention voltage: 1.5V (min.)
- Output Enable ($\overline{OE}$) and Two Chip Enables (CE1, CE2) inputs for ease in applications
- TTL compatible inputs and outputs
- Fully static operation:
  — No clock or refresh reguired
- Single 2.7V-3.6V power supply
- Wafer level burn in test mode
- Available in the know good die form and 48-pin 8*10mm TF-BGA

* Typical values are measured at V_{CC}=3.0V, T_A=25°C

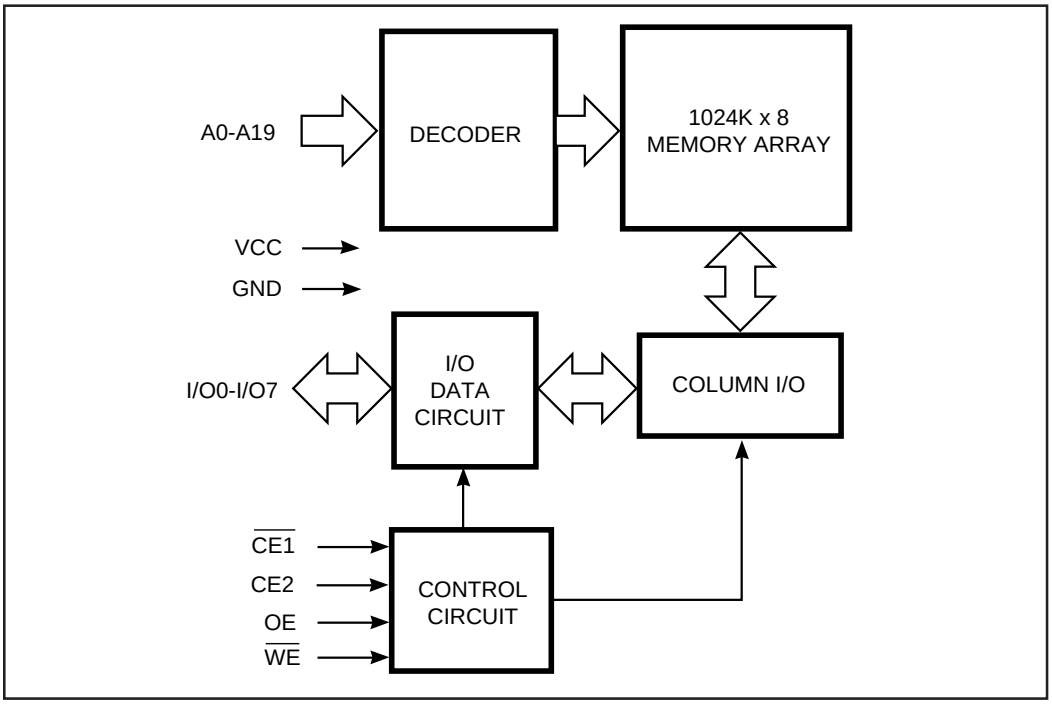
DESCRIPTION

The *ICSI* IC62LV1008L and IC62LV1008LL is a low voltage, 1,048,576 words by 8 bits, CMOS SRAM. It is fabricated using *ICSI*'s low voltage, six transistor (6T), CMOS technology. The device is targeted to satisfy the demands of the state-of-the-art technologies such as cell phones and pagers.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Additionally, easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

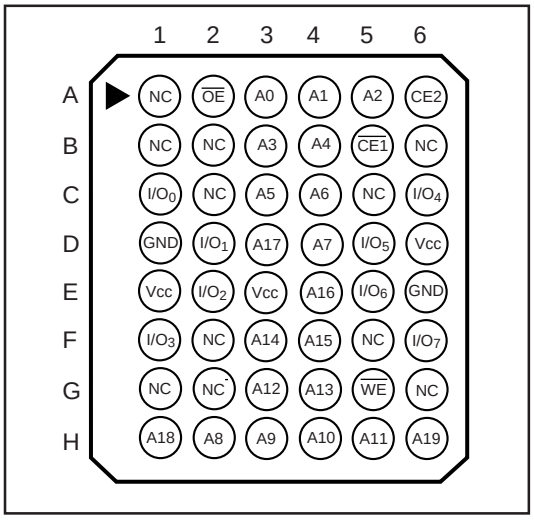
The IC62LV1008L and IC62LV1008LL are available in know good die form and 48-pin 8*10mm TF-BGA.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

48-Pin 8*10mm TF-BGA (TOP View)



PIN DESCRIPTIONS

A0-A19	Address Inputs
$\overline{CE}$1	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Data Input/Output
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$1	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-Down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V - 3.6V
Industrial	–40°C to +85°C	2.7V - 3.6V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
V_{CC}	Vcc related to GND	–0.3 to +4.0	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1][2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.0 V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage[1]		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]		–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	–1	1	µA

Notes:
1. $V_{IH(max.)}$ = V_{CC} +2.0V for pulse width less than 10 ns.
1. $V_{IL(min.)}$ = –2.0V for pulse width less than 10 ns.

IC62LV1008L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = 3.0V, $\overline{CE1}$ = V_{IL},CE2=V_{IH} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	30 35	— —	25 30	— —	20 25	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., f = 0 $\overline{CE1} \geq V_{IH}$ or CE2 ≤ V_{IL}, V_{IN} = V_{IH} or V_{IL},	Com. Ind.	— —	0.2 0.3	— —	0.2 0.3	— —	0.2 0.3	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 $\overline{CE1} \geq V_{CC}$ – 0.2V or CE2 ≤ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V	Com. Ind.	— —	35 50	— —	35 50	— —	35 50	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IC62LV1008LL POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = 3.0V, $\overline{CE1}$ = V_{IL},CE2=V_{IH} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	30 35	— —	25 30	— —	20 25	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., f = 0 $\overline{CE1} \geq V_{IH}$ or CE2 ≤ V_{IL}, V_{IN} = V_{IH} or V_{IL},	Com. Ind.	— —	0.2 0.3	— —	0.2 0.3	— —	0.2 0.3	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 $\overline{CE1} \geq V_{CC}$ – 0.2V or CE2 ≤ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V	Com. Ind.	— —	20 25	— —	20 25	— —	20 25	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	100	ns
t_{OHA}	Output Hold Time	10	—	10	—	15	—	ns
$t_{ACE}1$	$\overline{CE1}$ Access Time	—	55	—	70	—	100	ns
$t_{ACE}2$	CE2 Access Time	—	55	—	70	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	30	—	35	—	50	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	0	25	0	30	ns
$t_{LZCE}1$[2]	$\overline{CE1}$ to Low-Z Output	10	—	10	—	10	—	ns
$t_{LZCE}2$[2]	CE2 to Low-Z Output	10	—	10	—	10	—	ns
t_{HZCE}[2]	$\overline{CE1}$ or CE2 to Low-Z Output	0	20	0	25	0	30	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input Reference Level	1.3V
Output Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

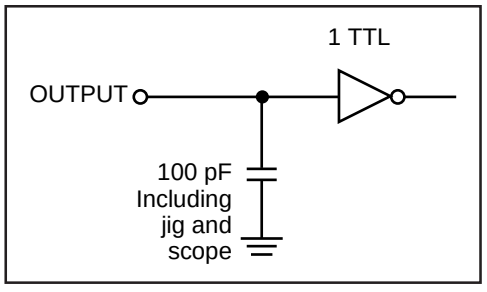


Figure 1

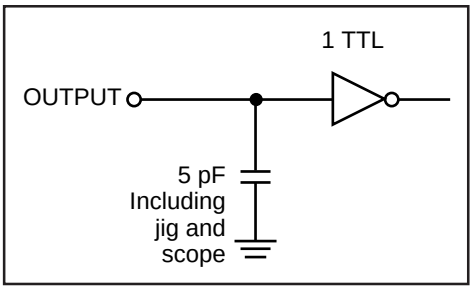
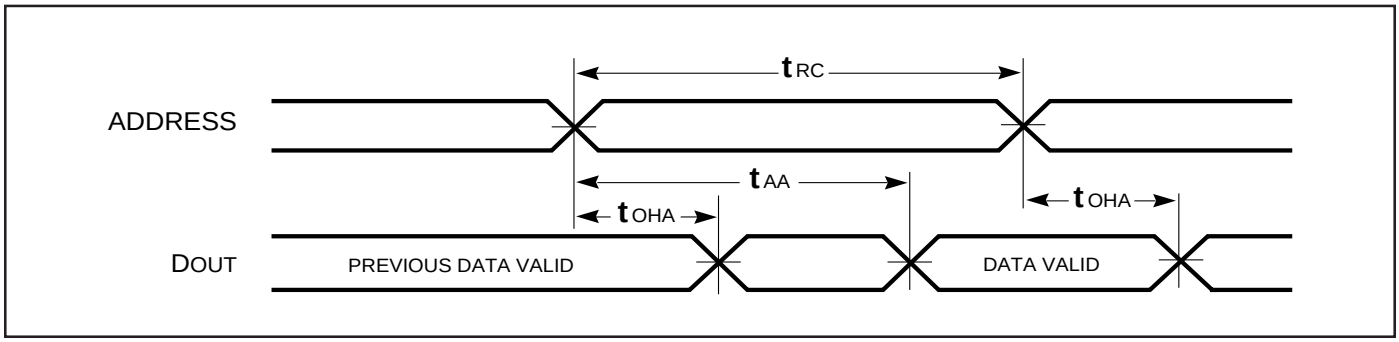


Figure 2

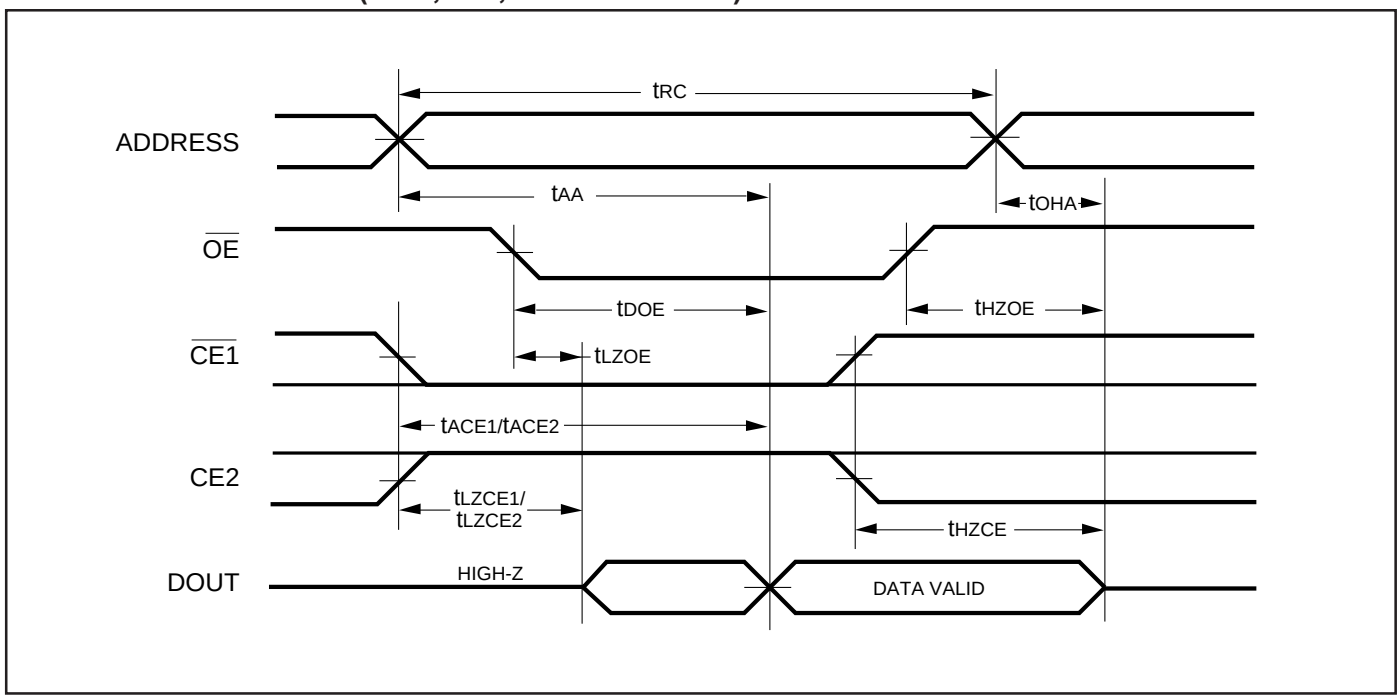
AC TEST LOADS

READ CYCLE NO.1[1,2] (Address controlled, $\overline{CE1}$ = $\overline{OE}$ = V_{IL} , CE2 = V_{IH})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CE1}$, $\overline{OE}$, CE2 controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

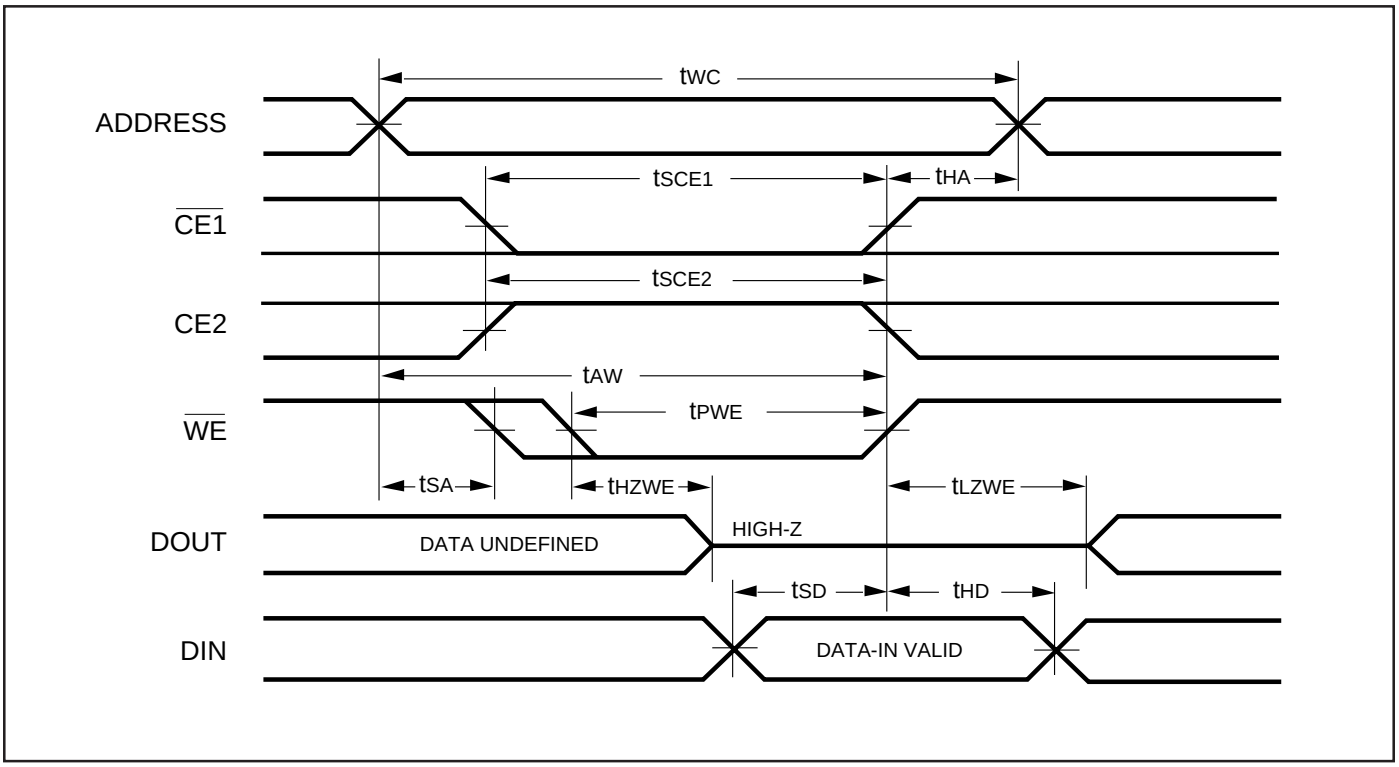
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range, Standard and Low Power)

Symbol	Parameter	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max	Unit
t_{WC}	Write Cycle Time	55	—	70	—	100	—	ns
$t_{SCE}1$	$\overline{CE}1$ to Write End	50	—	65	—	80	—	ns
$t_{SCE}2$	CE2 to Write End	50	—	65	—	80	—	ns
t_{AW}	Address Setup Time to Write End	50	—	65	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	45	—	55	—	80	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	30	—	30	—	40	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

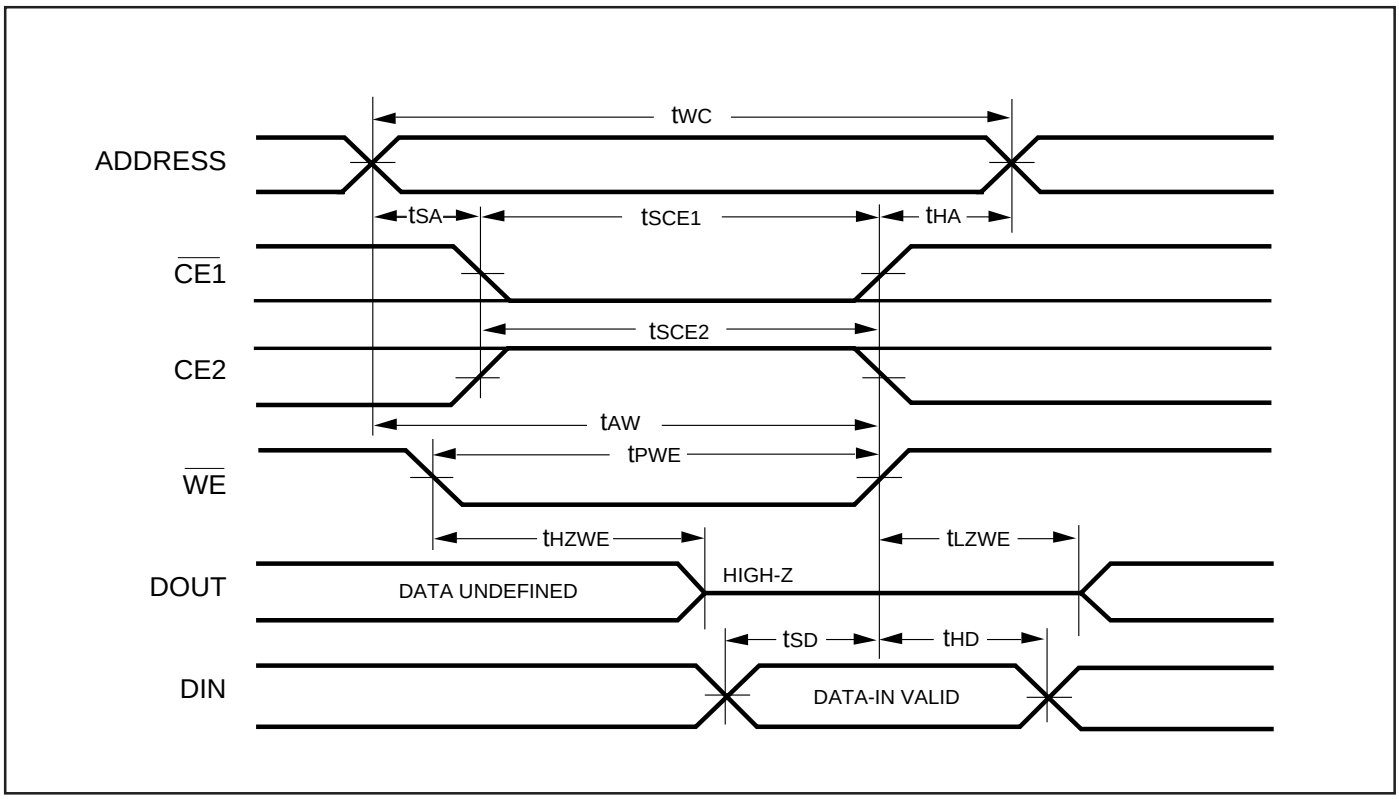
Notes:
1. Test conditions assume signal transition times of 5 ns or less, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}1$ LOW , CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$1, CE2 Controlled)[1,2]



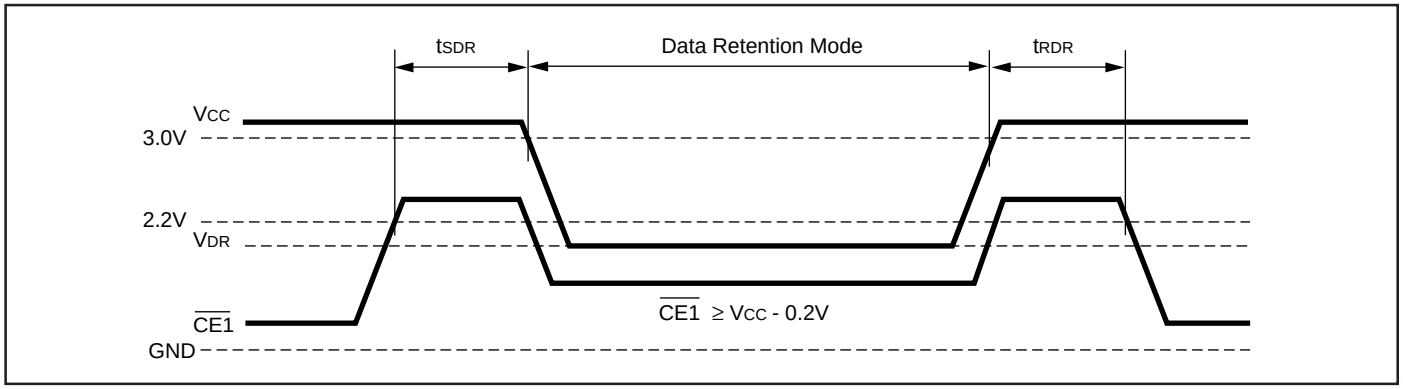
Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$1 LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the HIGH-z state if $\overline{OE}$ =V_{IH}.

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		1.5	3.6	V
I_{DR}	Data Retention Current	Vcc = 1.5V, $\overline{CE1} \geq$ Vcc – 0.2V	Com. (-L)	—	15	µA
			Com. (-LL)	—	6	µA
			Ind. (-L)	—	20	µA
			Ind. (-LL)	—	9	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		10	—	ns

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV1008L-55B	8*10mm TF-BGA
70	IC62LV1008L-70B	8*10mm TF-BGA
100	IC62LV1008L-100B	8*10mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV1008L-55BI	8*10mm TF-BGA
70	IC62LV1008L-70BI	8*10mm TF-BGA
100	IC62LV1008L-100BI	8*10mm TF-BGA

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IC62LV1008LL-55B	8*10mm TF-BGA
	IC62LV1008LL-55D	know good die
70	IC62LV1008LL-70B	8*10mm TF-BGA
	IC62LV1008LL-70D	know good die
100	IC62LV1008LL-100B	8*10mm TF-BGA
	IC62LV1008LL-100D	know good die

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IC62LV1008LL-55BI	8*10mm TF-BGA
	IC62LV1008LL-55DI	know good die
70	IC62LV1008LL-70BI	8*10mm TF-BGA
	IC62LV1008LL-70DI	know good die
100	IC62LV1008LL-100BI	8*10mm TF-BGA
	IC62LV1008LL-100DI	know good die

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