GENERAL DESCRIPTION

Samsung's S5N8947 16/32-bit RISC microcontroller is a cost-effective, high-performance microcontroller solution. The S5N8947 is designed as 2-channel 10/100Mbps Ethernet controller for use in managed communication hubs and routers. The S5N8947 also provides ATM Layer SAR (Segmentation and Reassembly) function with UTOPIA interface and the full-rate USB (Universal Serial Bus) function.

The S5N8947 is built around an outstanding CPU core: the 16/32-bit ARM7TDMI RISC processor designed by Advanced RISC Machines, Ltd. The ARM7TDMI core is a low-power, general purpose, microprocessor macro-cell that was developed for use in application-specific and custom-specific integrated circuits. Its simple, elegant, and fully static design is particularly suitable for cost-sensitive and power-sensitive applications.

Important peripheral functions including an UART channel, 2-channel GDMA, three 32-bit timers, watchdog timer, I^2C bus controller, SPI, and programmable I/O ports are supported. Built-in logic including an interrupt controller, DRAM controller, and a controller for ROM/SRAM and flash memory are also supported. The S5N8947's System Manager provides an internal 32-bit system bus arbiter and an external memory controller including control logic for a PCMCIA socket interface.

To reduce total system cost, the S5N8947 offers a unified cache, 2-channel 10/100Mbps Ethernet controller, SAR and USB. Most of the on-chip function blocks have been designed using an HDL synthesizer and the S5N8947 has been fully verified in Samsung's state-of-the-art ASIC test environment.

Table 1-1. S5N8946 vs. S5N8947

Item	S5N8946	S5N8947
Architecture	Only one mode: 10Base-T + SAR + USB	Two modes are supported: Mode 1. MII + SAR + USB + PCMCIA Mode 2. 2×MII + SAR + USB
	2 timer	3 timer
	-	1 watchdog timer
	-	SPI interface support
	-	PCMCIA support
Function	UTOPIA level 1 support	UTOPIA level 1/2 support
	Seven wire support (10 Mbps Ethernet Support)	MII/Seven wire support (10/100 Mbps Ethernet Support)
	USB support byte access.	USB support word access and DMA operation.
	SAR support hardwired big endian.	SAR support hardwired Big/Little endian.
Performance	50MHz operation	72MHz operation
	4K unified cache	8K unified cache
Operation Condition	3.3V	1.8V
Package	240 QFP	208 LQFP

FEATURES

— 8-Kbyte unified cache
— SAR (Segmentation and Reassembly)
— UTOPIA (the Universal Test & Operations PHY Interface for ATM) Level 1/2 Interface
— 2-channel 10/100Mbps Ethernet
— Full-rate USB controller
— 2-CH GDMA (General Purpose Direct Memory Access)
— UART (Universal Asynchronous Receiver and Transmtter)
— 3 programmable 32bits Timers
— Watchdog Timer
— 18 Programmable I/O ports
— Interrupt controller
— I^2C controller
— SPI (Serial Peripheral Interface)
— Built-in PLLs for System/USB
— PCMCIA ‘memory and I/O’ master modes
— Cost effective JTAG-based debug solution
— Boundary scan
— 3.3V I/Os and 1.8V core supply voltage
— Operating Frequency Up to 72MHz
— 208 LQFP Package

FUNCTIONAL BLOCK DESCRIPTIONS

BLOCK DIAGRAM

Mode 1 (1 SAR + 1 MII + 1 PCMCIA + 1 USB)

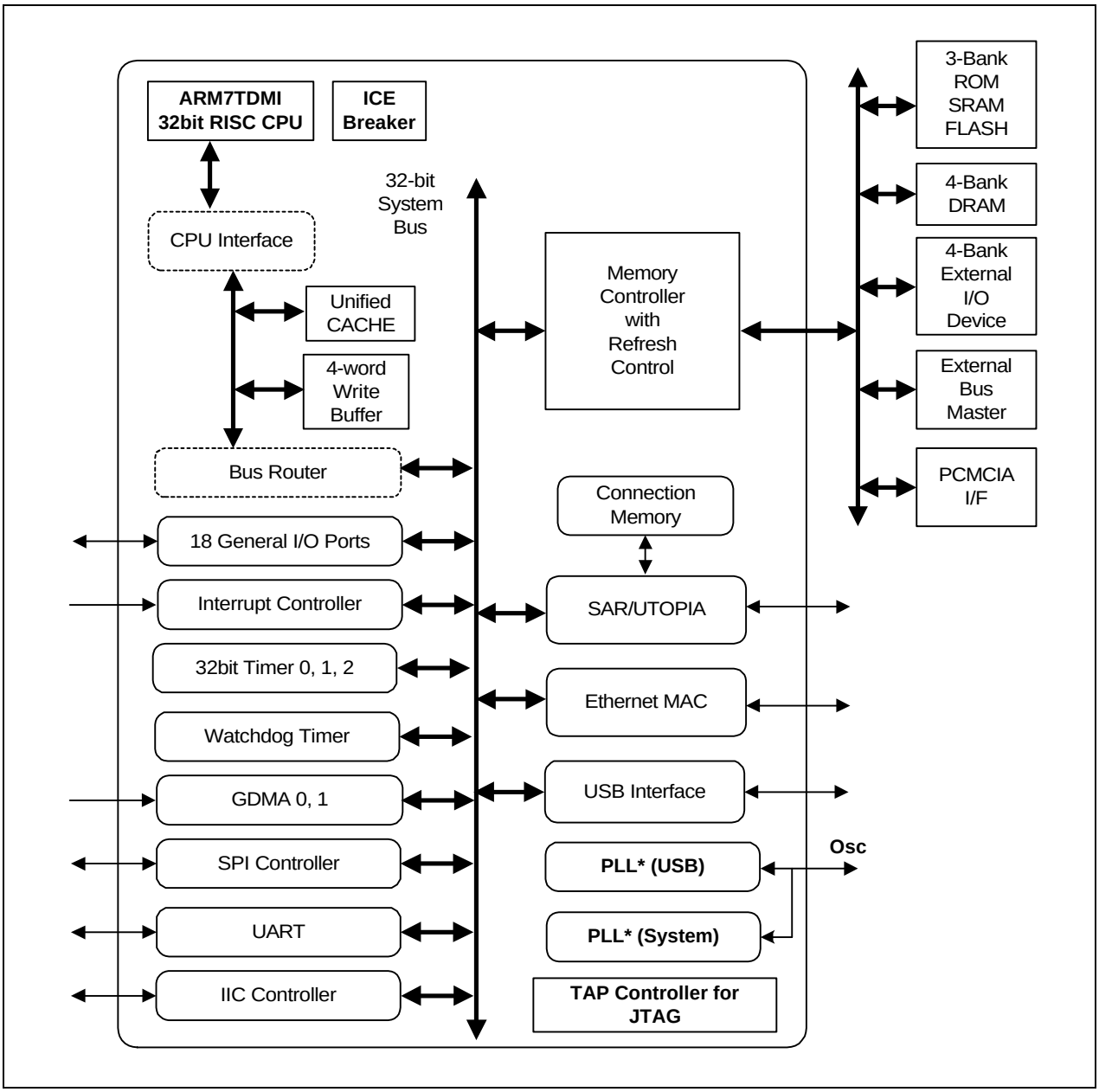

Figure 1-1. Top Block Diagram: Mode 1

Mode 2 (1 SAR + 2 MII + 1 USB)

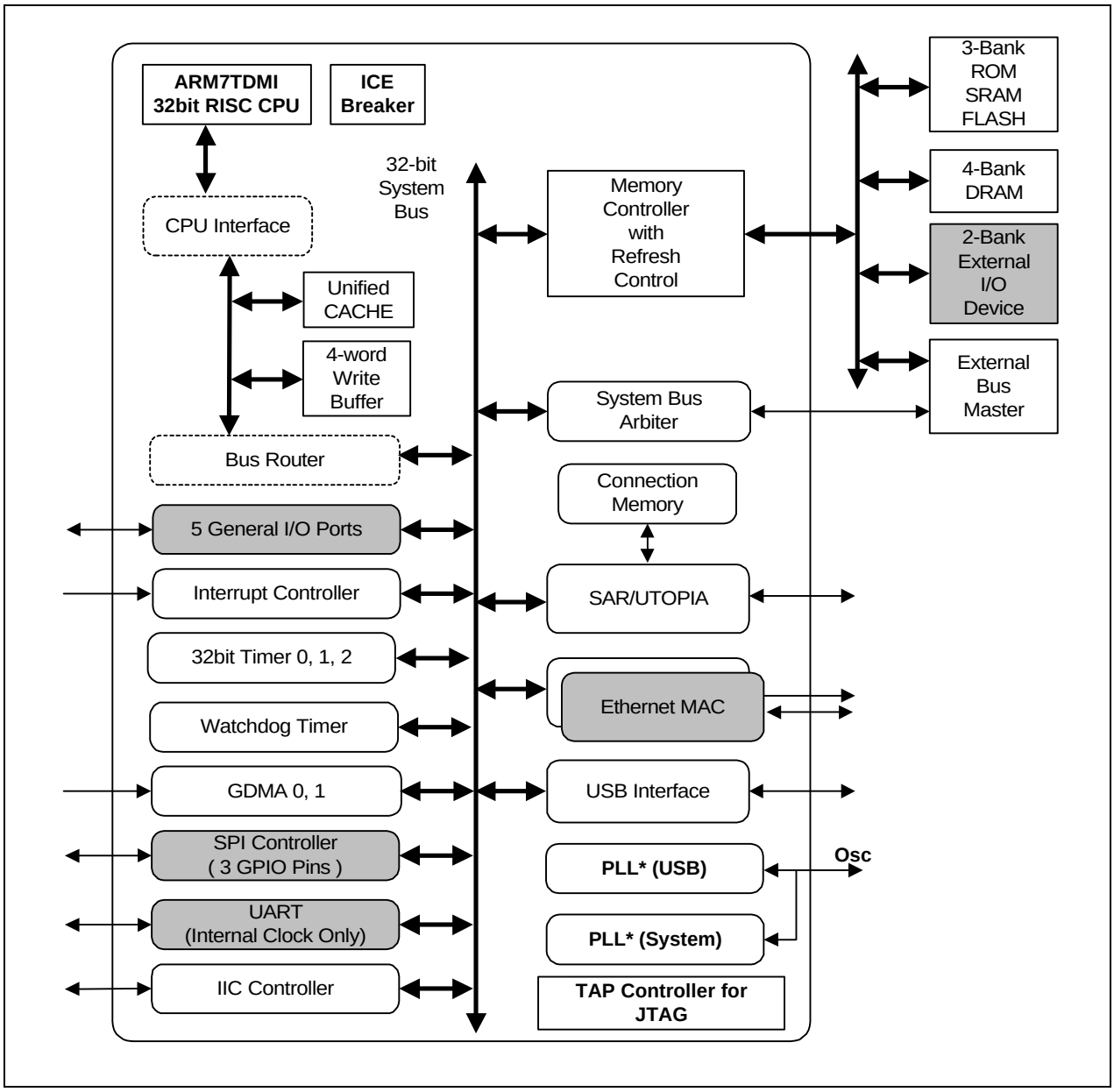

Figure 1-2. Top Block Diagram: Mode 2

ARCHITECTURE

— Integrated system for embedded Ethernet / USB / SAR
— Fully 16/32-bit RISC architecture
— Efficient and powerful ARM7TDMI core
— Little/Big-Endian mode is fully supported. (The internal register supports word access only.)
— Cost-effective JTAG-based debug solution
— Supports Boundary Scan

SYSTEM MANAGER

— 8/16/32-bit external bus support for ROM/SRAM, flash memory, DRAM and external I/O
— One external bus master with bus request/acknowledge pins
— Supports EDO/normal or SDRAM
— Programmable access cycle
— Four-word depth write buffer
— Cost-effective memory-to-peripheral DMA interface
— Supports PCMCIA ‘memory and I/O’ master mode

UNIFIED INSTRUCTION/DATA CACHE

— Two-way set-associative unified cache (8Kbytes)
— Supports LRU (least recently used) Protocol

SAR/UTOPIA INTERFACE

— Directly supports ATM Adaptation Layer Five (AAL5) Segmentation And Reassembly
— Segments and reassembles data up to 70Mbps
— A glueless UTOPIA level 1/2 interface is supprted (for receiving and transmitting ATM cells with SAR, it is a standard ATM interface between ATM link and physical layer).

ETHERNET

— 2-Channel 10/100Mbps Ethernet Controller
— 4 DMA engines with burst mode
— Full compliance with IEEE standard 802.3
— Supports MII interface (7-wire 10-Mbps interface is also supported).

USB CONTROLLER

Supports 12Mbps full rate function for universal serial bus

DMA CONTROLLER

— 2-channel general purpose DMA (for memory-to-memory, memory-to-SPI, SPI-to-memory, UART-to-memory, memory-to-UART data transfers without CPU intervention)

— Initiated by a software or a external DMA request

— Increments or decrements source or destination address in 8-bit, 16-bit, or 32-bit data transfers

UART

— UART block with DMA-based or interrupt-based operation

— Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit and receive

— Programmable baud rates

— Infra-red (IR) TX/RX support (IrDA)

TIMERS

— Three programmable 32-bit timers

— Interval mode or toggle mode operation

— Supports a watchdog timer

PROGRAMMABLE I/O

— 18 programmable I/O ports

— Pins individually configurable to input, output, or I/O mode for dedicated signals

INTERRUPT CONTROLLER

— 23 interrupt sources, including 7 external interrupt sources

— Normal or fast interrupt mode (IRQ, FIQ)

— Prioritized interrupt handling

I²C SERIAL INTERFACE

— Single master mode operation only

SPI

— Full duplex operation
— Work with data characters from 4 to 32 bits long
— Supports GDMA mode for SPI transmission and reception
— Single master SPI modes only supported
— Programmable baud rate generator
— Programmable clock phase and polarity

PLLS

— The external clock can be multiplied by on-chip PLLs to provide high frequency System/USB clock
— The input frequency is fixed to 12MHz
— The output frequency is 6 times the input clock for System
— The output frequency is 4 times the input clock for USB

NOTE

Refer to the Board guides for clock frequency which can be usable.
CM47_M66_MANUAL_V1.0.doc
CM47_M72_MANUAL10.doc

PIN DESCRIPTIONS

PIN CONFIGURATION

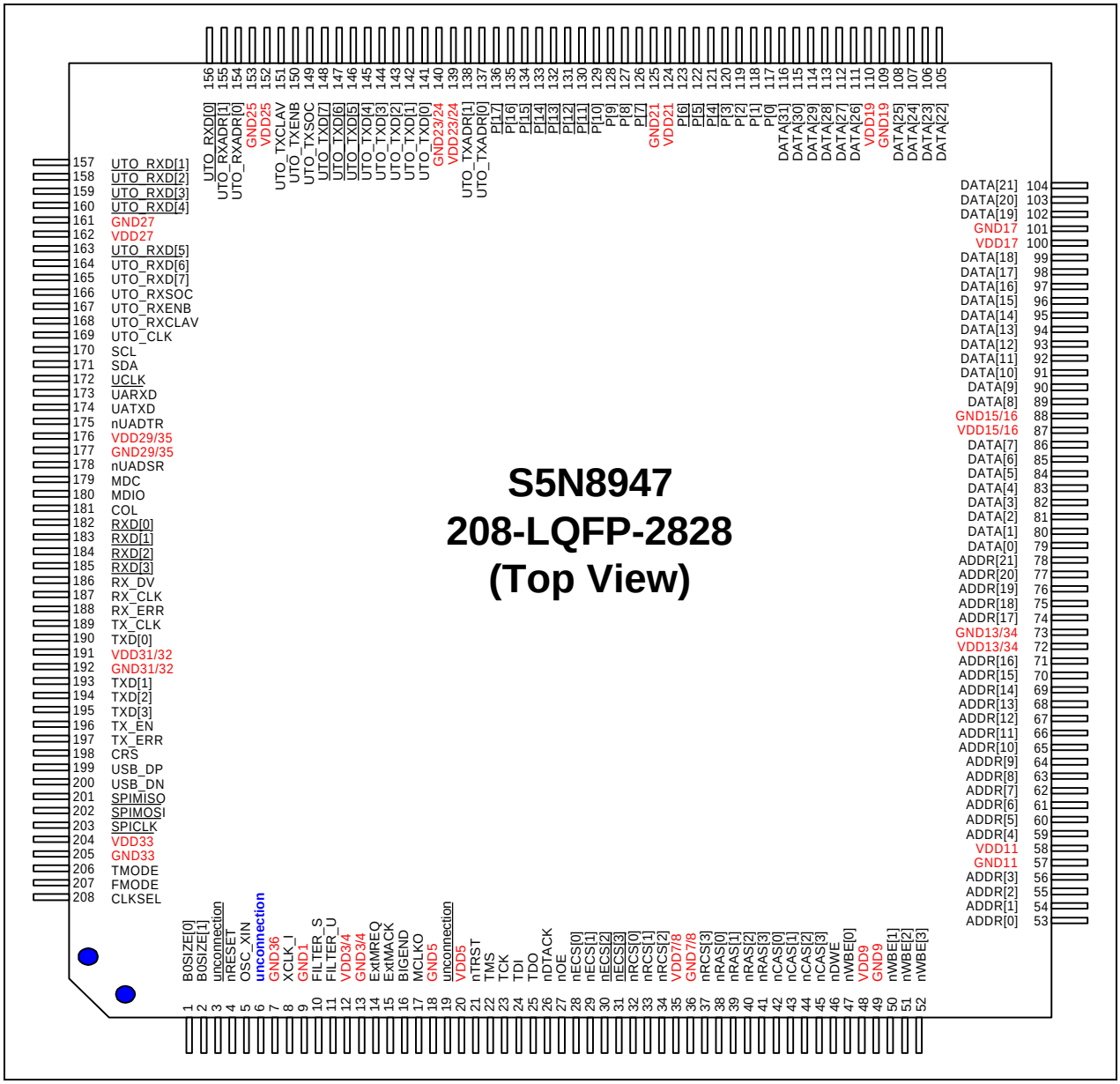

Figure 1-3. S5N8947 Pin Configuration

NOTE

Under-bar in the Figure 1-3 means the muxing pins.

LOGIC SYMBOL DIAGRAM

Mode 1 (1 SAR + 1 MII + 1 PCMCIA + 1 USB)

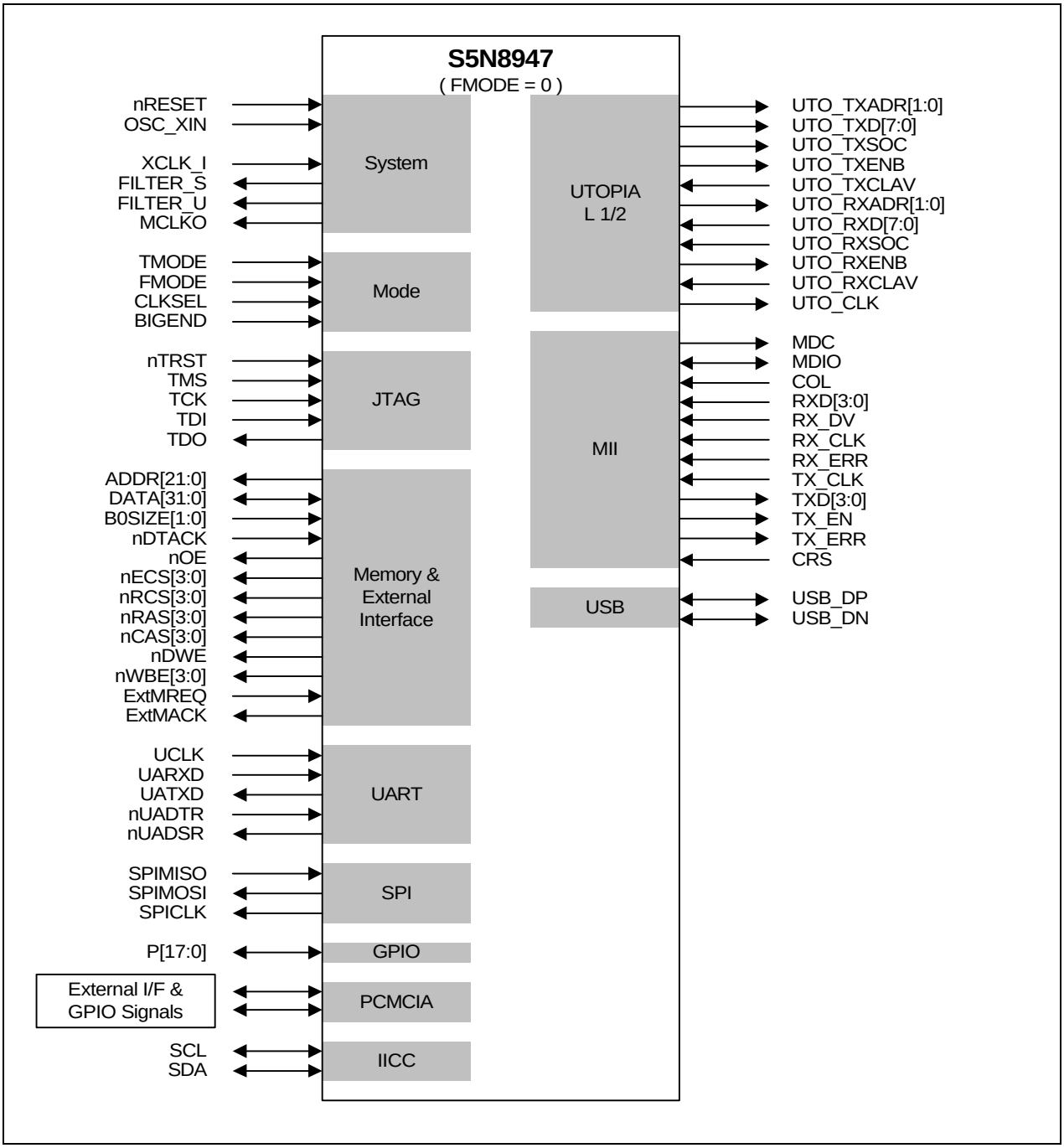

Figure 1-4. S5N8947 Logic Symbol Diagram (Mode 1)

Mode 2 (1 SAR + 2 MII + 1 USB)

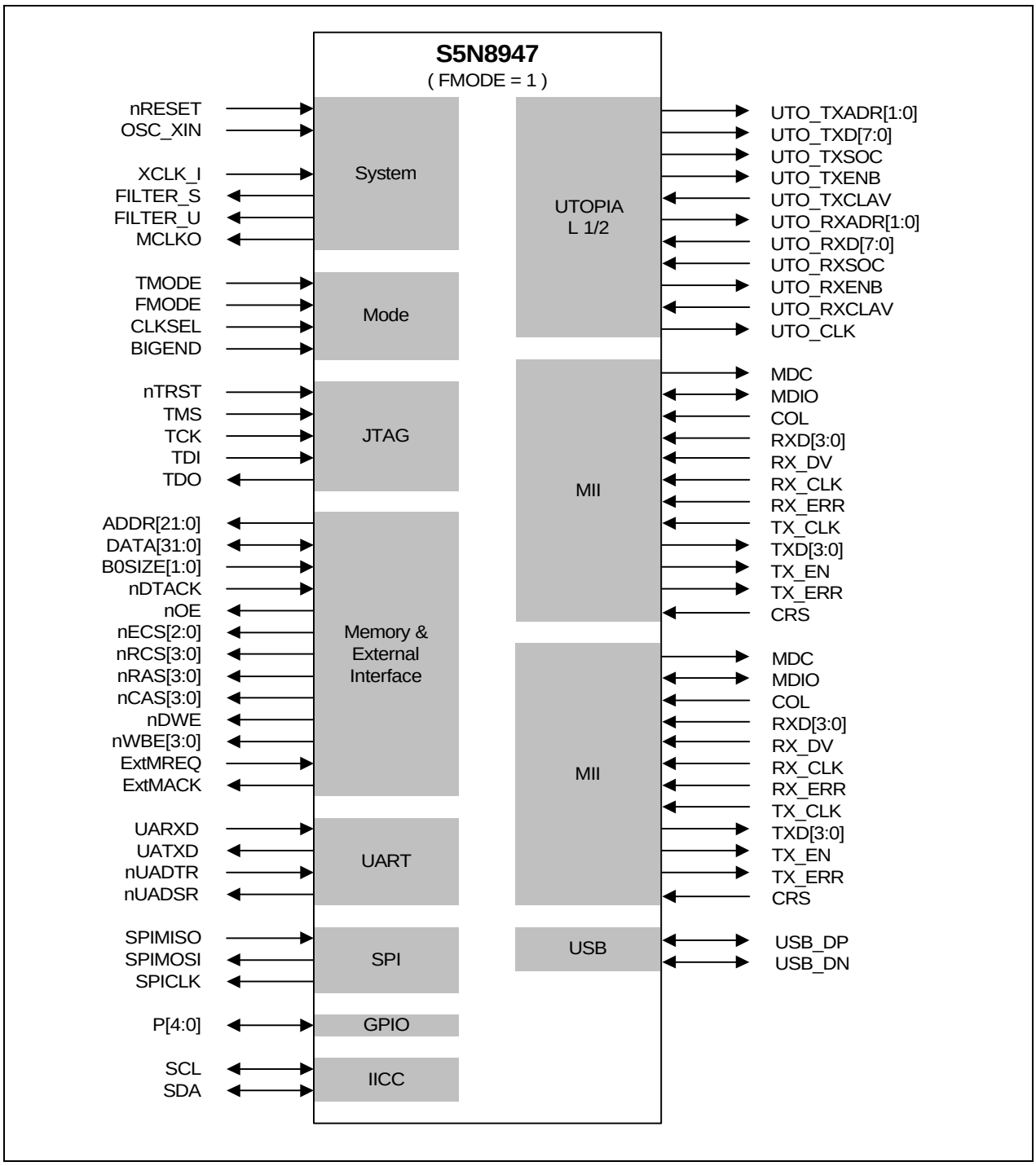

Figure 1-5. S5N8947 Logic Symbol Diagram (Mode 2)

Table 1-2. Pin Descriptions with the Pin number and Pad type

Pin No	Pin Name	I/O Type	Pad Type	Descriptions
1	B0SIZE[0]	I	Phic	
2	B0SIZE[1]	I	Phic	
*3	unconnection	I	Phic	Muxing with sRX_CLK
4	nRESET	I	Phtis	
5	OSC_XIN	I	Phsoscm2	OSC input
6	**unconnection**	O	Phsoscm2	
7	GND36	P	Vss3o	
8	XCLK_I	I	phic	
9	GND1	P	Vbb1_abb	
10	FILTER_S	O	Poar50_abb	
11	FILTER_U	O	Poar50_abb	
12	VDD3/4	P	Vdd1t_abb	1.8V
13	GND3/4	P	Vss1t_abb	
14	ExtMREQ	I	Phic	
15	ExtMACK	O	Phob1	
16	BIGEND	I	Phicd	
17	MCLKO	O	Phob8	
18	GND5	P	Vss3p	
*19	Unconnection	B	Phbcut4	Muxing with sMDIO
20	VDD5	P	Vdd3p	3.3V
21	nTRST	I	Phicu	
22	TMS	I	Phicu	
23	TCK	I	phic	
24	TDI	I	Phicu	
25	TDO	O	Phtot2	
26	NDTACK	I	Phicu	
27	NOE	O	Phot4	
28	NECS[0]	O	Phot4	
29	NECS[1]	O	Phot4	
*30	NECS[2]	O	Phot4	Muxing with sTXD[3]
*31	NECS[3]	O	Phot4	Muxing with sMDC
32	nRCS[0]	O	Phot4	
33	nRCS[1]	O	Phot4	
34	nRCS[2]	O	Phot4	

Table 1-2. Pin Descriptions with the Pin number and Pad type (Continued)

Pin No	Pin Name	I/O Type	Pad Type	Descriptions
35	VDD7/8	P	Vdd3o	3.3V
36	GND7/8	P	Vss3o	
37	nRCS[3]	O	Phot4	Not PCMCIA select
38	nRAS[0]	O	Phot4	
39	nRAS[1]	O	Phot4	
40	nRAS[2]	O	Phot4	
41	nRAS[3]	O	Phot4	
42	nCAS[0]	O	Phot4	
43	nCAS[1]	O	Phot4	
44	nCAS[2]	O	Phot4	
45	nCAS[3]	O	Phot4	
46	nDWE	O	Phot4	
47	nWBE[0]	O	Phot8	
48	VDD9	P	Vdd1ih	1.8V
49	GND9	P	Vss3i	
50	nWBE[1]	O	Phot8	nWBE[1]/IORD(PCMCIA only)
51	nWBE[2]	O	Phot8	nWBE[2]/IOWR(PCMCIA only)
52	nWBE[3]	O	Phot8	
53-56	ADDR[0:3]	O	Phot4	
57	GND11	P	Vss3i	
58	VDD11	P	Vdd1ih	1.8V
59-71	ADDR[4:16]	O	Phot8	
72	VDD13/34	P	Vdd3o	3.3V
73	GND13/34	P	Vss3o	
74-78	ADDR[17:21]	O	Phot8	
79-86	DATA[0:7]	B	Phbcut8	
87	VDD15/16	P	Vdd3o	3.3V
88	GND15/16	P	Vss3o	
89-99	DATA[8:18]	B	Phbcut8	
100	VDD17	P	Vdd1ih	1.8V
101	GND17	P	Vss3i	
102-108	DATA[19-25]	B	Phbcut8	
109	GND19	P	Vss3I	
110	VDD19	P	Vdd1ih	1.8V
111-116	DATA[26-31]	B	Phbcut8	

Table 1-2. Pin Descriptions with the Pin number and Pad type (Continued)

Pin No	Pin Name	I/O Type	Pad Type	Descriptions
117-120	P[0:3]	B	Phbcut4	
*121	P[4]	B	Phbcut4	Muxing with sTXD[0]
*122	P[5]	B	Phbcut4	Muxing with sTXD[1]
*123	P[6]	B	Phbcut4	Muxing with sTXD[2]
124	VDD21	P	Vdd3p	3.3V
125	GND21	P	Vss3p	
*126	P[7]	B	Phbcut4	Muxing with sRX_DV
127-129	P[8-10]	B	Phbcut4	
*130	P[11]	B	Phbcut4	Muxing with sCRS
*131	P[12]	B	Phbcut4	Muxing with sRXD[0]
*132	P[13]	B	Phbcut4	Muxing with sRXD[1]
*133	P[14]	B	Phbcut4	Muxing with sRXD[2]
*134	P[15]	B	Phbcut4	Muxing with sRXD[3]
135	P[16]	B	Phbcut4	
*136	P[17]	B	Phbcut4	Muxing with sRX_ERR
137-138	UTO_TXADR[0:1]	O	Phob4	
139	VDD23/24	P	Vdd3o	3.3V
140	GND23/24	P	Vss3o	
141-145	UTO_TXD[0:4]	O	Phob4	
*146	UTO_TXD[5]	O	Phob4	Muxing with bist_errob
*147	UTO_TXD[6]	O	Phob4	Muxing with bist_diag
*148	UTO_TXD[7]	O	Phob4	Muxing with bist_done
149	UTO_TXSOC	O	Phob4	
150	UTO_TXENB	O	Phob4	
151	UTO_TXCLAV	I	Phtis	
152	VDD25	P	Vdd1ih	1.8V
153	GND25	P	Vss3i	
154-155	UTOP_RXADR[0:1]	O	Phob4	
*156	UTO_RXD[0]	I	phtis	Muxing with bist_on
*157	UTO_RXD[1]	I	phtis	Muxing with bist_mode
*158	UTO_RXD[2]	I	phtis	Muxing with bist_memsel[0]
*159	UTO_RXD[3]	I	phtis	Muxing with bist_memsel[1]
*160	UTO_RXD[4]	I	phtis	Muxing with bist_memsel[2]
161	GND27	P	Vss3i	

Table 1-2. Pin Descriptions with the Pin number and Pad type (Continued)

Pin No	Pin Name	I/O Type	Pad Type	Descriptions
162	VDD27	P	Vdd1ih	1.8V
*163	UTO_RXD[5]	I	phtis	Muxing with bist_memsel[3]
164-165	UTO_RXD[6:7]	I	phtis	
166	UTO_RXSOC	I	Phtis	
167	UTO_RXENB	O	Phob4	
168	UTO_RXCLAV	I	Phtis	
169	UTO_CLK	O	Phob4	
170	SCL	B	Phbcud4	
171	SDA	B	Phbcud4	
*172	UCLK	I	phic	Muxing with sTX_CLK
173	UARXD	I	Phic	
174	UATXD	O	Phob4	
175	nUADTR	I	Phic	
176	VDD29/35	P	Vdd3o	3.3V
177	GND29/35	P	Vss3o	
178	nUADSR	O	Phob4	
179	MDC	O	Phob4	
180	MDIO	B	Phbcut4	
181	COL	I	Phic	7-wire pin
*182	RXD[0]	I	Phic	Muxing with test_mode[0], 7-wire pin
*183	RXD[1]	I	Phic	Muxing with test_mode[1]
*184	RXD[2]	I	Phic	Muxing with test_mode[2]
*185	RXD[3]	I	Phic	Muxing with test_mode[3]
186	RX_DV	I	Phic	
187	RX_CLK	I	Phic	7-wire pin
188	RX_ERR	I	Phic	
189	TX_CLK	I	Phic	7-wire pin
190	TXD[0]	O	Phob4	7-wire pin
191	VDD31/32	P	Vdd3o	3.3V
192	GND31/32	P	Vss3o	
193-195	TXD[1:3]	O	Phob4	
196	TX_EN	O	Phob4	7-wire pin
197	TX_ERR	O	Phob4	
198	CRS	I	Phic	7-wire pin
199	USB_DP	B	Pbusbfs	

Table 1-2. Pin Descriptions with the Pin number and Pad type (Continued)

Pin No	Pin Name	I/O Type	Pad Type	Descriptions
200	USB_DN	B	Pbusbfs	
*201	SPIMISO	I	Phic	SPI input data, Muxing with sCOL
*202	SPIMOSI	O	Phob4	SPI output data, Muxing with sTX_EN
*203	SPICLK	O	Phob4	SPI clock, Muxing with sTX_ERR
204	VDD33	P	Vdd1ih	1.8V
205	GND33	P	Vss3i	
206	TMODE	I	Phic	
207	FMODE	I	Phic	
208	CLKSEL	I	phic	

PAD DESCRIPTIONS

Input PADs

Pad Types	Descriptions
PHIC / PHICS / PHICU	3.3V interface LVCMOS level input buffer
PHIS / PHISD / PHISU	3.3V interface LVCMOS schmitt trigger level input buffer
PHTIS / PHTISD / PHTISU	5V tolerant for 3.3V interface CMOS schmit trigger level input buffer

Output PADs

Pad Types	Descriptions
PHOB (1/4/8)	3.3V LVCMOS normal output buffers
PHOT (1/4/8)	3.3V LVCMOS tri-state output buffers

Bi-Direction PADs

Pad Types	Descriptions
PHBCUT4 (PHBaTyz)	3.3V tri-state bi-direction buffers
PHBCUD4 (PHBaUDyz)	3.3V open-drain bi-directional buffers with pull-up

Power Pads

Pad Characteristics	Pad Types	Supply Voltage	Descriptions
1.8V Interface Digital I/O	vdd1i	1.8V	1.8V internal
3.3V Interface Digital I/O	Vdd3p	3.3V	3.3V pre-driver
	Vdd3o	3.3V	3.3V output-driver
1.8V Interface Digital I/O	Vss1i		Internal GND for 1.8V interface I/O
3.3V Interface Digital I/O	Vss3p		Pre-driver GND for 3.3V interface I/O
	Vss3o		Output-driver GND for 3.3V interface I/O
1.8V Interface Analog I/O	Vdd1t_abb	1.8V	1.8V total
1.8V Interface Analog I/O	Vss1t_abb		Total GND for 1.8V interface I/O
	Vss1_abb		Bulk-bias GND for 1.8V interface I/O

OPERATION DESCRIPTION

CPU CORE OVERVIEW

The S5N8947 CPU core is the ARM7TDMI processor, a general purpose, 32-bit microprocessor developed by Advanced RISC Machines, Ltd. (ARM). The core's architecture is based on Reduced Instruction Set Computer (RISC) principles. The RISC architecture makes the instruction set and its related decoding mechanisms simpler and more efficient than those with microprogrammed Complex Instruction Set Computer (CISC) systems. The resulting benefit is high instruction throughput and impressive real-time interrupt response. Pipelining is also employed so that all components of the processing and memory systems can operate continuously. The ARM7TDMI has a 32-bit address bus.

An important feature of the ARM7TDMI processor, and one which differentiates it from the ARM7 processor, is a unique architectural strategy called THUMB. The THUMB strategy is an extension of the basic ARM architecture and consists of 36 instruction formats. These formats are based on the standard 32-bit ARM instruction set, but have been re-coded using 16-bit wide opcodes.

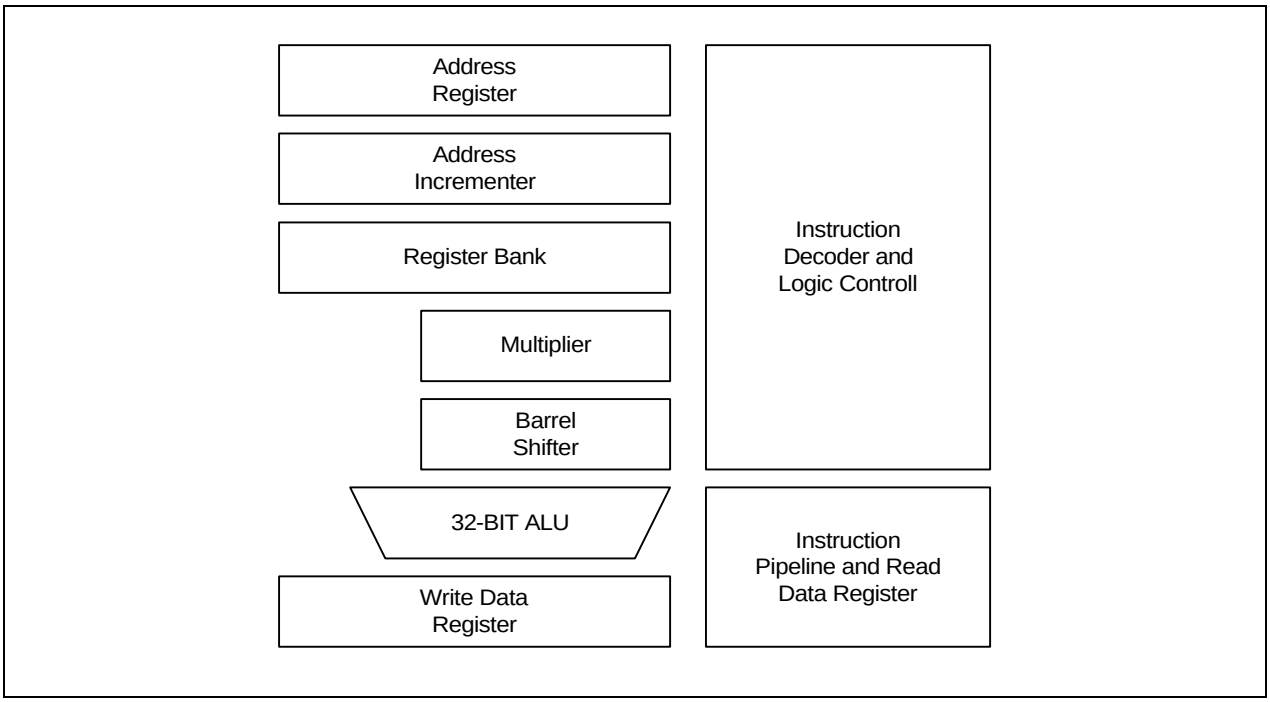

Figure 1-6. ARM7TDMI Core Block Diagram

Because THUMB instructions are one-half the bit width of normal ARM instructions, they produce very high-density code. When a THUMB instruction is executed, its 16-bit opcode is decoded by the processor into its equivalent instruction in the standard ARM instruction set. The ARM core then processes the 16-bit instruction as it would a normal 32-bit instruction. In other words, the THUMB architecture gives 16-bit systems a way to access the 32-bit performance of the ARM core without incurring the full overhead of 32-bit processing. Because the ARM7TDMI core can execute both standard 32-bit ARM instructions and 16-bit THUMB instructions, it lets you mix routines of THUMB instructions and ARM code in the same address space. In this way, you can adjust code size and performance, routine by routine, to find the best programming solution for a specific application.

INSTRUCTION SET

The S5N8947 instruction set is divided into two subsets: a standard 32-bit ARM instruction set and a *16-bit THUMB instruction set*.

The 32-bit ARM instruction set is comprised of thirteen basic instruction types which can be divided into four broad classes:

— Four types of branch instructions which control program execution flow, instruction privilege levels, and switching between ARM code and THUMB code.

— Three types of data processing instructions which use the on-chip ALU, barrel shifter, and multiplier to perform high-speed data operations in a bank of 31 registers (all with 32-bit register widths).

— Three types of load and store instructions which control data transfer between memory locations and the registers. One type is optimized for flexible addressing, another for rapid context switching, and the third for swapping data.

— Three types of co-processor instructions which are dedicated to controlling external co-processors. These instructions extend the off-chip functionality of the instruction set in an open and uniform way.

NOTE

All 32-bit ARM instructions can be executed conditionally.

The 16-bit THUMB instruction set contains 36 instruction formats drawn from the standard 32-bit ARM instruction set. The THUMB instructions can be divided into four functional groups:

— Four branch instructions.

— Twelve data processing instructions, which are a subset of the standard ARM data processing instructions.

— Eight load and store register instructions.

— Four load and store multiple instructions.

NOTE

Each 16-bit THUMB instruction has a corresponding 32-bit ARM instruction with the identical processing model.

The 32-bit ARM instruction set and the 16-bit THUMB instruction sets are good targets for compilers of many different high-level languages. When assembly code is required for critical code segments, the ARM programming technique is straightforward, unlike that of some RISC processors which depend on sophisticated compiler technology to manage complicated instruction interdependencies.

Pipelining is employed so that all parts of the processor and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

OPERATING STATES

From a programmer's point of view, the ARM7TDMI core is always in one of two operating states. These states, which can be switched by software or by exception processing, are:

— *ARM state* (when executing 32-bit, word-aligned, ARM instructions), and

— *THUMB state* (when executing 16-bit, half-word aligned THUMB instructions).

OPERATING MODES

The ARM7TDMI core supports seven operating modes:

— User mode: the normal program execution state

— FIQ (Fast Interrupt Request) mode: for supporting a specific data transfer or channel process

— IRQ (Interrupt ReQuest) mode: for general purpose interrupt handling

— Supervisor mode: a protected mode for the operating system

— Abort mode: entered when a data or instruction pre-fetch is aborted

— System mode: a privileged user mode for the operating system

— Undefined mode: entered when an undefined instruction is executed

Operating mode changes can be controlled by software, or they can be caused by external interrupts or exception processing. Most application programs execute in User mode. Privileged modes (that is, all modes other than User mode) are entered to service interrupts or exceptions, or to access protected resources.

REGISTERS

The S5N8947 CPU core has a total of 37 registers: 31 general-purpose 32-bit registers, and 6 status registers. Not all of these registers are always available. Which registers are available to the programmer at any given time depends on the current processor operating state and mode.

NOTE

When the S5N8947 is operating in ARM state, 16 general registers and one or two status registers can be accessed at any time. In privileged mode, mode-specific banked registers are switched in.

Two register sets, or banks, can also be accessed, depending on the core's current state: the ARM state register set and the *THUMB state register* set:

— The ARM state register set contains 16 directly accessible registers: R0-R15. All of these registers, except for R15, are for general-purpose use, and can hold either data or address values. An additional (seventeenth) register, the CPSR (Current Program Status Register), is used to store status information.

— The THUMB state register set is a subset of the ARM state set. You can access eight general registers, R0-R7, as well as the program counter (PC), a stack pointer register (SP), a link register (LR), and the CPSR. Each privileged mode has a corresponding banked stack pointer, link register, and saved process status register (SPSR).

The THUMB state registers are related to the ARM state registers as follows:

— THUMB state R0-R7 registers and ARM state R0-R7 registers are identical

— THUMB state CPSR and SPSRs and ARM state CPSR and SPSRs are identical

— THUMB state SP, LR, and PC map directly to ARM state registers R13, R14, and R15, respectively

In THUMB state, registers R8-R15 are not part of the standard register set. However, you can access them for assembly language programming and use them for fast temporary storage, if necessary.

EXCEPTIONS

An exception arises whenever the normal flow of program execution is interrupted. For example, when processing must be diverted to handle an interrupt from a peripheral. The processor's state just prior to handling the exception must be preserved so that the program flow can be resumed when the exception routine is completed. Multiple exceptions may arise simultaneously.

To process exceptions, the S5N8947 uses the banked core registers to save the current state. The old PC value and the CPSR contents are copied into the appropriate R14 (LR) and SPSR register. The PC and mode bits in the CPSR are forced to a value which corresponds to the type of exception being processed.

The S5N8947 core supports seven types of exceptions. Each exception has a fixed priority and a corresponding privileged processor mode, as shown in following Table

Table 1-3. S5N8947 CPU Exceptions

Exception	Mode on Entry	Priority
Reset	Supervisor Mode	1 (highest)
Data Abort	Abort Mode	2
FIQ	FIQ Mode	3
IRQ	IRQ Mode	4
Prefetch Abort	Abort Mode	5
Undefined Instruction	Undefined Mode	6
SWI	Supervisor Mode	6 (lowest)

HARDWARE STRUCTURE

SYSTEM MANAGER

Overview

The S5N8947 microcontroller's System Manager has the following functions.

— Arbitrates system bus access requests from several master blocks, based on fixed priorities.

— Provides the required memory control signals for external memory accesses. For example, if a master block such as the DMA controller or the CPU generates an address, which corresponds to a DRAM bank, the System Manager's DRAM controller generates the required normal/EDO or SDRAM access signals. The interface signals for normal/EDO or SDRAM can be switched by SYSCFG[31].

— Provides the required signals for bus traffic between the S5N8947 and ROM/SRAM and the external I/O banks.

— Compensates for differences in bus width for data transfer between the external memory bus and the internal data bus.

— Supports both little and big endian for external memory or I/O devices. Internal registers, however, operate under big-endian mode.

— Supports both motorola mode and intel mode for external I/O devices

— Supports an external bus master with bus request(ExtMREQ) and bus acknowledge(ExtMACK)

— Supports PCMCIA 'memory and I/O' master mode

System Manager Registers

To control external memory operations, the System Manager uses a dedicated set of special registers. By programming the values in the System Manager special registers, you can specify such things as:

— Memory type

— External data access cycle

— External memory and I/O device access cycle

— Memory bank locations

— Size of each memory bank to be used for arbitrary address spacing

The System Manager uses special register setting to control the generation and processing of the control signals, addresses, and data that are required by external devices in a standard system configuration. Special registers are also used to control access to ROM/SRAM/Flash banks, a PCMCIA interface, up to four DRAM banks and four external I/O banks, and a special register mapping area.

The address resolution for each memory bank base pointer is 64 Kbytes (16 bits). The base address pointer is 10 bits. This gives a total addressable memory bank space of 16 M words.

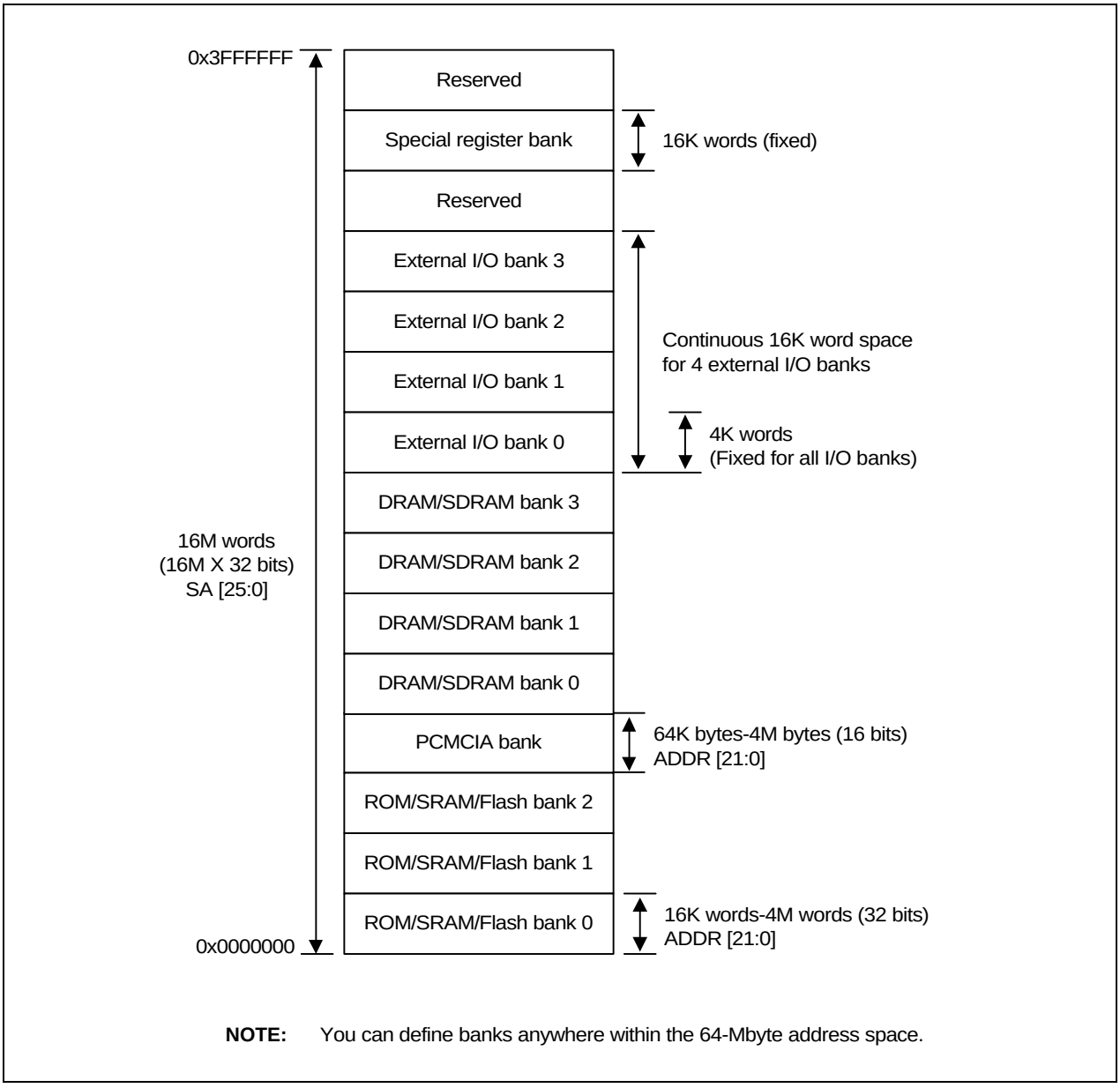

Figure 1-7. S5N8947 System Memory Map

System Memory Map

Followings are several important features to note about the S5N8947 system memory map:

— The size and location of each memory bank is determined by the register settings for “current bank base pointer” and “current bank end pointer”. You can use this base/next bank pointer concept to set up a consecutive memory map. To do this, you set the base pointer of the “next bank” to the same address as the next pointer of the “current bank”. Please note that when setting the bank control registers, the address boundaries of consecutive banks must not overlap. This can be applied even if one or more banks are disabled.

— Four external I/O banks are defined in a continuous address space. A programmer can only set the base pointer for external I/O bank 0. The start address of external I/O bank 1 is then calculated as the external I/O bank 0 start address +16 K. Similarly, the start address for external I/O bank 2 is the external I/O bank 0 start address + 32 K, and the start address for external I/O bank 3 is the external I/O bank 0 start address + 48 K. Therefore, the total consecutive addressable space of the four external banks is defined as the start address of external I/O bank 0 + 64 K bytes.

— Within the addressable space, the start address of each I/O bank is not fixed. You can use bank control registers to assign a specific bank start address by setting the bank’s base pointer. The address resolution is 64 K bytes. The bank’s start address is defined as “base pointer << 16” and the bank’s end address (except for external I/O banks) is “next pointer << 16 – 1”.

After a power-on or system reset, all bank address pointer registers are initialized to their default values. In this means that a system reset automatically defines ROM bank 0 as a 32-Mbyte space with a start address of zero. This means that, except for ROM bank 0, all banks are undefined following a system startup.

The reset values for the next pointer and base pointer of ROM bank 0 are 0x200 and 0x000, respectively. This means that a system reset automatically defines ROM bank 0 as a 32-Mbyte space with a start address of zero. This initial definition of ROM bank 0 lets the system power-on or reset operation pass control to the user-supplied boot code that is stored in external ROM. (This code is located at address 0 in the system memory map.) When the boot code (i.e. ROM program) executes, it performs various system initialization tasks and reconfigures the system memory map according to the application’s actual external memory and device configuration.

The initial system memory map following system startup is shown in following:

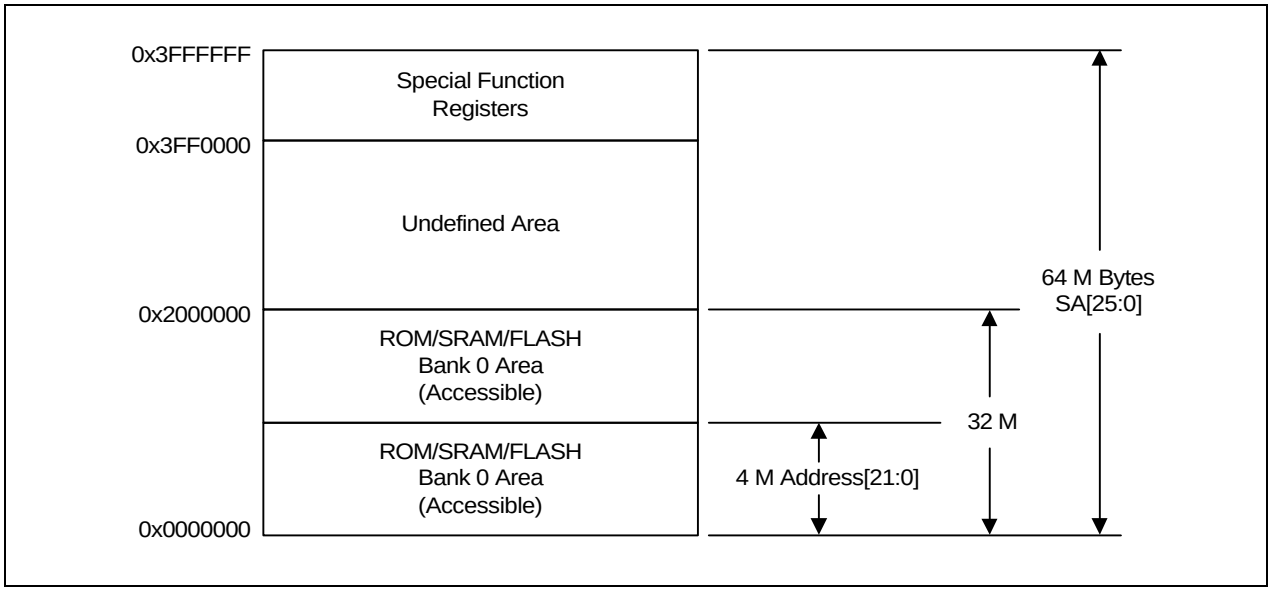

Figure 1-8. Initial System Memory Map (After Reset)

INSTRUCTION / DATA CACHE

The S5N8947 CPU has a unified internal 8-Kbyte instruction/data cache. The cache is configured using two-way, set-associative addressing. The replacement algorithm is pseudo-LRU (Least Recently Used). The cache line size is four words (16 bytes). When a miss occurs, four words must be fetched consecutively from external memory. Typically, RISC processors take advantage of unified instruction/data caches to improve performance.

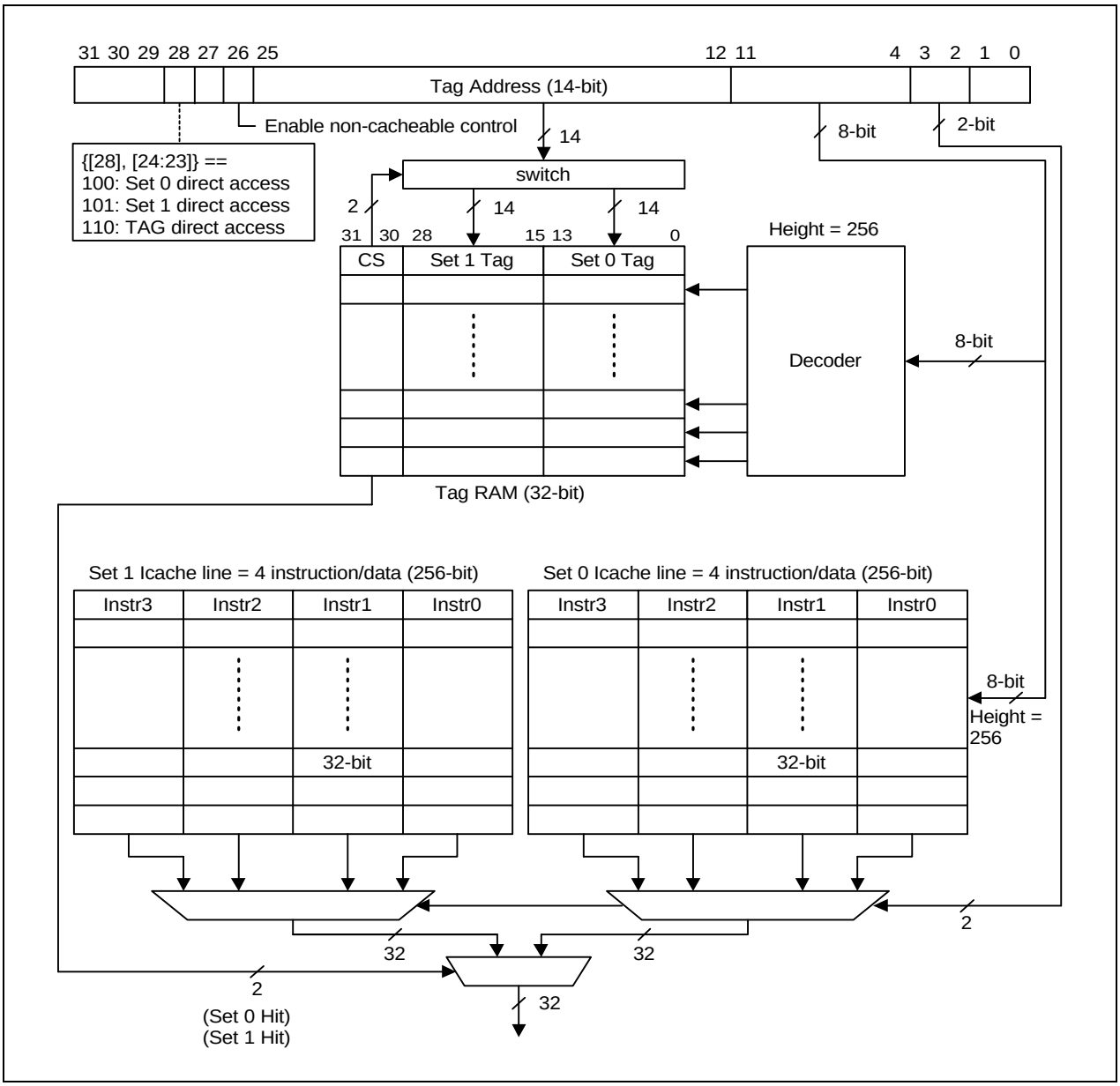

Figure 1-9. Memory Configuration for 8-Kbyte Cache

I²C BUS CONTROLLER

The S5N8947's Internal IC bus (I²C-bus) controller has the following important features:

— It requires only two bus lines, a serial data line (SDA) and a serial clock line (SCL). When the I²C-bus is free, both lines are High level.

— Each device that is connected to the bus is software-addressable by a unique address. Slave relationships on the bus are constant. The bus master can be either a master-transmitter or a master-receiver. The I²C bus controller supports only single master mode.

— It supports 8-bit, bi-directional, serial data transfers.

— The number of ICs that you can connect to the same I²C-bus is limited only by the maximum bus capacitance of 400 pF.

Following figure shows a block diagram of the S5N8947's I²C-bus controller.

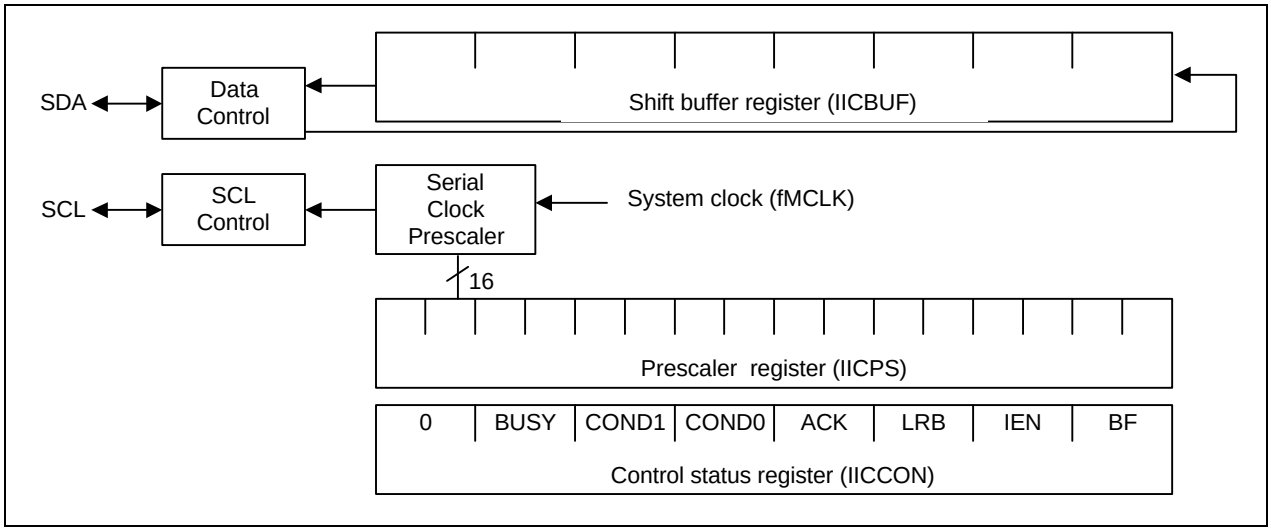

Figure 1-10. I²C-Bus Block Diagram

ETHERNET CONTROLLER

The S5N8947 has 2-channel Ethernet controllers which operate at either 100/10-Mbits per second in half-duplex or full-duplex mode. In half-duplex mode, the controller supports the IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. In full-duplex mode, it supports the IEEE 802.3 MAC Control Layer, including the Pause operation for flow control.

Block Diagram

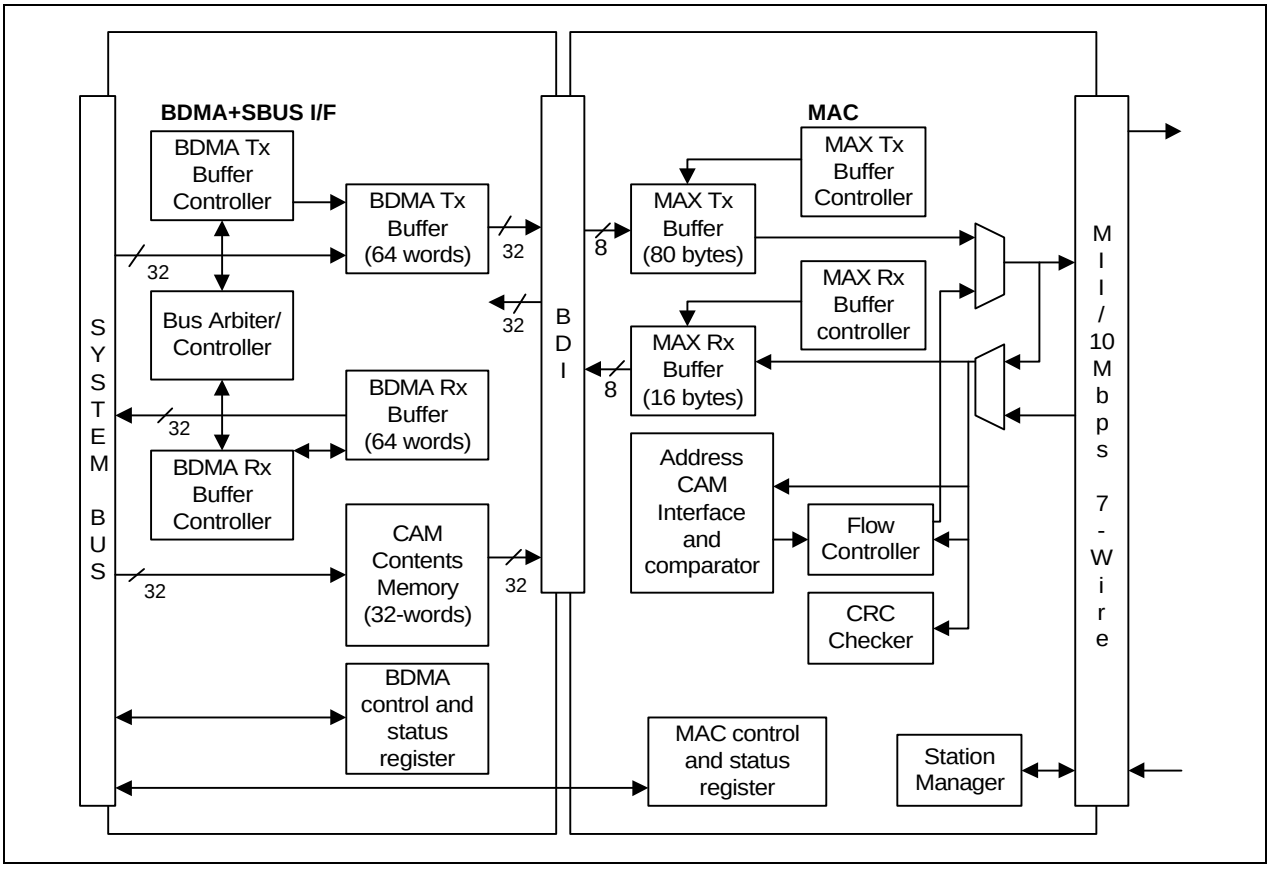

Figure 1-11. Ethernet Controller Block Diagram

Features and Benefits

The most important features and benefits of the S5N8947 Ethernet controller are as follows:

— Cost-effective connection to an external Repeater Interface Controller(RIC)/Ethernet backbone
— Buffered DMA (BDMA) engine using Burst mode
— BDMA Tx/Rx buffers (256 bytes/256 bytes)
— MAC Tx/Rx FIFOs (80 bytes/16 bytes) to support re-transmit after collision without DMA request and to handle DMA latency
— Data alignment logic
— Supports for old and new media (compatible with existing 10-Mbit/s networks)
— Full IEEE 802.3 compatibility for existing applications
— Provides a standard Media Independent Interface (MII)
— Provides an external 7-wire interface, also.
— Station Management (STA) signaling for external physical layer configuration and link negotiation
— On-chip CAM (21 addresses)
— Full-duplex mode for doubled bandwidth
— Pause operation hardware support for full-duplex flow control
— Long packet mode for specialized environments
— Short packet mode for fast testing
— PAD generation for ease of processing and reduced processing time
— Support for old and new media: Compatible with existing 100/10Mbit/s networks.
— Full IEEE 802.3 compatibility: Compatible with existing hardware and software.
— Standard CSMA/CD, Full duplex capability at 100/10 Mbit/s: Increase in data throughput performance.

SAR AND UTOPIA INTERFACE

The S5N8947 provides ATM layer Segmentation and Reassembly (SAR) function over an 8bit UTOPIA interface. The S5N8947 delivers an integrated solution for performing the SAR tasks required to communicate over an ATM network. The device translates packet-based data into 53-byte ATM cells that are asynchronously mapped into various physical media. The S5N8947 can be effectively applied for equipment requiring an interface between packet-based data and ATM-based networks.

Block Diagram

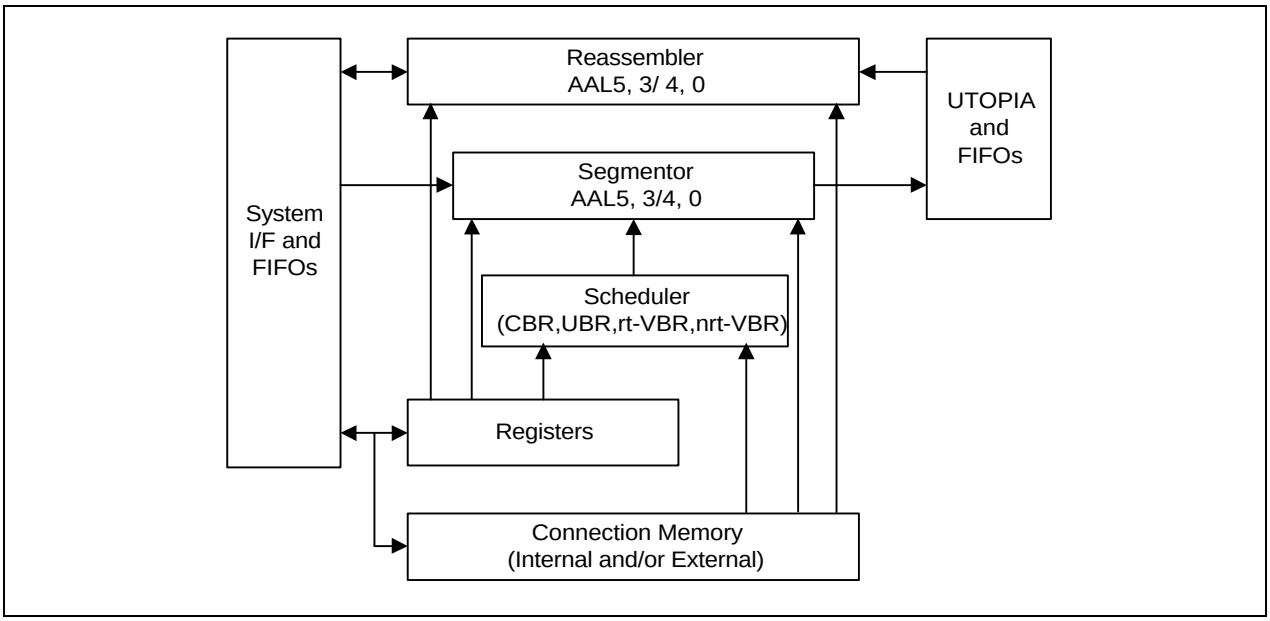

Figure 1-12. SAR Function Block Diagram

Features and Benefits

— Supports CBR, UBR, rt-VBR and nrt-VBR traffic with rates set on a per-VC or per-VP basis.

— Supports AAL0 (raw cells) and AAL5 segmentation and reassembly.

— Segments and reassembles data up to about 70Mbps via UTOPIA interface.

— Generates and verifies CRC-10 for OAM cells and AAL3/4 cells.

— Supports concurrent OAM cells and AAL5 cells on each active connection.

— Supports simultaneous segmentation and reassembly of up to 32 connections with internal connection memory and up to 4K connections with external system memory.

— On chip 8Kbytes SRAM for internal connection memory.

— Supports Contents Addressable Memory (CAM) for channel mapping (up to 32 connections).

— Supports packet sizes up to 64Kbytes.

— Supports scatter and gather packet capability for large packets.

— Start of Packet offset available for ease of implementing bridging and routing between different protocols.

— Provides glue-less UTOPIA level 2 interface (up to 3 PHYs).

— Supports big and little endian.

USB CONTROLLER

The Universal Serial Bus (USB) is an industry standard bus architecture for computer peripheral attachment. The USB provides a single interface for easy, plug-and-play, hot-plug attachment of peripherals such as keyboard, mouse, speakers, printers, scanners, and communication devices. The USB allows simultaneous use of many different peripherals with a combined transfer rate of up to 12 Mbit/s.

The S5N8947 controller includes a highly flexible integrated USB peripheral controller that lets designers implement a variety of microcontroller-based USB peripheral devices for telephony, audio, or other high-end applications. The S5N8947 controller is intended for USB peripherals that use the full-speed signalling rate of 12 Mbit/s. The USB low-speed rate (1.5 Mbit/s) is not supported. An integrated USB transceiver is provided to minimize system device count and cost. The USB peripheral controller's features meet or exceed all of the USB device class resource requirements defined by the USB specification Version 1.0 and 1.1. Consult the USB specification for details about overall USB system design. The integrated USB peripheral controller provides a very efficient and easy-to-use interface, so that device software (or firmware) does not incur the overhead of managing low-level USB protocol requirements.

The USB peripheral controller hardware implements a number of USB standard commands directly; the rest can be implemented in device software. In addition, the USB peripheral controller provides a high degree of flexibility to help designers accommodate vendor- or device-class-specific commands, as well as any new features that might be added in future USB specifications.

Robust error detection and management features are provided so the device software can manage transfers in any number of ways as required by the application. The USB suspend/resume, reset, and remote wake up features are also supported.

Block Diagram

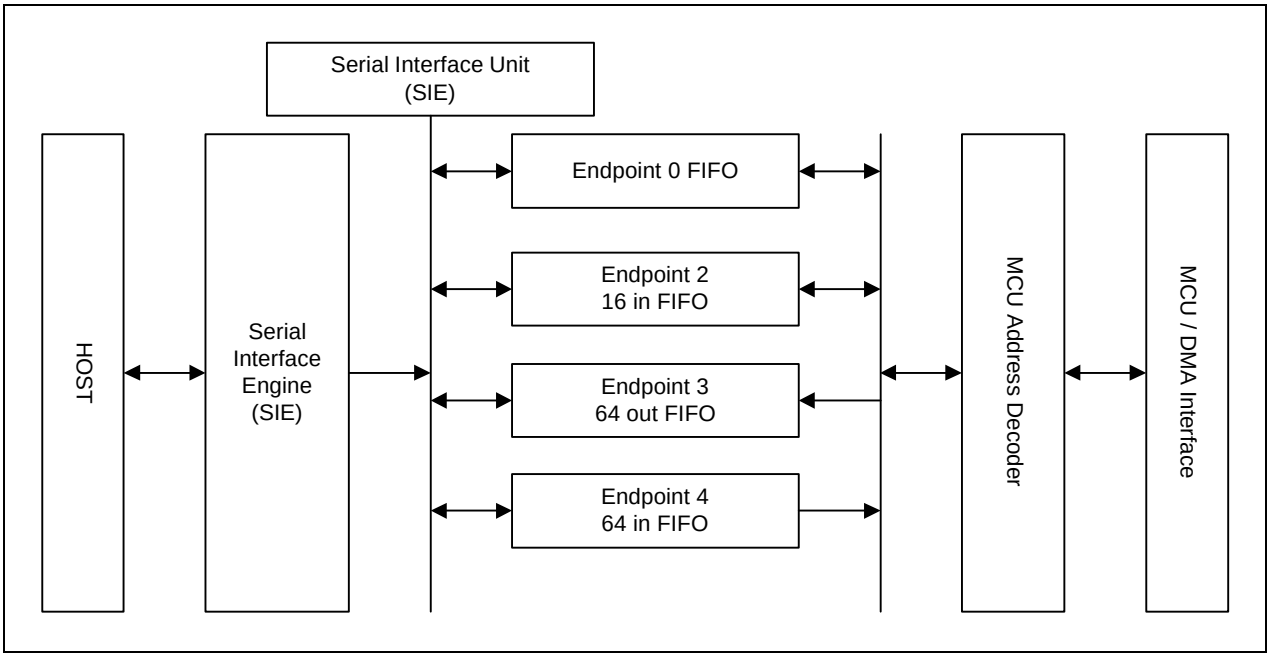

Figure 1-13. USB Module Block Diagram

DMA CONTROLLER

The S5N8947 has a two-channel general DMA controller, called the GDMA. The two-channel GDMA performs the following data transfers without CPU intervention:

— Memory-to-memory (memory to/from memory)

— UART-to-memory (serial port to/from memory)

— SPI-to-memory (SPI port to/from memory)

The on-chip GDMA can be started by software and/or by an external DMA request (nXDREQ). Software can also be used to restart a GDMA operation after it has been stopped.

The CPU can recognize when a GDMA operation has been completed by software polling and/or when it receives an appropriate internally generated GDMA interrupt. The S5N8947 GDMA controller can increment or decrement source or destination addresses and conduct 8-bit (byte), 16-bit (half-word), or 32-bit (word) data transfers.

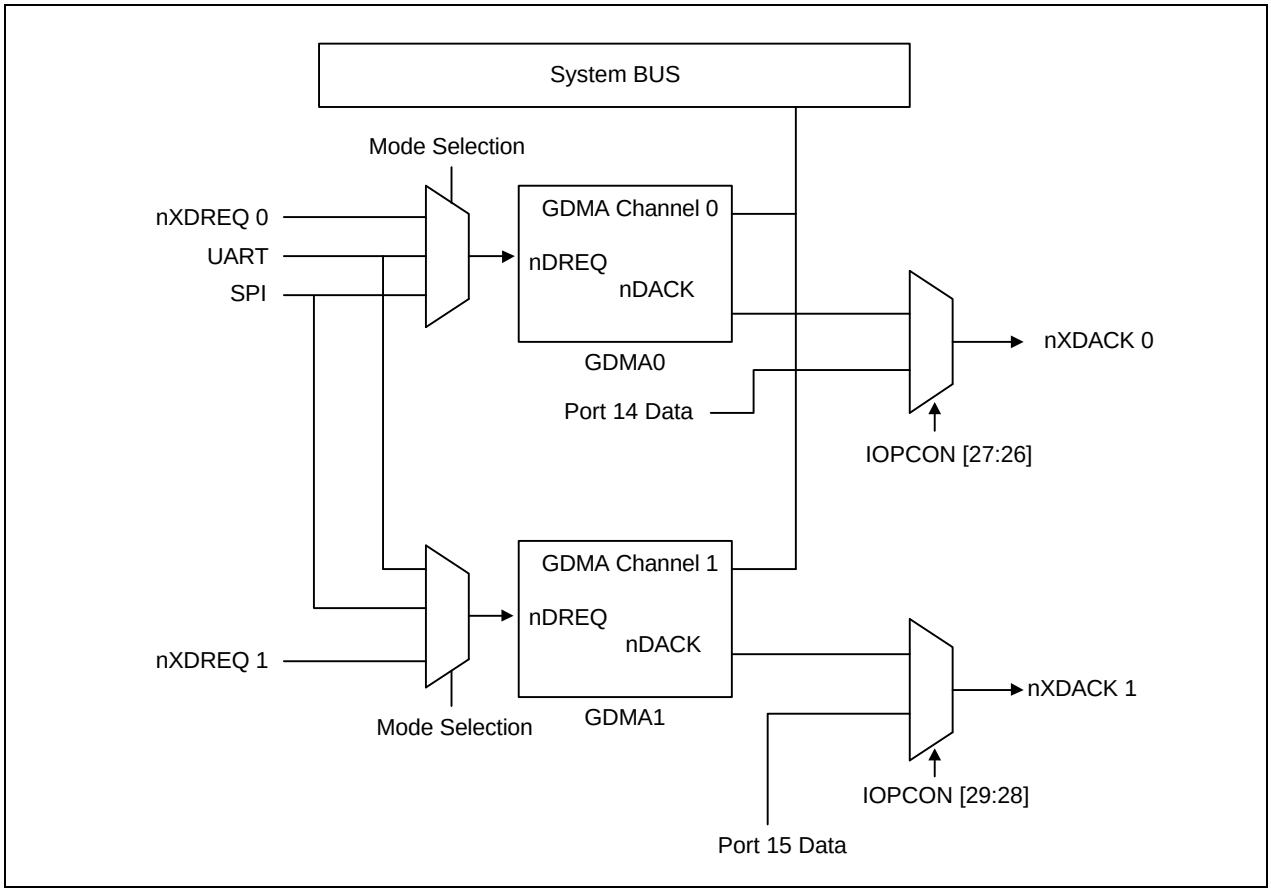

Figure 1-14. GDMA Controller Block Diagram

UART

The S5N8947 Universal Asynchronous Receiver/Transmitter (UART) unit provides an asynchronous serial I/O (SIO) port. This can operate in interrupt-based or DMA-based mode. That is, the UART can generate internal interrupts or DMA requests to transfer data between the CPU and the serial I/O port.

The most important features of the S5N8947 UART include:

— Programmable baud rates

— Infra-red (IR) transmit/receive

— Insertion of one or two Stop bits per frame

— Selectable 5-bit, 6-bit, 7-bit, or 8-bit data transfers

— Parity checking

This unit has a baud rate generator, transmitter, receiver, and a control unit, as shown in next figure. The baud-rate generator can be driven by the internal system clock, MCLK. The transmitter and receiver block use this baud rate clock and have independent data buffer registers and data shifters.

Transmit data is written first to the transmit buffer register. From there, it is copied to the transmit shifter and then shifted out by the transmit data pin, UATXDn. Receive data is shifted in by the receive data pin, UARXDn. It is then copied from the shifter to the receive buffer register when one data byte has been received.

This unit provides software controls for mode selection, and for status and interrupt generation.

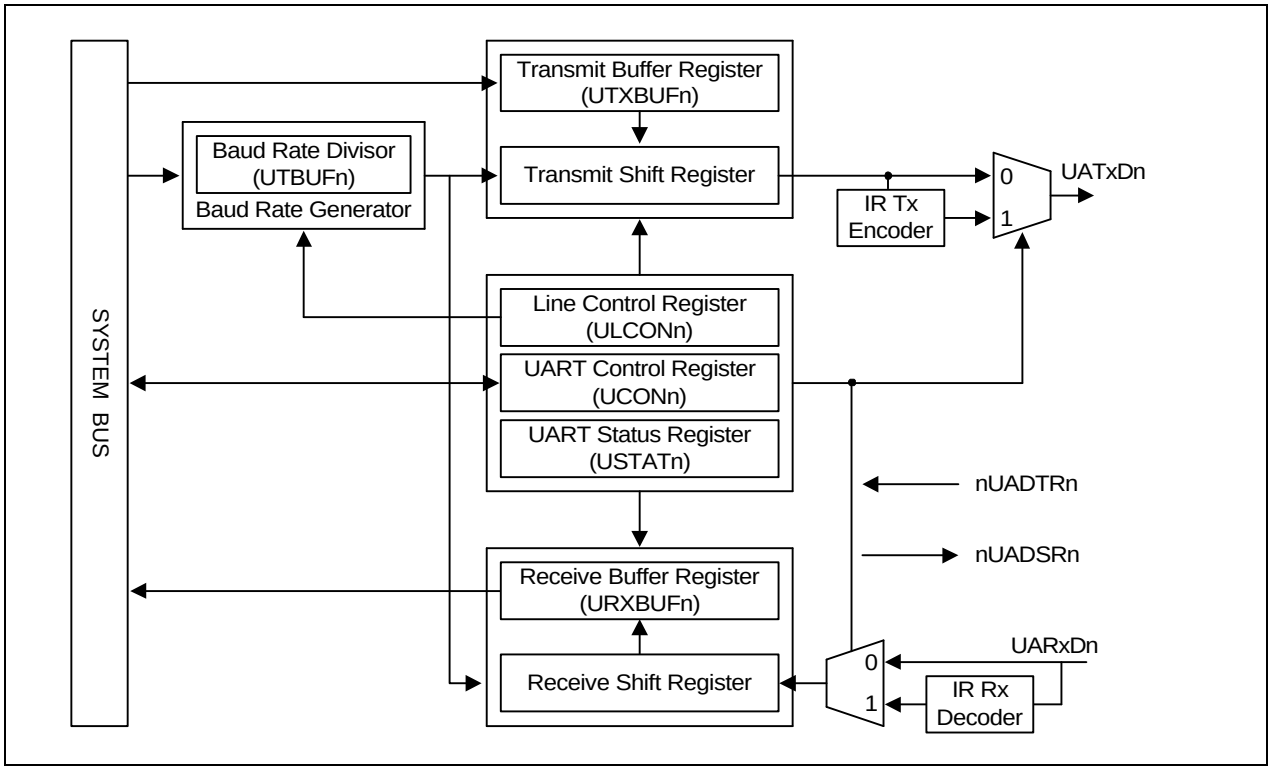

Figure 1-15. UART Block Diagram

TIMERS

The S5N8947 has three 32-bit timers. These timers can operate in interval mode or in toggle mode. The output signals are TOUT0 and TOUT1, respectively.

You enable or disable the timers by setting control bits in the timer mode register, TMOD. An interrupt request is generated whenever a timer count-out (down count) occurs.

Watchdog timer is also implemented in the S5N8947. The following guidelines apply to watchdog timer functions:

— When a watchdog timer is enabled, it loads a data value to its count register and begins decrementing the count register value by the system clock.

— If the reset from the watchdog timer (WDRESET) reaches to zero, the Watchdog will start its reset sequence. The reset value is then reloaded and the watchdog timer is disabled.

— The WDRESET performs the same function as the External Reset (System Reset) to each block.

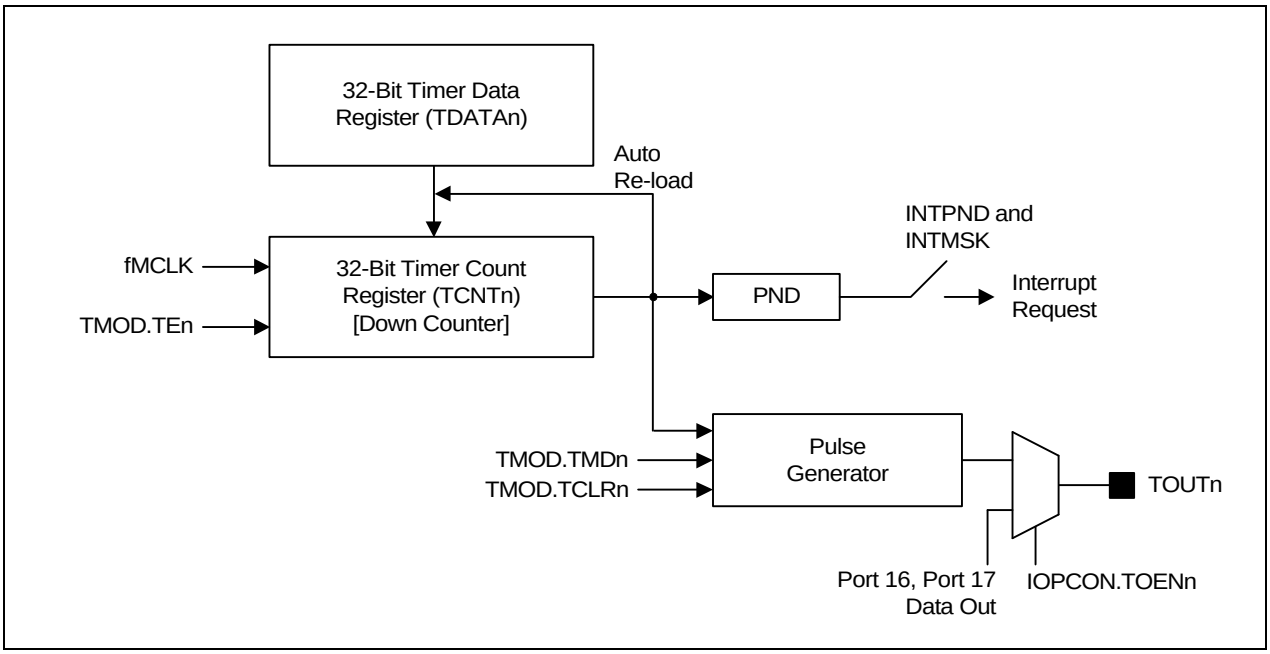

Figure 1-16. 32-Bit Timer Block Diagram

I/O PORTS

The S5N8947 has 18 programmable I/O ports. You can configure each I/O port to input mode, output mode, or special function mode. To do this, you write the appropriate settings to the IOPMOD, IOPCON0 and IOPCON1 registers. User can set filtering for the input ports using IOPCON0/1 register.

Port[0] can be used as nCE1 for PCMCIA interface or SPICLK, port[1] as nCE2 for PCMCIA interface or SPIMOSI, port[2] as nIOIS16 for PCMCIA interface or SPIMISO, port[3] as nALE for PCMCIA interface, port[4] as RW(external data transceiver direction) for PCMCIA interface, or port[7:5] as xINTREQ[2:0] depending on the settings in IOPCON0 register. And port[11:8] can be used as xINTREQ[6:3], port[13:12] as nXDREQ[1:0], port[15:14] as nXDACK[1:0], port[16] as TOUT0, or port[17] as TOUT1 depending on the settings in IOPCON1 register.

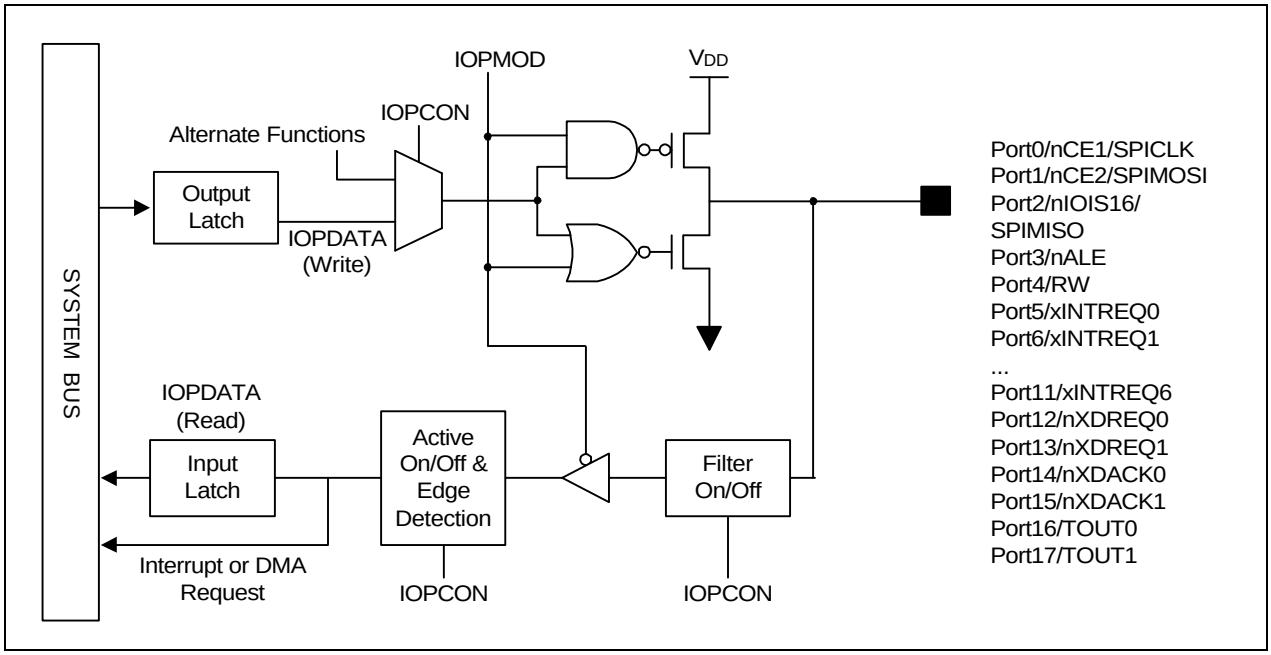

Figure 1-17. I/O Port Function Diagram

INTERRUPT CONTROLLER

The S5N8947 interrupt controller has a total of 23 interrupt sources. Interrupt requests can be generated by internal function blocks and external pins.

The ARM7TDMI core recongnizes two kinds of interrupts: a normal interrupt request (IRQ), and a fast interrupt request (FIQ). Therefore all S5N8947 interrupts can be categorized as either IRQ or FIQ. The S5N8947 interrupt controller has an interrupt pending bit for each interrupt source.

Four special registers are used to control interrupt generation and handling:

— Interrupt priority registers. The index number of each interrupt source is written to the pre-defined interrupt priority register field to obtain that priority. The interrupt priorities are pre-defined from 0 to 22.

— Interrupt mode register. Defines the interrupt mode, IRQ or FIQ, for each interrupt source.

— Interrupt pending register. Indicates that an interrupt request is pending. If the pending bit is set, the interrupt pending status is maintained until the CPU clears it by writing a "1" to the appropriate pending register. When the pending bit is set, the interrupt service routine starts whenever the interrupt mask register is "0". The service routine must clear the pending condition by writing a "1" to the appropriate pending bit. This avoids the possibility of continuous interrupt requests from the same interrupt pending bit.

— Interrupt mask register. Indicates that the current interrupt has been disabled if the corresponding mask bit is "1". If an interrupt mask bit is "0" the interrupt will be serviced normally. If the global mask bit (bit 23) is set to "1", no interrupts are serviced. However, the source's pending bit is set if the interrupt is generated. When the global mask bit has been set to "0", the interrupt is serviced.

Table 1-4. S5N8947 Interrupt Sources

Index Values	Interrupt Sources
[22]	SPI interrupt
[21]	I^2C-bus interrupt
[20]	Ethernet controller 1 Rx interrupt
[19]	Ethernet controller 1 Tx interrupt
[18]	Ethernet controller 0 Rx interrupt
[17]	Ethernet controller 0 Tx interrupt
[16]	SAR Tx/Rx done interrupt
[15]	SAR Tx/Rx error interrupt
[14]	USB interrupt
[13]	GDMA channel 1 interrupt
[12]	GDMA channel 0 interrupt
[11]	Timer 2 interrupt
[10]	Timer 1 interrupt
[9]	Timer 0 interrupt
[8]	UART receive and error interrupt
[7]	UART transmit interrupt
[6]	External interrupt 6
[5]	External interrupt 5
[4]	External interrupt 4
[3]	External interrupt 3
[2]	External interrupt 2
[1]	External interrupt 1
[0]	External interrupt 0

SPI

The S5N8947 provides a Serial Peripheral Interface (SPI), which is used for register access of other devices, EEPROM and A/D converter. The S5N8947 SPI is full duplex, synchrounous channel and it consists of four signal, receive serial data, transmit serial data, clock and select. Inner clock generator create SPI clock and SPI signals are synchronized with this clock.

SPI can be operated with the help of GDMA. So multiple characters can be transmitted and received without host intervention. Otherwise, the host should transmit and receive individual character back-to-back with polling method.

SPI does not operate in slave mode and it also cannot be used for multimaster environment. It works with data characters from 4 to 32 bits long. Clock phase and polarity can be configured.

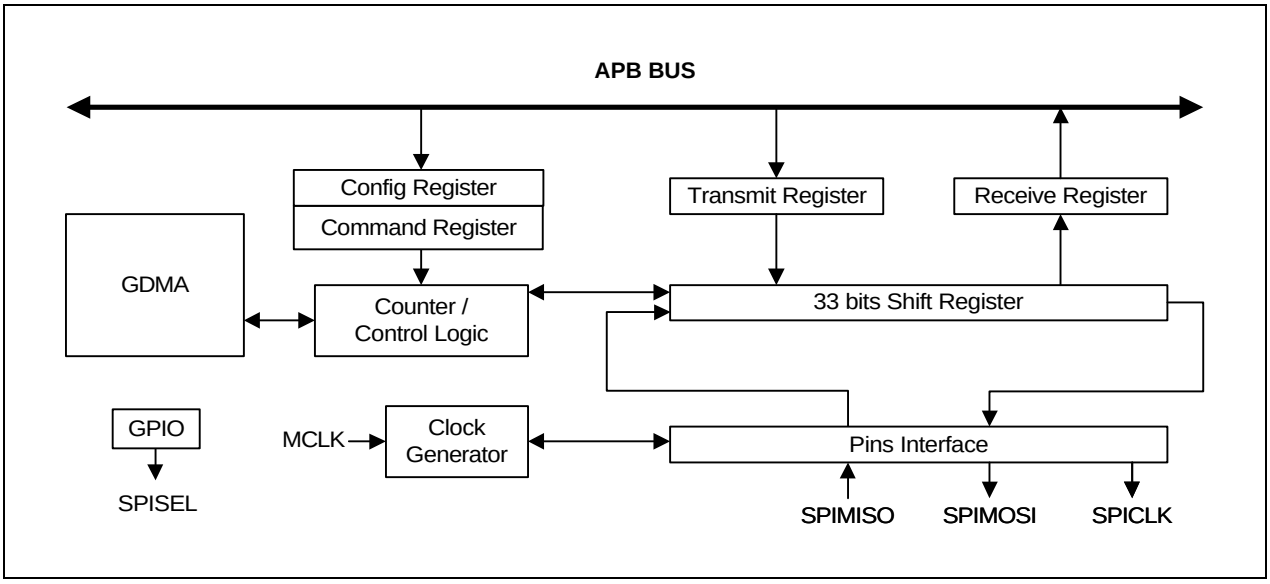

Figure 1-18. I/O Block Diagram of SPI (Serial Peripheral Interface)

SPECIAL FUNCTION REGISTERS

Table 1-5. Speclal Function Registers

Group	Registers	Offset	R/W	Description	Reset/Value
System Manager	SYSCFG	0x0000	R/W	System configuration register	0x23FF0000
	PCMCON	0x3000	R/W	PCMCIA Interface control register	0x80000000
	EXTACON0	0x3008	R/W	External I/O timing register 1	0x00000000
	EXTACON1	0x300C	R/W	External I/O timing register 2	0x00000000
	EXTDBWTH	0x3010	R/W	Data bus width for each memory bank	0x00000000
	ROMCON0	0x3014	R/W	ROM/SRAM/Flash bank 0 control register	0x20000060
	ROMCON1	0x3018	R/W	ROM/SRAM/Flash bank 1 control register	0x00000060
	ROMCON2	0x301C	R/W	ROM/SRAM/Flash bank 2 control register	0x00000060
	PCMOFFSET	0x3020	R/W	PCMCIA bank offset register	0x0000000
	DRAMCON0	0x3024	R/W	DRAM bank 0 control register	0x00000000
	DRAMCON1	0x3028	R/W	DRAM bank 1 control register	0x00000000
	DRAMCON2	0x302C	R/W	DRAM bank 2 control register	0x00000000
	DRAMCON3	0x3030	R/W	DRAM bank 3 control register	0x00000000
	REFEXTCON	0x3034	R/W	Refresh and external I/O control register	0x83FD0000
Ethernet1 (BDMA)	BDMATXCON	0x9000	R/W	Buffered DMA receive control register	0x00000000
	BDMARXCON	0x9004	R/W	Buffered DMA transmit control register	0x00000000
	BDMATXPTR	0x9008	R/W	Transmit trame descriptor start address	0x00000000
	BDMARXPTR	0x900C	R/W	Receive frame descriptor start address	0x00000000
	BDMARXLSZ	0x9010	R/W	Receive frame maximum size	Undefined
	BDMASTAT	0x9014	R/W	Buffered DMA status	0x00000000
	CAM	0x9100-0x917C	R/W	CAM content (32 words)	Undefined
	BDMATXBUF	0x9200-0x92FC	R/W	BDMA Tx buffer (64 words) for test mode addressing	Undefined
	BDMARXBUF	0x9800-0x99FC	R/W	BDMA Rx buffer (64 words) for test mode addressing	Undefined
Ethernet1 (MAC)	MACON	0xA000	R/W	Ethernet MAC control register	0x00000000
	CAMCON	0xA004	R/W	CAM control register	0x00000000
	MACTXCON	0xA008	R/W	MAC transmit control register	0x00000000
	MACTXSTAT	0xA00C	R/W	MAC transmit status register	0x00000000
	MACRXCON	0xA010	R/W	MAC receive control register	0x00000000
	MACRXSTAT	0xA014	R/W	MAC receive status register	0x00008000
	STADATA	0xA018	R/W	Station management data	0x00000000
	STACON	0xA01C	R/W	Station management control and address	0x00006000

Table 1-5. Speclal Function Registers (Continued)

Group	Registers	Offset	R/W	Description	Reset/Value
Ethernet1 (MAC)	CAMEN	0xA028	R/W	CAM enable register	0x00000000
	EMISSCNT	0xA03C	R/W	Missed error count register	0x00000000
	EPZCNT	0xA040	R	Pause count register	0x00000000
	ERMPZCNT	0xA044	R	Remote pause count register	0x00000000
	ETXSTAT	0x9040	R	Transmit control frame status	0x00000000
Ethernet2 (BDMA)	BDMATXCON	0xE000	R/W	Buffered DMA receive control register	0x00000000
	BDMARXCON	0xE004	R/W	Buffered DMA transmit control register	0x00000000
	BDMATXPTR	0xE008	R/W	Transmit trame descriptor start address	0x00000000
	BDMARXPTR	0xE00C	R/W	Receive frame descriptor start address	0x00000000
	BDMARXLSZ	0xE010	R/W	Receive frame maximum size	Undefined
	BDMASTAT	0xE014	R/W	Buffered DMA status	0x00000000
	CAM	0xE100-0xE17C	R/W	CAM content (32 words)	Undefined
	BDMATXBUF	0xE200-0xE2FC	R/W	BDMA Tx buffer (64 words) for test mode addressing	Undefined
	BDMARXBUF	0xE800-0xE9FC	R/W	BDMA Rx buffer (64 words) for test mode addressing	Undefined
Ethernet2 (MAC)	MACON	0xF800	R/W	Ethernet MAC control register	0x00000000
	CAMCON	0xF804	R/W	CAM control register	0x00000000
	MACTXCON	0xF808	R/W	MAC transmit control register	0x00000000
	MACTXSTAT	0xF80C	R/W	MAC transmit status register	0x00000000
	MACRXCON	0xF810	R/W	MAC receive control register	0x00000000
	MACRXSTAT	0xF814	R/W	MAC receive status register	0x00008000
	STADATA	0xF818	R/W	Station management data	0x00000000
	STACON	0xF81C	R/W	Station management control and address	0x00006000
	CAMEN	0xF828	R/W	CAM enable register	0x00000000
	EMISSCNT	0xF83C	R/W	Missed error count register	0x00000000
	EPZCNT	0xF840	R	Pause count register	0x00000000
	ERMPZCNT	0xF844	R	Remote pause count register	0x00000000
	ETXSTAT	0xE040	R	Transmit control frame status	0x00000000

Table 1-5. Speclal Function Registers (Continued)

Group	Registers	Offset	R/W	Description	Reset/Value
USB	FA	0x7000	R/W	Function address register	0x00000000
	PM	0x7004	R/W	Power/System management register	0x00000000
	INT	0x7008	R/W	Interrupt register	0x00000000
	INTE	0x700C	R/W	Interrupt Enable register	0x0000041F
	FN	0x7010	R	Frame Number register	0x00000000
	DFMR	0x705C	R/W	Direct FIFO access mode register	0x00000000
	DFA	0x7060	R/W	Direct FIFO access address register	0x00000000
	DFD	0x7064	R/W	Direct FIFO access data register	0x00000000
	E0SC	0x7014	R/W	Endpoint 0 Status Control register	0x00005080
	E0SA	0x7018	R/W	Endpoint 0 DMA Start Address register	0x00000000
	E0XDS	0x701C	R/W	Endpoint 0 Receive/Transmit Data Size register	0x00000000
	E0LDS	0x7020	R/W	Endpoint 0 Limit Data Size register	0x00800000
	E2SC	0x7034	R/W	Endpoint 2 Status Control register	0x00005080
	E2SA	0x7038	R/W	Endpoint 2 DMA Start Address register	0x00000000
	E2TDS	0x703C	R/W	Endpoint 2 Transmit Data Size register	0x00000000
	E3SC	0x7040	R/W	Endpoint 3 Status Control register	0x00000004
	E3SA	0x7044	R/W	Endpoint 3 DMA Start Address register	0x00000000
	E3RDS	0x7048	R/W	Endpoint 3 Transmit Data Size register	0x00000000
	E4SC	0x7050	R/W	Endpoint 4 Status Control register	0x00005080
	E4SA	0x7054	R/W	Endpoint 4 DMA Start Address register	0x00000000
	E4TDS	0x7058	R/W	Endpoint 4 Transmit Data Size register	0x00000000
SAR	SW_RESET	0x8000	R/W	Software reset register	0x00000000
	GLOBAL_MODE	0x8008	R/W	Global mode register	0x00000000
	TIMEOUT_BASE	0x800C	R/W	Base multiple for receive packet timeout register	0x00FF7FFF
	TX_READY1	0x8010	R/W	Transmit ready first packet or subpacket address	0x00000000
	TX_READY2	0x8014	R/W	Transmit ready last packet or subpacket address	0x00000000
	TX_DONE_ADDR	0x8018	R/W	Transmit packet done queue base address register	0x00000000
	TX_DONE_SIZE	0x801C	R/W	Transmit packet done queue size register	0x00C00000
	RX_POOL0_ADDR	0x8020	R/W	Receive queue 0 base address register	0x00000000

Table 1-5. Speclal Function Registers (Continued)

Group	Registers	Offset	R/W	Description	Reset/Value
SAR	RX_POOL0_SIZE	0x8024	R/W	Receive queue 0 size register	0x00C00000
	RX_POOL1_ADDR	0x8028	R/W	Receive queue 1 base address register	0x00000000
	RX_POOL1_SIZE	0x802C	R/W	Receive queue 1 size register	0x00C00000
	RX_POOL2_ADDR	0x8030	R/W	Receive queue 2 base address register	0x00000000
	RX_POOL2_SIZE	0x8034	R/W	Receive queue 2 size register	0x00C00000
	RX_POOL3_ADDR	0x8038	R/W	Receive queue 3 base address register	0x00000000
	RX_POOL3_SIZE	0x803C	R/W	Receive queue 3 size register	0x00C00000
	RX_DONE0_ADDR	0x8040	R/W	Receive packet done queue 0 base address register	0x00000000
	RX_DONE0_SIZE	0x8044	R/W	Receive packet done queue 0 size register	0x00C00000
	RX_DONE1_ADDR	0x8048	R/W	Receive packet done queue 1 base address register	0x00000000
	RX_DONE1_SIZE	0x804C	R/W	Receive packet done queue 1 size register	0x00C00000
	UTOPIA_CONFIG	0x8050	R/W	UTOPIA interface configuration register	0x00C00000
	UTOPIA_TIMEOUT	0x8054	R/W	UTOPIA interface timeout register	0xFFFFFFFF
	CLOCK_RATIO	0x8064	R/W	Ratio of SAR clock freq toUNI interface speed	0x0000008E
	DONE_INT_MASK	0x8070	R/W	Interrupt mask for done interrupt register	0xFFFFFFFF
	ERR_INT_MASK	0x8074	R/W	Interrupt mask for error interrupt register	0xFFFFFFFF
	DONE_INT_STAT	0x8078	R/W	Interrupt status for done interrupt register	0x00000000
	ERR_INT_STAT	0x807C	R/W	Interrupt status for error interrupt register	0x00000000
	1/R_LOOKUP_TBL	0x8080	R/W	Base address of 1/Rate lookup table	0x00000000
	VP_LOOKUP_TBL	0x8084	R/W	Base address of VP lookup table	0x00200000
	UBR_SCH_TBL	0x8088	R/W	Base address and entry number of UBR schedule	0x0030007F
	CBR_SCH_TBL	0x808C	R/W	Base address and entry number of CBR schedule	0x0038007F
	CELL_BUFF	0x8090	R/W	Base address and entry number of cell buffer	0x0040000F
	SCH_CONN_TBL	0x8094	R/W	Base address and entry number of scheduler connection table	0x0050001F
	AAL_CONN_TBL	0x8098	R/W	Base address and entry number of AAL connection table	0x0060001F
	SAR_CONN_TBL	0x809C	R/W	Base address and entry number of SAR connection table	0x00700000
	CAM_VPVC/CN	0x8100-0x81FC	R/W	CAM VPCI, VCI and connection number register	0x00000000

Table 1-5. Speclal Function Registers (Continued)

Group	Registers	Offset	R/W	Description	Reset/Value
SAR	CONFIGURATION	0x8200	R/W	Clock control and connection memory configuration register	0x00000046
	EXT_CMBASE	0x8204	R/W	External connection memory base address register	0x00000000
I/O Ports	IOPMOD	0x5000	R/W	I/O port mode register	0x00000000
	IOPCON0	0x5004	R/W	I/O port control 0 register	0x00000000
	IOPCON1	0x5008	R/W	I/O port control 1 register	0x00000000
	IOPDATA	0x500C	R/W	I/O port data register	Undefined
SPI	SPICFG	0x5804	R/W	SPI configuration register	0x0000000F
	SPISTS	0x5808	R	SPI status register	0x00000000
	SPICMD	0x580C	R/W	SPI command register	0x00000000
	TXCHR	0x5810	R/W	SPI transmit register	0x00000000
	RXCHR	0x5814	R	SPI receive register	0x00000000
Interrupt Controller	INTMOD	0x4000	R/W	Interrupt mode register	0x00000000
	INTPND	0x4004	R/W	Interrupt pending register	0x00000000
	INTMSK	0x4008	R/W	Interrupt mask register	0x00FFFFFF
	INTPRI0	0x400C	R/W	Interrupt priority register 0	0x03020100
	INTPRI1	0x4010	R/W	Interrupt priority register 1	0x07060504
	INTPRI2	0x4014	R/W	Interrupt priority register 2	0x0B0A0908
	INTPRI3	0x4018	R/W	Interrupt priority register 3	0x0F0E0D0C
	INTPRI4	0x401C	R/W	Interrupt priority register 4	0x13121110
	INTPRI5	0x4020	R/W	Interrupt priority register 5	0x00161514
	INTOFFSET	0x4024	R	Interrupt offset address register	0x0000005C
	INTPNDPRI	0x4028	R	Interrupt pending priority register	0x00000000
	INTPNDTST	0x402C	W	Interrupt pending test register	0x00000000
	INTOSET_FIQ	0x4030	R	FIQ interrupt offset register	0x0000005C
	INTOSET_IRQ	0x4034	R	IRQ interrupt offset register	0x0000005C
I ^{2}C Bus	IICCON	0XF000	R/W	I^{2}C bus control status register	0x00000000
	IICBUF	0xF004	R/W	I^{2}C bus shift buffer register	Undefined
	IICPS	0xF008	R/W	I^{2}C bus prescaler register	0x00000000
	IICCOUNT	0xF00C	R	I^{2}C bus prescaler counter register	0x00000000

Table 1-5. Speclal Function Registers (Continued)

Group	Registers	Offset	R/W	Description	Reset/Value
GDMA	GDMACON0	0xB000	R/W	GDMA channel 0 control register	0x00000000
	GDMACON1	0xC000	R/W	GDMA channel 1 control register	0x00000000
	GDMASRC0	0xB004	R/W	GDMA source address register 0	Undefined
	GDMADST0	0xB008	R/W	GDMA destination address register 0	Undefined
	GDMASRC1	0xC004	R/W	GDMA source address register 1	Undefined
	GDMADST1	0xC008	R/W	GDMA destination address register 1	Undefined
	GDMACNT0	0xB00C	R/W	GDMA channel 0 transfer count register	Undefined
	GDMACNT1	0xC00C	R/W	GDMA channel 1 transfer count register	Undefined
UART	ULCON	0xD000	R/W	UART line control register	0xXXXXXX00
	UCON	0xD004	R/W	UART control register	0xXXXXXX00
	USTAT	0xD008	R	UART status register	0xXXXXXXC0
	UTXBUF	0xD00C	W	UART transmit holding register	Undefined
	URXBUF	0xD010	R	UART receive buffer register	Undefined
	UBRDIV	0xD014	R/W	Baud rate divisor register	0xXXXXXX00
Timers	TMOD	0x6000	R/W	Timer mode register	0x00000000
	TDATA0	0x6004	R/W	Timer 0 data register	0x00000000
	TDATA1	0x6008	R/W	Timer 1 data register	0x00000000
	TDATA2	0x600C	R/W	Timer 2 data register	0x00000000
	TCNT0	0x6010	R/W	Timer 0 count register	0xFFFFFFFF
	TCNT1	0x6014	R/W	Timer 1 count register	0xFFFFFFFF
	TCNT2	0x6018	R/W	Timer 2 count register	0xFFFFFFFF
	WDCON	0x601C	R/W	Watchdog Timer Control register	0xFFFFFF00
	WDCNT	0x6020	R	Watchdog Timer Count register	0xFFFFFFFF

ELECTRIC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 1-6. Absolute Maximum Ratings

Parameter	Symbol	Rating		Units
Supply Voltage	V_{DD}	1.8V V_{DD}	2.7	V
		3.3V V_{DD}	3.8	
DC input Voltage	V_{IN}	1.8V input buffer	2.7	V
		1.8V interface 3.3V tolerant input buffer	3.8	
Operating Temperature	T_{OPR}	– 40 to 85		°C
Storage Temperature	T_{STG}	– 65 to 150		°C

RECOMMENDED OPERATING CONDITIONS

Table 1-7. Recommaended Operating Conditions

Parameter	Symbol	Rating		Units
Supply Voltage	V_{DD}/V_{DDA}	1.8V V_{DD}	1.8 ± 0.15	V
		3.3V V_{DD}	3.3 ± 0.3	
Oscillator Frequency	f_{OSC}	12		MHz
External Loop Filter Capacitance	L_F	320		pF
Industrial Temperature Range	T_A	-40 to 85		°C

Table 1-8. Power Dissipation

Parameter	Symbol	Min	Typ	Max	Units
Power Dissipation	P_D		300		mW

NOTE

It is strongly recommended that all the supply pins (V_{DD}/V_{DDA}) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Table 1-9. DC Electrical Characteristics

V_{DD} = 1.8 ± 0.15 V, V_{EXT} = 3.0 ± 0.3V, T_A = -40 to 85 °C (in case of 3.3V-tolerant I/O)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	LVCMOS I/F	V_{IH}	–	1.27	–	–	V
Low level input voltage	LVCMOS I/F	V_{IL}	–	–	–	0.57	V
Switching threshold		V_T	LVCMOS	–	$0.55V_{DD}$	–	V
Schmitt trigger positive-going threshold		V_{T+}	LVCMOS	–	–	1.27	–
Schmitt trigger negative-going threshold		V_{T-}	LVCMOS	0.57	–	–	–
High level input current	Input buffer	I_{IH}	$V_{IN} = V_{DD}$	– 10	–	10	µA
	Input buffer with pull-up			5	18	40	
Low level input current	Input buffer	I_{LH}	$V_{IN} = V_{SS}$	– 10	–	10	µA
	Input buffer with pull-up			– 40	– 18	– 5	
High level output voltage	Type B1 to B12	V_{OH}	I_{OH} = – 1 mA	V_{DD} – 0.05	–	–	V
	Type B1		I_{OH} = – 1 mA	1.2			
	Type B2		I_{OH} = – 2 mA				
	Type B4		I_{OH} = – 4 mA				
	Type B6		I_{OH} = – 6 mA				
Low level output voltage	Type B1 to B12	V_{OL}	I_{OL} = 1 mA			0.05	V
	Type B1		I_{OL} = 1 mA			0.45	
	Type B2		I_{OL} = 2 mA				
	Type B4		I_{OL} = 4 mA				
	Type B6		I_{OL} = 6 mA				
Tri-state output leakage current		I_{OZ}	$V_{OUT} = V_{SS}$ or V_{DD}	– 10		10	µA
Operating current		I_{OP}	V_{DD} = 1.8V, fMCLK = 72MHz			100 ~ 150	mA

PACKAGE DIMENSION

This section describes the mechanical data for the S5N8947 208-pin LQFP package.

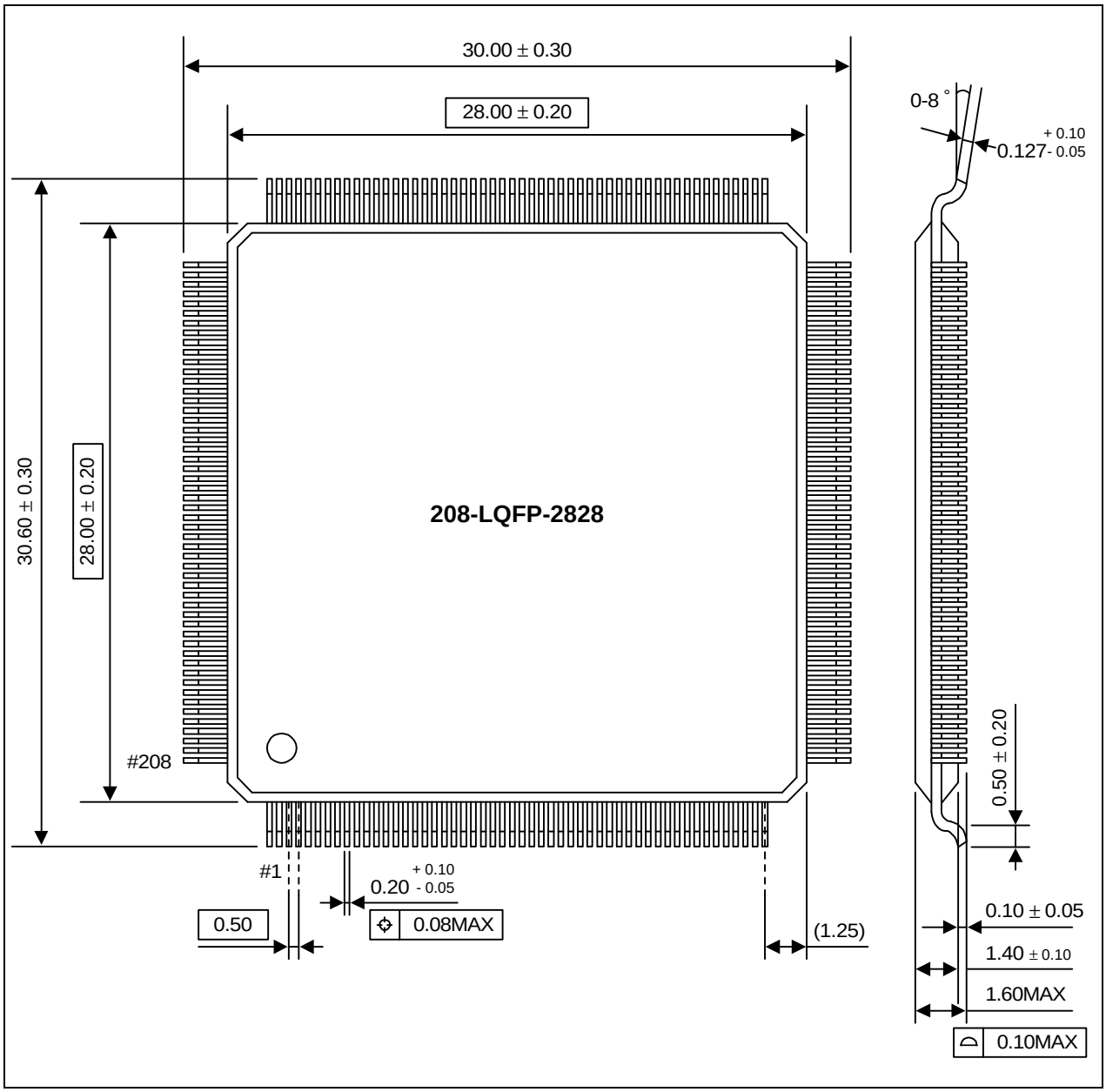

Figure 1-19. 208-LQFP-2828 Package Dimensions

SAMSUNG ELECTRONICS

INTRODUCTION

GENERAL DESCRIPTION

S5N8950 is an optimized chip of ADSL DMT transceiver supporting G.992.1, G.992.2 and T1.413, and provides a total ADSL DMT chipset solution with AFE chip (S5N8951) for both CO and CPE applications. It supports various interfaces of UTOPIA level 1 and 2 for ATM data, and serial interface for Non-ATM data, and host interface compatible with Motorola and Intel type processors. The S5N8950 is available as 176 LQPF-2424 package. It is fully compatible with G.Lite and G.dmt standards to satisfy interoperability with other chipsets. For CO or CPE application, evaluation tool kits are provided.

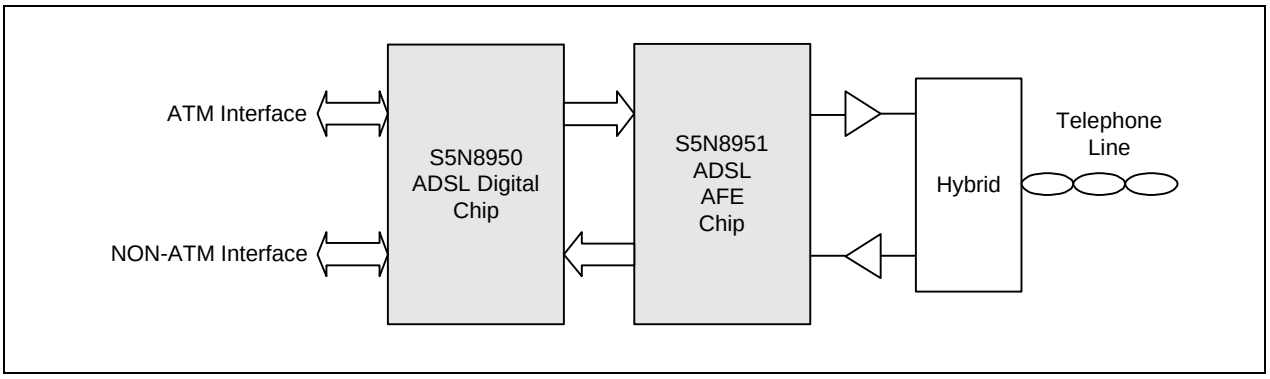

Figure 2-1. Samsung ADSL Solution Configuration

MAIN FEATURES

— Power and performance optimized single port DMT chip.
— Supports ITU-T G.992.1 (G.dmt), G.992.2 (G.Lite) and T1.413 Issue 2 standards.
— Same chip for both ATU-C and ATU-R.
— Supports STM serial interface, and ATM UTOPIA level 1 and level 2 interfaces.
— Flexible host interface for motorola and Intel type controller.
— 14 Bit ADC and DAC interface to AFE.
— Supports all of the framing modes.
— Dual latency paths: fast and interleaved.
— Reed-solomon forward error correction with interleaving.
— 3-D trellis coding and Viterbi algorithm.
— Supports rate adaptive mode.
— Adaptive frequency and time domain equalization.
— Downloadable coefficients of rate-conversion filter banks.
— Supports both the FDM-based and EC-based DMT line coding.
— 0.18 um 1.8 V CMOS technology.
— 3.3V external interface.
— Industrial operation temperature: -40°C to 85°C.
— 176 LQFP-2424.
— Low power consumption (less than 0.4W).
— Power management.
— ATU-C: DSLAM, Routers at CO.
— ATU-R: Routers at SOHO, stand-alone modems, PC mother boards, and so forth.

SIGNAL INFORMATION

This chapter provides the S5N8950 pin information, *e.g.*, pin configuration, assignment, and description. Figure 2 shows the logical pin configuration of S5N8950. Figure 3 shows the physical pin assignment of S5N8950. Table 1 shows the pin description of S5N8950 according to pin number, while Table 2 shows the I/O driver description of S5N8950. Table 3 summarizes the pin information in terms of interface.

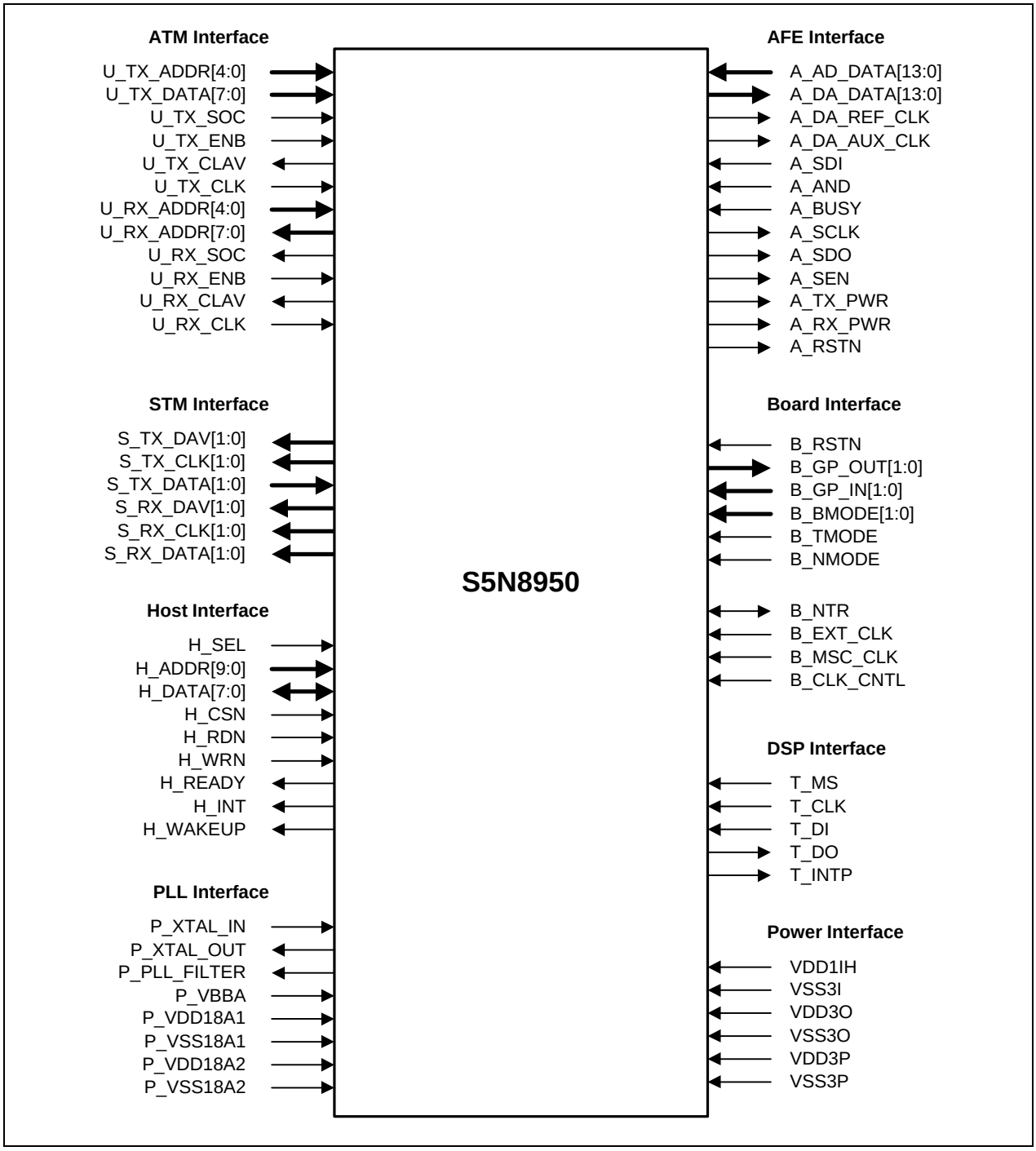

Figure 2-2. Logical Pin Configuration of S5N8950

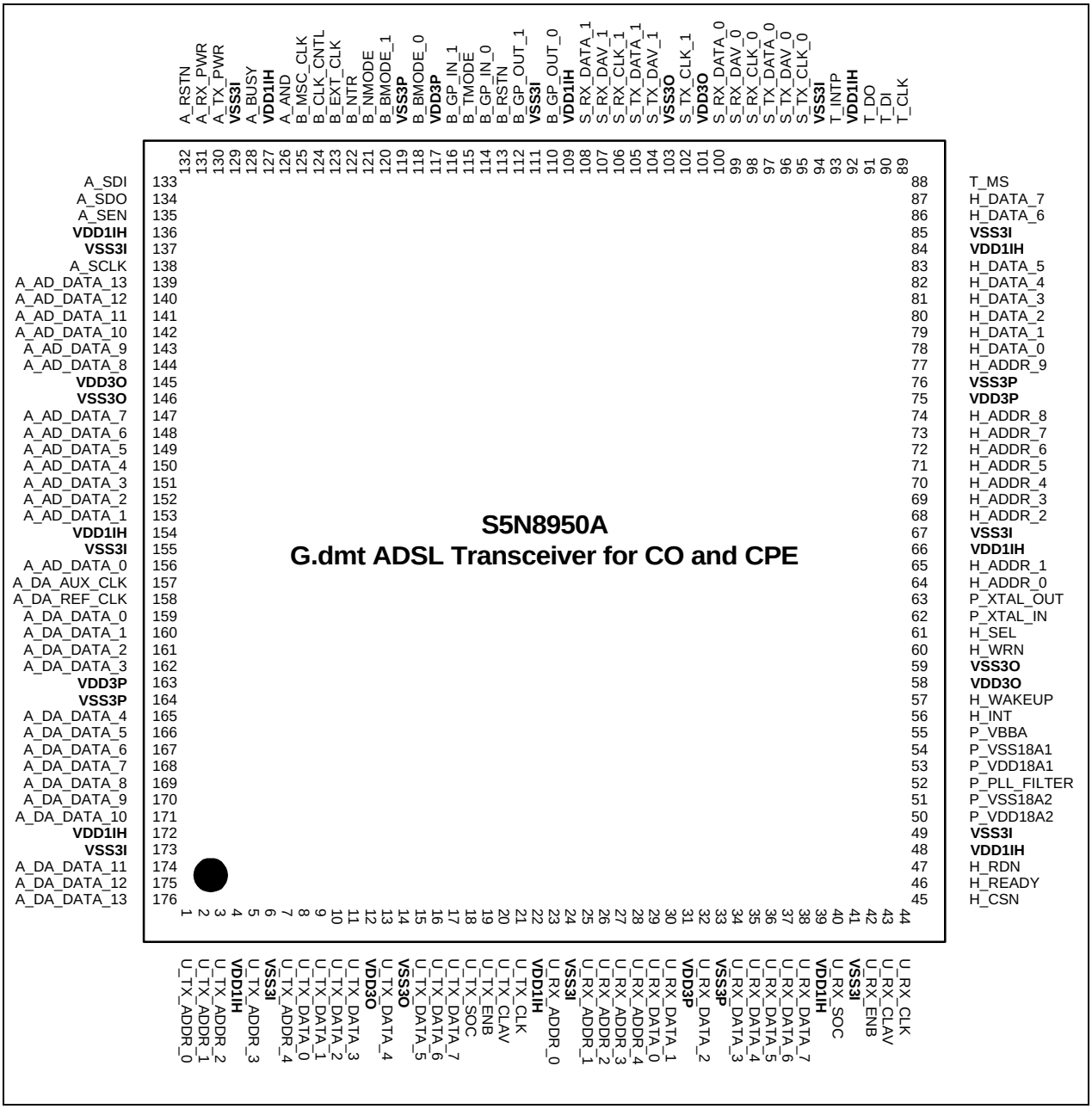

Figure 2-3. Pin Assignment of S5N8950

Table 2-1. Pin Description of S5N8950 According to Pin Number

Pin	Name	Type	Driver	Description
1	U_TX_ADDR_0	I	PHTICD	Utopia Tx address 0
2	U_TX_ADDR_1	I	PHTICD	Utopia Tx address 1
3	U_TX_ADDR_2	I	PHTICD	Utopia Tx address 2
4	VDD1IH	P	VDD1IH	1.8V internal power supply
5	U_TX_ADDR_3	I	PHTICD	Utopia Tx address 3
6	VSS3I	P	VSS3I	Ground
7	U_TX_ADDR_4	I	PHTICD	Utopia Tx address 4
8	U_TX_DATA_0	I	PHTICD	Utopia Tx data 0
9	U_TX_DATA_1	I	PHTICD	Utopia Tx data 1
10	U_TX_DATA_2	I	PHTICD	Utopia Tx data 2
11	U_TX_DATA_3	I	PHTICD	Utopia Tx data 3
12	VDD3O	P	VDD3O	3.3V pad power supply
13	U_TX_DATA_4	I	PHTICD	Utopia Tx data 4
14	VSS3O	P	VSS3O	Ground
15	U_TX_DATA_5	I	PHTICD	Utopia Tx data 5
16	U_TX_DATA_6	I	PHTICD	Utopia Tx data 6
17	U_TX_DATA_7	I	PHTICD	Utopia Tx data 7
18	U_TX_SOC	I	PHTICD	Utopia Tx start of cell
19	U_TX_ENB	I	PHTICD	Utopia Tx enable
20	U_TX_CLAV	OZ	PHTOT4	Utopia Tx cell available
21	U_TX_CLK	I	PHTICD	Utopia Tx clock
22	VDD1IH	P	VDD1IH	1.8V internal power supply
23	U_RX_ADDR_0	I	PHTICD	Utopia Rx address 0
24	VSS3I	P	VSS3I	Ground
25	U_RX_ADDR_1	I	PHTICD	Utopia Rx address 1
26	U_RX_ADDR_2	I	PHTICD	Utopia Rx address 2
27	U_RX_ADDR_3	I	PHTICD	Utopia Rx address 3
28	U_RX_ADDR_4	I	PHTICD	Utopia Rx address 4
29	U_RX_DATA_0	OZ	PHTOT4	Utopia Rx data 0
30	U_RX_DATA_1	OZ	PHTOT4	Utopia Rx data 1
31	VDD3P	P	VDD3P	3.3V pad power supply
32	U_RX_DATA_2	OZ	PHTOT4	Utopia Rx data 2
33	VSS3P	P	VSS3P	Ground
34	U_RX_DATA_3	OZ	PHTOT4	Utopia Rx data 3
35	U_RX_DATA_4	OZ	PHTOT4	Utopia Rx data 4

Table 2-1. Pin Description of S5N8950 According to Pin Number (Continued)

Pin	Name	Type	Driver	Description
36	U_RX_DATA_5	OZ	PHTOT4	Utopia Rx data 5
37	U_RX_DATA_6	OZ	PHTOT4	Utopia Rx data 6
38	U_RX_DATA_7	OZ	PHTOT4	Utopia Rx data 7
39	VDD1IH	P	VDD1IH	1.8V internal power supply
40	U_RX_SOC	OZ	PHTOT4	Utopia Rx start of cell
41	VSS3I	P	VSS3I	Ground
42	U_RX_ENB	I	PHTICD	Utopia Rx enable
43	U_RX_CLAV	OZ	PHTOT4	Utopia Rx cell available
44	U_RX_CLK	I	PHTICD	Utopia Rx clock
45	H_CSN	I	PHTICD	Chip selection
46	H_READY	OZ	PHTOT4	Host CPU Ready
47	H_RDN	I	PHTICD	Read enable
48	VDD1IH	P	VDD1IH	1.8V internal power supply
49	VSS3I	P	VSS3I	Ground
50	P_VDD18A2	I	VDD1T_ABB	1.8V analog power supply
51	P_VSS18A2	I	VSS1T_ABB	1.8V analog ground
52	P_PLL_FILTER	O	POAR50_ABB	PLL capacitor connected to filter
53	P_VDD18A1	I	VDD1T_ABB	1.8V analog power supply
54	P_VSS18A1	I	VSS1T_ABB	1.8V analog ground
55	P_VBBA	I	VBB1_ABB	Bulk ground
56	H_INT	O	PHTOT4	Host interrupt
57	H_WAKEUP	O	PHTOT4	Host wakeup
58	VDD3O	P	VDD3O	3.3V pad power supply
59	VSS3O	P	VSS3O	Ground
60	H_WRN	I	PHTICD	Host write enable
61	H_SEL	I	PHTICD	Host type
62	P_XTAL_IN	I	PHSOSCM26	XTAL input for clock
63	P_XTAL_OUT	O	PHSOSCM26	XTAL output for clock
64	H_ADDR_0	I	PHTICD	Host address bus 0
65	H_ADDR_1	I	PHTICD	Host address bus 1
66	VDD1IH	P	VDD1IH	1.8V internal power supply
67	VSS3I	P	VSS3I	Ground
68	H_ADDR_2	I	PHTICD	Host address bus 2
69	H_ADDR_3	I	PHTICD	Host address bus 3
70	H_ADDR_4	I	PHTICD	Host address bus 4

Table 2-1. Pin Description of S5N8950 According to Pin Number (Continued)

Pin	Name	Type	Driver	Description
71	H_ADDR_5	I	PHTICD	Host address bus 5
72	H_ADDR_6	I	PHTICD	Host address bus 6
73	H_ADDR_7	I	PHTICD	Host address bus 7
74	H_ADDR_8	I	PHTICD	Host address bus 8
75	VDD3P	P	VDD3P	3.3V pad power supply
76	VSS3P	P	VSS3P	Ground
77	H_ADDR_9	I	PHTICD	Host address bus 9
78	H_DATA_0	B	PHTBCDT6SM	Host data bus 0
79	H_DATA_1	B	PHTBCDT6SM	Host data bus 1
80	H_DATA_2	B	PHTBCDT6SM	Host data bus 2
81	H_DATA_3	B	PHTBCDT6SM	Host data bus 3
82	H_DATA_4	B	PHTBCDT6SM	Host data bus 4
83	H_DATA_5	B	PHTBCDT6SM	Host data bus 5
84	VDD1IH	P	VDD1IH	1.8V internal power supply
85	VSS3I	P	VSS3I	Ground
86	H_DATA_6	B	PHTBCDT6SM	Host data bus 6
87	H_DATA_7	B	PHTBCDT6SM	Host data bus 7
88	T_MS	I	PHTICD	TeakLite JTAG test mode select
89	T_CLK	I	PHTICD	TeakLite JTAG test clock
90	T_DI	I	PHTICD	TeakLite JTAG test input data
91	T_DO	OZ	PHTOT4	TeakLite JTAG test output data
92	VDD1IH	P	VDD1IH	1.8V internal power supply
93	T_INTP	O	PHTOT4	TeakLite TJAM interrupt to host
94	VSS3I	P	VSS3I	Ground
95	S_TX_CLK_0	O	PHTOT4	Serial Tx clock 0
96	S_TX_DAV_0	O	PHTOT4	Serial Tx data valid signal 0
97	S_TX_DATA_0	I	PHTICD	Serial Tx data 0
98	S_RX_CLK_0	O	PHTOT4	Serial Rx clock 0
99	S_RX_DAV_0	O	PHTOT4	Serial Rx data valid signal 0
100	S_RX_DATA_0	O	PHTOT4	Serial Rx data 0
101	VDD3O	P	VDD3O	3.3V pad power supply
102	S_TX_CLK_1	O	PHTOT4	Serial Tx clock 0
103	VSS3O	P	VSS3O	Ground
104	S_TX_DAV_1	O	PHTOT4	Serial Tx data valid signal 1
105	S_TX_DATA_1	I	PHTICD	Serial Tx data 1

Table 2-1. Pin Description of S5N8950 According to Pin Number (Continued)

Pin	Name	Type	Driver	Description
106	S_RX_CLK_1	O	PHTOT4	Serial Rx clock 1
107	S_RX_DAV_1	O	PHTOT4	Serial Rx data valid signal 1
108	S_RX_DATA_1	O	PHTOT4	Serial Rx data 1
109	VDD1IH	P	VDD1IH	1.8V internal power supply
110	B_GP_OUT_0	O	PHTOT4	General purpose output 0
111	VSS3I	P	VSS3I	Ground
112	B_GP_OUT_1	O	PHTOT4	General purpose output 1
113	B_RSTN	I	PHTISD	System reset
114	B_GP_IN_0	I	PHTICD	General purpose input 0
115	B_TMODE	I	PHTICD	Test Mode
116	B_GP_IN_1	I	PHTICD	General purpose input
117	VDD3P	P	VDD3P	3.3V pad power supply
118	B_BMODE_0	I	PHTICD	TeakLite boot mode selection
119	VSS3P	P	VSS3P	Ground
120	B_BMODE_1	I	PHTICD	TeakLite boot mode selection
121	B_NMODE	I	PHTICD	NAND tree test mode
122	B_NTR	B	PHTBCDT6SM	ATM Network Timing Reference
123	B_EXT_CLK	I	PHTICD	External clock
124	B_CLK_CNTL	I	PHTICD	Clock control signal
125	B_MSC_CLK	I	PHTICD	Misc. clock for BIRA test
126	A_AND	I	PHTICD	Audible noise detection
127	VDD1IH	P	VDD1IH	1.8V internal power supply
128	A_BUSY	I	PHTICD	AFE busy signal
129	VSS3I	P	VSS3I	Ground
130	A_TX_PWR	O	PHTOT4	TX line driver power enable
131	A_RX_PWR	O	PHTOT4	RX line driver power enable
132	A_RSTN	O	PHOB2	AFE reset
133	A_SDI	I	PHICD	AFE serial input data
134	A_SDO	O	PHOB2	AFE serial output data
135	A_SEN	O	PHOB2	AFE serial enable
136	VDD1IH	P	VDD1IH	1.8V internal power supply
137	VSS3I	P	VSS3I	Ground
138	A_SCLK	O	PHOB2	AFE serial clock
139	A_AD_DATA_13	I	PHICD	ADC data 13
140	A_AD_DATA_12	I	PHICD	ADC data 12

Table 2-1. Pin Description of S5N8950 According to Pin Number (Continued)

Pin	Name	Type	Driver	Description
141	A_AD_DATA_11	I	PHICD	ADC data 11
142	A_AD_DATA_10	I	PHICD	ADC data 10
143	A_AD_DATA_9	I	PHICD	ADC data 9
144	A_AD_DATA_8	I	PHICD	ADC data 8
145	VDD3O	P	VDD3O	3.3V pad power supply
146	VSS3O	P	VSS3O	Ground
147	A_AD_DATA_7	I	PHICD	ADC data 7
148	A_AD_DATA_6	I	PHICD	ADC data 6
149	A_AD_DATA_5	I	PHICD	ADC data 5
150	A_AD_DATA_4	I	PHICD	ADC data 4
151	A_AD_DATA_3	I	PHICD	ADC data 3
152	A_AD_DATA_2	I	PHICD	ADC data 2
153	A_AD_DATA_1	I	PHICD	ADC data 1
154	VDD1IH	P	VDD1IH	1.8V internal power supply
155	VSS3I	P	VSS3I	Ground
156	A_AD_DATA_0	I	PHICD	ADC data 0
157	A_DA_AUX_CLK	O	PHOB2	DAC data auxiliary clock
158	A_DA_REF_CLK	O	PHOB2	DAC data reference clock
159	A_DA_DATA_0	O	PHOB2	DAC data 0
160	A_DA_DATA_1	O	PHOB2	DAC data 1
161	A_DA_DATA_2	O	PHOB2	DAC data 2
162	A_DA_DATA_3	O	PHOB2	DAC data 3
163	VDD3P	P	VDD3P	3.3V pad power supply
164	VSS3P	P	VSS3P	Ground
165	A_DA_DATA_4	O	PHOB2	DAC data 4
166	A_DA_DATA_5	O	PHOB2	DAC data 5
167	A_DA_DATA_6	O	PHOB2	DAC data 6
168	A_DA_DATA_7	O	PHOB2	DAC data 7
169	A_DA_DATA_8	O	PHOB2	DAC data 8
170	A_DA_DATA_9	O	PHOB2	DAC data 9
171	A_DA_DATA_10	O	PHOB2	DAC data 10
172	VDD1IH	P	VDD1IH	1.8V internal power supply
173	VSS3I	P	VSS3I	Ground
174	A_DA_DATA_11	O	PHOB2	DAC data 11

Table 2-1. Pin Description of S5N8950 According to Pin Number (Continued)

Pin	Name	Type	Driver	Description
175	A_DA_DATA_12	O	PHOB2	DAC data 12
176	A_DA_DATA_13	O	PHOB2	DAC data 13

Table 2-2. I/O Driver Description of S5N8950

Pad	I/O	Description
PHTICD	I	5V tolerant for 3.3V interface LVCMOS level input buffer with pull-down
PHISD	I	3.3V interface LVCMOS Schmitt-Trigger level input buffer with pull-down
PHSCKDSD	I	3.3V LCMOS Schmitt Trigger level input clock driver pull-down.
PHTISD	I	5V tolerant for 3.3V interface LVCMOS Schmitt-Trigger level input buffer with pull-down
PHICD	I	3.3V interface LVCMOS level input buffer with pull-down
PHOB2	O	3.3V LVCMOS normal output buffer driving 2mA
PHTOT4	OZ	5V tolerant for 3.3V interface tri-state output buffer driving 4mA
PHTBCDT6SM	B	3.3V interface 5V tolerant LVCMOS level tri-state bi-directional buffer driving 6mA medium slew rate control with pull-down
VDD1IH	I	VDD for 1.8V internal power in the near by 3.3V pad.
VSS3I	I	VSS for 1.8V internal power in the near by 3.3V pad.
VDD3O	I	VDD for 3.3V output driver power
VSS3O	I	VSS for 3.3V output driver power
VDD3P	I	VDD for 3.3V pre- driver power
VSS3P	I	VSS for 3.3V pre- driver power

Table 2-3. Pin Summary in Terms of Interface

Name	Type	Driver	Function
UTOPIA Interface			
U_TX_ADDR[4:0]	I	PHTICD	Utopia Tx address [4:0]
U_TX_DATA[7:0]	I	PHTICD	Utopia Tx data [7:0]
U_TX_SOC	I	PHTICD	Utopia Tx start of cell
U_TX_ENB	I	PHTICD	Utopia Tx enable
U_TX_CLAV	OZ	PHTOT4	Utopia Tx cell available
U_TX_CLK	I	PHTICD	Utopia Tx clock, 25MHz
U_RX_ADDR[4:0]	I	PHTICD	Utopia Rx address [4:0]
U_RX_DATA[7:0]	OZ	PHTOT4	Utopia Rx data [7:0]
U_RX_SOC	OZ	PHTOT4	Utopia Rx start of cell
U_RX_ENB	I	PHTICD	Utopia Rx enable
U_RX_CLAV	OZ	PHTOT4	Utopia Rx cell available
U_RX_CLK	I	PHTICD	Utopia Rx clock, 25MHz
STM Interface			
S_TX_DAV[1:0]	O	PHTOT4	Serial Tx data valid signal [1:0]
S_TX_CLK[1:0]	O	PHTOT4	Serial Tx clock [1:0]
S_TX_DATA[1:0]	I	PHTICD	Serial Tx data [1:0]
S_RX_DAV[1:0]	O	PHTOT4	Serial Rx data valid signal [1:0]
S_RX_CLK[1:0]	O	PHTOT4	Serial Rx clock [1:0]
S_RX_DATA[1:0]	O	PHTOT4	Serial Rx data [1:0]
Host Interface			
H_SEL	I	PHTICD	Host type: [0]=Motorola / [1]= Intel
H_ADDR[9:0]	I	PHTICD	Host address bus [9:0]
H_DATA[7:0]	B	PHTBCDT6SM	Host data bus [7:0]
H_CSN	I	PHTICD	Chip selection
H_RDN	I	PHTICD	Not used.
			Read enable: active low
H_WRN	I	PHTICD	Motorola: [0]=write enable / [1]=read enable Intel: Write enable: active low
H_READY	OZ	PHTOT4	Motorola: Host CPU DTACK - active low Intel: Host CPU Ready - active high
H_INT	O	PHTOT4	Motorola: Interrupt IRQ - active low Intel: Interrupt INT - active high
H_WAKEUP	O	PHTOT4	Host wakeup

Table 2-3. Pin Summary in Terms of Interface (Continued)

Name	Type	Driver	Function
AFE Interface			
A_AD_DATA[13:0]	I	PHICD	ADC data
A_DA_DATA[13:0]	O	PHOB2	DAC data
A_DA_REF_CLK	O	PHOB2	DAC data reference clock
A_DA_AUX_CLK	O	PHOB2	DAC data auxiliary clock (Not Used)
A_SDI	I	PHICD	AFE serial input data
A_SCLK	O	PHOB2	AFE serial clock
A_SDO	O	PHOB2	AFE serial output data
A_SEN	O	PHOB2	AFE serial enable (active low)
A_RSTN	O	PHOB2	AFE reset (active low)
A_BUSY	I	PHTICD	AFE busy (active high) / TL 2-nd interrupt
A_AND	I	PHTICD	Audible noise detection (active high)
A_TX_PWR	O	PHTOT4	TX line driver power enable (active high)
A_RX_PWR	O	PHTOT4	RX line driver power enable (active high)
Board Interface			
B_RSTN	I	PHTISD	System reset (active low)
B_GP_OUT[1:0]	O	PHTOT4	General purpose output
B_GP_IN[1:0]	I	PHTICD	General purpose input
B_BMODE[1:0]	I	PHTICD	TeakLite boot mode selection [0] = simple reset [1] = boot from Host CPU (normal mode) [2] = boot from JTAG (emulation mode) [3] = self-booting (test mode)
B_TMODE	I	PHTICD	Test Mode Enable [0] Normal [1] Test mode
B_NMODE	I	PHTICD	NAND tree test mode [0] NAND tree test mode [1] Normal
B_NTR	B	PHTBCDT6SM	ATM network timing reference
B_EXT_CLK	I	PHTICD	External clock for test mode
B_MSC_CLK	I	PHTICD	Misc. clock for test mode
B_CLK_CNTL	I	PHTICD	Clock control signal [0] = 8950 uses PLL clocks. [1] = 8950 uses external clocks.
		DSP JTAG	Interface
T_MS	I	PHTICD	DSP JTAG test mode select

Table 2-3. Pin Summary in Terms of Interface (Continued)

Name	Type	Driver	Function
T_CLK	I	PHTICD	DSP JTAG test clock
T_DI	I	PHTICD	DSP JTAG test input data
T_DO	OZ	PHTOT4	DSP JTAG test output data
T_INTP	O	PHTOT4	DSP JTAG interrupt to host
PLL Interface			
P_XTAL_IN	I	PHSOSCM26	XTAL input for clock.
P_XTAL_OUT	O		XTAL output for clock.
P_PLL_FILTER	O	POAR50_ABB	Internal PLL pump out connected to filter
P_VDD18A2	I	VDD1T_ABB	1.8V digital power supply
P_VSS18A2	I	VSS1T_ABB	1.8V digital ground
P_VDD18A1	I	VDD1T_ABB	1.8V analog power supply
P_VSS18A1	I	VSS1T_ABB	1.8V analog ground
P_VBBA	I	VBB1_ABB	Bulk ground
Power Interface			
VDD1IH	I	VDD1IH	1.8V internal power in the near by 3.3V pad.
VSS3I	I	VSS3I	1.8V internal ground in the near by 3.3V pad.
VDD3O	I	VDD3O	3.3V output-driver power
VSS3O	I	VSS3O	3.3V output-driver ground
VDD3P	I	VDD3P	3.3V pre-driver power
VSS3P	I	VSS3P	3.3V pre-driver ground

FUNCTION DESCRIPTION

OVERVIEW

The G.dmt ADSL system consists of two main chips; G.dmt ADSL transceiver chip (S5N8950) and Analog Front End chip (S5N8951). The AFE provides an analog interface with the line drivers and hybrid components to connect the PSTN network. S5N9850 provides all the digital functions of the G.dmt as depicted in Figure 4.

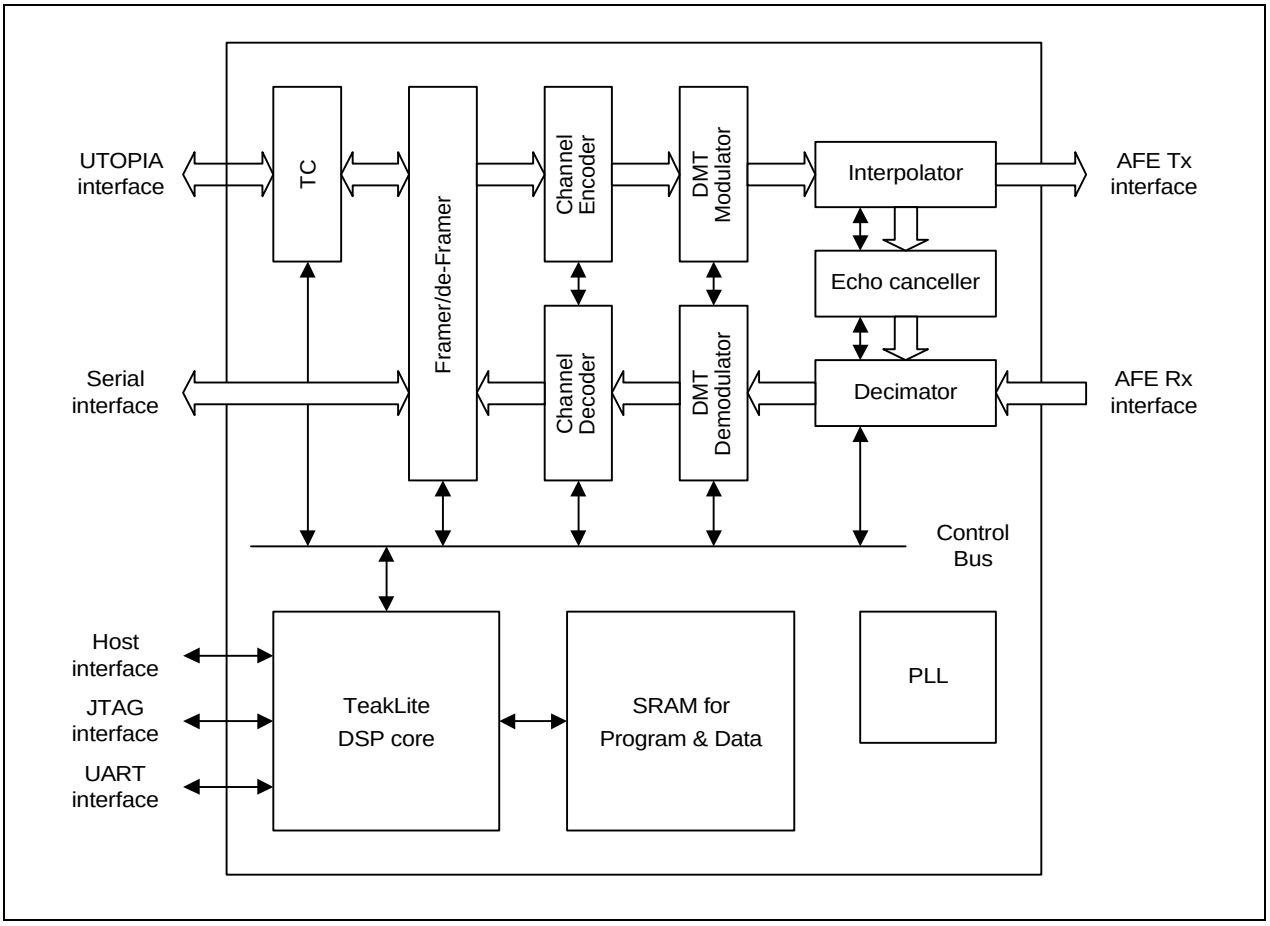

Figure 2-4. Block Diagram

The input bit stream is divided into bit slices in Framer/de-Framer module, and they are fed into the DMT modulator, which are allocated to 256 sub-channels according to the bit-loading table. The bit slices are then converted to frequency-domain complex samples by the QAM encoder. The 256 complex samples are changed to 512 time-domain samples by IFFT in the DMT modulator. The Tx filter in the Interpolator module performs band separation and interpolation functions.

The received signals are attenuated and distorted in terms of both phase and amplitude. PLL fixes the phase errors using the pilot-tone transmitted from the CO side. The synchronization recovery algorithm uses a known synchronization symbol defined in the standard for frame synchronization. The TEQ in the Decimator module is a filter that adaptively alters the channel so that the impulse response is reduced to the length of the cyclic prefix, which will be removed prior to FFT in the DMT demodulator module. The FEQ in the DMT demodulator module is a one tap complex adaptive filter for each sub-channel, which adjusts the gains and phases of the received signals. The equalizers are adaptively updated due to the transmission channel environment.

In FDM-based DMT modulation, the frequency band, 0 to 1.104MHz, is divided into 256 equally spaced sub-channels, of which 26kHz (#6) to 134kHz (#31) is allocated for the upstream, and 142kHz (#33) to 1.100MHz (#255) for the downstream. The Nyquist rate of the downstream and upstream, therefore, should be 2.208MHz and 276kHz, respectively.

DMT inherently transmits an optimized time-variable spectrum. This spectrum is adjusted according to the desired data rate and the transmission characteristics (transfer function and noise spectrum) on each and every sub-channel. For this, CO and CPE transmit pseudo random signals defined in the standard to each other during initialization. They measure the quality of each of these received signals and then decide whether a tone has sufficient quality to be used for further transmission and, if so, how much data this tone should carry relative to the other tones that are used. They inform the bit loading result to each other.

SUB-MODULE FUNCTIONAL DESCRIPTION

DMT Modulator/Demodulator

QAM Encoder and Decoder

An algorithmic constellation encoder shall be used to construct constellations. Data bits from the DMT symbol buffer shall be extracted and these bits form a binary word $\{V_{b-1}, V_{b-2}, \ldots, V_1, V_0\}$. The first bit extracted shall be V_0, the LSB. For a given sub-channel, the encoder shall select an odd-integer point (X, Y) from the square-grid constellation based on the b bits. For example, for b=2, the four constellation points are labeled 0, 1, 2, 3 corresponding to $(V_1, V_0) = (0, 0), (0, 1), (1, 0), (1, 1)$, respectively.

Gain-Scaling

For the transmission of data symbols, gain-scaling factors, g_i, shall be applied to all tones as requested by the ATU-R and possibly updated during show-time via the bit swap procedure. If $b_i > 0$ then only values of g_i within a range of approximately 0.75 to 1.33 (i.e., 0 +/- 2.5dB) may be used to equalize the expected error rates for all data-carrying sub-channels. If $b_i = 0$, then only g_i values of 0 or 1 may be used. During synchronization no gain scaling shall be applied to any tone. Each point, (X_i, Y_i), or complex number, $Z_i = X_i + jY_i$, output from the encoder is multiplied by g_i: $Z_i' = g_i Z_i$

IFFT/FFT

The FFT/IFFT performs DMT modulation and demodulation simultaneously. In the TX path, the IFFT operation makes the Hermitian Symmetry of the DMT symbol in the frequency domain and transforms into a time domain representation. In the RX path, the FFT operation transforms the time-domain DMT symbol into a frequency domain representation.

Frequency-Domain Equalizer (FEQ)

Since each sub-channel output of the FFT will be scaled in magnitude and offset in phase by the values of the channel transfer function at the corresponding center frequency for the tone, FEQ will be adaptively scale each sub-channel by the inverse of the channel gain and phase so that common decision boundary can be used in decoding the constellations. The FEQ is a one-tap complex adaptive filter for each sub-channel.

Interpolator/Decimator

Interpolation Filter

Interpolation filter is in front of DAC in transmitter. It is used to interpolate the filter input signal, which is zeros-inserted between filter input data samples, and remove the mirror image of the interpolated signals. Therefore the sampling rate becomes higher. By using interpolation filter, the analog filter next to DAC can be low-order and easily implemented.

Decimation Filter

Decimation filter is next to ADC in receiver. It is used to remove the mirror image of the received signals and decimate the filter input signal, which is over-sampled in ADC. Therefore the filter output signal becomes Nyquist rate. By using over-sampling and decimation, the analog filter in front of ADC can be low-order and easily implemented.

Time-Domain Equalizer (TEQ)

The Time domain Equalizer (TEQ) is a filter to shorten channel so that the effective length of the channel impulse response is reduced to the length of the cyclic prefix or less in a minimum-mean-square distortion sense. If channel impulse response is very short, zero inter-channel-interference can be achieved by appending to each block of samples of transmit signal a cyclic prefix (CP) that is the same length as the shortened impulse response, but impulse responses of most practical channels are much longer than the CP length. One solution is to use the TEQ for shortening the channel impulse response

Channel Encoder/Decoder

CRC Generator and CRC Checker

CRC (cyclic redundancy check) is used extensively in detecting transmission error over a channel. Two cyclic redundancy checks – one for the fast data buffer and one for the interleaved data buffer – are generated for each super-frame and transmitted in the first frame of the following super-frame. At the receiver, CRC is generated for the one super-frame, and then CRC checker compares the resulting CRC and the CRC received in the first frame of next super-frame.

Scrambler and De-scrambler

The scrambler is used to randomize the binary data stream output from the fast and interleaved data buffers. This ensures that random data is transmitted even when constant data is applied to the system. The scrambler transforms input stream by XORing the data with a 18^{th} and 24^{th} previous data. The de-scrambler accepts the error protected data stream output from the Reed-Solomon decoder and perform de-scrambling by reversing the function of the scrambler at the transmitter.

Reed Solomon Encoder and Decoder

The RS CODEC is used to detect and correct the errors imposed on a channel. The decoder is programmable and the programmable parameter are codeword length N ($1 \leq N \leq 255$), and redundancy R (R = 0, 2, 4, 6, 8, 10, 12, 14, 16).

Interleaver and De-interleaver

The function of the interleaver is to rearrange the input bit stream into different order. The programmable interleaver depths D are 1, 2, 4, 8, 16, 32, and 64. The de-interleaver is supposed to reverse that process and restore the original order of the sequence.

Framer and De-framer

The Framer/De-framer in S5N8950 supports ITU-T Recommendation G.992.1, G.992.2 and T1.413 frame structure, EOC/AOC insertion/extraction, and NTR (Network Timing Reference) at ATU-C. The framer generates super-frame structure as defined in G.992.1, G.992.2, and T1.413 standards. The single latency mode, dual latency mode and four framing modes are fully supported. The EOC/AOC and the payload data are inserted in the super-frame structure by the framer and are extracted from the super-frame structure by the de-framer.

Cell TC

HEC Generation

The HEC byte is generated in the transmit direction as described in ITU-T Recommendation I.432, including the recommended modulo 2 addition of pattern 01010101 to the HEC bits. The generator polynomial coefficient set used and the HEC sequence generation procedure is in accordance with ITU-T Recommendation I.432.

Idle Cell Insertion

Idle cells are inserted in the transmit direction for cell rate decoupling. Cell TC discards the idle cells at the receiver modem.

Scrambling

Scrambling of the cell payload field is used in the transmit direction to improve the security and robustness of the HEC cell delineation mechanism. In addition, it randomizes the data in the information field, for possible improvement of the transmission performance. The self-synchronizing scrambler polynomial $x^{43}+1$ and procedures defined in the ITU-T Recommendation I.432 are implemented.

Cell Delineation

The identification of cell boundaries in the payload is performed using a coding law checking the HEC field in the cell header according to the algorithm described in the ITU-T Recommendation I.432.

INTERFACE

UTOPIA INTERFACE

S5N8950 provides both UTOPIA level 1 and 2 interfaces for ATM data. The UTOPIA interface is designed to run at maximum 25MHz. While UTOPIA level 1 supports only one PHY device, while UTOPIA level 2 supports multi-PHY devices, which is accomplished by a single pair of handshake signals for each direction, *e.g.*, U_TX_ENB/U_TX_CLAV for data transmission and U_RX_ENB/U_RX_CLAV for data reception. The U_TX_ADDR and U_RX_ADDR are used to distinguish between ports, using a register per port to set a specific address match. Internally each port is handled separately with independent data buffers, to avoid any queue blocking problems. In S5N8950, two ports for UTOPIA level 2 interface are provided and two registers for each port, TC.CFG[0] and TC.CFG [1], are used for matching a unique address to port. In the Tx direction, when a channel address is detected on the U_TX_ADDR, the U_TX_CLAV signal is driven to indicate whether or not the channel has room to accept a new cell. The U_TX_ADDR is also sampled on the falling edge of U_TX_ENB to select a channel for cell transfer. The Rx interface is similar in operation and timing, when a channel address is detected on the U_RX_ADDR, the U_RX_CLAV signal is driven to indicate if a received cell is available to be read. On the falling edge of U_RX_ENB, the U_RX_ADDR is sampled to select a channel for a received cell. If a channel is scanned too slowly in the Rx direction or a channel is not scanned for a long time, cell overrun may occur causing cells to be discarded. Loss of cells in overrun conditions is recorded in the status register, TC.CELL_LOSS_CNT[1/0]. The number of discarded cell by HEC error is recorded in the status register, TC.HEC_ERR_CNT[1/0].

STM INTERFACE

S5N8950 has a STM interface for serial data transmission. It supports envelope and indicate modes for 3-pin STM interface, and 2-pin STM interface. The STM interface is designed to run at maximum 17 MHz. The bit rate in STM transmission mode is restricted to maximum 8 Mbps, while that in ATM mode is maximum 12 Mbps.

HOST INTERFACE

S5N8950 has an asynchronous parallel bus slave interface in operation with Motorola MC68000 bus type or Intel 8086 bus type. Thus, S5N8950 is controlled and configured by an external host processor across the host interface. Two interface types are supported: Motorola and Intel type interfaces. The H_SEL pin makes the choice: 0 and 1 select Motorola and Intel type interfaces, respectively.

The interface circuit with MC68000 processor or Intel 8086 is quite simple. The ATU-C and ATU-R control interface between MC68000 or 8086 and S5N8950 uses an 8-bit data bus and a 10-bit address bus as illustrated in Figure 5 or Figure 6. The host processor is only permitted to access registers by byte size, while S5N8950 control program should access by word size, that is, 16 bits. In case of 32 bit processor interface like MPC860, the chip select must be programmed as a 8-bits so that dynamic bus sizing and correct word steering occurs.

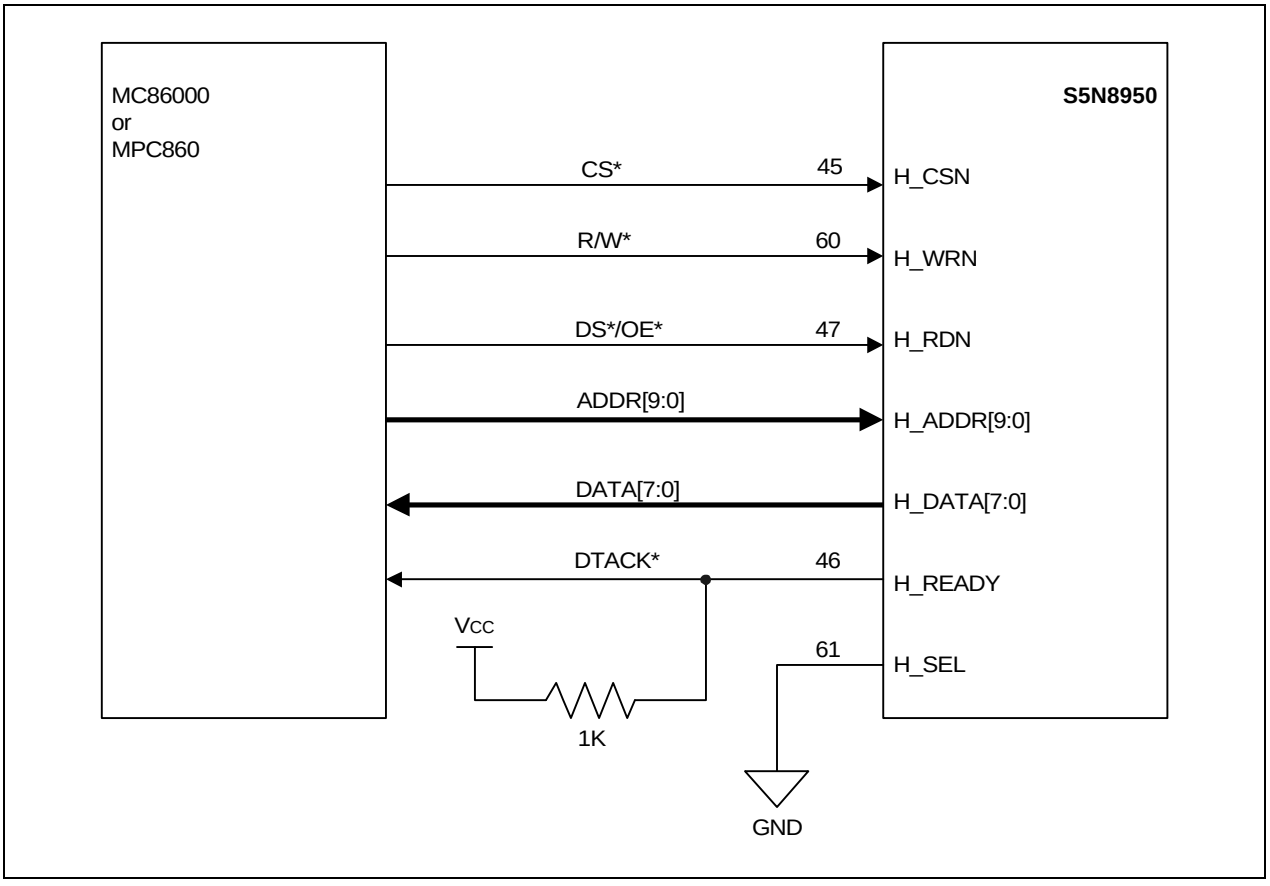

Figure 2-5. MC68000 Bus Type Processor Interface Circuit Diagram

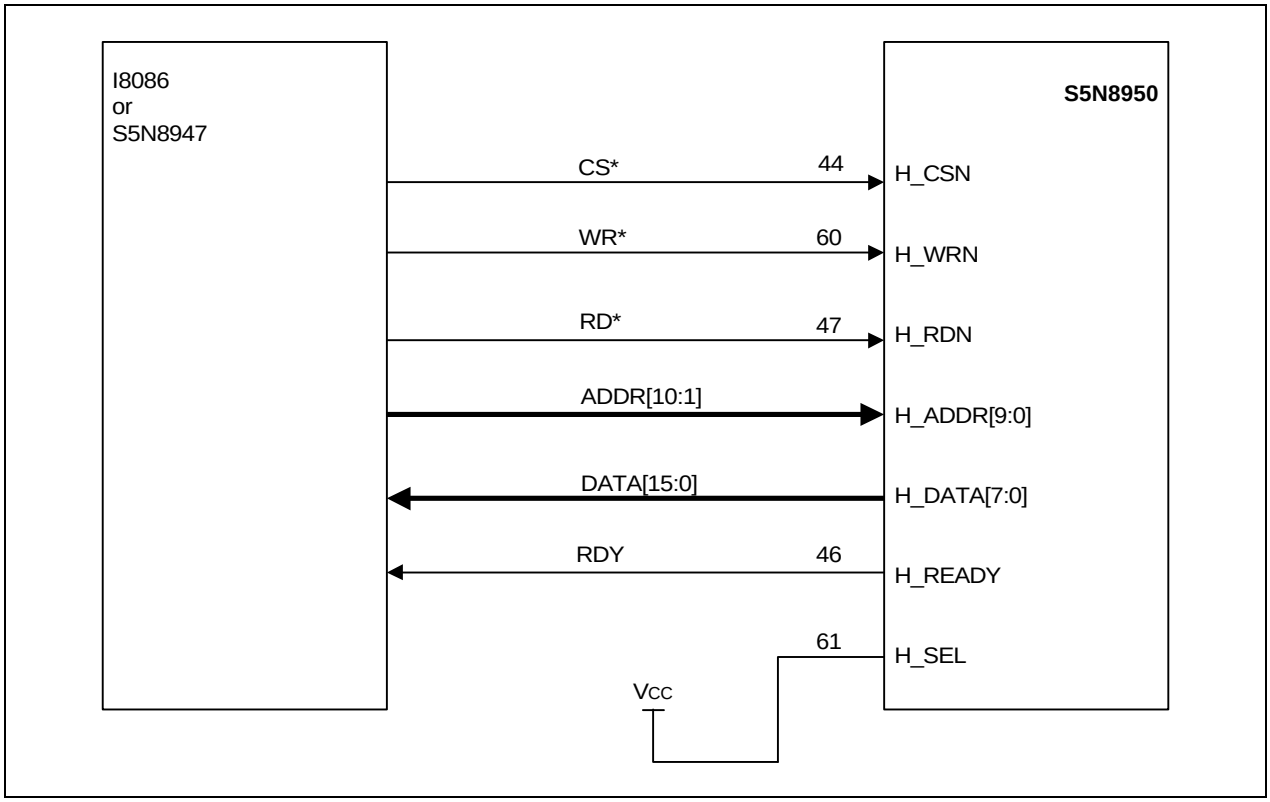

Figure 2-6. Intel 8086 Bus Type Processor Interface Circuit Diagram

AFE INTERFACE

The AFE interface signals of the S5N8950 are categorized into two parts. The first is TX and RX data path signals. And the other is an AFE serial control signal. The TX and RX data path signals are ADC and DAC signals synchronized to the A_DA_REF_CLK signal. The AFE serial control interface consists of an active-low enable output pin (A_SEN), a serial clock output pin (A_SCLK), a data output pin (A_SDO), a data input pin (A_SDI), additional AFE busy status input pin (A_BUSY), and AFE chip reset output pin (A_RSTN). S5N8950 can access AFE registers with these signals. And all the ADSL physical operation is performed by the S5N8950, so the AFE chip is controlled by the S5N8950. Figure shows the AFE interface circuit diagram between S5N8950 and S5N8951.

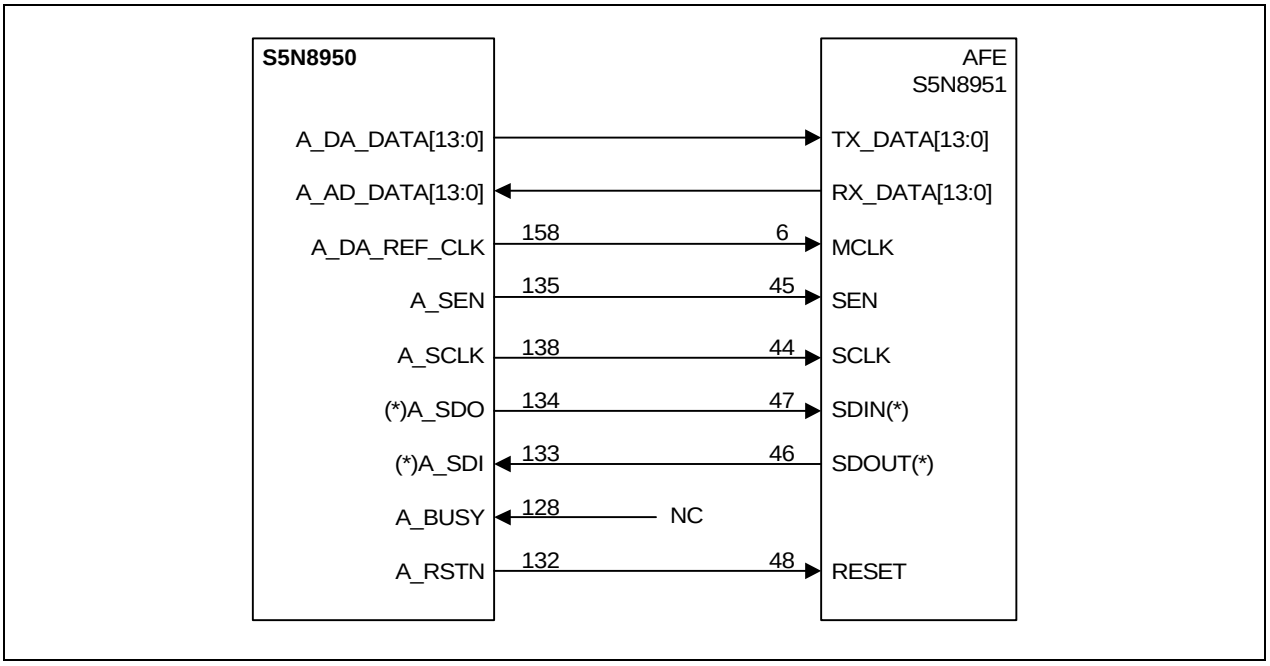

Figure 2-7. AFE Interface Circuit Diagram

Please keep in mind that A_SDO signal of S5N8950 must be connected with SDIN signal of S5N8951 and A_SDI signal of S5N8950 must be connected with SDOUT signal of S5N8951.

TIMING INFORMATION

AFE INTERFACE

Data Path

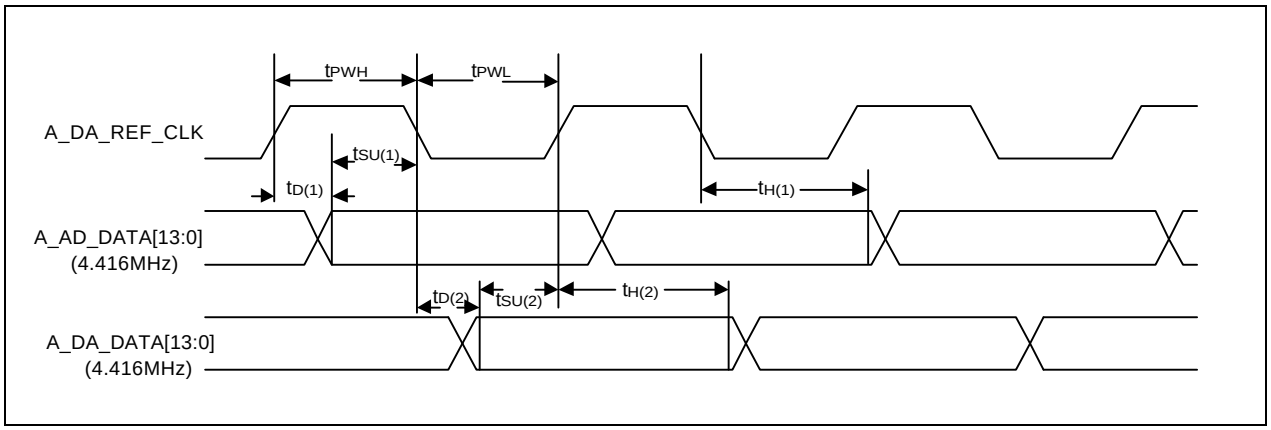

Figure 2-8. Timing Diagram of Data Path Signals Between S5N8950 and S5N8951

Table 2-4. Timing Values of Data Path Signals Between S5N8950 and S5N8951

Parameter	Symbol	Min	Typ	Max	Unit
A_AD_DATA delay after A_DA_REF_CLK↑	$t_{D(1)}$	0		10	ns
A_AD_DATA setup time to A_DA_REF_CLK ↓	$t_{SU(1)}$	10			ns
A_AD_DATA hold time after A_DA_REF_CLK ↓	$t_{H(1)}$	10			ns
A_DA_DATA delay after A_DA_REF_CLK ↓	$t_{D(2)}$	0		10	ns
A_DA_DATA setup time to A_DA_REF_CLK ↑	$t_{SU(2)}$	10			ns
A_DA_DATA hold time after A_DA_REF_CLK ↑	$t_{H(2)}$	10			ns
A_DA_REF_CLK high time	t_{PWH}		112		ns
A_DA_REF_CLK low time	t_{PWL}		112		ns

Serial Control Path

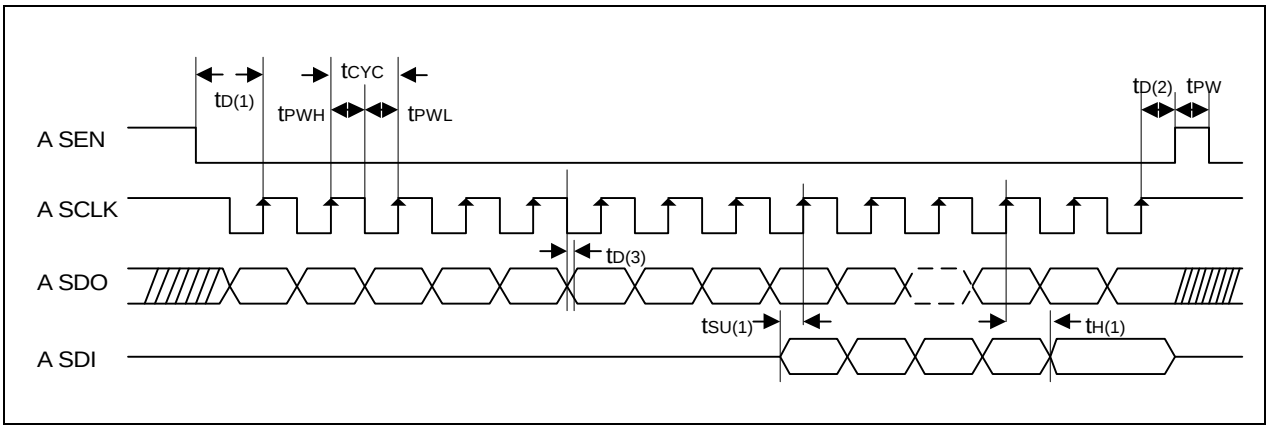

Figure 2-9. Timing Diagram of AFE Control Interface

Table 2-5. Timing Values of AFE Control Interface

Parameter	Symbol	Min	Typ	Max	Unit
A_SCLK period	t_{CYC}		896		ns
A_SCLK high time	t_{PWH}		448		ns
A_SCLK low time	t_{PWL}		448		ns
A_SCLK ↑ delay after A_SEN ↓	$t_{D(1)}$		784		ns
A_SEN↑ delay after A_SCLK ↑	$t_{D(2)}$		112		ns
A_SDO delay after A_SCLK ↓	$t_{D(3)}$	0		10	ns
A_SDI setup time to A_SCLK ↑	$t_{SU(1)}$	10			ns
A_SDI hold time after A_SCLK ↑	$t_{H(1)}$	10			ns
A_SEN pulse width	t_{PW}	896			ns

HOST BUS INTERFACE

Write Cycle Timing of Motorola Type Interface

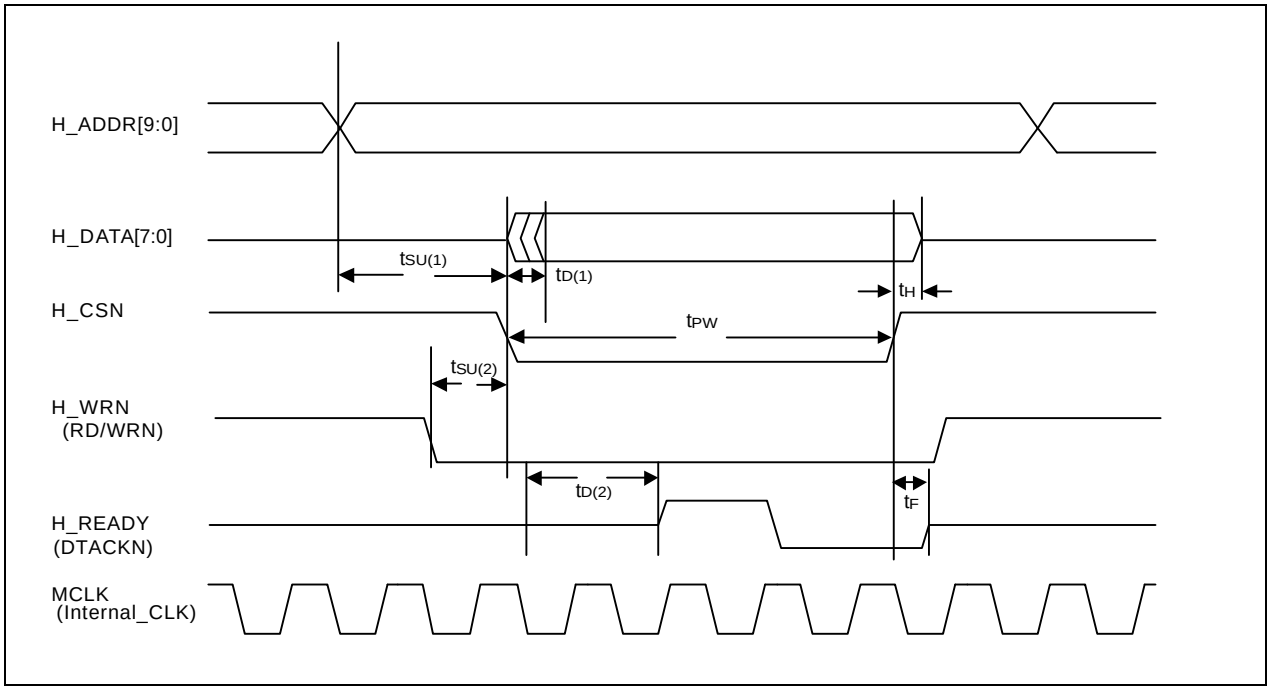

Figure 2-10. Write Cycle Timing of Motorola MC68000 Type Bus Interface

Table 2-6. Write Timing Value of Motorola MC68000 Type Bus Interface

Parameter	Symbol	Min	Typ	Max	Unit
H_ADDR setup time to H_CSN↓	$t_{SU(1)}$	0			ns
H_WRN↓ setup time to H_CSN↓	$t_{SU(2)}$	0			ns
H_DATA valid data after H_CSN↓	$t_{D(1)}$			50	ns
H_READY↑ delay after H_CSN↓	$t_{D(2)}$			112	ns
H_DATA hold time after H_CSN↑	t_H	0			ns
H_READY↓ float time to tri-state after H_CSN↑	t_F	1		10	ns
H_CSN pulse width	t_{PW}	168			ns

Read Cycle Timing of Motorola Type Interface

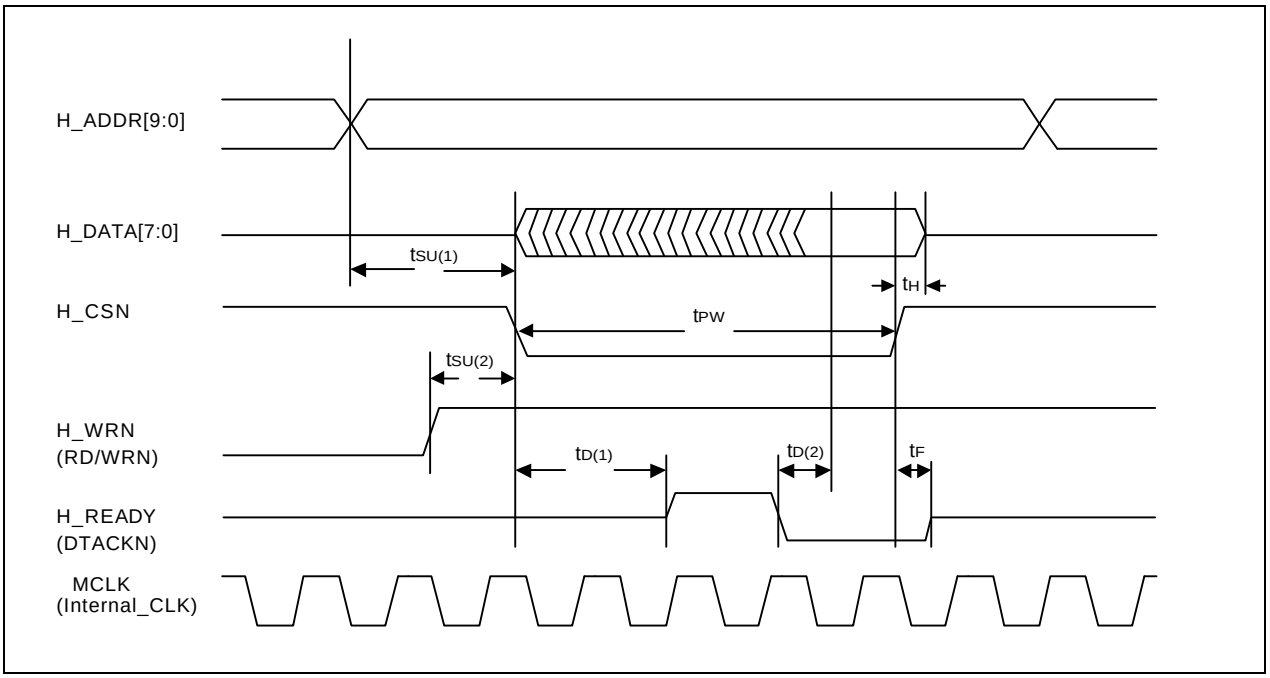

Figure 2-11. Read Cycle Timing of Motorola MC68000 Bus Type Interface

Table 2-7. Read Cycle Timing Values of Read Cycle of Motorola Type Bus Interface

Parameter	Symbol	Min	Typ	Max	Unit
H_ADDR setup time to H_CSN↓	$t_{SU(1)}$	0			ns
H_WRN setup time to H_CSN↓	$t_{SU(2)}$	0			ns
H_READY delay after H_CSN↓	$t_{D(1)}$			112	ns
H_DATA valid data after H_READY↓	$t_{D(2)}$			0	ns
H_DATA hold time after H_CSN↑	t_H	0			ns
H_READY float time to tri-state after H_CSN↑	t_F	1		10	ns
H_CSN pulse width	t_{PW}	168			ns

Write Cycle Timing of Intel Type Interface

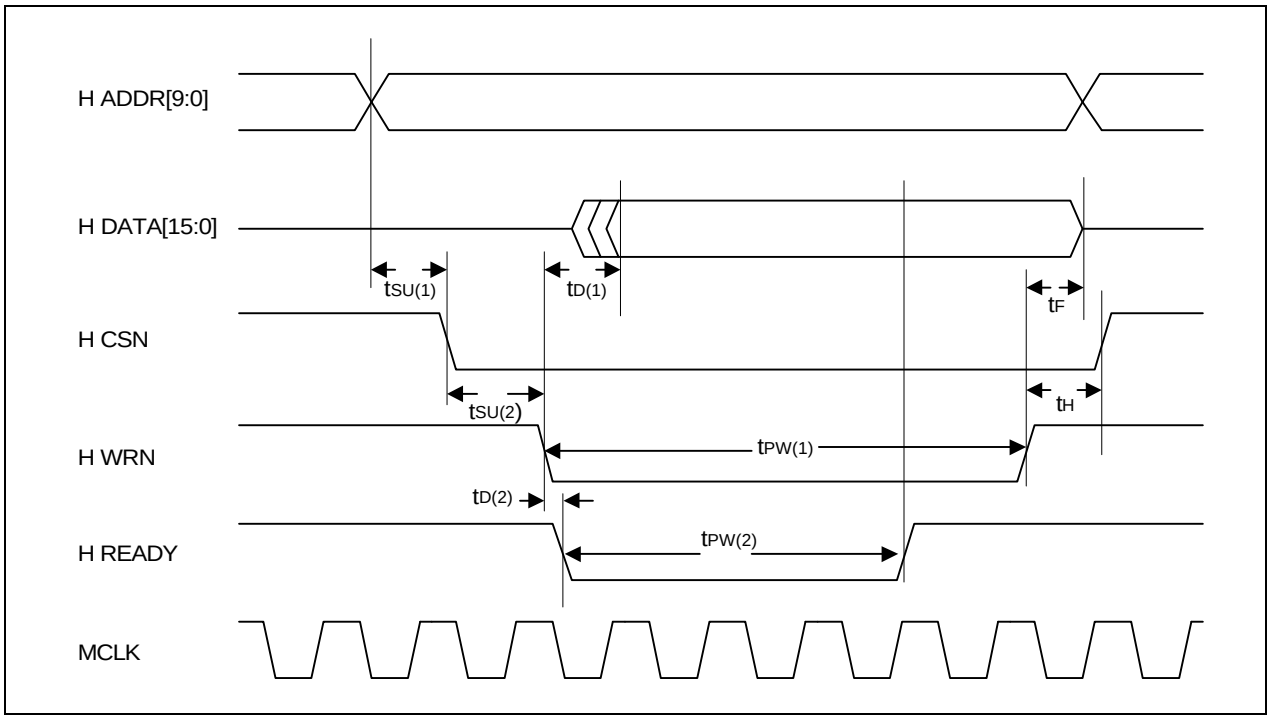

Figure 2-12. Write Cycle Timing of Intel 8086 Bus Type Interface

Table 2-8. Write Cycle Timing Values of Intel 8086 Bus Type Interface

Parameter	Symbol	Min	Typ	Max	Unit
H_ADDR setup time to H_CSN↓	$t_{SU(1)}$	0			ns
H_CSN setup time to H_WRN↓	$t_{SU(2)}$	0			ns
H_DATA valid data after H_WRN↓	$t_{D(1)}$			50	ns
H_READY delay after H_WRN↓	$t_{D(2)}$			10	ns
H_DATA float time to tri-state after H_WDN↑	t_F	0			ns
H_DATA hold time after H_WRN↑	t_H	0			ns
H_WRN pulse width	$t_{PW(1)}$	168			ns
H_READY pulse width	$t_{PW(2)}$	168		280	ns

Write Cycle Timing of Intel Type Interface

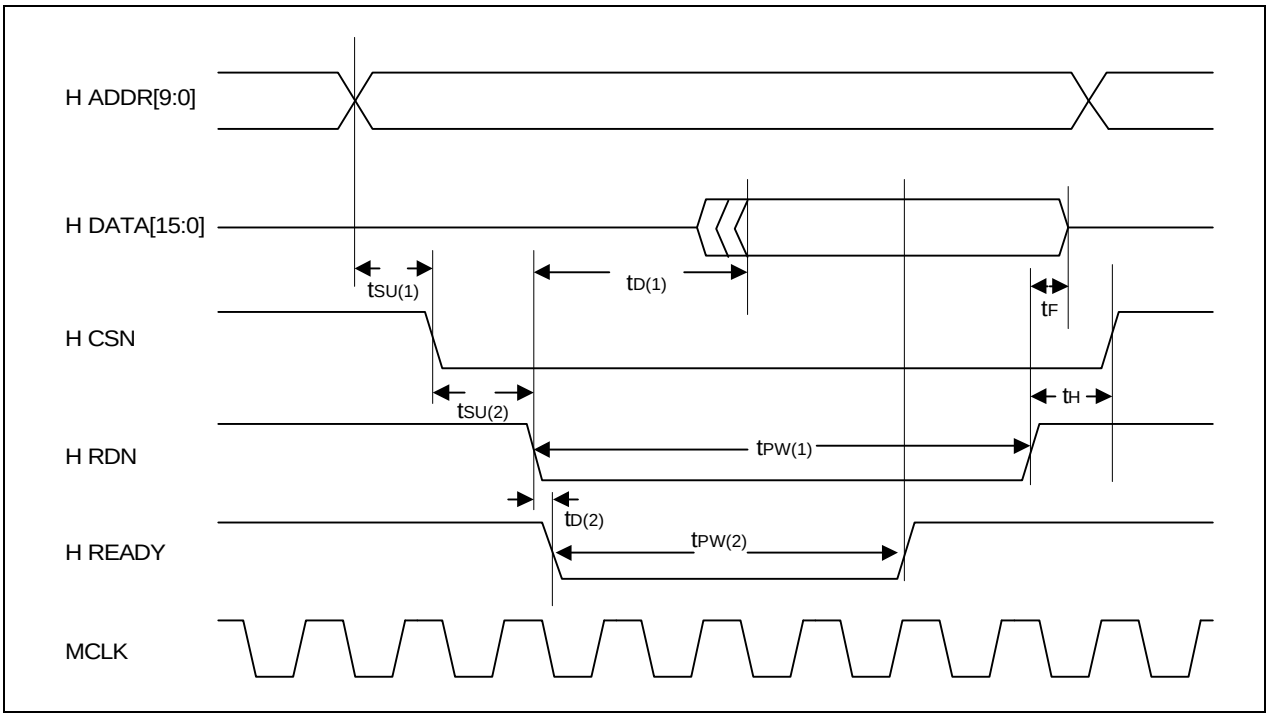

Figure 2-13. Read Cycle Timing of Intel 8086 Bus Type Interface

Table 2-9. Read Cycle Timing Values of Intel 8086 Bus Type Interface

Parameter	Symbol	Min	Typ	Max	Unit
H_ADDR setup time to H_CSN↓	$t_{SU(1)}$	0			ns
H_CSN setup time to H_RDN↓	$t_{SU(2)}$	0			ns
H_DATA valid data after H_RDN↓	$t_{D(1)}$			168	ns
H_READY delay after H_RDN↓	$t_{D(2)}$	0		10	ns
H_DATA float time to tri-state after H_RDN↑	t_F	0			ns
H_CSN hold time after H_RDN↑	t_H	0			ns
H_RDN pulse width	$t_{PW(1)}$	168			ns
H_READY pulse width	$t_{PW(2)}$	168		280	ns

STM INTERFACE

Indicate Mode in STM Interface

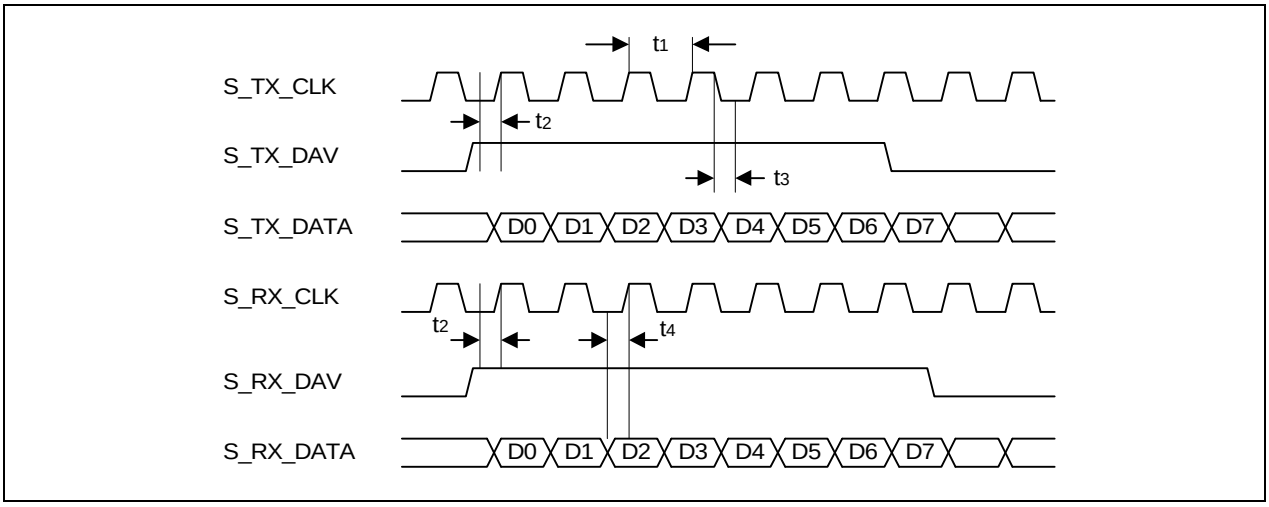

Figure 2-14. Tx/Rx Timing Diagram of Indicate Mode in STM Interface

Table 2-10. Tx/Rx Timing Values of Indicate Mode in STM Interface

Parameter	Description	Min	Max	Unit
t_1	S_TX_CLK frequency	1	20	MHz
t_2	S_TX(RX)_CLK ↑ from S_TX(RX)_DAV ↑	1/(4t1)	1/(4t1)	ns
t_3	DATA Valid after S_TX_CLK ↓	1/(4t1)		ns
t_4	S_RX_CLK ↑ from Valid DATA output	1/(4t1)	1/(4t1)	ns

Envelope Mode in STM Interface

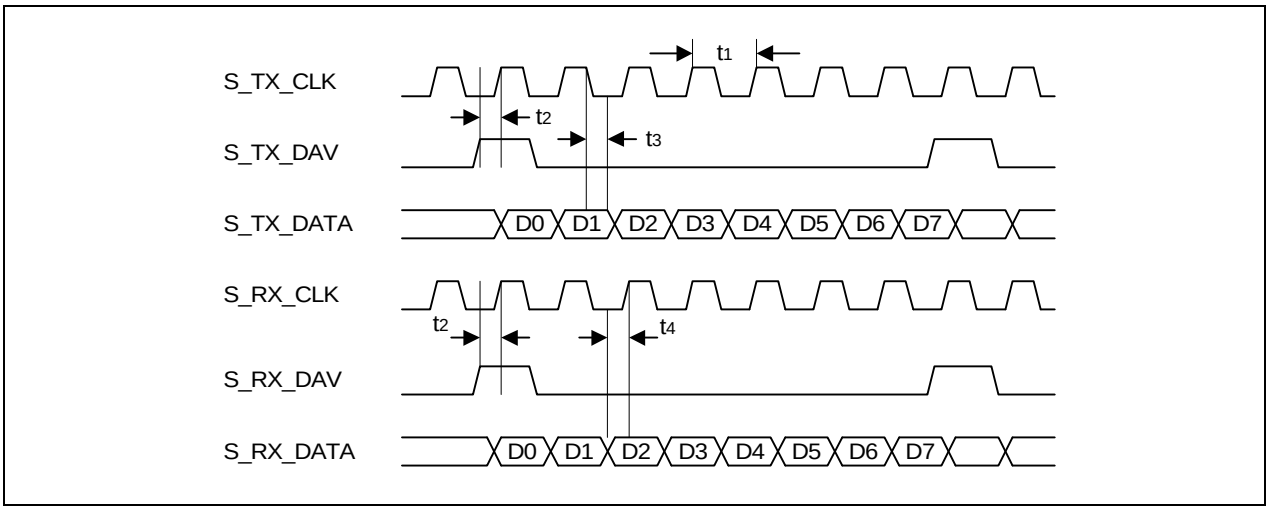

Figure 2-15. Tx/Rx Timing Diagram of Envelope Mode in STM Interface

Table 2-11. Tx/Rx Timing Values of Envelope Mode in STM Interface

Parameter	Description	Min	Max	Unit
t_1	S_TX_CLK frequency	1	20	MHz
t_2	S_TX(RX)_CLK ↑ from S_TX(RX)_DAV ↑	1/(4t1)	1/(4t1)	ns
t_3	DATA Valid after S_TX_CLK ↓	1/(4t1)		ns
t_4	S_RX_CLK ↑ from Valid DATA output	1/(4t1)	1/(4t1)	ns

2-Pin STM Interface

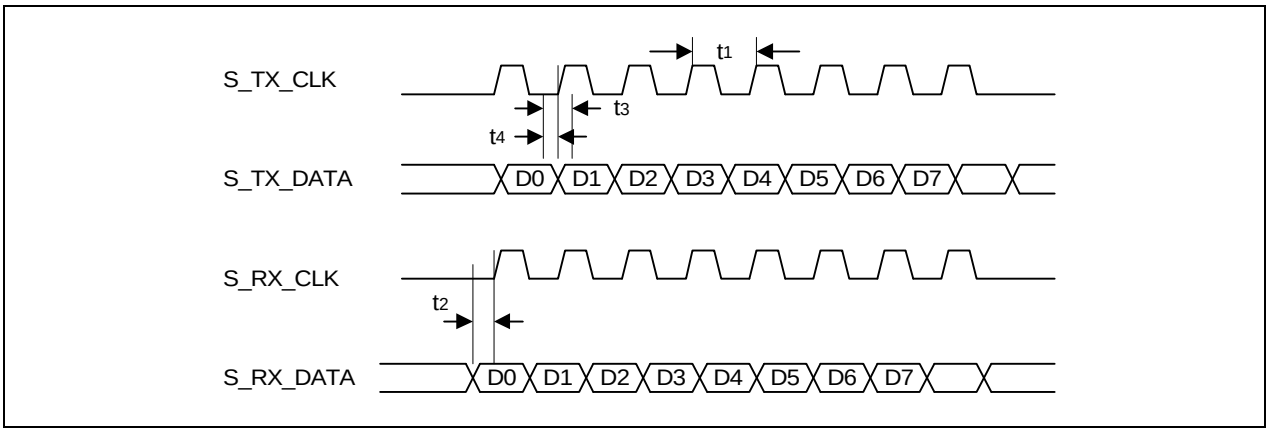

Figure 2-16. Tx/Rx Timing Diagram of 2-Pin STM Interface

Table 2-12. Tx/Rx Timing Values of 2-Pin STM Interface

Parameter	Description	Min	Max	Unit
t_1	S_TX_CLK frequency	1	20	MHz
t_2	S_RX_CLK ↑ from Valid DATA output	1/(4t1)	1/(4t1)	ns
t_3	DATA Hold after S_TX_CLK ↑	1	3	ns
t_4	DATA Setup before S_TX_CLK ↑	1	3	ns

ELECTRICAL SPECIFICATION

The values presented in the following table apply for all inputs and/or outputs unless specified otherwise. All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device.

ABSOLUTE MAXIMUM RATINGS

Table 2-13. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
I_{LATCH}	Latch-up Current	± 200	mA
T_{STG}	Storage Temperature	£-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Table 2-14. Recommended Operating Conditions

Symbol	Parameter		Rating	Unit
V_{DD}	DC input Voltage	1.8 V I/O	1.65 ~ 1.95	V
		3.3V I/O	3.00 ~ 3.60	
		5V tolerant I/O	3.00 ~ 3.60	
	Analog Core DC Supply Voltage	1.8V core	1.8 ± 5 %	
T_A	Ambient Operating Temperature		£- 40 ~ 85	°C

POWER DISSIPATION

Table 2-15. Power Dissipation

Symbol	Parameter	Min	Typ	Max	Unit
P_D	Power Dissipation		< 400		mW

DC CHARACTERISTICS

Table 2-16. DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	2.0			V
V_{IL}	Input Low Voltage			0.8	
V_{OH}	Output High Voltage	2.4			
V_{OL}	Output Low Voltage			0.4	
V_T	Switching Threshold		1.4		
V_{T+}	Schmitt Trigger, Positive-going Threshold			2.0	
V_{T-}	Schmitt Trigger, Negative-going Threshold	0.8			
I_{IH}	Input High Current ($V_{IN} = V_{DD}$)	-10(10)	(33)	10(60)	µA
I_{IL}	Input Low Current ($V_{IN} = V_{SS}$)	-10(-60)	(-33)	10(-10)	
I_{OZ}	Tri-state Output Leakage Current	-10		10	
I_{DD}	Quiescent Supply Current			100	
C_{IN}	Input Capacitance			4	pF
C_{OUT}	Output Capacitance			4	

NOTE: ( ) – Input buffer with pull-down

PACKAGE INFORMATION

S5N8950 employs 176 LQPF-2424. Figure shows 176 LQFP-2424 package dimension.

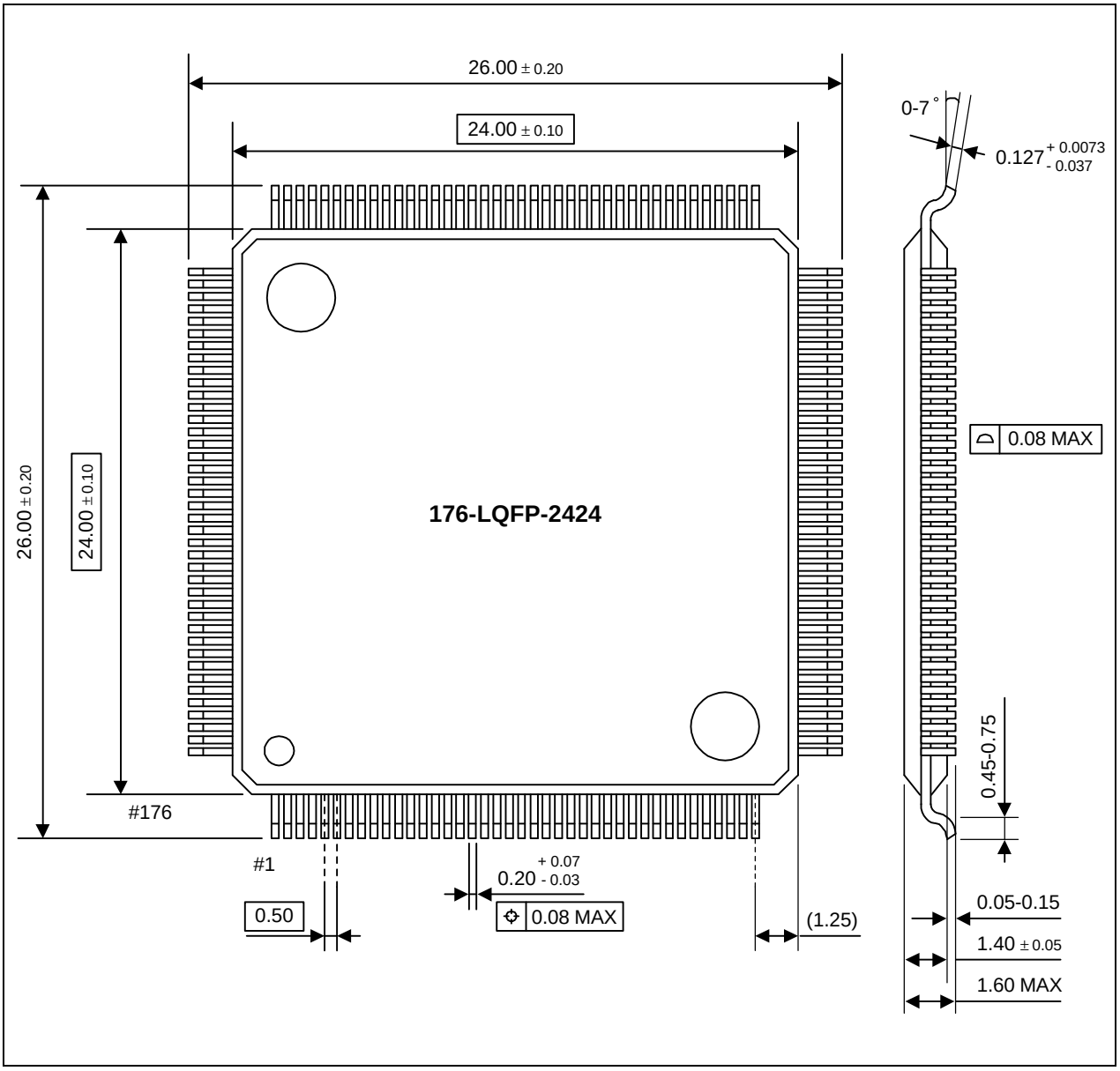

Figure 2-17. 176 LQFP-2424 Package Dimension

NOTES

OVERVIEW

This chapter provides an overview of the S5N8951X ADSL ATU-C & ATU-R analog front end chip.

GENERAL DESCRIPTIONS

The S5N8951X is Analog Front End IC designed for DMT based universal ADSL (Asymmetric Digital Subscribe Line) modems with 0.35u fully CMOS technology.

It has 25.875 ~ 138kHz Upstream channel and 142.312 ~ 1104kHz bandwidth Downstream channel. The S5N8951X includes AGC, LPF, ADC, DAC. The AGC has 40dB gain 0.4dB step in RX mode and –24dB gain 2dB step in TX mode with 12bit/8bit control bits. Anti alias LPF has 1104kHz passband frequency in RX path and 138kHz in TX path. Samsung's ADSL AFE chip provides 14bit ADC at 4.416M or 8.832M sample rates and 14bit 4.416MHz, 8.832MHz DAC.

An 10bit DAC support VCXO control for timing recovery. The VCXO is divided into a crystal driver at 35.328MHz.

FEATURES

- Integrated Analog Front End (AFE) for ADSL ATU-C & ATU-R
- Complies with G.dmt and G.lite
- Up to 1104kHz down stream and 138kHz upstream channel
- 14bit 4.416MHz/s or 8.832MHz/s ADC
- 14bit 4.416MHz or 8.832MHz DAC
- Selectable 14bit or 7bit-2phase ADC/DAC digital interface
- 5^{th}-order Low Pass anti-alias Filter TX/RX paths
- RX 40dB 0.4dB step gain range with 12bit control signal
- TX -24dB 2dB step gain range with 8bit control signal
- 10bit 4kHz VCXO DAC
- Fully 0.35um CMOS technology
- 3.3V Power supply operation
- 0.4W Power comsumption

ABSOLUTE MAXIMUM RATINGS

Table 3-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	DC Supply Voltage	-0.3		3.8	V
V_{IN}	DC Input Voltage	-0.3		V_{DD}+0.3	V
	5V Tolerant	-0.3		5.5	V
I_{IN}	DC Input Current	-10		10	mA
T_{OPR}	Operation Temperature	-40		85	degree °C
T_{STG}	Storage Temperature	-40		125	degree °C

ELECTRICAL SPECIFICATIONS

Table 3-2. Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes/Conditions
General					
Power Supply	3.0	3.3	3.6	V	
Power Consumption		450		mW	Normal Operation
Rx Path					
THD		70			
SNR		70			
AGC Gain Minimum Range		0		dB	12bit Control
AGC Gain Maximum Range		40		dB	12bit Control
AGC Step Size		0.4		dB	
AGC Step Error			0.2	dB	
AGC Input Range			2	Vppd	
LPF Cut Off Frequency		1104		kHz	5^{th} Butterworth
LPF Output Range			2	Vppd	
LPF Pass Band Ripple	-1		1	dB	
LPF Stop Band Attenuation	60			dB	At 4.416MHz
TX Path					
THD		70			
SNR		70			
AGC Gain Minimum Range		0		dB	8bit Control
AGC Gain Maximum Range		-24		dB	8bit Control
AGC Step Size		2		dB	
AGC Step Error			0.2	dB	

Table 3-2. Electrical Specifications (Continued)

Parameter	Min	Typ	Max	Units	Notes/Conditions
AGC Output Range			2	Vppd	
LPF Cut Off Frequency		138		kHz	5th Chebyshev
LPF Pass Band Ripple	-1		1	dB	
LPF Stop Band Attenuation	24			dB	At 276kHz
LPF Input Range			2	Vppd	
ADC					
Resolution		14		bits	
Effective Number Of Bits		13		bits	
Sampling Rate		4.416		MHz	Selectable 8.832MHz
Full Scale Input Range		2.0		Vppd	
DAC					
Resolution		14		bits	
Effective Number Of Bits		12		bits	
Sampling Rate		4.416		MHz	Selectable 8.832MHz
Full Scale Output Range		2.0		Vppd	
VCXO DAC					
Resolution		10		bits	
Sampling Rate		4		kHz	
Maximum Output Range		2.5		V	
Minimum Output Range		0.5		V	

SIGNAL DESCRIPTION

FUNCTIONAL BLOCK DIAGRAM

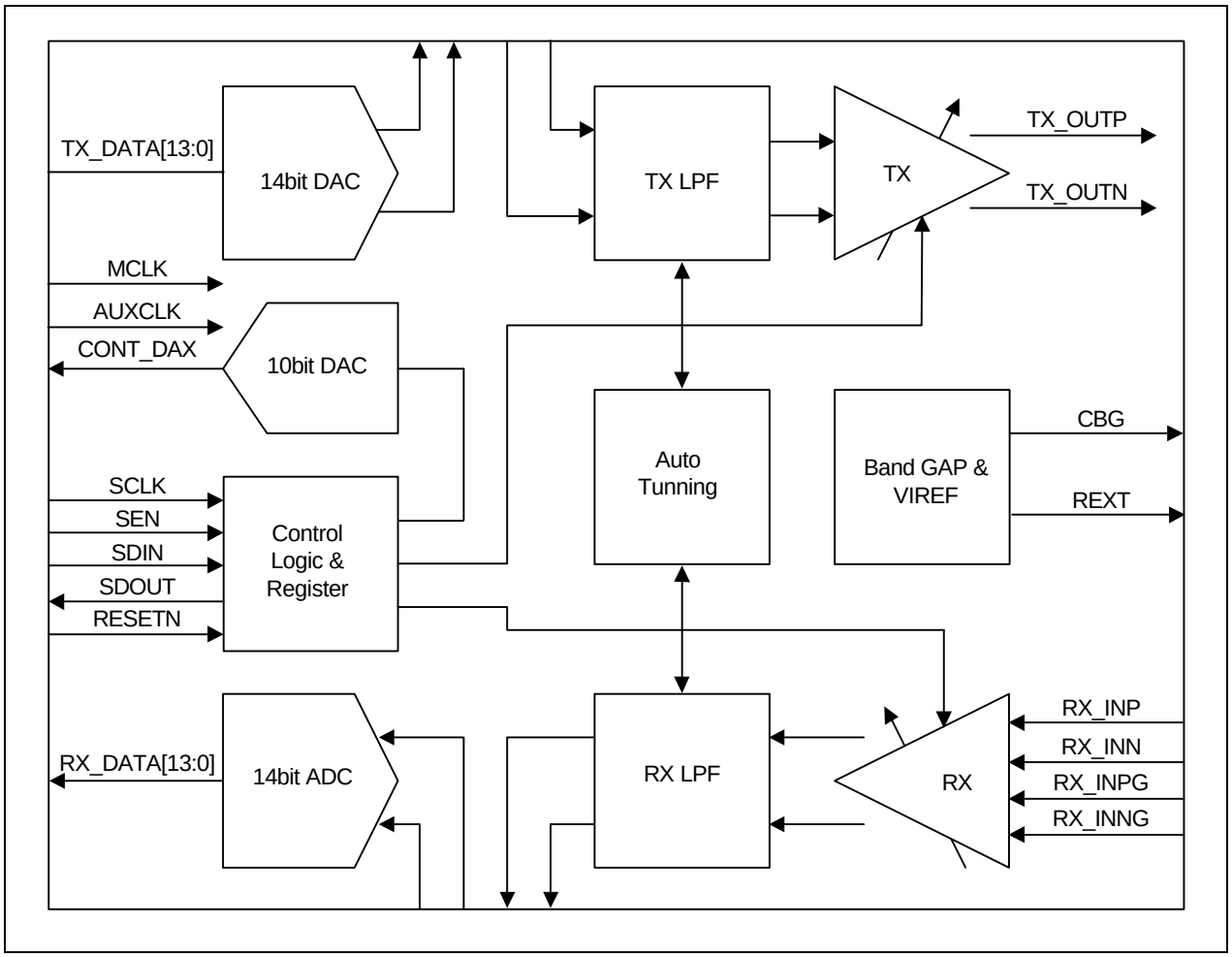

Figure 3-1. S5N8951X Functional Block Diagram

I/O PINS DESCRIPTION

Table 3-3. I/O Pins Description

Signal Name	Num	Type	I/O	Description
General Pins				
RESETN	47	CMOS	I	System Reset. Active Low
CS0	48	CMOS	I	Chip Select
TM1	49	CMOS	I	Digital Interface Selection “0” = 14bits, “1” = 7bits*2
TM0	50	CMOS	I	“0” = RT, “1” = CO
DAC Interface				
TX_DATA[13:0]	92~100, 1~5	CMOS	I	DAC 14bit Data Inputs If TM1=1, TX_DATA[13:7] is invalid
MCLK	6	CMOS	I	Master Clock 8.832MHz (Selectable 17.664MHz)
AUXCLK	10	CMOS	I	In 7bits Data Interface mode, AUXCLK=MCLK/2 In 14bits Data Interface mode, pin is open or ground.
TX_DACOP	88	Analog	-	DAC Current Positive Output for TX path
TX_DACON	87	Analog	-	DAC Current Negative Output for TX path
COMP_DAC	86	Analog	-	Compensation Capacitor 0.1uF Connection for TX path
IREF_DAC	85	Analog	-	External Resistor 1.24k Connection
ADC Interface				
RX_DATA[13:0]	11~ 24	CMOS	O	ADC 14bit Data Outputs (f TM1=1, [13:7] is always low)
RX_ADCIP	27	Analog	-	ADC Positive Input
RX_ADCIN	28	Analog	-	ADC Negative Input
BGR_ADC	31	Analog	-	ADC Band gap Reference Output
REFT_ADC	32	Analog	-	ADC Top Reference Output
REFB_ADC	33	Analog	-	ADC Bottom Reference Output
DSP Interface				
SCLK	43	CMOS	I	Serial Data Clock
SEN	44	CMOS	I	Serial Data Enable
SDOUT	45	CMOS	O	Serial Data Output
SDIN	46	CMOS	I	Serial Data Input
TX Pass Interface				
TX_OUTP	75	Analog	-	Tx Analog Positive Output
TX_OUTN	74	Analog	-	Tx Analog Positive Output
TX_FINP	83	Analog	-	Tx Filter Analog Positive Input
TX_FINN	84	Analog	-	Tx Filter Analog Negative Input

Table 3-3. I/O Pins Description (Continued)

Signal Name	Num	Type	I/O	Description
RX Pass Interface				
RX_INP	56	Analog	-	Rx Analog Positive Input
RX_INN	55	Analog	-	Rx Analog Negative Input
RX_INPG	54	Analog	-	Rx Analog External -14dB Gain Positive Input
RX_INNG	53	Analog	-	Rx Analog External -14dB Gain Negative Input
RX_FOUTP	30	Analog	-	Rx Filter Analog Positive Output
RX_FOUTN	29	Analog	-	Rx Filter Analog Negative Output
Voltage Reference				
TX_VCOM	78	Analog	-	TX Pass Common Mode Voltage
RX_VCOM	62	Analog	-	Rx Pass Common Mode Voltage
REXT_REF	65	Analog	-	Reference Current External Resistor 6.8K
VCXO Interface				
CONT_DAX	39	Analog	-	VCXO Control Voltage Output (Only RT)
CO Pass (TM0 = “1”)				
RX_AOUTP	58	Analog	-	Rx AGC Analog Positive Output
RX_AOUTN	59	Analog	-	Rx AGC Analog Negative Output
RX_FINN	60	Analog	-	Rx Filter Analog Negative Input
RX_FINP	61	Analog	-	Rx Filter Analog Positive Input
TX_AINP	79	Analog	-	Tx AGC Analog Positive Input
TX_AINN	80	Analog	-	Tx AGC Analog Positive Input
TX_FOUTN	81	Analog	-	Tx Filter Analog Negative Output
TX_FOUTP	82	Analog	-	Tx Filter Analog Negative Output
Power Supply				
AVDD_DAC	89	Supply	-	Tx Analog DAC VDD
ASUB_DAC	90	Supply	-	Tx Analog DAC SUB
AVSS_DAC	91	Supply	-	Tx Analog DAC VSS
DVDD_DAC	9	Supply	-	Tx Digital DAC VDD
DVSS_DAC	7,8	Supply	-	Tx Digital DAC VSS
AVDD_DAX	37	Supply	-	VCXO DAC Analog VDD
AVSS_DAX	38	Supply	-	VCXO DAC Analog VSS
AVDD_ADC	34	Supply	-	Rx Analog ADC VDD
ASUB_ADC	35	Supply	-	Rx Analog ADC SUB
AVSS_ADC	36	Supply	-	Rx Analog ADC VSS
DVDD_ADC	26	Supply	-	Rx Digital ADC VDD

Table 3-3. I/O Pins Description (Continued)

Signal Name	Num	Type	I/O	Description
DVSS_ADC	25	Supply	-	Rx Digital ADC VSS
AVDD_TX	76,77	Supply	-	Tx Path VDD
AVSS_TX	72,73	Supply	-	Tx Path VSS
ASUB_TX	71	Supply	-	TX Path SUB
AVDD_FAT	69,70	Supply	-	Filter Auto Tuning VDD
AVSS_FAT	67.68	Supply	-	Filter Auto Tuning VSS
AVDD_RX	57	Supply	-	Rx Filter VDD
AVSS_RX	52	Supply	-	Rx Filter VSS
ASUB_RX	51	Supply	-	Rx Filter SUB
AVDD_REF	66	Supply	-	Reference VDD
AVSS_REF	64	Supply	-	Reference VSS
ASUB_REF	63	Supply	-	Reference SUB
DVDD_CTL	40	Supply	-	Control Logic VDD
DSUB_CTL	41	Supply	-	Digital Substrate VSS
DVSS_CTL	42	Supply	-	Control Logic VSS

PIN CONFIGURATIONS (TOP VIEW)

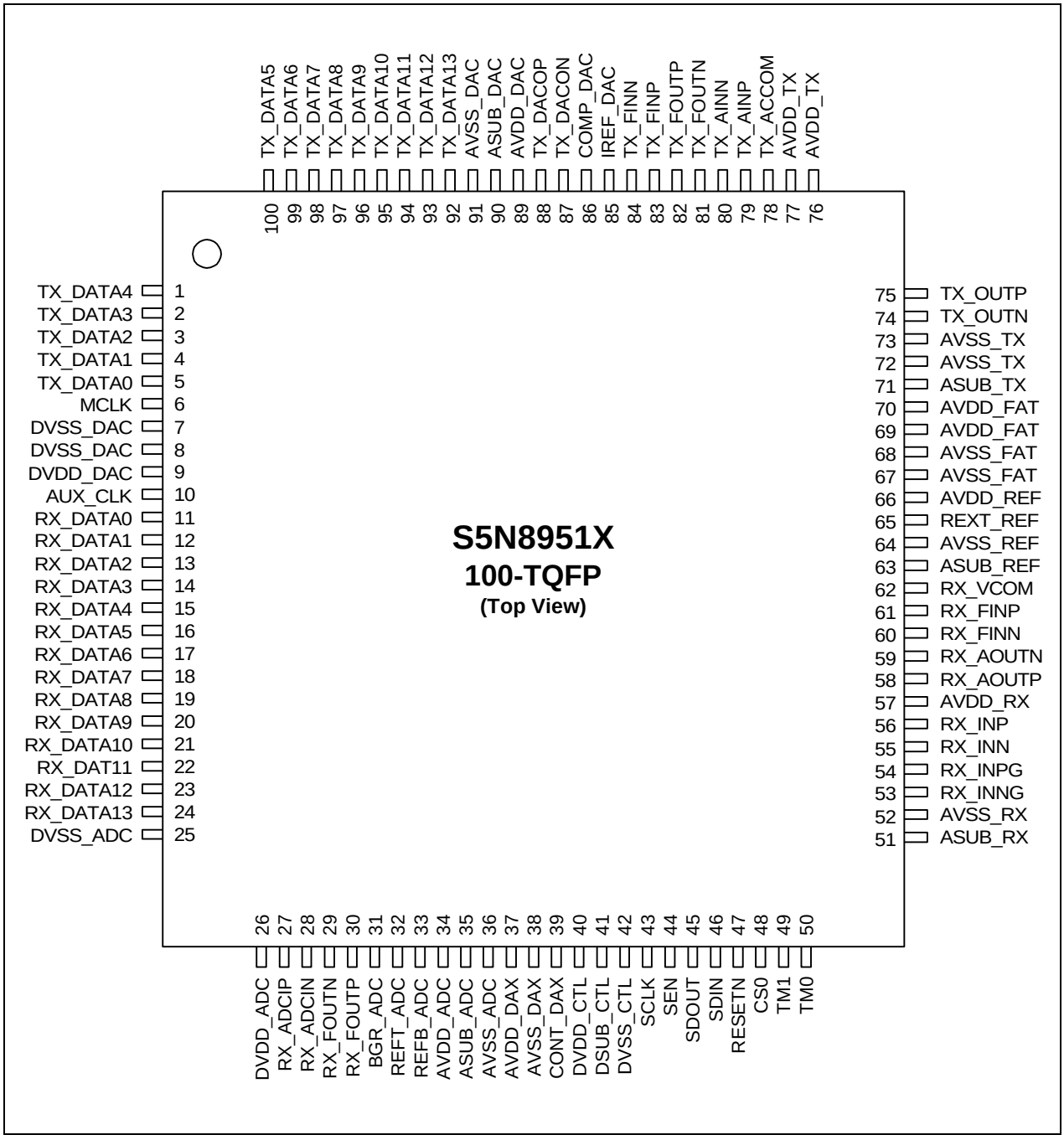

Figure 3-2. Pin Configurations (Top View)

BLOCK DESCRIPTIONS

ADC / DAC

S5N8951X has a 14bit resolution ADC 4.416M/8.832M sample frequency. The input of ADC is fully differential 2.0Vppd Max. The ADC transforms the signal into a digital 14bit output.

There are two type of DAC's in S5N8951X. One is for TX. It is 14bit 4.416MHz/8.832MHz frequency. Samsung's DMT (S5N8950) transmit 14bit parallel data to the AFE chip. The other DAC is for VCXO control. It has 10bit resolution 4kHz frequency. Internal registers of S5N8951X transform 10bit VCXO control serial data from DSP into 10bit parallel data. And VCXO output analog signal CONT_DAX (Pin #39).

TX/RX LPF

RX FILTERS

The combination of the external filter (an LC ladder filter typically) with the integrated low pass filter must provide:

— DMT sidelobe and out of band (anti-aliasing) attenuation

— Anti alias filter (60dB rejection @ image frequency)

— On chip tuning circuit included.

TX FILTERS

The TX Filters act not only to suppress the DMT sidebands but also as smoothing filters on the D/A converter's output to suppress the image spectrum.

For this reason they are realized in a time continuous approach and on chip tuning circuit included

TX/RX AGC

TX AGC has 0 ~ -24dB gains with 2dB step. It is controlled through 8bit serial digital signal from DSP. Internal registers of Samsung AFE Chips transform 8bit parallel control data. It outputs 2Vppd fully differential signal to line driver.

RX AGC has low noise 0~40dB gains with 0.4dB step and It is controlled through 12bit + 1MSB control signal. If 1MSB is high, another RX input pass pin#53 RX_INNG #54 RX_INNP (For example, external -14dB gain pass) is seclected. It inputs 2Vppd fully differential signal to RX LPF.

DIGITAL SIGNAL INTERFACE

COMMAND SIGNAL INTERFACE

This description hold for ATU-R (S5N8951X).

The chip consists of four kinds of register map:

— Power Control
— Transmitter AGC
— Receiver AGC
— VCXO Control
— Clock Selection

Serial interfaces use three pins:

— Clock
— Serial data input (25-bit: 2bit cs + 5bit address + 1bit r/w + 16 bit data + 1bit dummy)
— Serial data output (16 bit data)
— Enable

SERIAL DATA CONFIGURATION

Table 3-4. Serial Data Configuration

Register	Serial Data (SDAT)																							
	CS		Address					R/W	Data															Dummy
	CS1	CS0	A4	A3	A2	A1	A0	R/W	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X
PWR_CTL	CS0	CS0	X	X	0	0	0	R/W	X	X	X	X	X	X	X	X	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	X
TX_AGC	CS0	CS0	X	X	0	0	1	R/W	X	X	X	X	X	X	X	X	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	X
RX_AGC	CS0	CS0	X	X	0	1	0	R/W	X	X	X	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X
VCXO_CTL	CS0	CS0	X	X	0	1	1	R/W	X	X	X	X	X	X	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	X
CLK_SEL	CS0	CS0	X	X	1	0	0	R/W	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CK1	CK0	X

NOTE: X = Don't care
R/W =0 → Read
R/W =1 → Write

REGISTER MAP

Power Control

The power on/off control of AFE blocks on this chip is set by the PWR_CTL register, (XX000), as described below:

Table 3-5. PWR_CTL Register (A4A3A2A1A0=XX000)

Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Reset Value									0	0	0	0	0	0	0	0

Power Control is as follow.

Table 3-6. Power Control Register Value

PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	HEX	Descripcion
0	0	0	0	0	0	0	0	0000	Normal Operation
0	0	0	0	0	0	0	1	0001	N/A
0	0	0	0	0	0	1	0	0002	N/A
0	0	0	0	0	1	0	0	0004	TX DAC Power Down
0	0	0	0	1	0	0	0	0008	TX Filter & AGC Power Down
0	0	0	1	0	0	0	0	0010	RX ADC Power Down
0	0	1	0	0	0	0	0	0020	Rx Filter Power Down
0	1	0	0	0	0	0	0	0040	Rx AGC Power Down
1	0	0	0	0	0	0	0	0080	VCXO DAC Power Down
Adding Power Down (based on upper power down)									
0	0	0	0	0	0	1	1	0003	N/A
0	0	0	0	1	1	0	0	000C	TX Path Power Down
0	1	1	1	0	0	0	0	0070	Rx Path Power Down
1	1	1	1	1	1	1	1	00FF	Whole Chip Power Down

Transmitter AGC

The main functions of the TX path are controlled by the TX_AGC registers, as described below:

Table 3-7. TX_AGC Register (A4A3A2A1A0=XX001)

Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
Reset Value									0	0	0	1	0	0	0	1

TA[7:0] TX path output attenuator gain setting. 0 to –24dB attenuation in 2dB steps. (default is 0dB).

Table 3-8. Transmitter AGC Register Value

TA[7]	TA[6]	TA[5]	TA[4]	TA[3]	TA[2]	TA[1]	TA[0]	HEX	GAIN (dB)
0	0	0	1	0	0	0	1	0011	0
0	0	0	1	0	0	1	0	0012	-2
0	0	0	1	0	1	0	0	0014	-4
0	0	0	1	1	0	0	0	0018	-6
0	0	1	0	0	0	0	1	0021	-6
0	0	1	0	0	0	1	0	0022	-8
0	0	1	0	0	1	0	0	0024	-10
0	0	1	0	1	0	0	0	0028	-12
0	1	0	0	0	0	0	1	0041	-12
0	1	0	0	0	0	1	0	0042	-14
0	1	0	0	0	1	0	0	0044	-16
0	1	0	0	1	0	0	0	0048	-18
1	0	0	0	0	0	0	1	0081	-18
1	0	0	0	0	0	1	0	0082	-20
1	0	0	0	0	1	0	0	0084	-22
1	0	0	0	1	0	0	0	0088	-24

Recieve AGC

The main functions of the RX path are controlled by the RX_AGC register, as described below:

Table 3-9. RX_AGC Register (A4A3A2A1A0=XX010)

Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				RA 12	RA 11	RA 10	RA9	RA8	RA7	RA6	RA4	RA4	RA3	RA2	RA1	RA0
Reset Value				0	0	0	0	0	1	0	0	1	0	0	0	0

RA[11:0]: Receive path input gain setting 0 to 40dB gain in 0.4dB steps. (default is 0dB).

RA[12] is “1”,the external attenuation gain(For example –14dB) path pin#53 RX_INNG #54 RX_INPG will be enable. RA[12] should only be utilized the short line conditions.

Table 3-10. RX Gain Register Value

RA [12]	RA [11]	RA [10]	RA [9]	RA [8]	RA [7]	RA [6]	RA [5]	RA [4]	RA [3]	RA [2]	RA [1]	RA [0]	HEX	GAIN(dB)
1	0	0	0	0	1	0	0	1	0000 ~ 1111				1090 ~ 109F	-14.0 ~ -8.0
1	0	0	0	1	0	0	0	1	0000 ~ 1111				1110 ~ 111F	-8.0 ~ -2.0
1	0	0	1	0	0	0	0	1	0000 ~ 1111				1210 ~ 121F	-2.0 ~ 4.0
0	0	0	0	0	1	0	0	1	0	0	0	0	0090	0
0	0	0	0	0	1	0	0	1	0	0	0	1	0091	0.4
0	0	0	0	0	1	0	0	1	0	0	1	0	0092	0.8
0	0	0	0	0	1	0	0	1	0	0	1	1	0093	1.2
0	0	0	0	0	1	0	0	1	0	1	0	0	0094	1.6
0	0	0	0	0	1	0	0	1	0	1	0	1	0095	2.0
0	0	0	0	0	1	0	0	1	0	1	1	0	0096	2.4
0	0	0	0	0	1	0	0	1	0	1	1	1	0097	2.8
0	0	0	0	0	1	0	0	1	1	0	0	0	0098	3.2
0	0	0	0	0	1	0	0	1	1	0	0	1	0099	3.6
0	0	0	0	0	1	0	0	1	1	0	1	0	009A	4.0
0	0	0	0	0	1	0	0	1	1	0	1	1	009B	4.4
0	0	0	0	0	1	0	0	1	1	1	0	0	009C	4.8
0	0	0	0	0	1	0	0	1	1	1	0	1	009D	5.2
0	0	0	0	0	1	0	0	1	1	1	1	0	009E	5.6
0	0	0	0	0	1	0	0	1	1	1	1	1	009F	6.0
0	0	0	0	1	0	0	0	1	0000 ~ 1111				0110 ~ 011F	6.0 ~ 12.0
0	0	0	1	0	0	0	0	1	0000 ~ 1111				0210 ~ 021F	12.0 ~ 18.0
0	0	1	0	0	0	0	0	1	0000 ~ 1111				0410 ~ 041F	18.0 ~ 24.0
0	1	0	0	0	0	0	0	1	0000 ~ 1111				0810 ~ 081F	24.0 ~ 30.0
0	1	0	0	0	0	0	1	0	0000 ~ 1111				0820 ~ 082F	30.0 ~ 36.0
0	1	0	0	0	0	1	0	0	0000 ~ 1111				0840 ~ 084F	36.0 ~ 40.0

VCXO Control

The VCXO DAC is 10-bit voltage-mode DAC designed to be monotonic and intended to be

operated at a 4kHz update rate. In order to update the DAC, the user must write to the VCXO register through the serial port. The individual bit definitions are given below.

Table 3-11. VCXO_CTL Register (A4A3A2A1A0=XX011)

Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name							VC9	VC8	VC7	VC6	VC4	VC4	VC3	VC2	VC1	VC0
Reset Value							1	0	0	0	0	0	0	0	0	0

VC[9:0]: VCXO DAC 10-bit word. The DAC nominal output voltages for extreme and mid-scale codes are as follows.

— VC[9:0] = 0000000000 = 0.5V

— VC[9:0] = 1000000000 = 1.5V (mid-range)

— VC[9:0] = 1111111111 = 2.5V

A general expression for the DAC output voltage is

0.5V + (CODE / 1024) X (2.0V)

where *CODE* is the decimal integer value of the 10-bit word formed by VCXO[9:0].

Clock Selection

Main functions of Clock Selection are frequency selection of each MCLK/AUXCLK/ADC. The individual bit definitions are given below.

Table 3-12. CLK_SEL Register (A4A3A2A1A0=XX100)

Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name															CK1	CK0
Reset Value															0	0

TM1, CK[1:0]: Clock Selection has eight possible clocking configuration as follow.

Table 3-13. Clock Configuration

TM1	2 Phase	CK1	CK0	HEX	MCLK	AUXCLK	DAC	ADC
0	OFF	0	0	0000	4.416MHz	0	4.416MHz	2.208MHz
0	OFF	0	1	0001	4.416MHz	0	4.416MHz	4.416MHz
0	OFF	1	0	0002	8.832MHz	0	8.832MHz	4.416MHz
0	OFF	1	1	0003	8.832MHz	0	8.832MHz	8.832MHz
1	ON	0	0	0000	8.832MHz	4.416MHz	4.416MHz	4.416MHz
1	ON	0	1	0001	8.832MHz	4.416MHz	4.416MHz	2.204MHz
1	ON	1	0	0002	17.664MHz	8.832MHz	8.832MHz	8.832MHz
1	ON	1	1	0003	17.664MHz	8.832MHz	8.832MHz	4.416MHz

SERIAL DATA INTERFACE

Physical Interface

Serial interfaces use three pins:

— Clock
— Serial data (25-bit: 2bit cs + 5bit address + 1bit r/w + 16 bit data + 1bit dummy)
— Enable

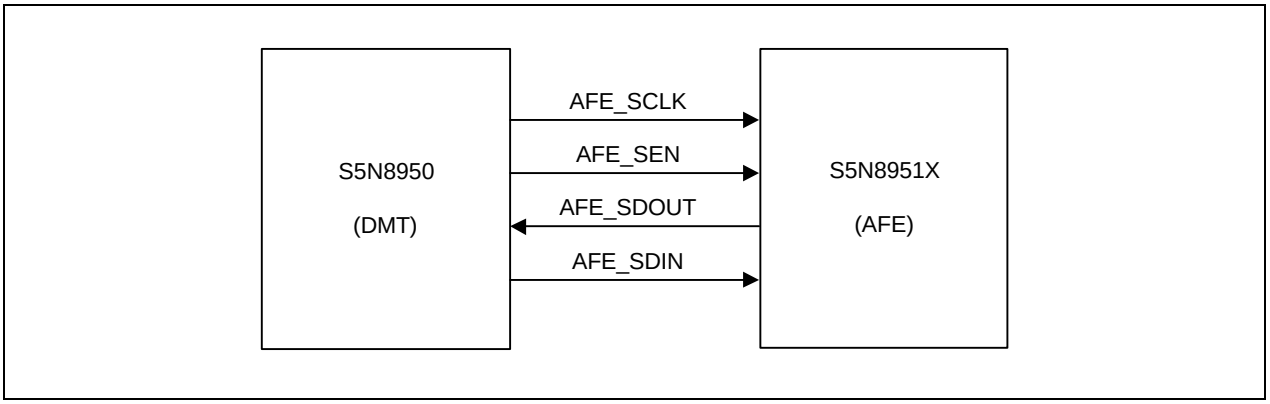

Figure 3-3. Control Register Interface

Waveform

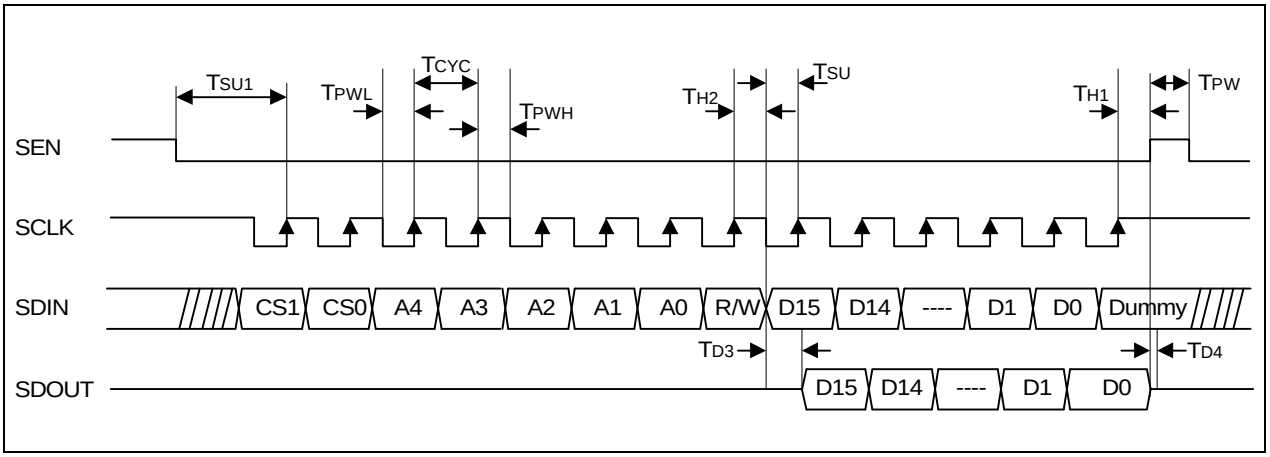

Figure 3-4. Register Control Waveform

Table 3-14. Register Control Timing

Parameter	Symbol	Min	Typ	Max	Unit	Note
SCLK Clock Period	T_{CYC}		905		nS	
SCLK High Time	T_{PWH}	452			nS	
SCLK Low Time	T_{PWL}	452			nS	
SEN Low To SCLK High	T_{SU1}	30			nS	
SCLK High to SEN High	T_{H1}	15			nS	
SEN Inactive Pulse Time	T_{PW}	905			nS	
SDIN Setup Time	T_{SU2}	15			nS	
SDIN Hold Time	T_{H2}	15			nS	
SCLK Low To SDOUT Delay	T_{D3}			30	nS	
SEN Inactive To SDOUT HiZ	T_{D4}			30	nS	

DATA INTERFACE

PHYSICAL INTERFACE

— ADC and DAC data transmission between S5N8951X and S5N8950

— Parallel Interface: 29 pin (14 ADC bit data, 14 DAC bit data, MCLK)

— Parallel Interface (2phase): 16 pin (7 ADC bit data, 7 DAC bit data, MCLK, AUXCLK)

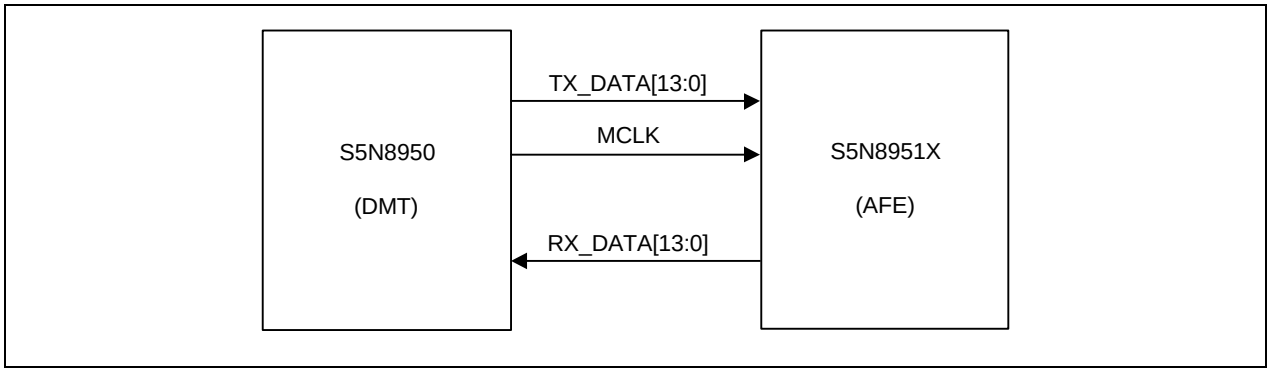

Figure 3-5. Data Interface

Waveform

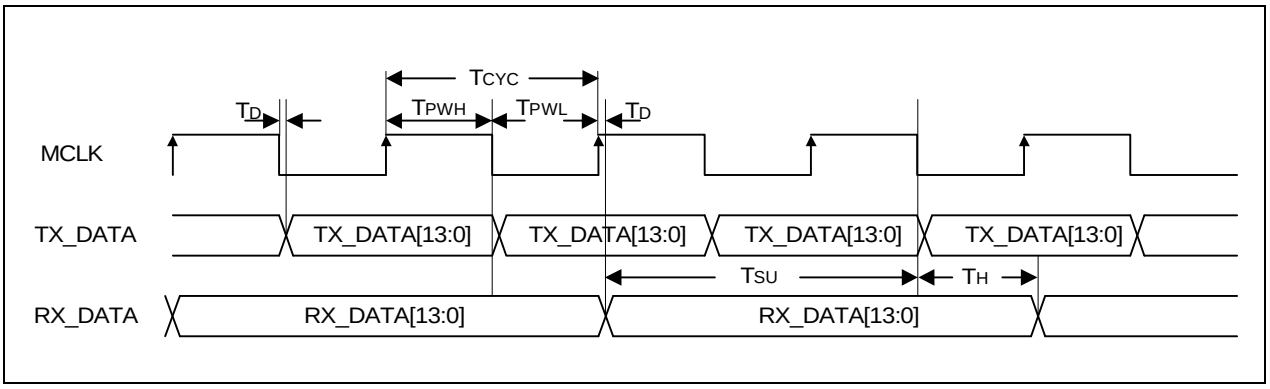

Figure 3-6. Data Interface Timing

Table 3-15. Data Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit	Note
MCLK Clock Period	T_{CYC}		113		nS	MCLK=4.416MHz
MCLK High Time	T_{PWH}		57		nS	MCLK=4.416MHz
MCLK Low Time	T_{PWL}		57		nS	MCLK=4.416MHz
DATA Delay after MCLK	T_{D}			10	nS	
RX_DATA setup to MCLK	T_{SU}	15			nS	MCLK=4.416MHz
RX_DATA hold to MCLK	T_{H}	42			nS	MCLK=4.416MHz
AUXCLK setup to MCLK	T_{SU2}			10	nS	
AUXCLK hold to MCLK	T_{H2}			10	nS	

APPLICATION CIRCUIT

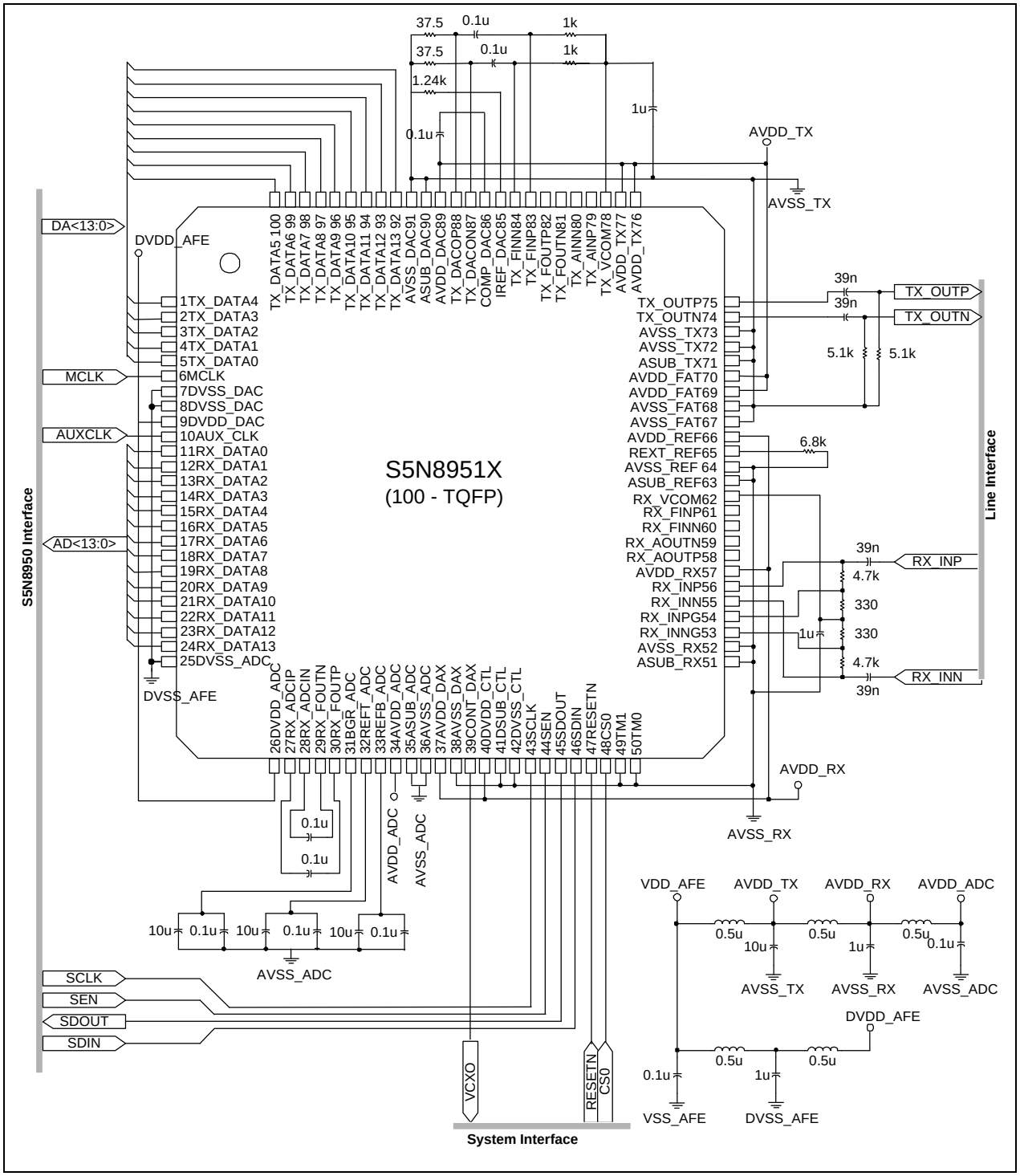

Figure 3-7. ATU-R Application Circuit

PACKAGE INFORMATION (100-TQFP-1414)

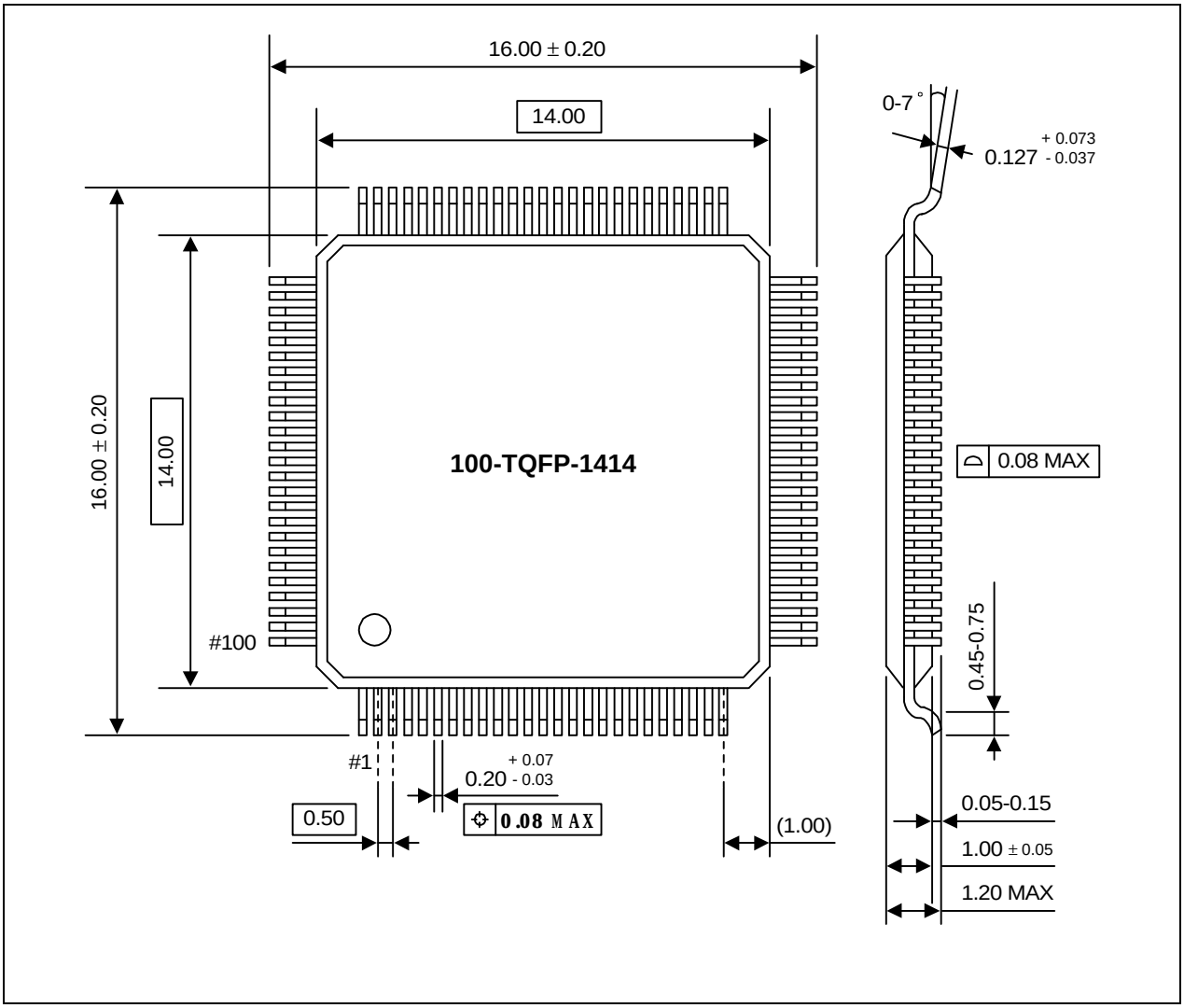

Figure 3-8. Package Dimension

Table 3-16. Revision History

Revision No.	Date	Description
1.0	2000-07-20	S5N8951X (Rev.1) Released.
2.0	2001-03-27	Pin Type changed (100-QFP-1420C → 100-TQFP-1414)