GENERAL DESCRIPTION

The M2006-11 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for clock frequency translation and jitter attenuation. It features serially programmable configuration of PLL frequency translation ratios, including FEC and inverse FEC. The device is similar to the M2006-04 (compatible pins and functions) but additionally provides automatic protection switching (APS) and automatic phase compensation functions.

FEATURES

- **Integrated SAW (surface acoustic wave) delay line**
- **VCSO frequency from 300 to 700MHz (Specify center frequency at time of order)**
- **Low phase jitter 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)**
- **Similar to the M2006-04 (and pin-compatible), except adds APS (automatic protection switching) and APC**
- **APS narrows loop bandwidth when switching input references to maintain GR-253 MTIE and TDEV compliance**
- **APS is triggered by a ≥ 4 ns clock phase change at input**
- **Automatic Phase Compensation (APC) function enables absorption of the input phase change.**
- **Narrow Bandwidth (NBW) control pin provides manual PLL control (set high for narrow bandwidth)**
- **Clock Add/Drop feature enables data FIFO centering**
- **Universal differential reference inputs support LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL**

PIN ASSIGNMENT (9 x 9 mm SMT)

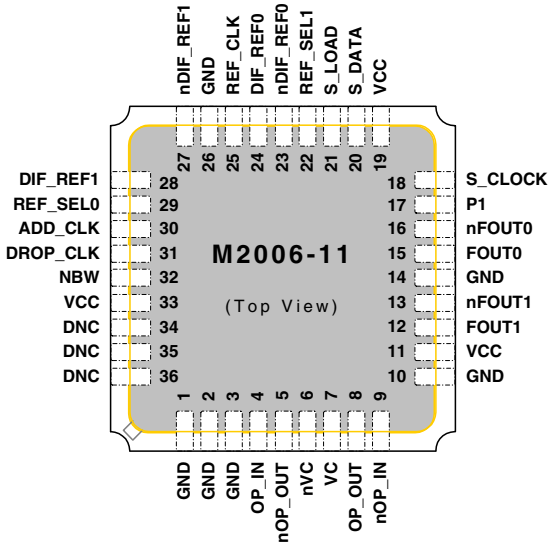


Figure 1: Pin Assignment

Example Input / Output Frequency Combinations

Input Clock (MHz)	VCSO Freq[1] (MHz)	Output Freq (MHz)	Application
19.44	622.08	622.08 155.52	OC-12/48
19.53125	625.00	156.25	Gigabit Ethernet

Table 1: Example Input / Output Frequency Combinations Using Power-up PLL Ratio

Note 1: Specify VCSO center frequency at time of order

- **Power-up default x32 multiplication ratio suitable for many optical networking applications**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

SIMPLIFIED BLOCK DIAGRAM

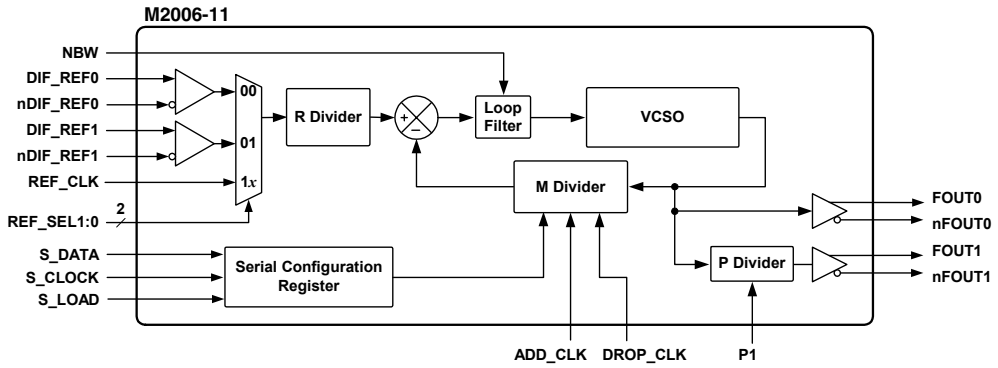


Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 8.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	FOUT1 nFOUT1	Output	No internal terminator	Clock output pairs. Differential LVPECL.
15 16	FOUT0 nFOUT0			
17	P1	Input	Internal pull-down resistor[1]	P Divider control. LVCMOS/LVTTL. For P1: Logic 1 sets divider to 4 Logic 0 sets divider to 1 See Table 5, P Divider Selection, on pg. 3
18 20 21	S_CLOCK S_DATA S_LOAD	Input	Internal pull-down resistors[1]	Serial input mode selection. LVCMOS/LVTTL. See Table 6, Serial Mode Function, on pg. 5 for how these three pins are used in combination.
22 29	REF_SEL1 REF_SEL0	Input	Internal pull-down resistors[1]	Reference clock input selection. LVCMOS/LVTTL. See Table 3, Reference Clock Input Selection, on pg. 3
23	nDIF_REF0	Input	Internal pull-up resistor[1]	Reference clock input pair 0. Differential LVPECL or LVDS.
24	DIF_REF0		Internal pull-down resistor[1]	
25	REF_CLK	Input	Internal pull-down resistor[1]	Reference clock input. LVCMOS/LVTTL.
27	nDIF_REF1	Input	Internal pull-up resistor[1]	Reference clock input pair 1. Differential LVPECL or LVDS.
28	DIF_REF1		Internal pull-down resistor[1]	
30	ADD_CLK	Input	Internal pull-down resistor[1]	Increases M divider count by 1 for one phase detector cycle, which adds one extra VCSO clock cycle over time (clock slip). LVCMOS/LVTTL.
31	DROP_CLK			Decreases M divider count by 1 for one phase detector cycle, which removes one VCSO clock cycle over time (clock slip). LVCMOS/LVTTL. See Table 9, Add / Drop Functions, on pg. 9.
32	NBW	Input	Internal pull-up resistor[1]	Narrow Bandwidth enable. LVCMOS/LVTTL: Logic 1 - Narrow loop bandwidth, R_{IN} set to 2MΩ Logic 0 - Wide (normal) bandwidth, R_{IN} set to 50kΩ
34, 35, 36	DNC			Do Not Connect.

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see **DC Characteristics** on pg. 10.

DETAILED BLOCK DIAGRAM

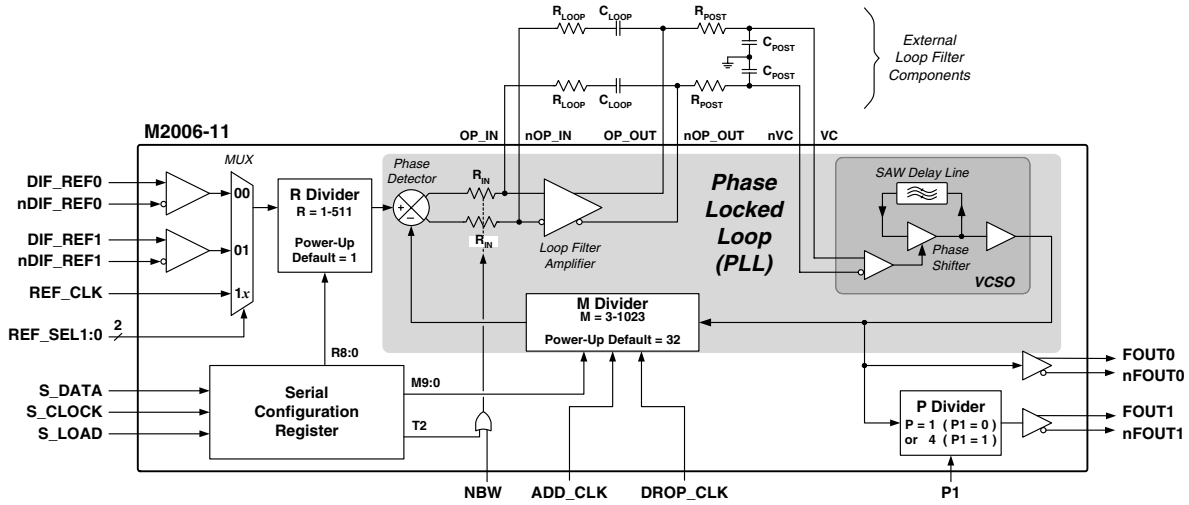


Figure 3: Detailed Block Diagram

PLL DIVIDER SELECTION TABLES

Reference Clock Input Selection

REF_SEL1:0 Pin Settings (Pins 22, 29)		Reference Input Selection
0	0	DIF_REF0, nDIF_REF0
0	1	DIF_REF1, nDIF_REF1
1	0	REF_CLK
1	1	

Table 3: Reference Clock Input Selection

Serial Programming M and R Divider Values

Serial Bits	Settings per Bit	Definition
T2:0	2 1 0	**Bandwidth and Test Values**
	0 0 0	Normal Bandwidth *
	1 0 0	Narrow Bandwidth *
	Note: T1 and T0, used for test automation, must be set to 0	
R8:0	8 7 6 5 4 3 2 1 0	**Feedback Divider Value "R"**
	0 0 0 0 0 0 0 0 1	R = 1 minimum, power-up default
	⋮	
	0 0 0 1 0 0 0 0 0	R = 16
	⋮	
	1 1 1 1 1 1 1 1 1	R = 511 maximum
M9:0	9 8 7 6 5 4 3 2 1 0	**Reference Divider Value "M"**
	0 0 0 0 0 0 0 0 1 1	M = 3 minimum
	⋮	
	0 0 0 0 1 0 0 0 0 0	M = 32 power-up default
	⋮	
	1 1 1 1 1 1 1 1 1 1	M = 1023 maximum

Table 4: Serial Programming M and R Divider Values

P Divider Selection

P1 Pin Setting (Pin 17)	P Divider Value	M2006-11-622.0800 Output Frequency, FOUT1 (MHz)
1	4	155.52
0	1	622.08

Table 5: P Divider Selector, Values, and Frequencies

Note *: If either the T2 bit or the NBW pin is asserted (logic 1, HIGH), the device goes into Narrow Bandwidth mode. See also Figure 4, Serial Configuration Register, on pg. 5 and the subsection titled Narrow Bandwidth (NBW) Pin, on pg. 7.

FUNCTIONAL DESCRIPTION

The M2006-11 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of three selectable input reference clocks.

An internal high "Q" SAW filter provides low jitter signal performance and controls the output frequency of the VCSO (Voltage Controlled SAW Oscillator).

The M2006-11 will default to a multiplying factor of 32 on power-up. The multiplying factor can be changed by serially programming the input and feedback dividers by way of the serial programming register.

A differential LVPECL signal provides the output clock for the device. A second differential output, which can be programmed to divide the output frequency by a factor of 4, is also available. The output frequency can be momentarily increased or decreased to add or subtract one net output clock cycle by asserting the ADD_CLK or DROP_CLK inputs, respectively.

An external loop filter sets the PLL bandwidth which can be optimized to provide jitter attenuation of the input reference clock.

The frequency agility, bandwidth control, and protection switch features make the M2006-11 ideal for use as a clock jitter attenuator, frequency translator, and clock frequency generator in OC-3 through OC-192 applications.

Input Reference Clocks

One input reference clock is selected from among two differential LVPECL clocks and one single-ended LVCMOS / LVTTL clock. The maximum input frequency is 700MHz.

The input reference clock is selected from DIF_CLK 0, DIF_CLK 1, or REF_CLK by selecting the appropriate REF_SEL0 and REF_SEL1 inputs.

The PLL

The PLL uses a phase detector and configurable dividers to synchronize the output of the VCSO with selected reference clock.

The “M Divider” divides the VCSO frequency, feeding the result into the phase detector. The selected input reference clock is divided by the “R Divider”. The result is fed into the other input of the phase detector.

The phase detector compares its two inputs. It then outputs pulses to the loop filter as needed to increase or decrease the VCSO frequency and thereby match and lock the divider output’s frequency and phase to those of the input reference clock.

M Divider, R Divider, and VCSO Frequency

The relationship between the VCSO (Fvcso) frequency, the M and R dividers, and the input reference frequency (Fref_clk) is:

$$Fvcso = Fref\_clk \times \frac{M}{R}$$

The ratio of M/R times input frequency must be such that it falls within the "lock" range of the VCSO.

On power-up the M and R dividers are set to 32 and 1, respectively. The M divider (10-bits) can be programmed for a maximum value of 1023 and a minimum value of 4. The R divider (9-bits) can be set to a maximum value of 511 and a minimum value of 1.

P Divider and Outputs

The M2006-11 provides a total of two differential LVPECL output pairs: FOUT0 and FOUT1. FOUT0 operates at the VCSO frequency while FOUT1 can operate at the VCSO frequency (Fvcso) or 1/4 Fvcso.

For example, FOUT1 can output 155.52MHz while FOUT0 outputs 622.08MHz.

One output divider (the “P” divider) is for the FOUT1 output pair. The P divider divides the VCSO frequency to produce one of two output frequencies (Fvcso or 1/4 Fvcso). The P1 pin selects the value for the P divider: logic 1 sets P to 4, logic 0 sets P to 1.

See Table 5, P Divider Selection, on pg. 3.

Serial Configuration Register

The M2006-11 is serially programmed by way of a three-wire interface, with the inputs being S_DATA, S_CLOCK, and S_LOAD.

When S_LOAD is LOW, configuration data is serially loaded from S_DATA into the Serial Configuration Register (or "shift register") with the rising edge of S_CLOCK. The T2 bit is loaded first, M0 last. (See point "a" in the timing diagram: "Figure 4, Serial Programming Timing Diagram," below.)

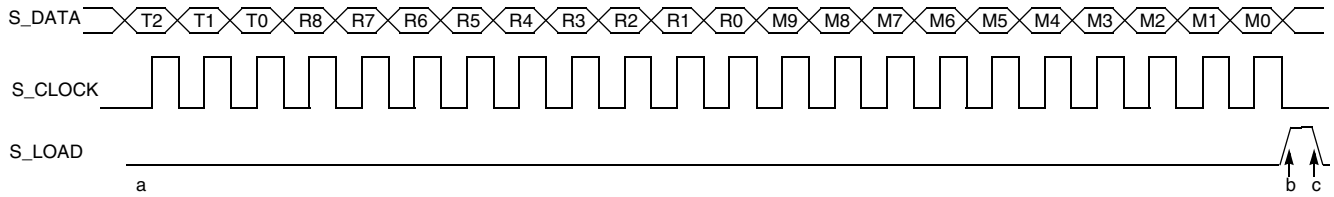
The contents of the shift register are loaded in parallel into the R and M dividers when S_LOAD transitions to HIGH (at point "b" in the timing diagram.)

The divider values are "latched" when S_LOAD transitions to LOW again (at point "c" in the diagram). This means the divider values remain loaded and unaffected by any serial input.

(If S_LOAD is held HIGH, any S_DATA input is passed directly to the R and M dividers on each rising edge of S_CLOCK.)

See also:
- Table 6, Serial Mode Function, below
- Figure 9, Setup and Hold Time, on pg. 12

Serial Programming Timing Diagram



Points a, b, and c used in section "Serial Configuration Register" above.
T1 and T0, which are used for test automation, must be set to 0.
T2 is set to 1 for normal bandwidth, 0 for narrow bandwidth. (If either NBW pin or T2 is asserted, device goes into Narrow Bandwidth mode.)

Figure 4: Serial Programming Timing Diagram

Serial Mode Function

L = Low; H = High; X = Don't care; ↑ = Rising Edge Transition; ↓ = Falling Edge Transition

S_LOAD	S_CLOCK	S_DATA	Conditions
L	↑	Data	Serial input mode. Shift register loads state of S_DATA on each rising clock of S_CLOCK. (However, serial input does not affect the values in the R and M dividers.)
↑	L	Data	Entire contents of the shift register are passed (in parallel) to the R and M dividers.
↓	L	Data	R and M divider values are latched.
L	X	X	Serial input does not affect the values in the R and M dividers.
H	↓	Data	Serial input affects dividers: S_DATA passed directly to R and M dividers as it is clocked.

Table 6: Serial Mode Function

Automatic Protection Switch (APS)

The M2006-11 includes a proprietary automatic protection switch (APS) circuit that prevents excessive phase transients of the output clocks upon input reference rearrangement. Upon the occurance of an input reference phase change, or phase transient, PLL bandwidth is lowered by the APS circuit. This limits the rate of phase change in the output clocks. With proper configuration of the external loop filter, the output clocks will comply with MTIE (maximum time interval error) specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The APS circuit uses a dedicated phase error detector at the PLL phase detector to detect a clock phase change. During normal operation with a stable reference clock, the PLL will be frequency locked and phase locked, resulting in very little error at the phase detector (<1 ns). Upon the selection of a new input reference clock at a different clock phase, a phase error will occur at the phase detector. The APS circuit is triggered with a phase error greater than 4 ns, upon which a narrow PLL bandwidth is applied. When the PLL locks to within 2 ns error at the phase detector, wide bandwidth (normal) operation is resumed.

The APS circuit is not suitable for situations in which an unstable reference is used. Under normal conditions the reference clock jitter should not induce phase jitter at the phase detector beyond 2 ns. (This includes when subjecting the system to jitter tolerance compliance testing.)

Because of this, the M2006-11 is not recommended for use with some Stratum DPLL clock sources, or with unstable recovered network clocks intended for loop timing configuration. It is also not recommended for complex FEC ratios where the phase detector is operated at less 1 MHz. For these applications the M2006-04 is suggested.

(The M2006-04 is identical to the M2006-11 except that it does not include the APS function or the APC function discussed in the following section.)

Automatic Phase Compensation (APC)

The M2006-11 also includes an automatic phase compensation (APC) circuit that is automatically enabled in conjunction with the APS circuit.

The APC circuit enables the PLL to absorb most of the phase change of the input clock which reduces re-lock time and also the generation of wander. (Wander is created in this case by the generation of extra output clock cycles.)

The APC circuit is triggered by same >4 ns phase transient (at the phase detector) that triggers the APS circuit. Once triggered, a new VCSO clock edge is selected for the phase detector feedback input. (The clock edge selected is the one closest in phase to the new input clock phase.) The residual phase detector phase error following reselection is approximately 3-to-4 ns. The narrow bandwidth selected by the APS circuit minimizes VCSO drifting and switch transients during the process.

Narrow Bandwidth (NBW) Pin

The M2006-11 includes a manual narrow bandwidth (NBW) setting that can be selectively enabled by asserting the NBW input (pin 32) to logic 1. When the NBW pin is logic 0, the M2006-11 operates in the nominal wider bandwidth mode.

If either NBW pin or the serially programmed T2 bit is asserted (logic 1, HIGH), the device goes into Narrow Bandwidth mode. See Table 4, Serial Programming M and R Divider Values, on pg. 3 and Figure 4, Serial Configuration Register, on pg. 5

In relation to the APS circuit, the NBW setting functions as follows:

- Setting NBW to logic 1, the NBW function overrides the APS circuit to force narrow bandwidth mode.
- Setting NBW to logic 0, the APS circuit can automatically turn on and off narrow bandwidth mode.

The NBW pin operates by controlling the values of R_{IN}, an internal loop filter component as illustrated in Figure 3, pg. 3. In normal operation when NBW is set to logic 0, R_{IN} = 16kΩ When NBW is asserted to logic 1, R_{IN} is increased to 2MΩ

NBW Pin Setting (Pin 32)	Internal Value R_{IN} [1]	PLL Configuration (Loop Bandwidth)
0	50kΩ	Normal Loop Bandwidth
1	2MΩ	Narrow Loop Bandwidth

Table 7: NBW Pin Settings

Note 1: With the same set of loop filter components

Compared to normal operation (when pin NBW = logic 0), setting NBW to logic 1 does the following:

- Loop bandwidth is decrease by a factor of 40
- Loop damping factor is decreased by a factor of 6.3

Indiscriminate use of the NBW pin can lead to an under damped loop configuration. A loop damping factor of >0.5 should be maintained to assure stable loop operation.

The NBW pin is useful for two main applications:

- NBW can be selectively asserted high to manually assert and hold a temporary narrow loop bandwidth operation during the phase locking to a newly selected clock reference input. When configured with the right loop filter component values, this can assure that M2006-11 clock output slew rate is sufficiently decreased to meet GR-253-CORE MTIE and TDEV.
- NBW can be tied to logic 1 to permanently enable lower loop bandwidth which might be preferred for a given jitter attenuation application.

Loop Bandwidth Calculator

A free loop bandwidth calculator is available.

Call 508-852-5400, ICS Communications Modules business unit (CMBU), Worcester, MA.

This calculator can be used to determine the loop filter values needed to obtain a desired loop bandwidth and damping factor. Pass band peaking can also be calculated. The calculator is also useful for understanding the effect of the NBW selection on loop filter characteristics.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2006-11 requires the use of an external loop filter components. These are connected to the provided filter pins (see Figure 5). Due to the differential signal path design, the implementation consists of two identical complementary RC filters as shown in Figure 5, below.

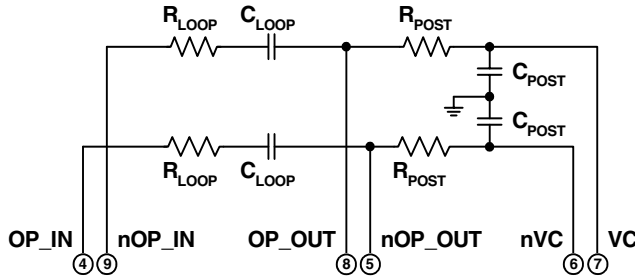


Figure 5: External Loop Filter

PLL bandwidth is affected by the "M" value as well as the VCSO frequency. See Table 8, External Loop Filter Component Values, on pg. 8.

External Loop Filter Component Values [1]
M2006-11-622.080

VCSO Parameters: K_{VCO} = 800kHz/V, VCSO Bandwidth = 70kHz

Device Configuration						Example External Loop Filter Component Values				Nominal Performance Using These Values		
F_{Ref} (MHz)	$F_{Phase\ Detector}$ (MHz)	F_{VCSO} (MHz)	M Divider Value	NBW Pin	R_{IN}	R loop	C loop	R post	C post	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
19.44	19.44	622.08	32	0	50k	39kΩ	0.10µF	20kΩ	220pF	3.4kHz	4.4	0.1
				1	2M					115Hz	0.7	2.2
19.44	19.44	622.08	32	0	50k	150kΩ	0.10µF	82kΩ	15pF	14kHz	16.77	0.001
				1	2M					310Hz	2.7	0.25
19.44	19.44	622.08	32	0	50k	910Ω	10µF	100kΩ	220pF	770Hz	10	0.02
				1	2M					20Hz	1.6	0.5
155.52	155.52	622.08	4	0	50k	15kΩ	0.10µF	100kΩ	15pF	10kHz	4.7	0.1
				1	2M					338Hz	0.75	2.0
155.52	155.52	622.08	4	0	50k	2kΩ	10µF	50kΩ	220pF	1.4kHz	6.3	0.05
				1	2M					40Hz	1	1.25

Table 8: External Loop Filter Component Values

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking.

Add / Drop Clock

The ADD_CLK and DROP_CLK inputs increment or decrement the M (feedback) divider on the rising edge of the Add or Drop clock for one phase detector cycle. This results in a momentary increase or decrease in output frequency and an extra or missing VCSO output clock cycle (clock slip) relative to the input reference clock.

The ADD_CLK (pin 30) and DROP_CLK (pin 31) inputs are intended to be used for pointer realignment in the data channel FIFO register. The assertion of either pin imparts a single VCSO cycle slip over time. The rate at which the cycle occurs is determined by the loop filter bandwidth, which is influenced by the external loop filter components selection (see Table 8, External Loop Filter Component Values, on pg. 8).

Adding One Clock Cycle

When ADD_CLK is transitioned from low to high, one extra clock will be output by the VCSO relative to the reference input. This is accomplished by incrementing the feedback divider (M Divider) by one count for one phase detector cycle period (one R Divider output cycle).

This incrementing of the feedback divider creates an immediate error at the phase detector input equal to one VCSO clock cycle. In the process of relocking the phase of the M Divider output to the R Divider output, the PLL forces the VCSO frequency to slightly increase (several ppm) and then decrease once locked. The net effect is a single “cycle slip” of the VCSO over several milliseconds. A VCSO frequency of 622.08MHz represents a cycle time of 1.6 nsec, which is the phase error imparted on the phase detector with one ADD_CLK command.

The rate of cycle slip is controlled by the loop bandwidth during normal operation as listed in Table 8. The APS circuit, which lowers loop bandwidth following an input transient over 4 ns, is not invoked unless is there is also high phase noise on the reference clock input.

Dropping One Clock Cycle

The DROP_CLK pin works the same way, except that when this pin transitions from to low to high, the feedback counter is decremented by one count which subtracts one VCSO output clock over time.

How Assertions Affect the Add / Drop Functions

Both ADD_CLK and DROP_CLK modify the M Divider following the next rising edge of the reference clock into the phase detector (the R Divider output). Only one ADD_CLK assertion or DROP_CLK assertion can be made per phase detector clock cycle. Additional assertions during a given phase detector cycle will be ignored. Additional assertions prior to phase detector realignment will accumulate as additional phase detector error, and will cause further VCSO frequency offset.

An accumulated offset of over 4 nsec will trigger the APS mode, which will lower the loop bandwidth accordingly until the phase error is less than 2 ns.

How Output Divider Affects the Add / Drop Functions

The divider block (P Divider) between the VCSO output and the FOUT1 clock output pair also influences the effect of ADD_CLK and DROP_CLK assertions relative to the FOUT1 output. When P1 is low (forces P Divider = 1) the ADD_CLK or DROP_CLK pin will add or subtract one entire clock cycle upon a single assertion (this is always true for the FOUT0 output clock pair). When P1 is high (forces P Divider = 4) the ADD_CLK or DROP_CLK pin will add or subtract one quarter of a clock cycle upon a single assertion, as would be expected by the clock division.

Add / Drop Functions

X = Don't care; ↑ = Rising Edge Transition

ADD_CLK	DROP_CLK	Conditions
↑	X	Adds one extra clock cycle to the VCSO clock output, over time, when asserted.
X	↑	Subtracts one clock cycle to the VCSO clock output, over time, when asserted.

Table 9: Add / Drop Functions

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 10: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings ard stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage	3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	0		+70	°C

Table 11: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3 Volts ± 5%, T_A = 0 °C to 70 °C, VCSO Frequency = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
	I_{CC}	Power Supply Current			162		mA
Differential Inputs	V_{P-P}	Peak to Peak Input Voltage	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.15			V
	V_{CMR}	Common Mode Input		0.5		V_{cc} - .85	V
LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	P1, S_LOAD, S_CLOCK, S_DATA, REF_SEL0, REF_SEL1, REF_CLK, ADD_CLK, DROP_CLK, NBW	2		V_{cc} + 0.3	V
	V_{IL}	Input Low Voltage		-0.3		0.8	V
Inputs with Pull-down	I_{IH}	Input High Current	(All Inputs *except* nDIF_REF0, nDIF_REF1, NBW)			150	µA
	I_{IL}	Input Low Current		-5			µA
	$R_{pulldown}$	Internal Pull-down Resistor			51		kΩ
Inputs with Pull-up	I_{IH}	Input High Current	nDIF_REF0, nDIF_REF1, NBW			5	µA
	I_{IL}	Input Low Current		-150			µA
	R_{pullup}	Internal Pull-up Resistor			51		kΩ
All Inputs	C_{in}	Input Capacitance	All Inputs			4	pF
Differential Outputs	V_{OH}	Output High Voltage	FOUT_0, nFOUT_0, FOUT_1, nFOUT_1	V_{cc} - 1.4		V_{cc} - 1.0	V
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V
	V_{P-P}	Peak to Peak Output Voltage		0.6		0.85	V

Table 12: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3 Volts ± 5%, T_A = 0 °C to 70 °C, VCSO Frequency = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V

Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
F_{IN}	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.3		700	MHz	
		S_CLOCK			50	MHz	
		REF_CLK	0.3		200	MHz	
F_{PD}	Phase Detector Frequency Range				175	MHz	
F_{OUT}	Output Frequency Range	FOUT0, nFOUT0, FOUT1, nFOUT1	75		700	MHz	
APR	VCSO Pull-Range		±120	±200		ppm	
Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-72		dBc/Hz	Fin=19.44_MHz M=32, R=1
		10kHz Offset		-94		dBc/Hz	
		100kHz Offset		-123		dBc/Hz	
J(t)	Jitter (rms)	12kHz to 20MHz		0.5		ps	
		50kHz to 80MHz		0.5		ps	
odc	Output Duty Cycle [1]		40	50	60	%	P1 = 0 or 1
t_R	Output Rise Time [1] for FOUT0, nFOUT0 and FOUT1,nFOUT1	P1 = 0	200	275	400	ps	20% to 80%
t_F	Output Fall Time [1] for FOUT0, nFOUT0 and FOUT1,nFOUT1	P1 = 0	200	275	400	ps	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK	5			ns	
		S_CLOCK to S_LOAD	5			ns	
t_H	Hold Time	S_DATA to S_CLOCK	5			ns	
		S_CLOCK to S_LOAD	5			ns	
t_{LOCK}	PLL Lock Time				100	ms	
t_{IPW}	Input Pulse Width[1]	S_LOAD	10			ns	
		ADD_CLK	10			ns	
		DROP_CLK	10			ns	
MTIE	Mean Time Interval Error			Compliant with GR-253-CORE			

Note 1: See Parameter Measurement Information on pg. 12.

Table 13: AC Characteristics

PARAMETER MEASUREMENT INFORMATION

Input and Output Rise and Fall Time

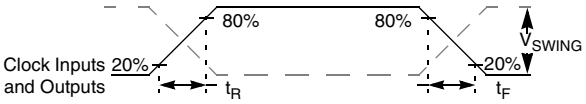


Figure 6: Input and Output Rise and Fall Time

Output Duty Cycle

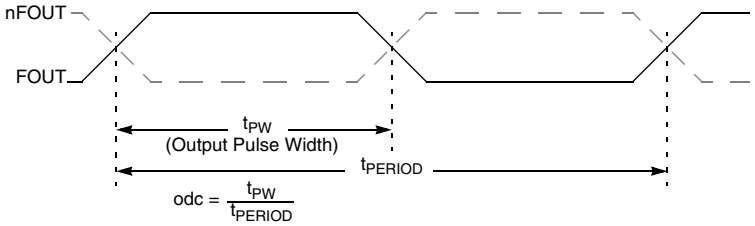


Figure 7: Output Duty Cycle

Differential Input Level

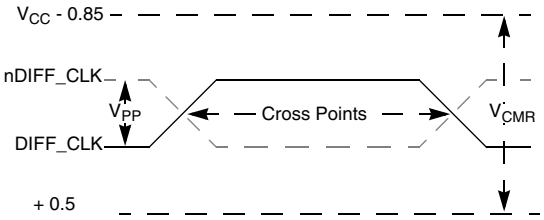


Figure 8: Differential Input Level

Setup and Hold Time

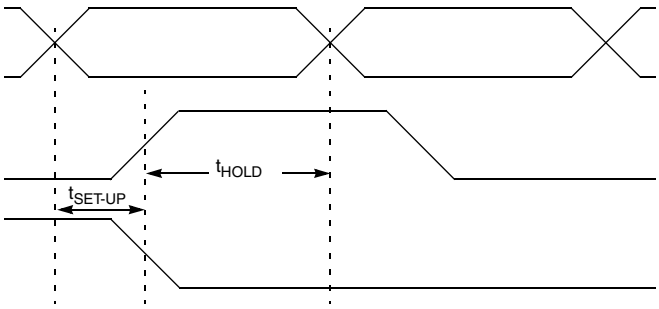


Figure 9: Setup and Hold Time

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

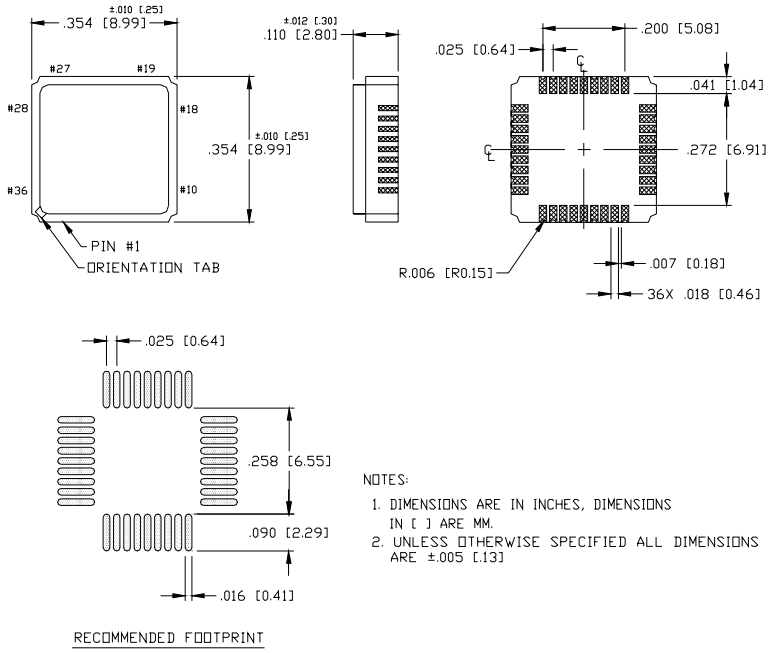


Figure 10: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

For VCSO Frequency (MHz)	Order Part Number
622.08	**M2006-11-622.0800**

Table 14: Ordering Information

Consult ICS for the availability of other VCSO frequencies.