4Mb Late Write HSTL High Speed Synchronous SRAM (256K x 18 Organization)

## Description

The CXK77B1840 is a high speed BiCMOS synchronous static RAM with common I/O pins, organized as 262,144-words by 18-bits. This synchronous SRAM integrates input registers, high speed RAM, output registers/latches, and a one-deep write buffer onto a single monolithic IC. Four different read protocols - Register-Register (R-R), Register-Latch (R-L), Register-Flow Thru (R-FT), and Dual Clock (DC), and an enhanced write protocol - Late (Delayed) Write (LW), are supported, providing a flexible, high-performance user interface.

All input signals except $\overline{G}$ (Output Enable) and ZZ (Sleep Mode) are registered on the positive edge of K clock.

Read cycles can be controlled in one of four ways - with registered outputs in Register-Register mode, with latched outputs in Register-Latch mode, with flow-through outputs in Register-Flow Thru mode, or with registered outputs using a dedicated output control clock (C clock) in Dual Clock mode. The read protocol is user-selectable through external mode pins M1 and M2.

Write cycles follow a Late Write protocol, where data is provided to the SRAM one clock cycle after the address and control signals, eliminating one dead cycle from Read-to-Write transitions. In this scheme, when a write cycle is initiated, the address and data stored in the SRAM's write buffer during the previous write cycle are directed to the SRAM's memory core, while, simultaneously, the address and data from the current write cycle are stored in the SRAM's write buffer. In both Register-Latch and Register-Flow Thru modes, when $\overline{SW}$ (Global Write Enable) is driven active, the subsequent positive edge of K clock tri-states the SRAM's output drivers immediately, allowing consecutive Read-Write-Read operations. The write cycle is internally self-timed, which eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The output drivers are series terminated, and the output impedance is programmable through an external impedance matching resistor RQ. By connecting RQ between ZQ and $V_{SS}$, the output impedance of all 18 DQ pins can be precisely controlled.

Sleep (power down) mode control is provided through the asynchronous ZZ input. 250 MHz operation is obtained from a single 3.3V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

## Features

| | | R-R Mode | R-L, R-FT Modes | **DC Mode** |
|---|---|---|---|---|
| • Fast Cycle/Access Time | | $t_{KHKH}$ / $t_{KHQV}$ | $t_{KHKH}$ / $t_{KHQV}$ | $t_{KHKH}$ / $t_{KHQV}$ |
| CXK77B1840 | -4A | 4.0ns / 2.3ns | 4.8ns / 4.8ns | 4.0ns / 5.2ns |
| | -4 | 4.0ns / 2.3ns | 5.3ns / 5.3ns | 4.0ns / 5.2ns |
| | -45A | 4.0ns / 2.3ns | 5.3ns / 5.3ns | 4.5ns / 6.0ns |
| | -45 | 5.0ns / 2.5ns | 6.5ns / 6.5ns | 4.5ns / 6.5ns |

Note: Contact Sony Memory Marketing for availability of DC mode functionality.

- 4 synchronous modes of operation, selectable by mode pins:
  Register-Register; Register-Latch; Register-Flow Thru; Dual Clock
- Single +3.3V power supply: 3.3V ± 5%
- Dedicated output supply voltage: $V_{DDQ}$ (1.5V typical)
- Inputs and outputs are HSTL / extended HSTL compatible.
- Differential clock input (K/$\overline{K}$, C/$\overline{C}$).
- All inputs (except asynchronous $\overline{G}$ and ZZ) and outputs are registered on a single clock edge.
- Byte Write capability.
- Late Write scheme to eliminate one dead cycle from Read-to-Write transitions.
- Self-timed write cycles.
- Sleep (power down) mode.
- JTAG boundary scan (subset of IEEE standard 1149.1).
- 119 pin (7x17) Plastic Ball Grid Array (PBGA) package.

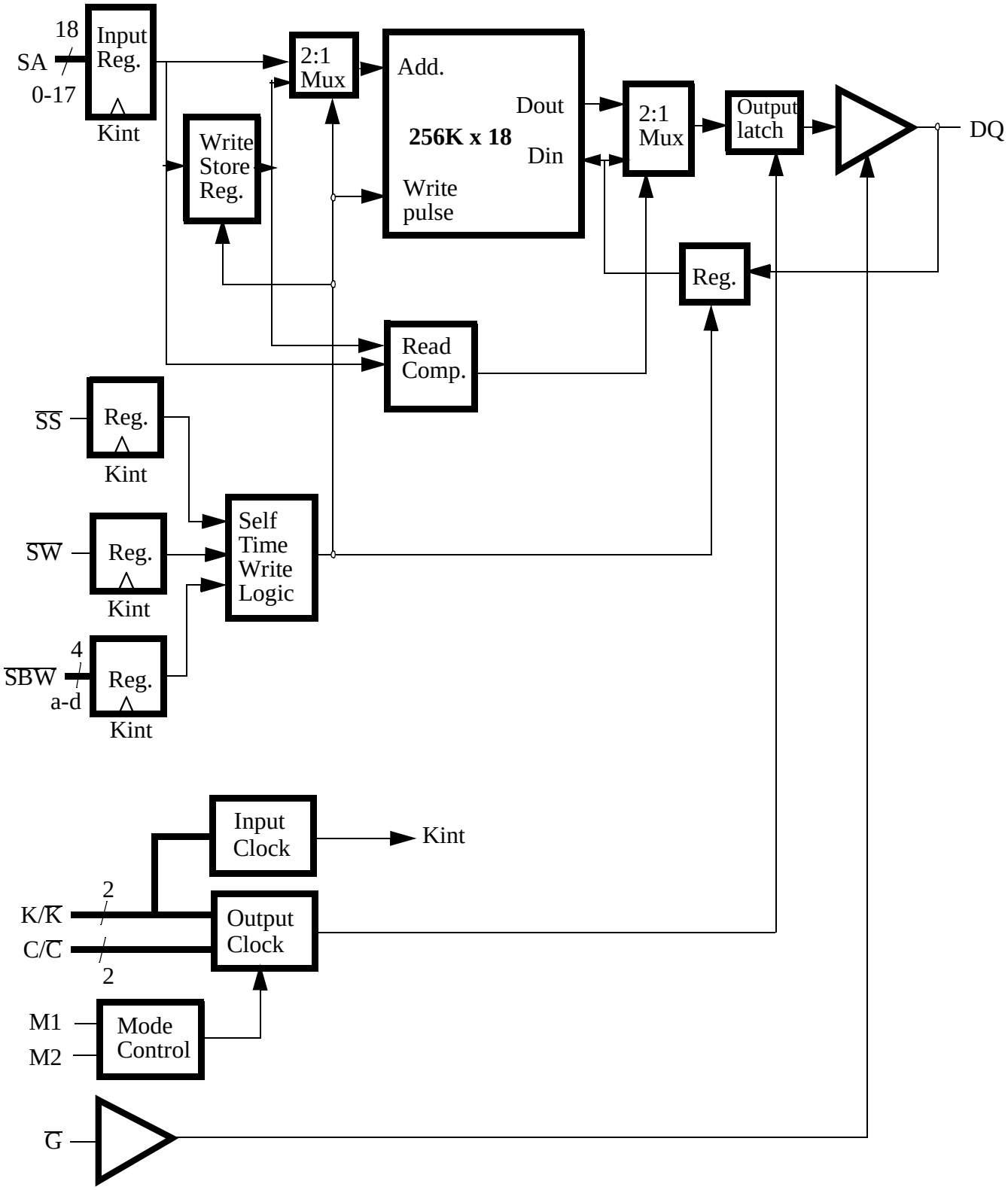
## Pin Configuration (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | SA6 | SA7 | NC | SA3 | SA2 | $V_{DDQ}$ |
| B | NC | NC | SA8 | NC | SA4 | NC | NC |
| C | NC | SA12 | SA5 | $V_{DD}$ | SA0 | SA13 | NC |
| D | DQ0b | NC | $V_{SS}$ | ZQ | $V_{SS}$ | DQ8a | NC |
| E | NC | DQ1b | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | NC | DQ7a |
| F | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | DQ6a | $V_{DDQ}$ |
| G | NC | DQ2b | $\overline{SBW}$b | $\overline{C}$ | $V_{SS}$ | NC | DQ5a |
| H | DQ3b | NC | $V_{SS}$ | C | $V_{SS}$ | DQ4a | NC |
| J | $V_{DDQ}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{DDQ}$ |
| K | NC | DQ4b | $V_{SS}$ | K | $V_{SS}$ | NC | DQ3a |
| L | DQ5b | NC | $V_{SS}$ | $\overline{K}$ | $\overline{SBW}$a | DQ2a | NC |
| M | $V_{DDQ}$ | DQ6b | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| N | DQ7b | NC | $V_{SS}$ | SA14 | $V_{SS}$ | DQ1a | NC |
| P | NC | DQ8b | $V_{SS}$ | SA11 | $V_{SS}$ | NC | DQ0a |
| R | NC | SA10 | M1 | $V_{DD}$ | M2 | SA15 | NC |
| T | NC | SA17 | SA9 | NC | SA1 | SA16 | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

## Pin Description

| Symbol | Description | Symbol | Description | Symbol | Description |
|---|---|---|---|---|---|
| SA | Address Input (0-17) | $\overline{G}$ | Async. Output Enable | $V_{DDQ}$ | Output Power Supply |
| DQ | Data I/O (0-8), Bytes a,b | ZZ | Async. Sleep Mode | $V_{SS}$ | Ground |
| K,$\overline{K}$ | Differential Input Clocks | TCK | JTAG Clock (LVTTL) | $V_{REF}$ | Input Reference Voltage |
| C,$\overline{C}$ | Differential Output Control Clocks | TMS | JTAG Mode Select (LVTTL) | ZQ | Output Impedance Control Resistor Input |
| $\overline{SW}$ | Write Enable, Global | TDI | JTAG Data In (LVTTL) | M1,M2 | Mode Select |
| $\overline{SBW}$x | Write Enable, Bytes a,b | TDO | JTAG Data Out (LVTTL) | NC | No Connect |
| $\overline{SS}$ | Synchronous Select | $V_{DD}$ | +3.3V Power Supply | | |

# BLOCK DIAGRAM



## •Truth Tables

### Register - Register Mode

| ZZ | $\overline{SS}$ ($t_n$) | $\overline{SW}$ ($t_n$) | $\overline{SBW}$x ($t_n$) | $\overline{G}$ | Mode | $DQ_{0-17}$ ($t_n$) | $DQ_{0-17}$ ($t_{n+1}$) | $V_{DD}$ Current |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Sleep Mode. Power Down | Hi - Z | Hi - Z | $I_{SB}$ |
| L | H | X | X | X | Deselect | X | Hi - Z | $I_{DD}$ |
| L | L | H | X | H | Read | Hi - Z | Hi - Z | $I_{DD}$ |
| L | L | H | X | L | Read | X | $Q(t_n)$ | $I_{DD}$ |
| L | L | L | L | X | Write All Bytes (Bits 0-17) | X | $D(t_n)$ | $I_{DD}$ |
| L | L | L | X | X | Write Bytes With $\overline{SBW}$x=L | X | $D(t_n)$ | $I_{DD}$ |
| L | L | L | H | X | Abort Write | X | Hi - Z | $I_{DD}$ |

### Register - Latch and Register - Flow Thru Mode

| ZZ | $\overline{SS}$ ($t_n$) | $\overline{SW}$ ($t_n$) | $\overline{SBW}$x ($t_n$) | $\overline{G}$ | Mode | $DQ_{0-17}$ ($t_n$) | $DQ_{0-17}$ ($t_{n+1}$) | $V_{DD}$ Current |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Sleep Mode. Power Down | Hi - Z | Hi - Z | $I_{SB}$ |
| L | H | X | X | X | Deselect | Hi - Z | X | $I_{DD}$ |
| L | L | H | X | H | Read | Hi - Z | Hi - Z | $I_{DD}$ |
| L | L | H | X | L | Read | $Q(t_n)$ | X | $I_{DD}$ |
| L | L | L | L | X | Write All Bytes (Bits 0-17) | Hi - Z | $D(t_n)$ | $I_{DD}$ |
| L | L | L | X | X | Write Bytes With $\overline{SBW}$x=L | Hi - Z | $D(t_n)$ | $I_{DD}$ |
| L | L | L | H | X | Abort Write | Hi - Z | X | $I_{DD}$ |

### Dual Clock Mode

| ZZ | $\overline{SS}$ ($t_n$) | $\overline{SW}$ ($t_n$) | $\overline{SBW}$x ($t_n$) | $\overline{G}$ | Mode | $DQ_{0-17}$ ($t_n$) | $DQ_{0-17}$ ($t_{n+1}$) | $V_{DD}$ Current |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Sleep Mode. Power Down | Hi - Z | Hi - Z | $I_{SB}$ |
| L | H | X | X | X | Deselect | Hi - Z | X | $I_{DD}$ |
| L | L | H | X | H | Read | Hi - Z | Hi - Z | $I_{DD}$ |
| L | L | H | X | L | Read | $Q(t_n)$ | X | $I_{DD}$ |
| L | L | L | L | X | Write All Bytes (Bits 0-17) | Hi - Z | $D(t_n)$ | $I_{DD}$ |
| L | L | L | X | X | Write Bytes With $\overline{SBW}$x=L | Hi - Z | $D(t_n)$ | $I_{DD}$ |
| L | L | L | H | X | Abort Write | Hi - Z | Hi - Z | $I_{DD}$ |

## •Mode Select

This device supports four different JEDEC standard read protocols via mode pins M1 and M2. The mode pins must be set during power-up and cannot change during SRAM operation.

**Mode Select Truth Table.**

| | M1 | M2 |
|---|---|---|
| Register-Register | L | H |
| Register-Flow Thru | L | L |
| Register-Latch | H | L |
| Dual Clock | H | H |

## •Power-Up Sequence

Power supplies must power up in the following sequence: $V_{SS}$, $V_{DD}$, $V_{DDQ}$, $V_{REF}$, and Inputs. $V_{DDQ}$ must never exceed $V_{DD}$.

## •Absolute Maximum Ratings(1)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to +4.6 | V |
| Output Supply Voltage | $V_{DDQ}$ | -0.5 to +4.6 | V |
| Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 (4.6V max.) | V |
| Output Voltage | $V_{OUT}$ | -0.5 to $V_{DDQ}$+0.5 (4.6V max.) | V |
| Operating Temperature | $T_A$ | 0 to 70 | °C |
| Junction Temperature | $T_J$ | 0 to 110 | °C |
| Storage Temperature | $T_{stg}$ | -55 to 150 | °C |

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**•DC Recommended Operating Conditions.** **($V_{SS}$ = 0V, $T_A$ = 0 to 70°C)**

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3.13 | 3.3 | 3.47 | V |
| Output Supply Voltage | $V_{DDQ}$ | 1.4 | --- | 1.6(3) | V |
| Input Reference Voltage | $V_{REF}$ | 0.5 | --- | 1.0 | V |
| Input High Voltage | $V_{IH}$ | $V_{REF}$ + 0.2 | --- | $V_{DDQ}$ + 0.3(1) | V |
| Input Low Voltage | $V_{IL}$ | -0.3(2) | --- | $V_{REF}$ - 0.2 | V |
| Input High Voltage - Test Mode | $V_{TIH}$ | 2.0 | --- | $V_{DDQ}$+0.3 | V |
| Input Low Voltage - Test Mode | $V_{TIL}$ | -0.3 | --- | 0.8 | V |
| Clock Input Signal Voltage | $V_{IN}$ | -0.3 | --- | $V_{DDQ}$+0.3 | V |
| Clock Input Differential Voltage | $V_{DIF}$ | 0.4 | --- | $V_{DDQ}$+0.6 | V |
| Clock Input Common Mode Voltage | $V_{CM}$ | 0.5 | 0.75 | 1.0 | V |
| Clock Input Cross Point Voltage | $V_X$ | 0.5 | 0.75 | 1.0 | V |
| Output Impedance Control Resistor | RQ | 175 | 250 | 350 | Ω |

(1) $V_{IH}$ (Max) AC = $V_{DD}$+1.5 V for pulse width less than 2.0 ns.
(2) $V_{IL}$ (Min) AC = -1.5 V for pulse width less than 2.0 ns.
(3) Extended $V_{DDQ}$ support up to 2.0V is available - please contact marketing.

**•I/O Capacitance** **($T_A$ = 25°C, f = 1 MHz)**

| Item | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V | --- | 6 | pF |
| Clock Input Capacitance | $C_{CLK}$ | $V_{IN}$ = 0V | --- | 6 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = 0V | --- | 7 | pF |

Note: These parameters are sampled and are not 100% tested.

**•Programmable Impedance Output Drivers**

This device has programmable impedance output drivers. The output impedance is controlled by an external resistor, RQ, connected between the SRAM's ZQ pin and $V_{SS}$, and is equal to one-fifth the value of this resistor. For output impedance matching within a ±7.5% tolerance, RQ must be in the range of 175Ω to 350Ω. For maximum output drive, the ZQ pin can be connected directly to $V_{SS}$. For minimum output drive, the ZQ pin can be left open or connected to $V_{DDQ}$. The output impedance is updated whenever the drivers are in a Hi-Z state. At power up, 8192 clock cycles followed by a write or deselect operation are required to ensure that the output impedance has reached its desired value. After power up, periodic updates of the output impedance, via a write or deselect operation, are also required.

## •DC Electrical Characteristics

**($V_{DD}$ = 3.3V ± 5%, $V_{SS}$ = 0V, $T_A$ = 0 to 70°C)**

| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ | -1 | --- | 1 | uA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$ = $V_{SS}$ to $V_{DD}$<br>$\overline{G}$ = $V_{IH}$ | -10 | --- | 10 | uA |
| Power Supply Operating Current | $I_{DD}$[4] | Cycle = 6.0ns<br>Duty = 100%<br>$I_{OUT}$ = 0 mA | --- | 610 | --- | mA |
| Power Supply Operating Current | $I_{DD}$[4] | Cycle = 5.0ns<br>Duty = 100%<br>$I_{OUT}$ = 0 mA | --- | 650 | --- | mA |
| Power Supply Operating Current | $I_{DD}$[4] | Cycle = 4.5ns<br>Duty = 100%<br>$I_{OUT}$ = 0 mA | --- | 670 | --- | mA |
| Power Supply Operating Current | $I_{DD}$[4] | Cycle = 4.0ns<br>Duty = 100%<br>$I_{OUT}$ = 0 mA | --- | 695 | --- | mA |
| Power Supply Standby Current | $I_{SB}$ | ZZ ≥ $V_{IH}$ | --- | 60 | --- | mA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -6.0 mA<br>RQ=250Ω | $V_{DDQ}$-0.4 | --- | --- | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA<br>RQ = 250Ω | --- | --- | 0.4 | V |
| Output Driver Impedance | $R_{OUT}$[1,2,3] | $V_{OH}$ = $V_{DDQ}$/2<br>$V_{OL}$ = $V_{DDQ}$/2 | (RQ/5)*<br>0.925 | RQ/5 | (RQ/5)*<br>1.075 | Ω |

1. RQ needs to be in the range of 175Ω to 350Ω for proper control of the value of $R_{OUT}$.
   1.1 $R_{OUT}$ ≤ 38Ω (1.075 * 175Ω/5) when RQ ≤ 175Ω
   1.2 $R_{OUT}$ ≥ 64Ω (0.925 * 350Ω/5) when RQ ≥ 350Ω
2. For maximum output drive, ZQ pin can be tied directly to $V_{SS}$. The output impedance is as described in note 1.1.
3. For minimum output drive, ZQ pin can be no connect or tied to $V_{DDQ}$. The output impedance is as described in note 1.2.
4. Typical $I_{DD}$ values measured at $V_{DD}$ = 3.3V and $T_A$ = 25°C, with a 75% read / 25% write operation distribution.

## •AC Electrical Characteristics (Register-Register Mode)

| Item | Symbol | -4A | | -4 | | -45A | | -45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Cycle Time | $t_{KHKH}$ | 4.0 | --- | 4.0 | --- | 4.0 | --- | 5.0 | --- | ns |
| Clock High Pulse Width | $t_{KHKL}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| Clock Low Pulse Width | $t_{KLKH}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| Address Setup Time | $t_{AVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Address Hold Time | $t_{KHAX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Write Enables Setup Time | $t_{WVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Write Enables Hold Time | $t_{KHWX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Synchronous Select Setup Time | $t_{SVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Synchronous Select Hold Time | $t_{KHSX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Data Input Setup Time | $t_{DVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Data Input Hold Time | $t_{KHDX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Clock High to Output Valid | $t_{KHQV}$ | --- | 2.3 | --- | 2.3 | --- | 2.3 | --- | 2.5 | ns |
| Clock High to Output Hold | $t_{KHQX}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock High to Output Low-Z | $t_{KHQX1}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock High to Output High-Z | $t_{KHQZ}$ *2 | --- | 2.3 | --- | 2.3 | --- | 2.3 | --- | 2.5 | ns |
| Output Enable Low to Output Valid | $t_{GLQV}$ | --- | 2.3 | --- | 2.3 | --- | 2.3 | --- | 2.5 | ns |
| Output Enable Low to Output Low-Z | $t_{GLQX}$ *2 | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Output Enable High to Output High-Z | $t_{GHQZ}$ *2 | --- | 2.3 | --- | 2.3 | --- | 2.3 | --- | 2.3 | ns |
| Sleep Mode Enable Time | $t_{ZZE}$ *2 | --- | 20.0 | --- | 20.0 | --- | 20.0 | --- | 20.0 | ns |
| Sleep Mode Recovery Time | $t_{ZZR}$ *2 | 20.0 | --- | 20.0 | --- | 20.0 | --- | 20.0 | | ns |

1. All parameters are specified over the range $T_A$ = 0 to 70°C.
2. These parameters are sampled and are not 100% tested.

## •AC Electrical Characteristics (Register-Latch & Register-Flow Thru Modes)

| Item | Symbol | -4A | | -4 | | -45A | | -45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Cycle Time | $t_{KHKH}$ | 4.8 | --- | 5.3 | --- | 5.3 | --- | 6.5 | --- | ns |
| Clock High Pulse Width | $t_{KHKL}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| Clock Low Pulse Width | $t_{KLKH}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| Address Setup Time | $t_{AVKH}$ | 0.4*3 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Address Hold Time | $t_{KHAX}$ | 0.8*3 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Write Enables Setup Time | $t_{WVKH}$ | 0.4*3 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Write Enables Hold Time | $t_{KHWX}$ | 0.8*3 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Synchronous Select Setup Time | $t_{SVKH}$ | 0.4*3 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Synchronous Select Hold Time | $t_{KHSX}$ | 0.8*3 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Data Input Setup Time | $t_{DVKH}$ | 0.4*3 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Data Input Hold Time | $t_{KHDX}$ | 0.8*3 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Clock High to Output Valid | $t_{KHQV}$ | --- | 4.8 | --- | 5.3 | --- | 5.3 | --- | 6.5 | ns |
| Clock High to Output Hold (R-FT mode only) | $t_{KHQX}$*2 | 2.0 | --- | 2.0 | --- | 2.0 | --- | 2.0 | --- | ns |
| Clock High to Output Low-Z (R-FT mode only) | $t_{KHQX1}$*2 | 2.5 | --- | 2.5 | --- | 2.5 | --- | 3.0 | --- | ns |
| Clock Low to Output Valid (R-L mode only) | $t_{KLQV}$ | --- | 2.2 | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| Clock Low to Output Hold (R-L mode only) | $t_{KLQX}$*2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock Low to Output Low-Z (R-L mode only) | $t_{KLQX1}$*2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock High to Output High-Z | $t_{KHQZ}$*2 | --- | 2.2 | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| Output Enable Low to Output Valid | $t_{GLQV}$ | --- | 2.2 | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| Output Enable Low to Output Low-Z | $t_{GLQX}$*2 | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Output Enable High to Output High-Z | $t_{GHQZ}$*2 | --- | 2.2 | --- | 2.3 | --- | 2.3 | --- | 2.3 | ns |
| Sleep Mode Enable Time | $t_{ZZE}$*2 | --- | 20.0 | --- | 20.0 | --- | 20.0 | --- | 20.0 | ns |
| Sleep Mode Recovery Time | $t_{ZZR}$*2 | 20.0 | --- | 20.0 | --- | 20.0 | --- | 20.0 | --- | ns |

1. All parameters are specified over the range $T_A$ = 0 to 70°C.
2. These parameters are sampled and are not 100% tested.
3. For -4A, these parameters are measured from valid $V_{IH}/V_{IL}$ levels to the clock mid-point.
4. R-FT mode operation is verified functionally, but associated timing parameters are guaranteed by design only and are not 100% tested.

## •AC Electrical Characteristics (Dual Clock Mode)

| Item | Symbol | -4A | | -4 | | -45A | | -45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| K Clock Cycle Time | $t_{KHKH}$ | 4.0 | --- | 4.0 | --- | 4.5 | --- | 4.5 | --- | ns |
| K Clock High Pulse Width | $t_{KHKL}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| K Clock Low Pulse Width | $t_{KLKH}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| C Clock Cycle Time | $t_{CHCH}$ | 4.0 | --- | 4.0 | --- | 4.5 | --- | 4.5 | --- | ns |
| C Clock High Pulse Width | $t_{CHCL}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| C Clock Low Pulse Width | $t_{CLCH}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| K to C Clock Delay | $t_{KHCH}$ | 1.5 | --- | 1.5 | --- | 1.5 | --- | 1.5 | --- | ns |
| C to K Clock Delay | $t_{CHKH}$ | 0.8 | --- | 0.8 | --- | 0.8 | --- | 0.8 | --- | ns |
| Address Setup Time | $t_{AVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Address Hold Time | $t_{KHAX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Write Enables Setup Time | $t_{WVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Write Enables Hold Time | $t_{KHWX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Synchronous Select Setup Time | $t_{SVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Synchronous Select Hold Time | $t_{KHSX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Data Input Setup Time | $t_{DVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Data Input Hold Time | $t_{KHDX}$ | 0.8 | --- | 0.8 | --- | 1.0 | --- | 1.0 | --- | ns |
| K Clock High to Output Valid | $t_{KHQV}$ | --- | 5.2 | --- | 5.2 | --- | 6.0 | --- | 6.5 | ns |
| C Clock High to Output Valid | $t_{CHQV}$ | --- | 2.3 | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| C Clock High to Output Hold | $t_{CHQX}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| C Clock High to Output Low-Z | $t_{CHQX1}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| C Clock High to Output High-Z | $t_{CHQZ}$ *2 | --- | 2.3 | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| Output Enable Low to Output Valid | $t_{GLQV}$ | --- | 2.1 | --- | 2.1 | --- | 2.5 | --- | 2.5 | ns |
| Output Enable Low to Output Low-Z | $t_{GLQX}$ *2 | 0.5 | --- | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Output Enable High to Output High-Z | $t_{GHQZ}$ *2 | --- | 2.0 | --- | 2.0 | --- | 2.3 | --- | 2.3 | ns |
| Sleep Mode Enable Time | $t_{ZZE}$ *2 | --- | 20.0 | --- | 20.0 | --- | 20.0 | --- | 20.0 | ns |
| Sleep Mode Recovery Time | $t_{ZZR}$ *2 | 20.0 | --- | 20.0 | --- | 20.0 | --- | 20.0 | --- | ns |

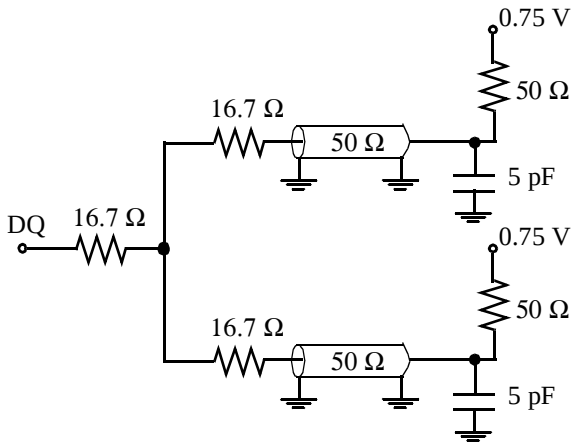
1. All parameters are specified over the range $T_A$ = 0 to 70°C.
2. These parameters are sampled and are not 100% tested.
3. Currently, DC mode operation is not verified functionally, and no timing parameters are guaranteed. Contact Sony Memory Marketing for availability.

• **AC Test Conditions ($V_{DDQ}$ = 1.5V)**

**($V_{DD}$ = 3.3V ± 5%, $T_A$ = 0 to 70°C)**

| Item | | Conditions | Notes |
|---|---|---|---|
| Input Reference Voltage | | $V_{REF}$ = 0.75V | |
| Input High Level | | $V_{IH}$ = 1.25V | |
| Input Low Level | | $V_{IL}$ = 0.25V | |
| Input Rise & Fall Time | | 1V/ns | |
| Clock | Input Reference Level | K/$\overline{K}$ cross; C/$\overline{C}$ cross | |
| | Input High Voltage | 1.25V | |
| | Input Low Voltage | 0.25V | |
| | Input Rise & Fall Time | 1V/ns | |
| Output Supply Voltage | | $V_{DDQ}$ = 1.5V | |
| Output Reference Level | | 0.75V | |
| Output Load Conditions | | | Fig.1<br>RQ = 250Ω |

**Fig. 1: AC Test Output Load ($V_{DDQ}$ = 1.5V)**

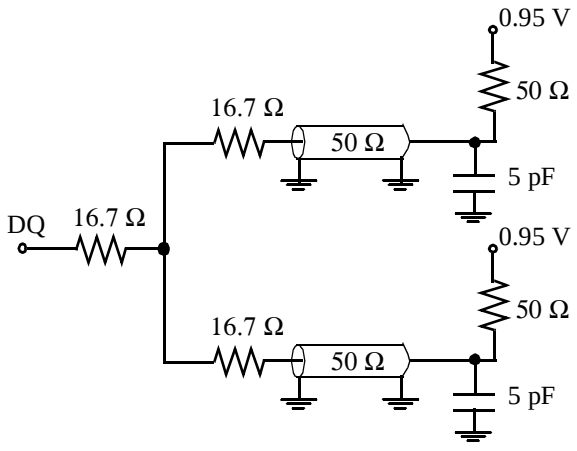


**•AC Test Conditions ($V_{DDQ}$ = 1.9V) .... for extended HSTL (<u>for R-L mode only</u>)**

**($V_{DD}$ = 3.3V ± 5%, $T_A$ = 0 to 70°C)**
**($V_{DDQ}$ = 1.9V ± 0.1V, $T_A$ = 0 to 70°C)**

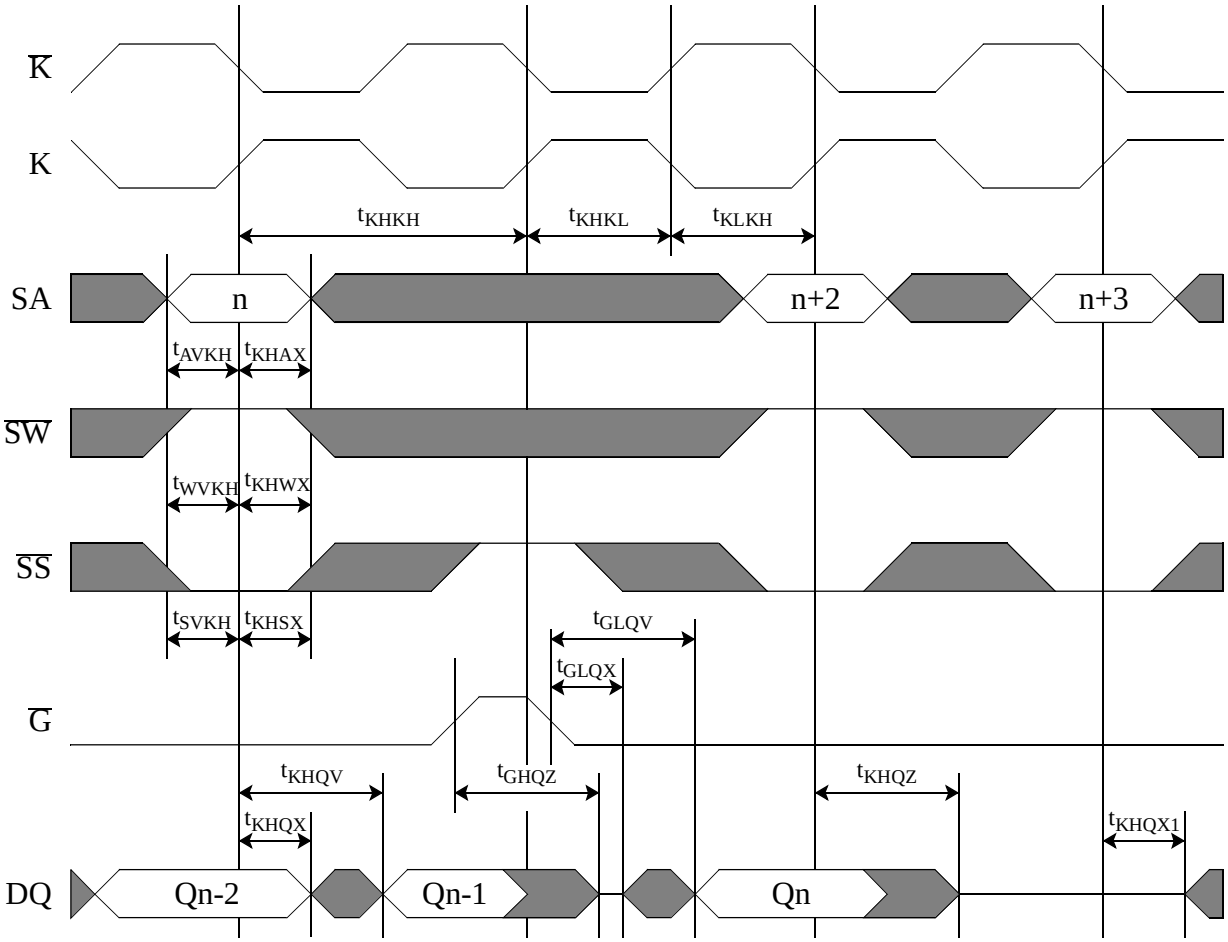
| Item | | Conditions | Notes |
|---|---|---|---|
| Input Reference Voltage | | $V_{REF}$ = 0.75V | |
| Input High Level (Address / Control) | | $V_{IHCA}$ = 1.25V | |
| Input Low Level (Address / Control) | | $V_{ILCA}$ = 0.25V | |
| Input High Level (Data) | | $V_{IHD}$ = 1.25V | |
| Input Low Level (Data) | | $V_{ILD}$ = 0.25V | |
| Input Rise & Fall Time | | 1V/ns | |
| Clock | Input Reference Level | K/$\overline{K}$ cross | |
| | PECL Input High Voltage | 1.45V | |
| | PECL Input Low Voltage | 0.75V | |
| | Input Rise & Fall Time | 1V/ns | |
| Output Supply Voltage | | $V_{DDQ}$ = 1.9V | |
| Output Reference Level | | 0.95V | |
| Output Load Conditions | | | Fig.2<br>RQ = 250Ω |

**Fig. 2: AC Test Output Load ($V_{DDQ}$ = 1.9V)**

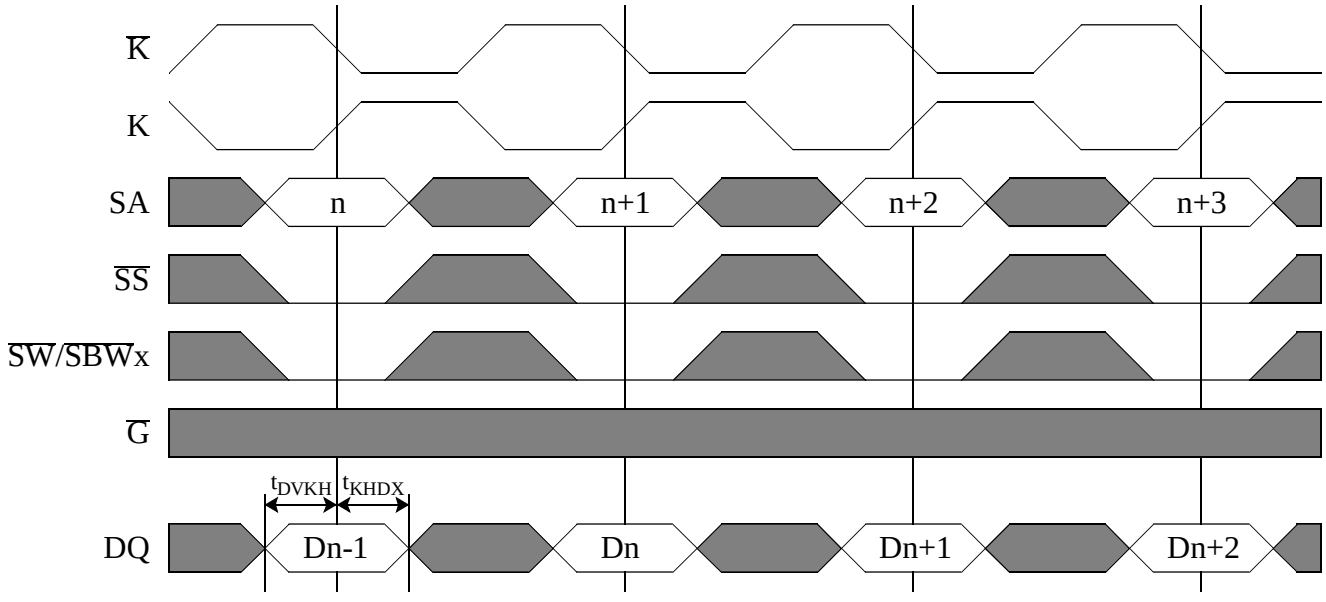


# Register - Register Mode

## Timing Diagram of Read and Deselect Operations

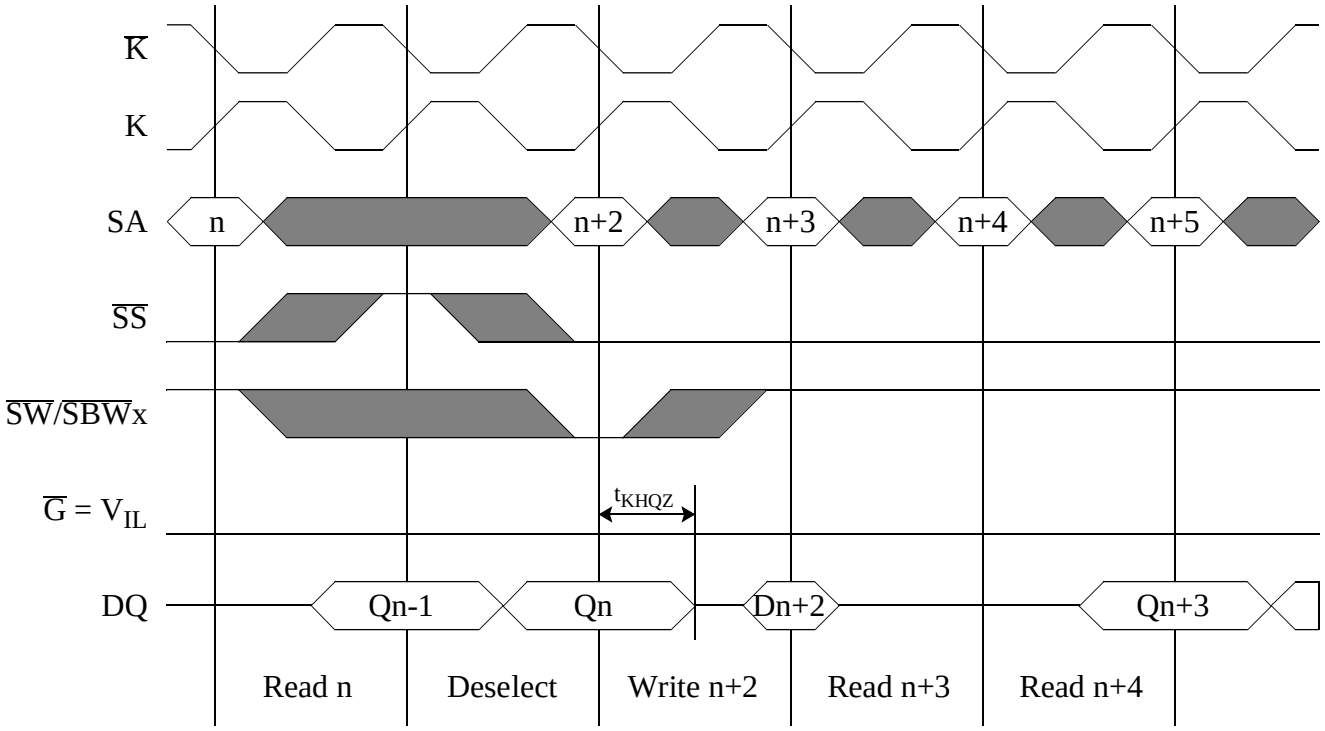



## Timing Diagram of Write Operations

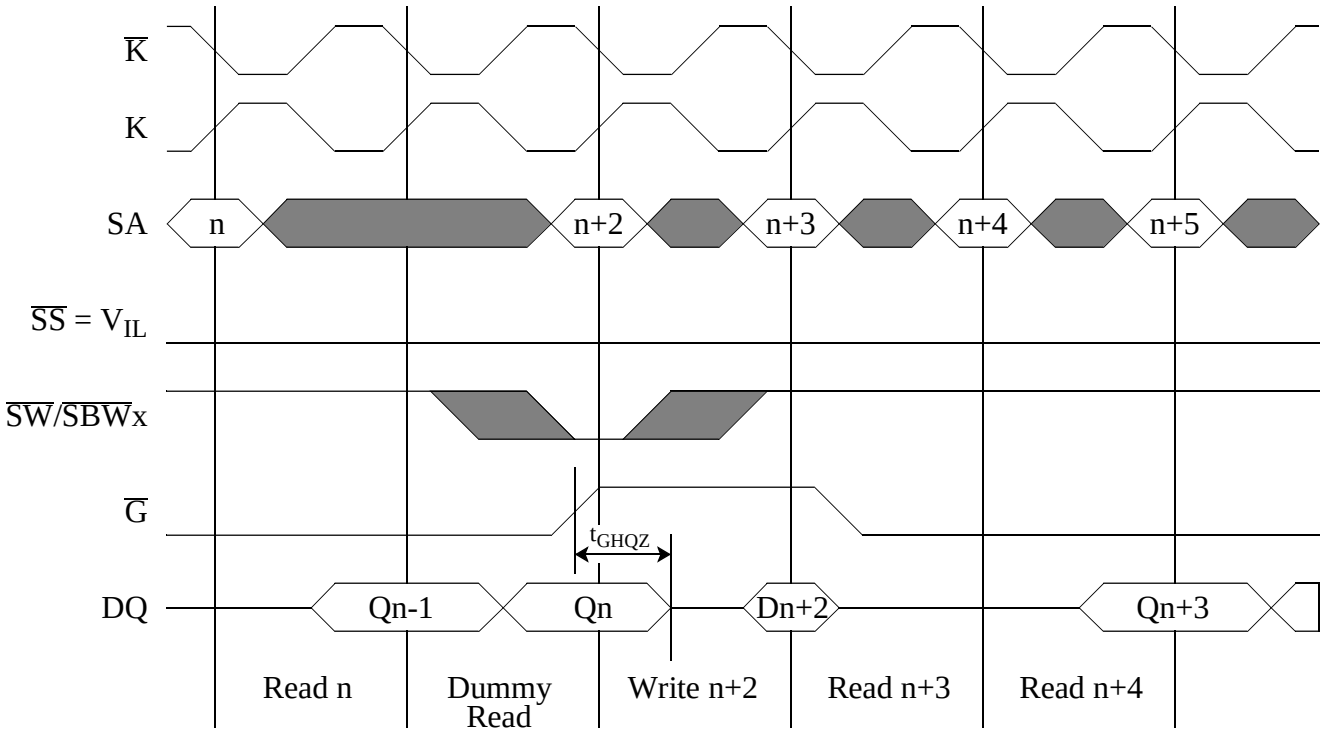


# Register - Register Mode

## Timing Diagram I of Read-Write-Read Operations ($\overline{SS}$ Controlled)

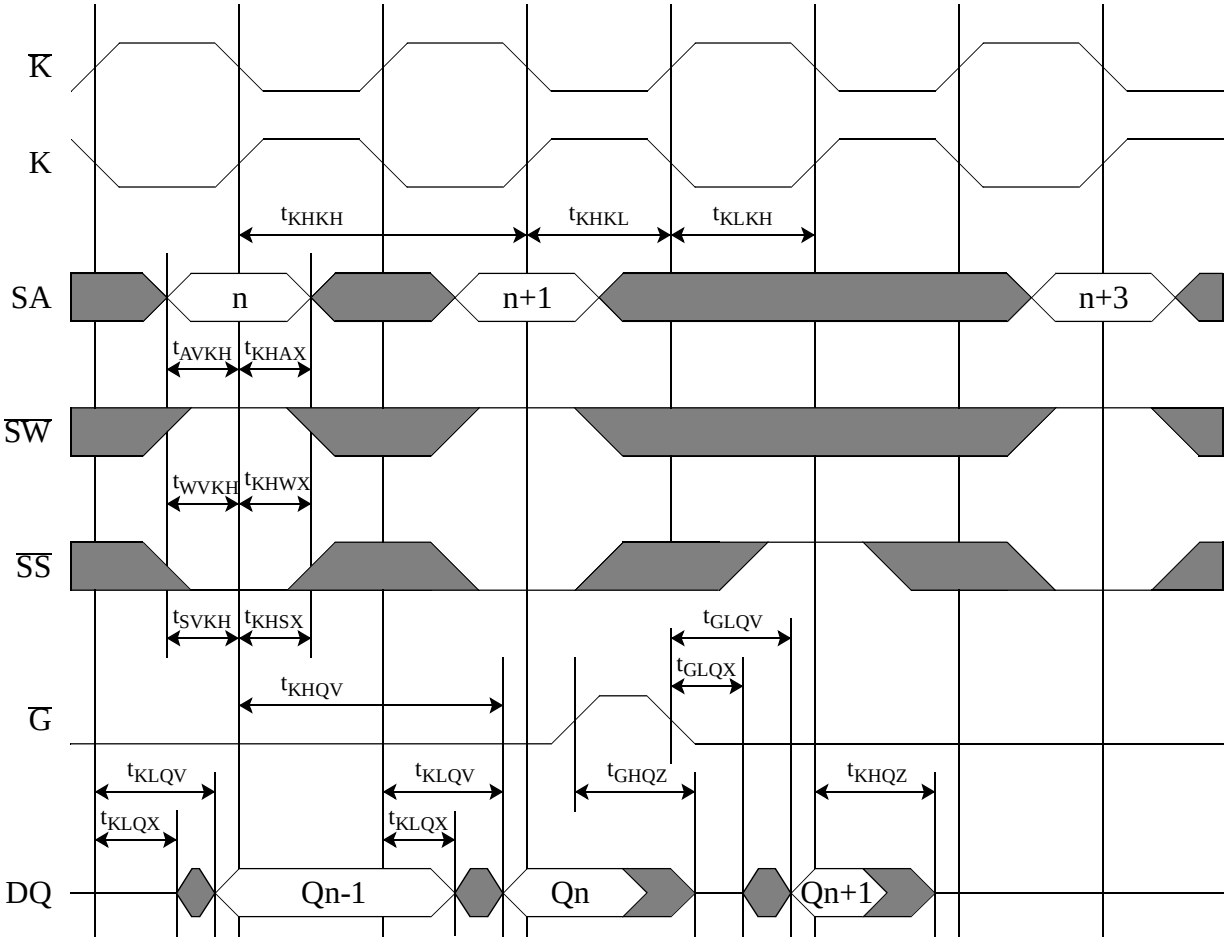



## Timing Diagram II of Read-Write-Read Operations ($\overline{G}$ Controlled)

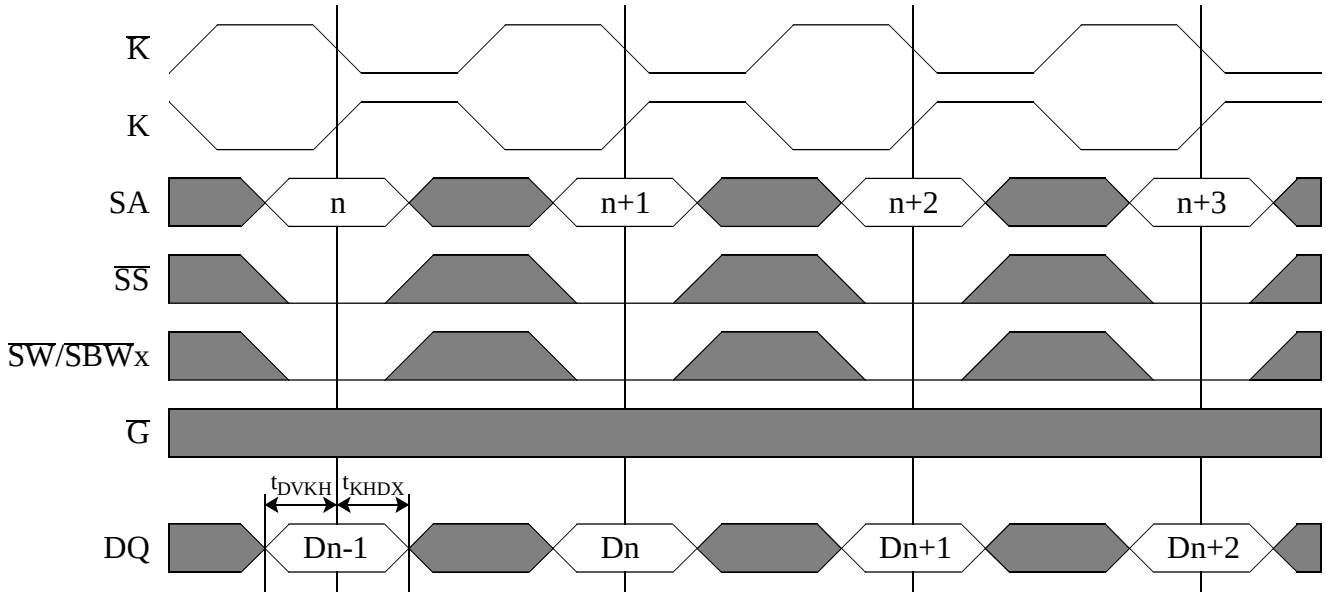


# Register - Latch Mode

## Timing Diagram of Read and Deselect Operations

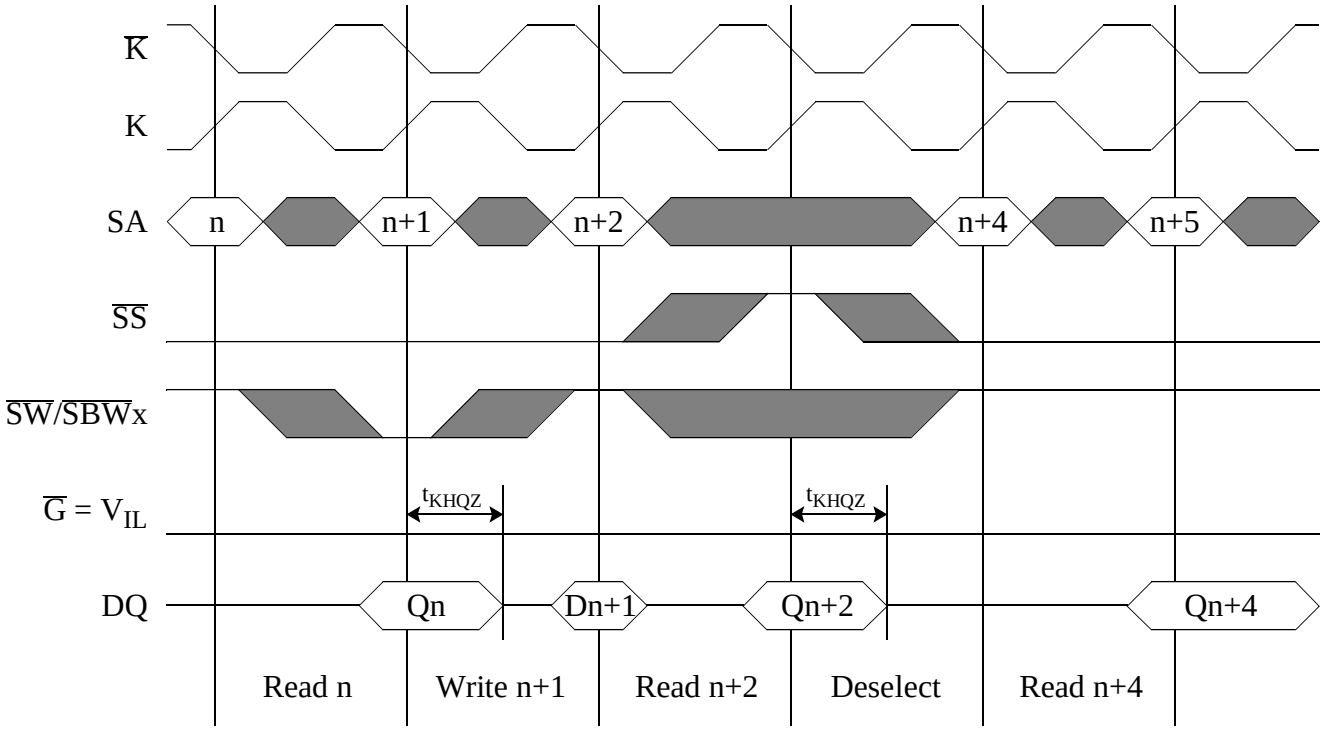



## Timing Diagram of Write Operations



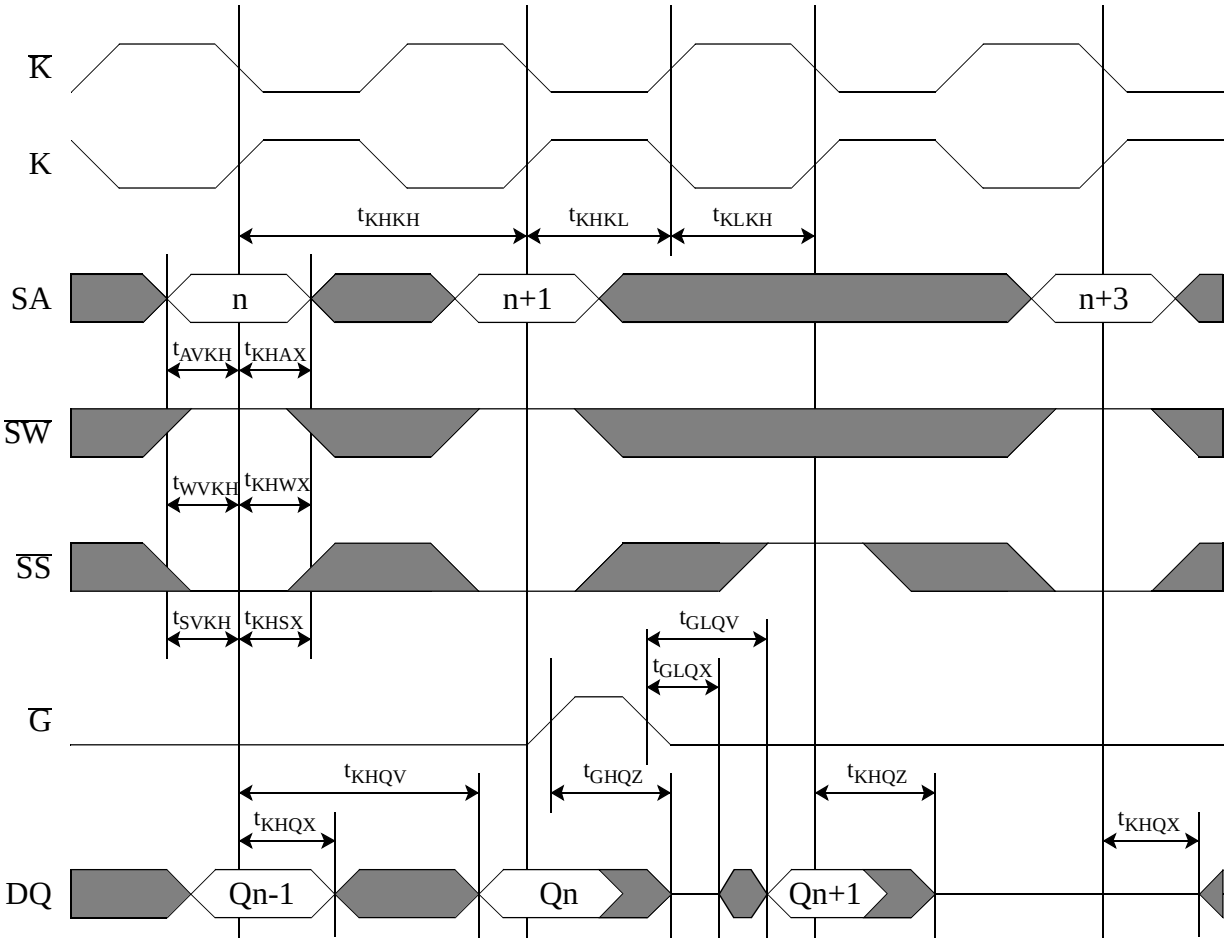
# Register - Latch Mode

## Timing Diagram of Read-Write-Read Operations

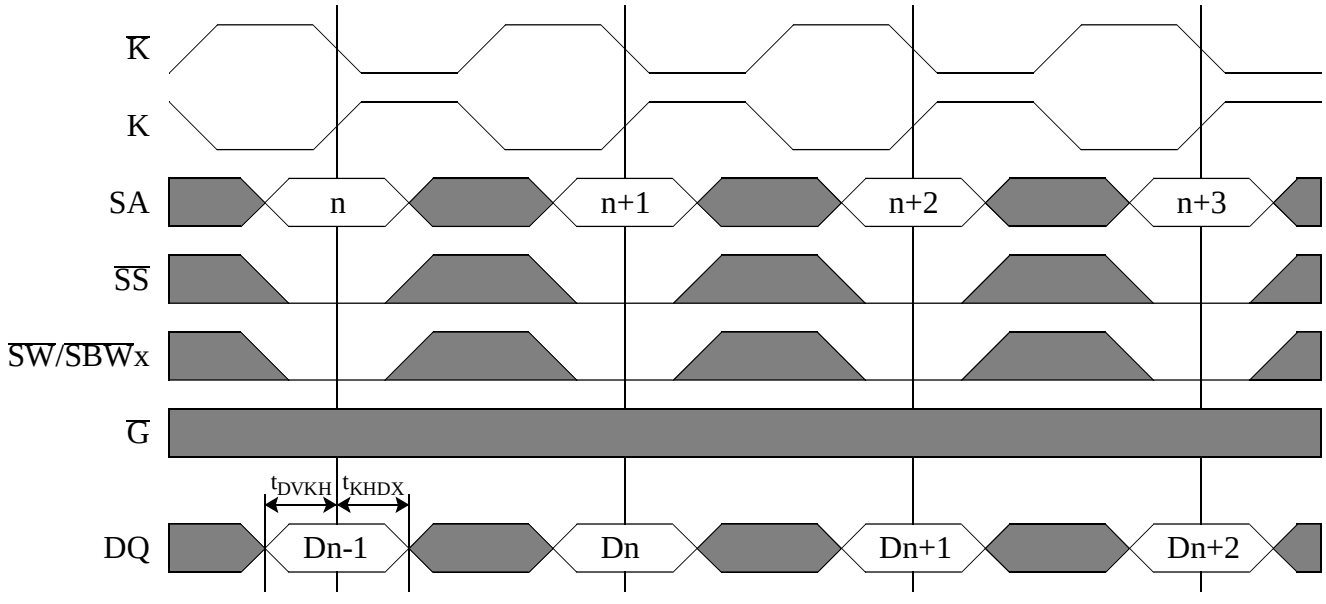


# Register - Flow Thru Mode

## Timing Diagram of Read and Deselect Operations

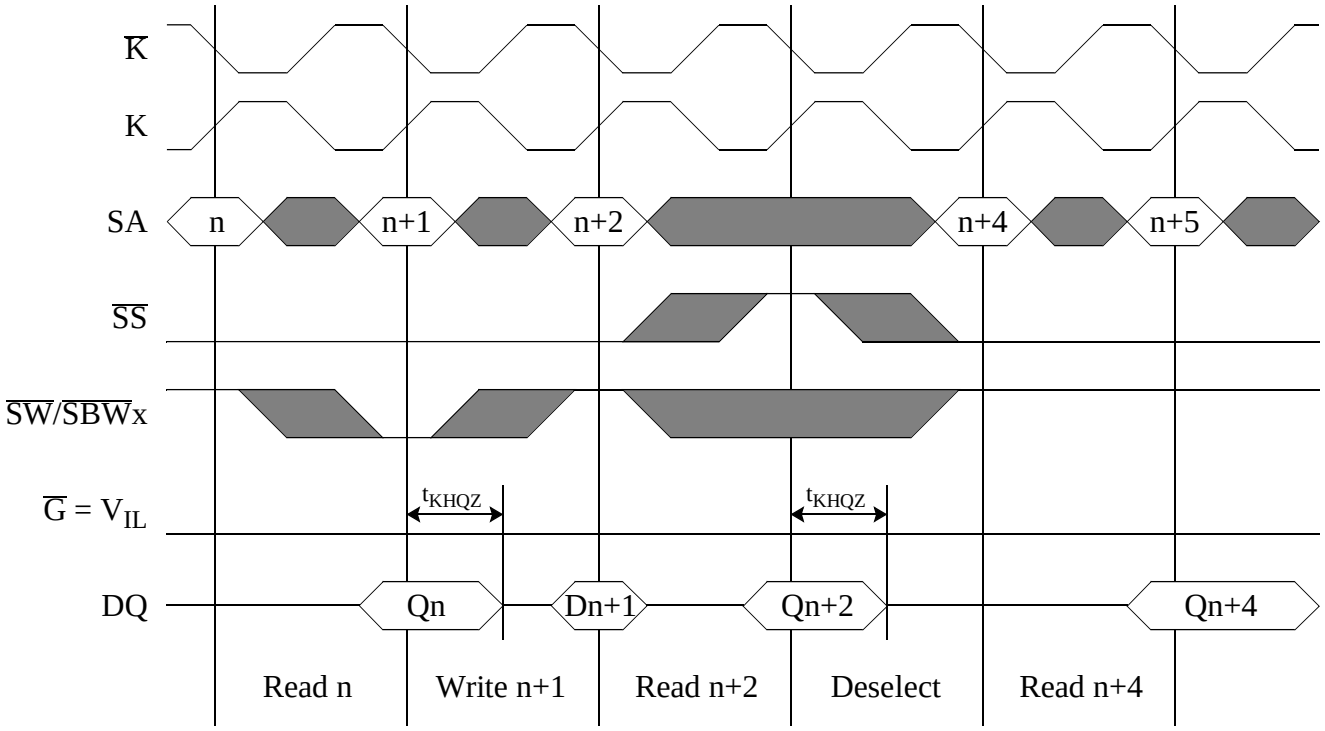



## Timing Diagram of Write Operations



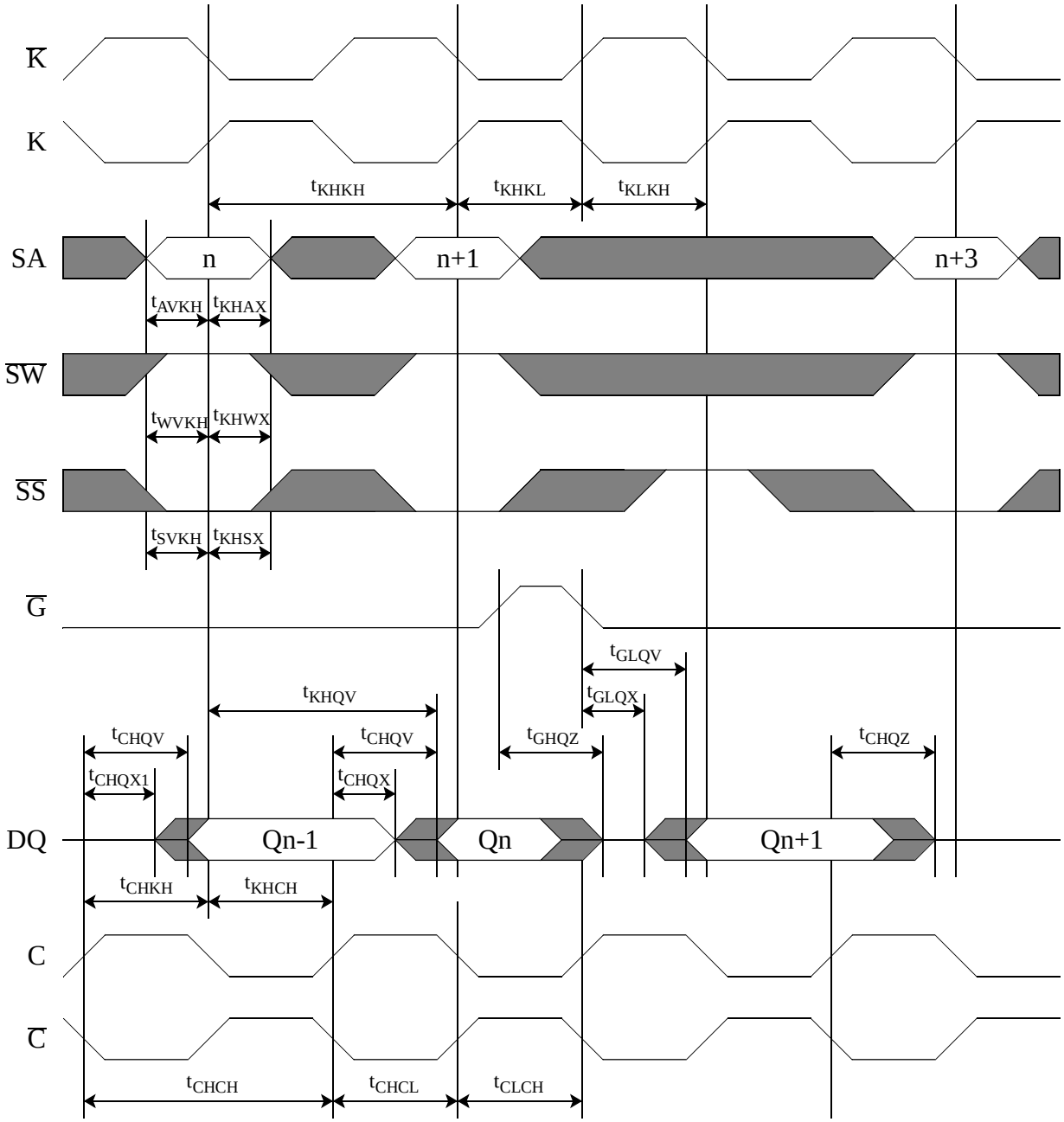
# Register - Flow Thru Mode

## Timing Diagram of Read-Write-Read Operations



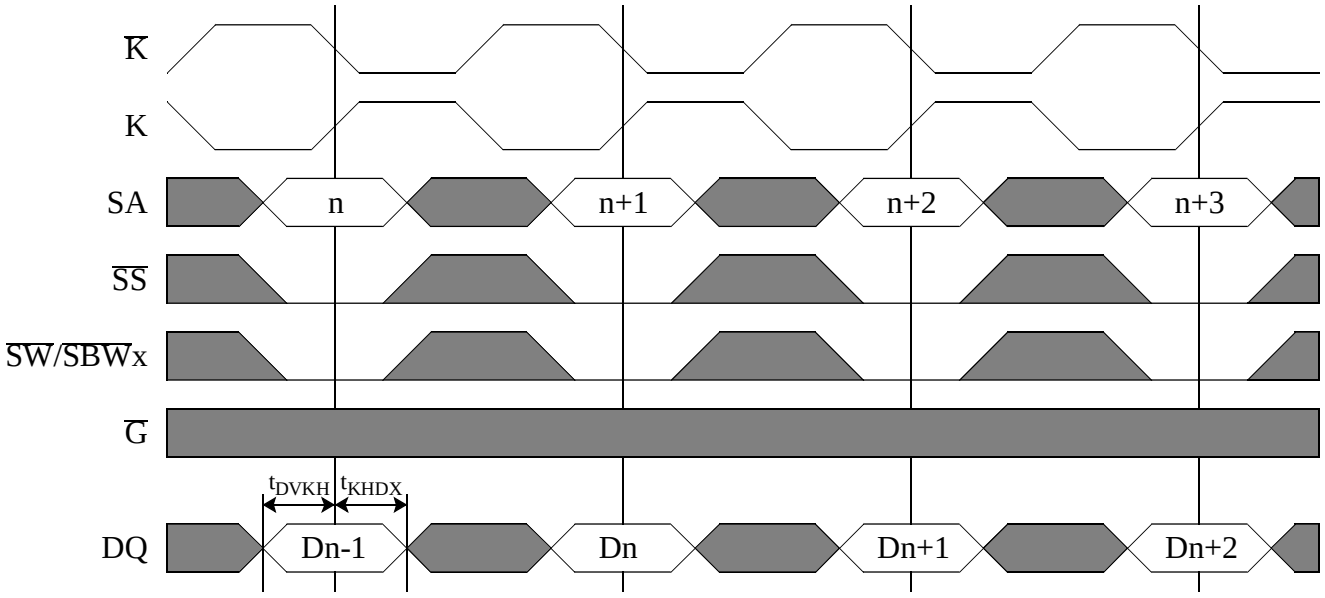
# Dual Clock Mode

## Timing Diagram of Read and Deselect Operations

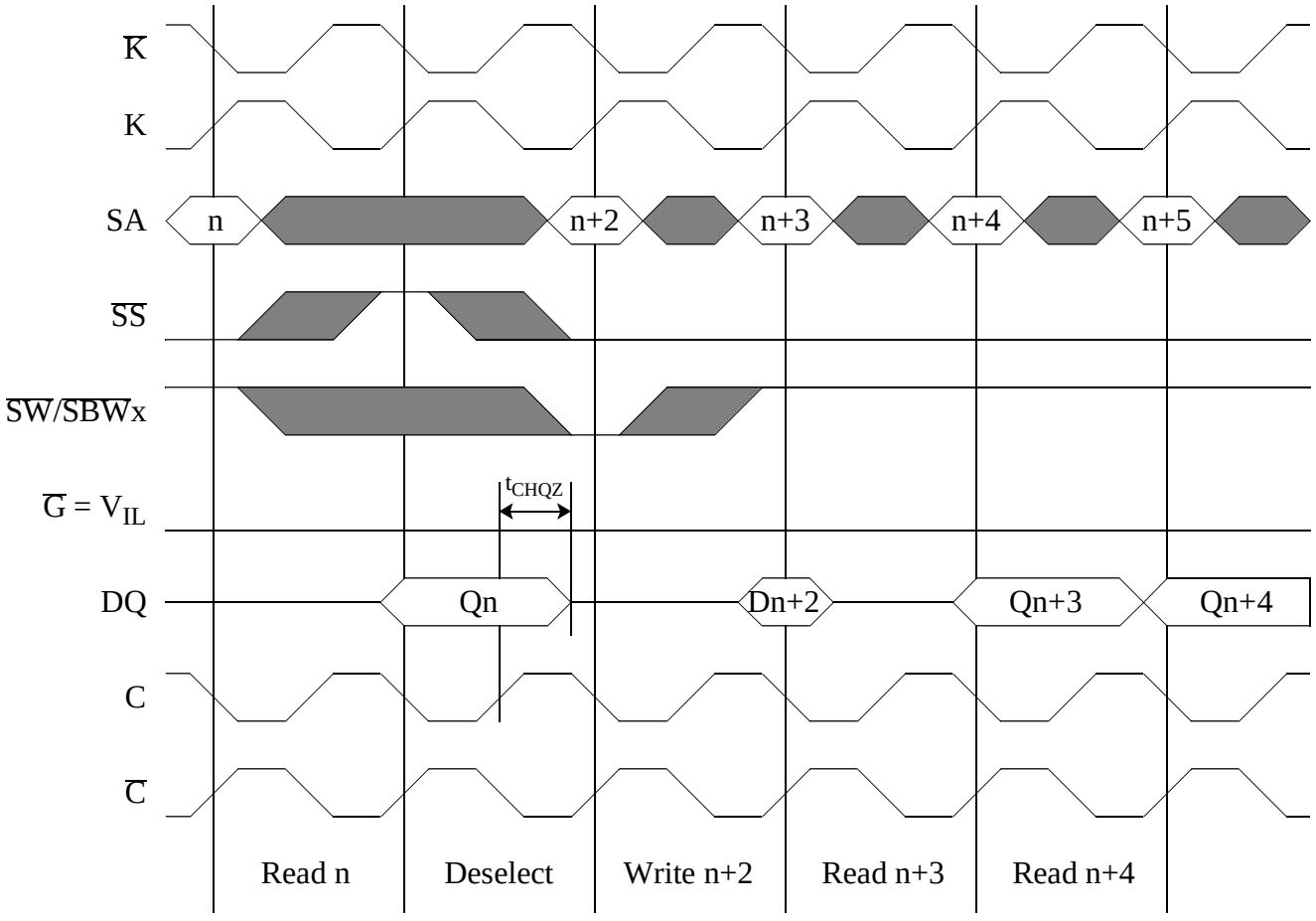


# Dual Clock Mode

## Timing Diagram of Write Operations

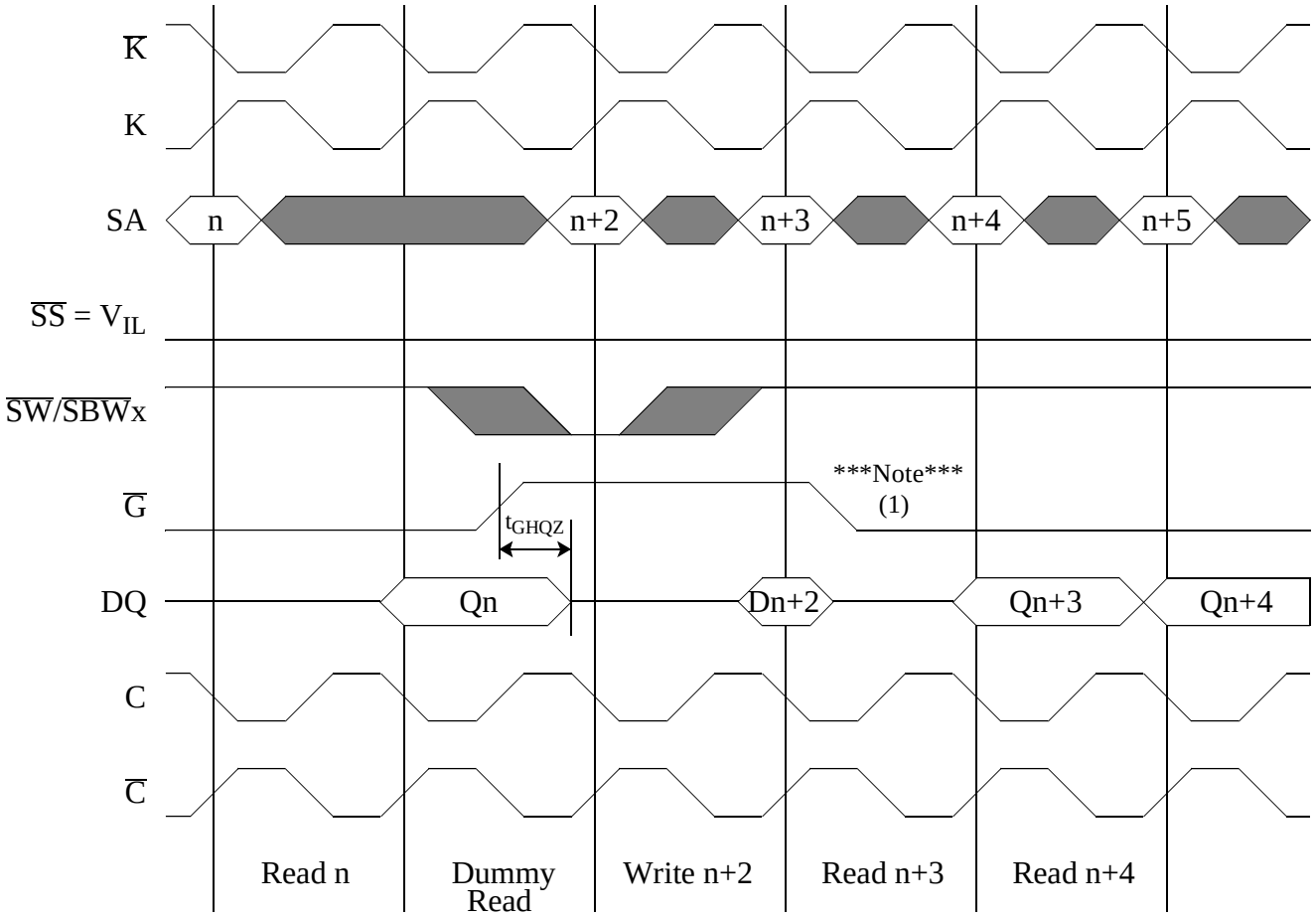



## Timing Diagram I of Read-Write-Read Operations (SS Controlled)



# Dual Clock Mode

**Timing Diagram II of Read-Write-Read Operations ($\overline{G}$ Controlled)**




Note 1: In order to prevent glitches on the data bus during write-read operations, when $\overline{G}$ is driven active (low) following the rising edge of K, the data bus will remain tri-stated until valid data from the most recent read operation is available. Specifically, the data bus will remain tri-stated for the **maximum** of the following three times:

1.$T_{KHQV}$
2.$T_{KHCH} + T_{CHQV}$
3.(K high to $\overline{G}$ low) + $T_{GLQV}$

# Test Mode Description

## Functional Description

The CXK77B1840 provides a JTAG boundary scan interface using a limited set of IEEE std. 1149.1 functions. The test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, the CXK77B1840 contains a TAP controller, Instruction register, Boundary scan register and Bypass register.

JTAG Inputs/Outputs are LVTTL compatible only.

## Test Access Port (TAP)

4 pins as defined in the Pin Description table are used to perform JTAG functions. The TDI input pin is used to scan test data serially into one of three registers (Instruction register, Boundary Scan register and Bypass register). TDO is the output pin used to scan test data serially out. The TDI pin sends the data into LSB of the selected register and the MSB of the selected register feeds the data to TDO. The TMS input pin controls the state transition of 16 state TAP controller as specified in IEEE std. 1149.1. Inputs on TDI and TMS are registered on the rising edge of TCK clock. The output data on TDO is presented on the falling edge of TCK. TDO driver is in active state only when TAP controller is in Shift-IR state or in Shift-DR state.

TCK, TMS, TDI must be tied low when JTAG is not used.

## TAP Controller

16 state controller is implemented as specified in IEEE std. 1149.1.

The controller enters reset state in one of two ways:

1. Power up.

2. Apply a logic 1 on TMS input pin on 5 consecutive TCK rising edges.

## Instruction Register (3 bits)

The JTAG Instruction register consists of a shift register stage and parallel output latch. The register is 3 bits wide and is encoded as follow:

| Octal | MSB.....LSB | | | Instruction |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Bypass |
| 1 | 0 | 0 | 1 | IDCODE. Read device ID |
| 2 | 0 | 1 | 0 | Sample-Z. Sample Inputs and tri-state DQs |
| 3 | 0 | 1 | 1 | Bypass |
| 4 | 1 | 0 | 0 | Sample. Sample Inputs. |
| 5 | 1 | 0 | 1 | Private. Manufacturer use only. |
| 6 | 1 | 1 | 0 | Bypass |
| 7 | 1 | 1 | 1 | Bypass |

**Bypass Register (1 bit)**

The Bypass Register is one bit wide and is connected electrically between TDI and TDO and provides the minimum length serial path between TDI and TDO.

**ID Registers (32 bits)**

The ID Register is 32 bits wide and is encoded as follows:

| | | |
|---|---|---|
| | ID[0} | 1 |
| Sony ID | ID[11:1] | 0000 1110 001 |
| Part Number | ID[27:12] | 0000 0000 0001 1000 |
| Revision Number | ID[31:28] | xxxx |

**Boundary Scan Register (51 bits)**

The Boundary Scan Registers are 51 bits wide and are listed as follows:

| | |
|---|---|
| DQ | 18 |
| SA | 18 |
| $\overline{SW}$, $\overline{SBW}$x | 3 |
| $\overline{SS}$, $\overline{G}$ | 2 |
| K, $\overline{K}$, C, $\overline{C}$ | 4 |
| ZZ | 1 |
| M1, M2 | 2 |
| ZQ | 1 |
| Place Holder | 2 |

K/$\overline{K}$, C/$\overline{C}$ inputs are sampled through one differential stage and internally inverted to generate internal K/$\overline{K}$, C/$\overline{C}$ signals for scan registers. Place Holder are required for some NC pins to maintain 51 bits Scan Register for different types of the same family SRAM and for density upgrades. All Place Holder Registers are connected to $V_{SS}$ internally regardless of pin connection externally.

## Scan Order (Order by exit sequence)

| | | | | | | |
|---|---|---|---|---|---|---|
| 26 | 3B | SA | | SA | 5B | 25 |
| 27 | - | $V_{SS}$ | | $V_{SS}$ | - | 24 |
| 28 | 3A | SA | | SA | 5A | 23 |
| 29 | 3C | SA | | SA | 5C | 22 |
| 30 | 2C | SA | | SA | 6C | 21 |
| 31 | 2A | SA | | SA | 6A | 20 |
| 32 | 1D | DQb | | DQa | 6D | 19 |
| 33 | 2E | DQb | | DQa | 7E | 18 |
| 34 | 2G | DQb | | DQa | 6F | 17 |
| 35 | 1H | DQb | | DQa | 7G | 16 |
| 36 | 3G | $\overline{\text{SBW}}$b | | DQa | 6H | 15 |
| 37 | 4D | ZQ | | $\overline{\text{G}}$ | 4F | 14 |
| 38 | 4E | $\overline{\text{SS}}$ | | K | 4K | 13 |
| 39 | 4G | $\overline{\text{C}}$ | | $\overline{\text{K}}$ | 4L | 12 |
| 40 | 4H | C | | $\overline{\text{SBW}}$a | 5L | 11 |
| 41 | 4M | $\overline{\text{SW}}$ | | DQa | 7K | 10 |
| 42 | 2K | DQb | | DQa | 6L | 9 |
| 43 | 1L | DQb | | DQa | 6N | 8 |
| 44 | 2M | DQb | | DQa | 7P | 7 |
| 45 | 1N | DQb | | ZZ | 7T | 6 |
| 46 | 2P | DQb | | SA | 5T | 5 |
| 47 | 3T | SA | | SA | 6R | 4 |
| 48 | 2R | SA | | SA | 4P | 3 |
| 49 | 4N | SA | | SA | 6T | 2 |
| 50 | 2T | SA | | M2 | 5R | 1 |
| 51 | 3R | M1 | | | | |

## Ordering Information.

| Part Number | Speed | | |
|---|---|---|---|
| | Register - Register | Register - Latch/ Register - Flow Thru | **Dual Clock** |
| CXK77B1840GB-4A | 4.0ns Cycle / 2.3ns Access | 4.8ns Cycle / 4.8ns Access | 4.0ns Cycle / 5.2ns Access |
| CXK77B1840GB-4 | 4.0ns Cycle / 2.3ns Access | 5.3ns Cycle / 5.3ns Access | 4.0ns Cycle / 5.2ns Access |
| CXK77B1840GB-45A | 4.0ns Cycle / 2.3ns Access | 5.3ns Cycle / 5.3ns Access | 4.5ns Cycle / 6.0ns Access |
| CXK77B1840GB-45 | 5.0ns Cycle / 2.5ns Access | 6.5ns Cycle / 6.5ns Access | 4.5ns Cycle / 6.5ns Access |

Note: Contact Sony Memory Marketing for availability of Dual Clock mode functionality.

**Revision History**

| Rev. # | Rev. date | Changes / Modifications to Data-Sheet |
|---|---|---|
| rev 4.0 | 8/22/97 | Initial version, based on TS-2 evaluation |
| rev 4.2 | 11/21/97 | Modified AC Electrical Characteristics:<br>R-R Mode:<br>-4.5+ $T_{KHKH}$ 5.0ns to 4.5ns<br>-4.5 $T_{GHQZ}$ 2.5ns to 2.3ns<br>-4.5 $T_{GHQZ}$ 2.5ns to 2.3ns<br>R-L, R-FT Modes:<br>-4 $T_{KHKH}$ 5.5ns to 5.0ns<br>-4.5+ $T_{KHQV}$ 6.5ns to 5.5ns<br>$T_{GHQZ}$ 2.5ns to 2.3ns<br>-4.5 $T_{GHQZ}$ 2.5ns to 2.3ns<br>-5 $T_{KHKH}$ 5.5ns to 6.0ns<br>DC Mode:<br>-4 $T_{KHQV}$ 5.5ns to 5.3ns<br>$T_{KHDX}$ 1.0ns to 0.8ns<br>$T_{GLQV}$ 2.3ns to 2.1ns<br>$T_{GHQZ}$ 2.3ns to 2.0ns<br>-4.5+ $T_{KHQV}$ 6.2ns to 6.0ns<br>$T_{GHQZ}$ 2.5ns to 2.3ns<br>-4.5 $T_{GHQZ}$ 2.5ns to 2.3ns<br>Renamed “-4” bin to “-40” bin in all modes.<br>Renamed “-4.5+” bin to “-45H” bin in all modes.<br>Renamed “-4.5” bin to “-45” bin in all modes.<br>Renamed “-5” bin to “-50” bin in all modes.<br><br>Modified DC Recommended Operating Conditions (page-6)<br>$V_{IH}$ min $V_{REF}$ + 0.1 to $V_{REF}$ + 0.2<br>$V_{IL}$ max $V_{REF}$ - 0.1 to $V_{REF}$ - 0.2<br>$V_{DIF}$ min 0.2V to 0.4V<br><br>Added extended HSTL AC Test Conditions (page-12)<br><br>Provided $I_{DD}$ & $I_{SB}$ typical values (page-7) |
| rev 4.3 | 01/15/98 | Modified AC Electrical Characteristics:<br>Added “-40A” bin to all modes.<br>Deleted “-40” bin from all modes.<br>Deleted “-50” bin from all modes.<br>Renamed “-45H” bin to “-45A” bin in all modes.<br><br>Modified extended HSTL AC Test Conditions (page-12) |

| Rev. # | Rev. date | Changes / Modifications to Data-Sheet |
|---|---|---|
| rev 4.4 | 04/14/98 | Modified AC Electrical Characteristics<br>Deleted "-45" bin from all modes.<br>Renamed "-40A" bin to "-4A" bin in all modes.<br>R-R Mode:<br>-4A $T_{KHKH}$ 4.5ns to 4.0ns<br>-45A $T_{KHKH}$ 4.5ns to 4.0ns<br>$T_{KHQV}$ 2.5ns to 2.3ns<br>$T_{KHQZ}$ 2.5ns to 2.3ns<br>$T_{GLQV}$ 2.5ns to 2.3ns<br>R-L, R-FT Modes:<br>Added "R-FT timing parameters guaranteed by design only" note for all bins.<br>Removed $T_{KHQZ1}$ from all bins.<br>-4A $T_{GHQZ}$ 2.3ns to 2.2ns<br>DC Mode:<br>Added "DC operation not functionally verified" note for all bins.<br>Removed $T_{KHQX}$ and $T_{KHQX1}$ from all bins.<br>-4A $T_{KHQV}$ 5.3ns to 5.2ns<br><br>Modified DC Recommended Operating Conditions (page-6)<br>RQ min 200Ω to 175Ω<br><br>Modified DC Electrical Characteristics (page-7)<br>$R_{OUT}$ min (RQ/5)*0.9Ω to (RQ/5)*0.925Ω<br>$R_{OUT}$ max (RQ/5)*1.1Ω to (RQ/5)*1.075Ω<br><br>Updated all timing diagrams (page-13 through page-21).<br><br>Added "Contact Sony Memory Marketing for DC model availability" note (page-1 and page-25).<br><br>Removed "Preliminary" from the data sheet |
| rev 4.5 | 08/12/98 | Modified AC Electrical Characteristics<br>R-L, R-FT Modes:<br>-4A $T_{KHKH}$ 5.0ns to 4.8ns<br>$T_{KHQV}$ 5.0ns to 4.8ns<br>-45A $T_{KHKH}$ 5.5ns to 5.3ns<br>$T_{KHQV}$ 5.5ns to 5.3ns |
| rev 4.6 | 08/20/98 | Modified AC Electrical Characteristics<br>Added "-4" bin to all modes.<br>Added "-45" bin to all modes. |