SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2037A
HORIZONTAL & VERTICAL DEFLECTION CIRCUIT

By B. D'HALLUIN

SUMMARY **Page**

I - INTRODUCTION

The TEA2037A is a horizontal and vertical deflection circuit for monitors and black and white TV sets.

This device includes all functions required for deflection, namely :
- Line and frame sync separation
- Line oscillator with phase comparator
- Driver stage for line deflection darlington transistor
- Frame oscillator
- Frame amplifier with flyback generator for direct drive of the vertical deflection yoke.

The TEA2037A is particularly well-suited for low-cost monitors since it is cased in a low-cost package and requires a few number of external components and hence optimized for small displays.

However, application areas are by no means limited. Sophisticated applications requiring various adjustment possibilities such as for display geometry and centering settings (amplitude, linearity,...) and operating at different line and frame frequencies (line frequencies up to 64kHz), are readily configured around TEA2037A.

In large screen applications, addition of a heatsink mounted on TEA2037A will enable the vertical deflection yoke current to be boosted to 2A peak-to-peak.

II - FUNCTIONAL DESCRIPTION OF TEA2037A

II.1 - General Description

The TEA2037A is a 16-pin DIP package. The 4 center pins (2 on each side) are connected together and used as heatsink.

From composite video or TTL-compatible sync. signals, the device will extract and generate all signals required for the line scanning darlington transistor and direct drive of the frame yoke.

The following functional blocks are implemented on-chip :
- Line and frame sync. separator
- Line oscillator
- Line phase comparator
- Line output stage
- Frame oscillator
- Frame amplifier
- Frame flyback generator
- Shunt regulator

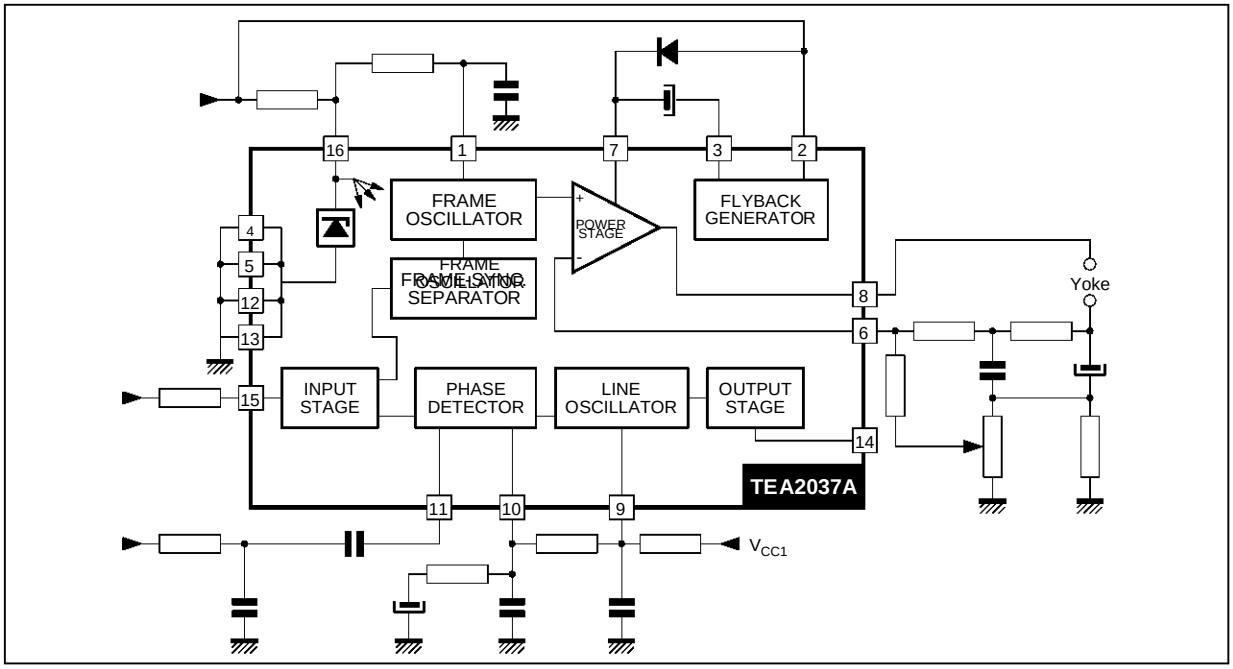
The common device power supply is implemented by the on-chip shunt regulator.

In order to optimize the drive to frame deflection yoke and also enable appropriate use of the flyback generator, the frame amplifier is powered by an independent supply.

The ground is connected to the 4 center pins of the device.

II.1.1 - Block Diagram

Figure 1

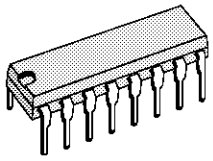


II.1.2 - Pin Description

1	Frame Oscillator
2	V_{CC2} (Flyback generator power supply)
3	Flyback Generator Output
4, 5	Ground
6	Frame Feed-back (frame amplifier inverting input)
7	V_{CC2} (positive power supply for frame output stage)
8	Frame Output (direct drive to frame yoke)
9	Line Oscillator
10	Phase Comparator Output
11	Phase Comparator Input (line flyback)
14	Line Output (drive to line darlington transistor)
15	Video Input (or TTL-compatible sync.)
16	V_{CC1} (shunt regulator)

II.1.3 - Package

Batwing DIP16
(plastic package)



II.2 - Sync. Pulse Separator

The TEA2037A extracts, first the line and frame sync. pulses from the composite video signal and then the largest pulses, i.e., the frame syncs.

II.2.1 - Extraction of Sync. Pulses from the Composite Video Signal (TV application)

Figure 2 : Synchronization Separator Circuit

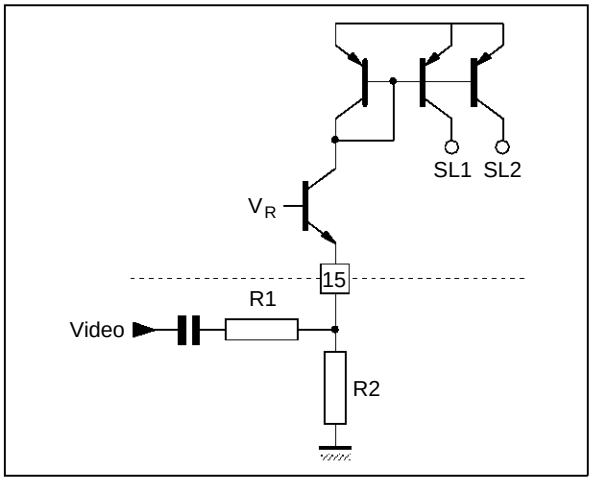
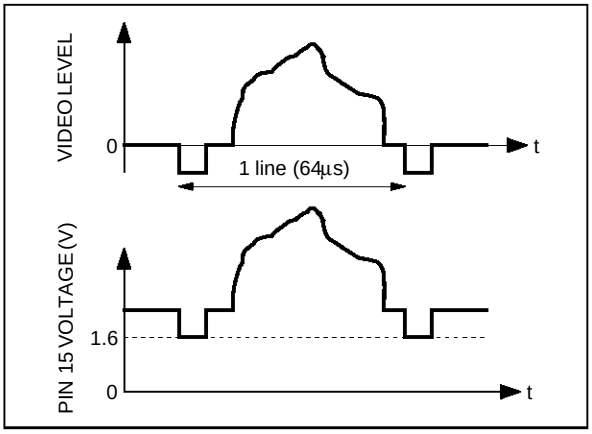


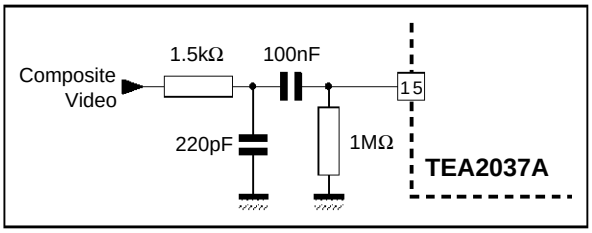
Figure 3



- The sync. detection level is set at 1.6V.
- The value of R2 is typically 1MΩ (fixed for a good internal bias).
- Resistor R1 limits the output current of Pin 15.

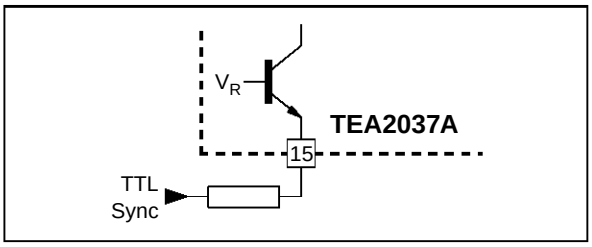
As illustrated in the Figure 4, it is recommended to employ a low-pass filter which will suppress high-frequency harmonics susceptible to produce jitters on line sync signal in composite video TV applications.

Figure 4



II.2.2 - Negative TTL Sync. (Monitor application)

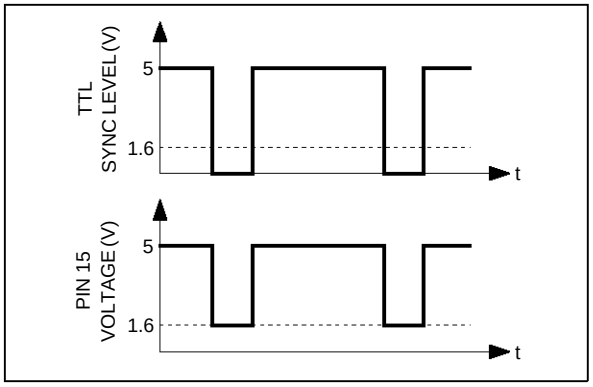
Figure 5



In monitor application, the sync. signal is generally separated from the video signal.

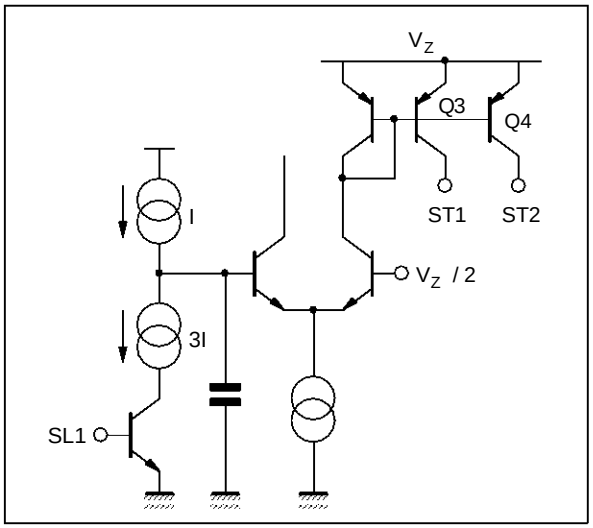
In this case, the sync. signal is applied to Pin 15 through a single limiting resistor. Similar to the former case, the sync. is detected when the input voltage falls below 1.6V level.

Figure 6



II.2.3 - Frame Sync. Extraction

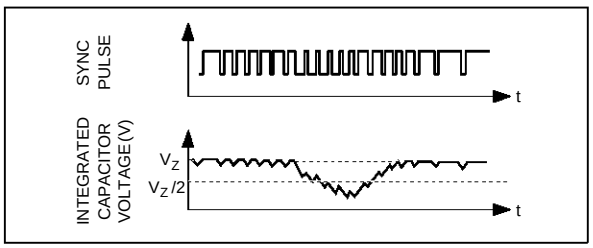
Figure 7 : Frame Separator



This function is processed internally and hence does not require any external component. Line and frame sync. pulses are distinguished by an integrated capacitor which is more or less discharged during each sync. pulse interval as follows :

- if the sync pulse duration is short, i.e. it is line sync, then the capacitor is slightly discharged
- on the other hand, if the pulse width is larger, the capacitor is fully discharged and an internal frame signal is thus generated.

Figure 8



II.3 - Line Oscillator

Figure 9

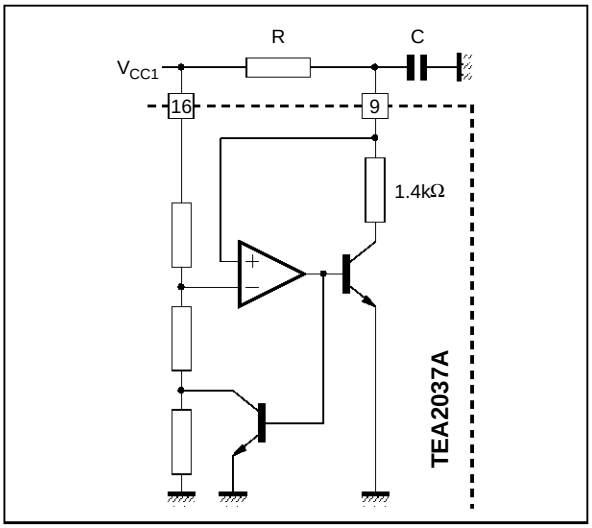
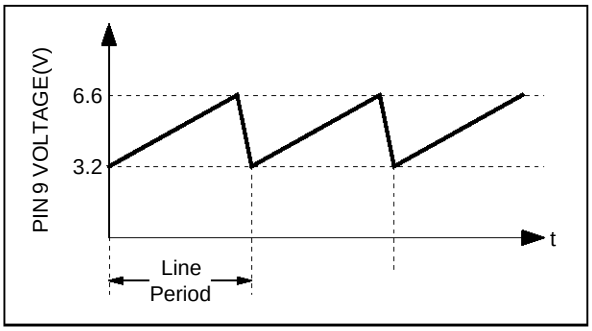


Figure 10



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- if the sync pulse duration is short, i.e. it is line sync, then the capacitor is slightly discharged
- on the other hand, if the pulse width is larger, the capacitor is fully discharged and an internal frame signal is thus generated.

The line saw-tooth is generated by charging an external capacitor on Pin 9 via a resistor connected to V_{CC1} (Pin 16).

The capacitor is discharged via an internal 1.4kΩ resistor. The saw-tooth amplitude is set by two on-chip threshold levels :

- lower threshold : 3.2V
- higher threshold : 6.6V

The free-running period is approximately given by the following relationship :

$$T_{OSC} \approx 0.85\,RC$$

The phase comparator will modify the capacitor charge by injecting a positive or negative current so as to produce correct phase and frequency relationships with respect to the synchronization signal.

II.4 - Line Output Stage

The line output stage has been designed for direct base drive of the horizontal scanning darlington transistor.

The low level interval on Pin 14, i.e. the power line transistor blocking period, is determined by the time when the voltage of the line oscillator capacitor (Pin 9) is below 4.8V (internally set threshold level). In a typical application, this interval corresponds to 22µs at 64µs free-running period.

Figure 11

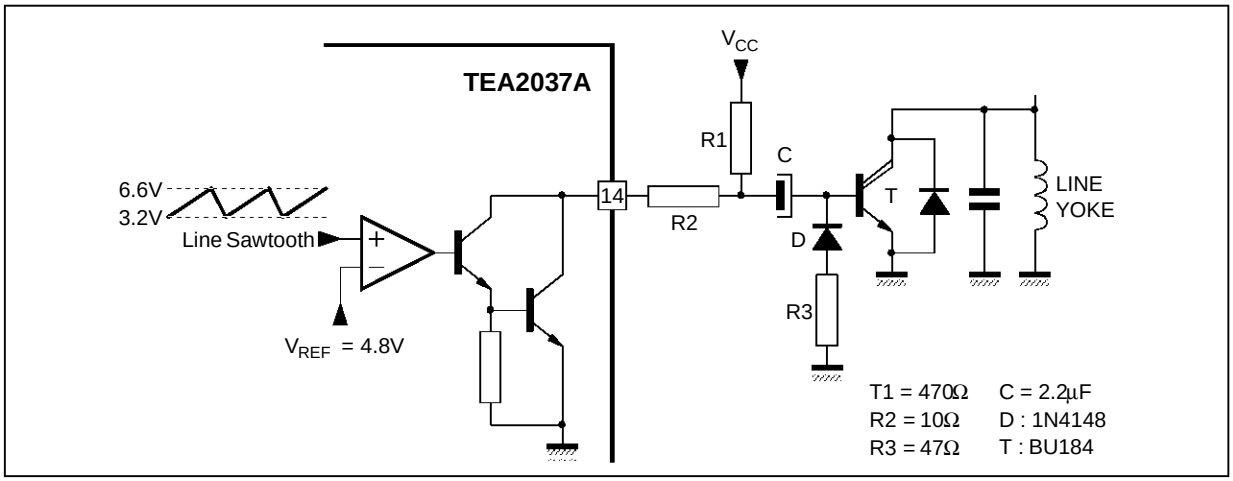
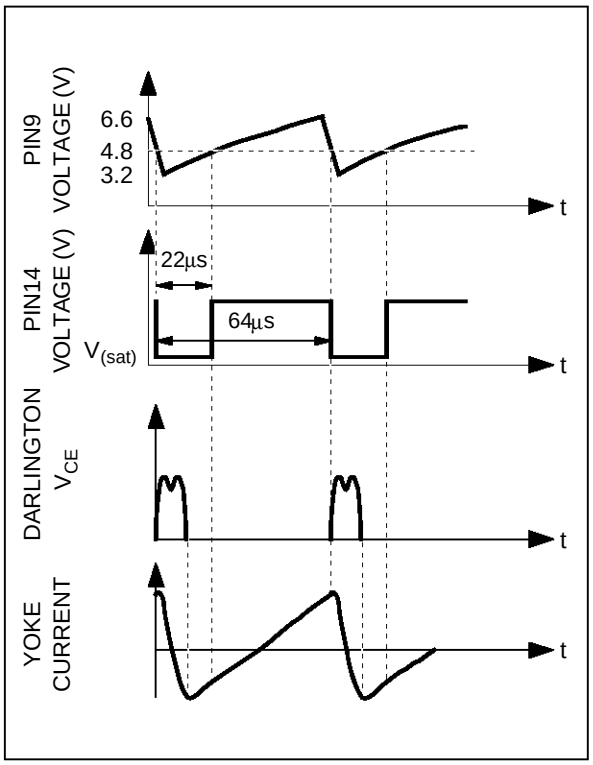


Figure 12

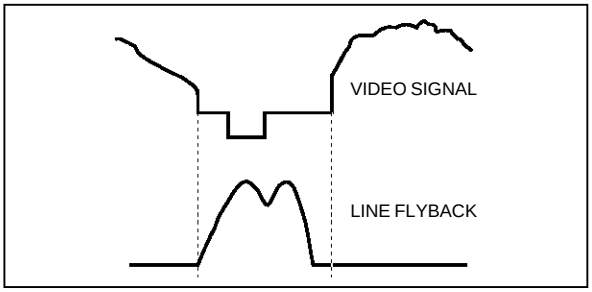


II.5 - Phase Comparator (PLL)

II.5.1 - Functional Description

The duty of phase comparator is to synchronize the horizontal scanning with the line sync pulse and ensure correct line flyback during the horizontal blanking phase.

Figure 13



The line flyback signal (i.e. the pulse on the collector of the line scanning transistor) is compared with the line sync. signal issued by sync. separator. If the detected coincidence is incorrect, the comparator will then generate an appropriate positive or negative current so as to charge or discharge the line oscillator capacitor thereby providing for frequency and phase locking.

II.5.2 - Phase Comparator Operation

Figure 14

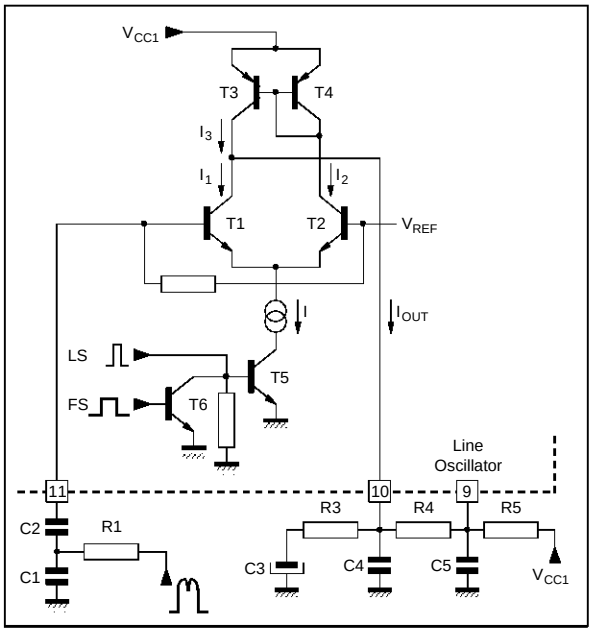
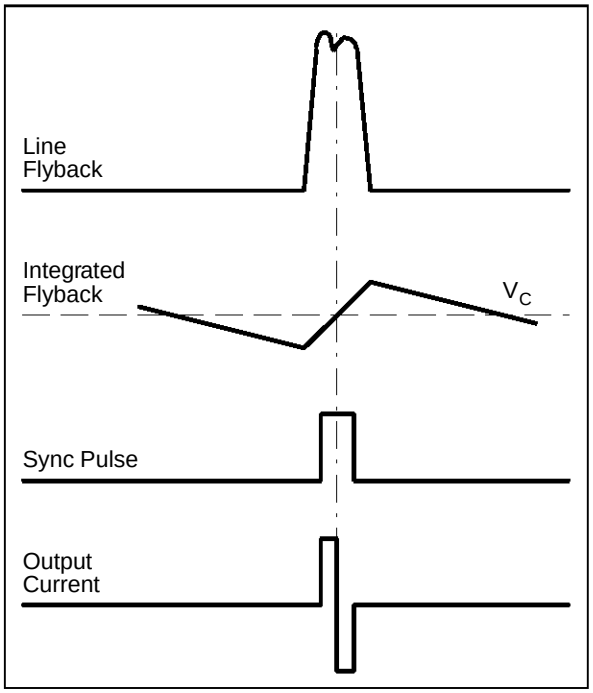


Figure 15 : Phase Comparator



The line flyback signal goes through integrator network R1C1 the output of which, a saw-tooth signal, is applied to comparator input (Pin 11) via capacitor C2.

The comparator input stage is formed by the differential pair T1 and T2. T3 and T4 transistors are arranged in current mirror configuration and thus :

$$i_3 = i_2$$

The sum of currents going through T1 and T2 transistors is determined by the current generator "I" so that :

$$I = i_1 + i_2$$

The comparator output current is the difference current through the differential pair, i.e. :

$$i_{OUT} = i_2 - i_1$$

The comparator is enabled by T5 transistor only during the line sync. interval.

Transistor T6 inhibits the phase comparison during the frame sync. interval.

During the first portion of the flyback, the voltage at comparator input (Pin 11) is lower than the reference voltage. T1 is off and T2 conducts ; consequently the comparator output goes positive :

$$i_{OUT} = + I$$

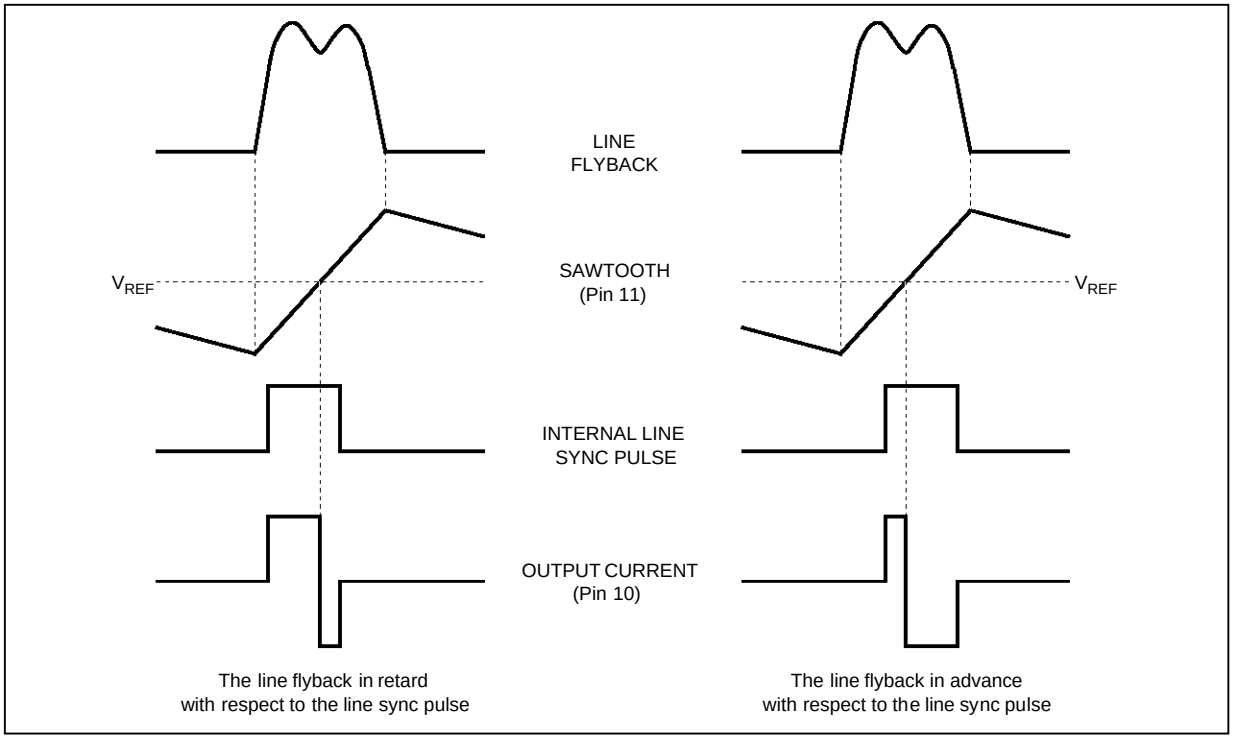
During the second portion, the input voltage exceeds the reference voltage and as a result, the comparator ouput falls to negative level :

$$i_{OUT} = - I$$

If the line flyback is in retard with respect to the horizontal sync. pulse (which is the case of too long line periods), the interval for which the phase comparator's output current is positive would increase. This current is then filtered and applied to the line oscillator capacitor (C5) thereby accelerating its charge-up phase and hence reducing the line period.

Inverse action takes place if the line flyback is in advance - the negative current at comparator's output will rise, C5 is charged more slowly and the line period is thus increased.

Figure 16



II.5.3 - Output Filter

Figure 17

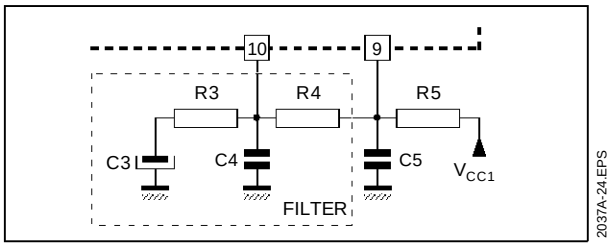
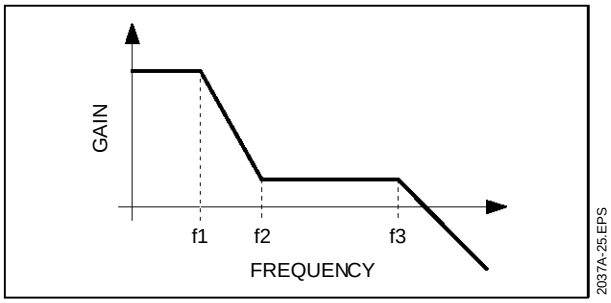


Figure 18



$$f_1 = \frac{1}{2\pi\,(R3 + R4)\,C3}$$

$$f_2 = \frac{1}{2\pi R3C3} \qquad f_3 = \frac{R3 + R4}{2\pi R3R4C4}$$

The duty of the output filter is to ensure the stability of the locked loop and its characteristics will have a partial influence on capture range and also on capture time.

The holding range, which is larger than the capture range, depends on the ratio of the current available at the comparator output and the charging current of the line oscillator. The holding range does not depend directly on the cut-off frequencies of the output filter. But, as the voltage range at the comparator output is limited, a too high value for R4 will limit the holding range.

The sync. pulse duration has significant influence on capture range and also on the holding range of the device. The output current duration is directly related to synchronization pulse width.

- First the R5 x C5 product is selected to yield the required free-running line oscillator frequency.
- Then, the value of C5 capacitor is selected as follows :
  - for monitor applications (large holding range) low value; e.g. : 2.2nF @ 16kHz, 1nF @ 32kHz
  - for TV applications
  - higher value; e.g. : 4.7nF @ 16kHz
- Finally, the filter components are selected to match the required capture range.
  (R4 ≤ 100kΩ to prevent comparator output saturation)

II.6 - Frame Oscillator

Similar to line oscillator, the frame saw-tooth is generated by charging an external capacitor on Pin 1 through a resistor connected to V_{CC1}.

Figure 19

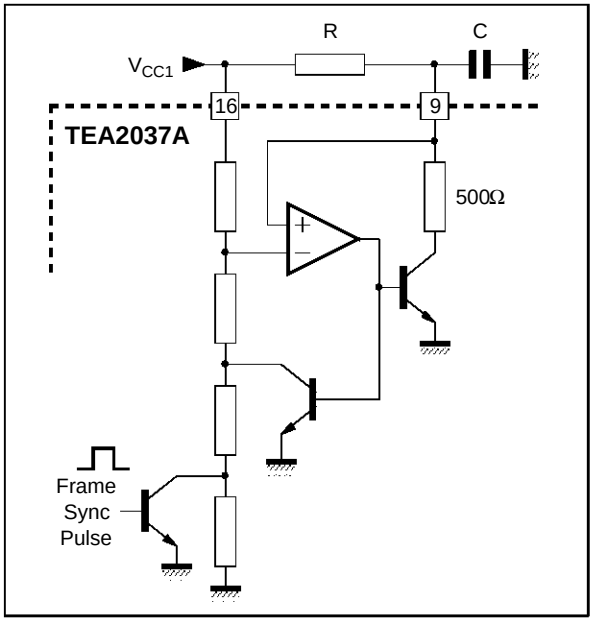
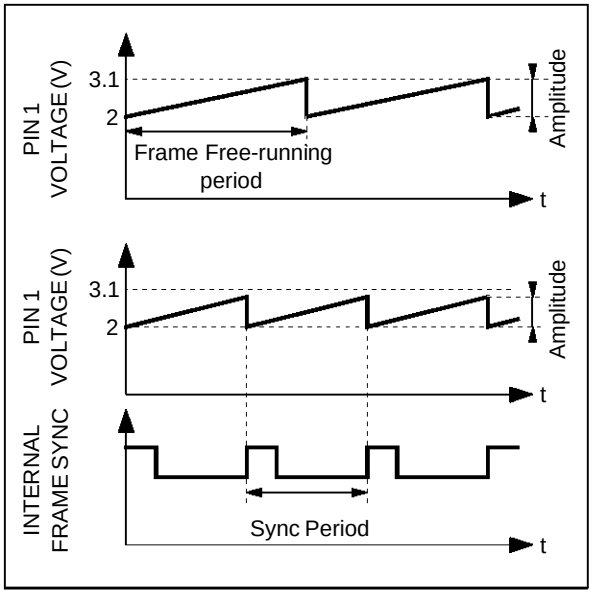


Figure 20



The capacitor is discharged via an internal 500Ω resistor. The saw-tooth amplitude is set at two on-chip threshold levels.

The free-running period is approximately given by :

$$T_{OSC} \approx 0.15\ RC$$

Synchronization is achieved by period reduction.

The frame sync. pulse issued by the sync. separator will modify the current through the resistor bridge which is used to set the saw-tooth threshold levels.

The minimum synchronized frame period (MSFP) is given by :

$$MSFP \approx \frac{T_{OSC}}{1.8}$$

II.7 - Frame Output Amplifier

The frame saw-tooth generated by frame oscillator is first inverted (Gain : - 0.4) and then applied to the non-inverting input of the frame amplifier. The output current capability of this amplifier is as high as ± 1A thus enabling to drive vertical deflection yokes requiring 2A peak-to-peak.

As a function of dissipated power, the device may require the addition of a heatsink.

A feed-back loop is connected to the inverting input of the frame amplifier (Pin 6).

As the CRT screen is not part of a sphere centered on the deflection center point, if the yoke is actually driven by a saw-tooth waveform, the image is expanded at the top and bottom. The yoke must therefore be provided with an "S" waveform current, by applying linearity correction.

Figure 21

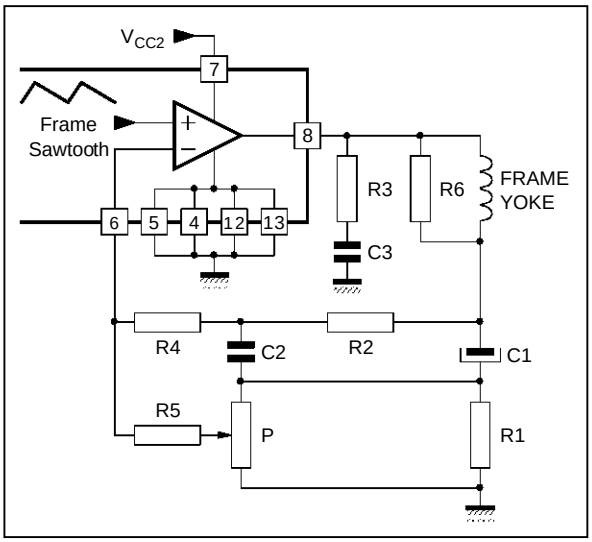
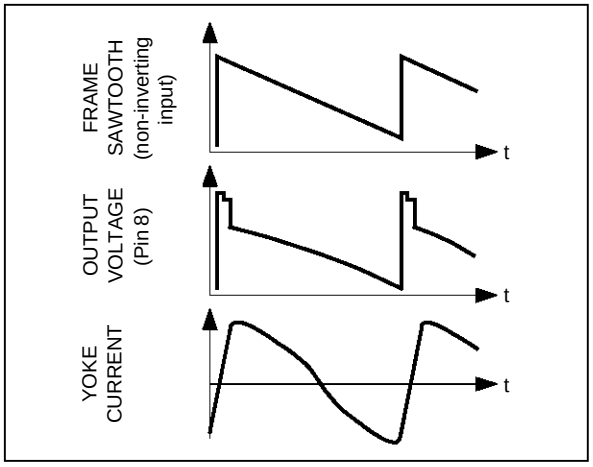


Figure 22



The circuit configuration depicted above does not require any linearity adjustment - only an amplitude adjustment potentiometer "P" has been provided for.

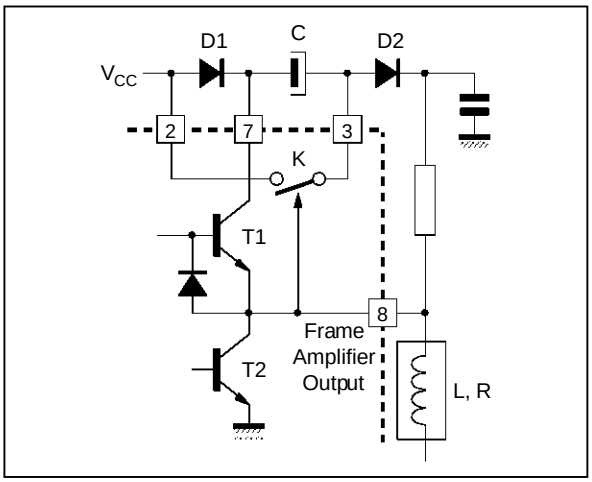
- **D.C. Feedback :** The C1 capacitor is charged to approximately 1/2 x V_{CC2}. Divider bridge formed by R2 + R4 and R5 networks will set the d.c. feedback. The component values of this divider network will be choosen to avoid saturation at top and bottom of the output voltage (Pin 6 biasing voltage is approximately 0.6V).
- **Linearity Correction :** Aparabolic signal at frame frequency is available on "+" terminal of the C1 capacitor. This signal is integrated by R2, C2 network. An "S" waveform is thus obtained, which is applied to Pin 6 via resistor R4.
  Any correction to this "S" waveform depends on C1 and C2 values. The linearity correction depends on ratio : R2/R4
- **Vertical Amplitude :** Frame current amplitude is determined by the value of measurement resistor "R1", potentiometer "P" settings and the value of "R5" resistor.

II.8 - Frame Flyback Generator

The output stage of the vertical amplifier includes a frame flyback generator connected to pin 3. During the vertical scanning flyback time, the value of the yoke inductance "L" must be taken into account since the time constant L/R is no longer negligible. In television applications, the frame blanking time is 1.6ms. Thus when $L/R > 1.6 \times 10^{-3}$, it is necessary to increase the supply voltage to the frame output amplifier so as to reduce the flyback time. This surplus is required only for the frame flyback and energy is wasted by boosting the supply to the amplifier at all times (during the frame scanning time, the minimum voltage is substantially RI, where I is peak-to-peak frame current).

The configuration of the flyback generator is depicted in Figure 23.

Figure 23

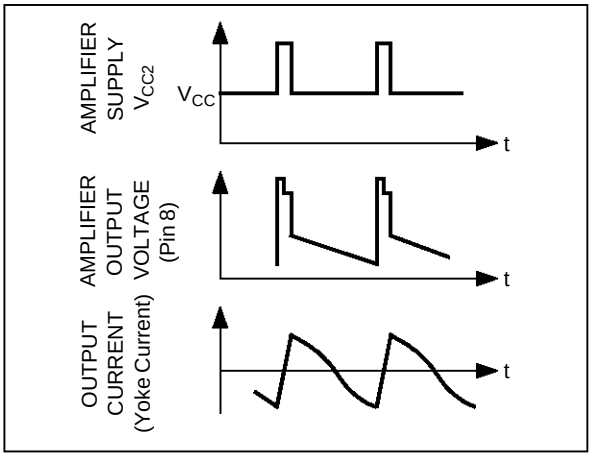


During the second half of the vertical scanning time, transistor T2 conducts and capacitor C is charged to V_{CC} through D1, D2, R3 and T2. (Switch K open)

On flyback, switch K closes and Pin 3 is connected to V_{CC}. The voltage at Pin 7 (V_{CC2}), which was equal to V_{CC} - V_{D1}, is almost doubled during the flyback time. The only external components required are therefore D1, D2 and C.

In addition to reducing the flyback time, the flyback generator reduces the power consumed by the power stage, and can in certain cases avoid the need to use a heatsink.

Figure 24



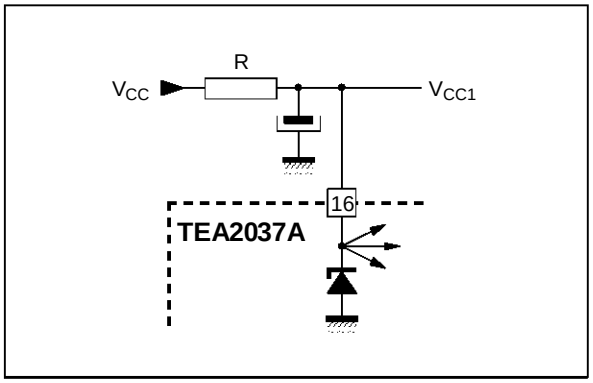
Diode D2 is a low-signal diode (1N4148) but diode D1 must be appropriately rated since the positive current in the first part of the saw-tooth is supplied to the yoke through D1 and T1. A 1N4001 is generally used.

II.9 - The shunt regulator

The TEA2037A incorporates an internal shunt regulator which delivers the common supply voltage V_{CC} to various blocks such as oscillators, comparator, sync separator and so on.

The voltage on Pin 16 is 9.7V (9V min, 10.5V max). The value of the series resistor R must be so calculated to obtain a 15mA current on Pin 16 - this current can be 10mA min. and 20mA max.

Figure 25



The external current supply from V_{CC1} to both oscillators (i.e. line and frame) can be neglected in majority of cases.

The resistor value is found to be 1.2kΩ at V_{CC} = +28V.

At V_{CC} = + 12V, and taking into account the voltage tolerance on Pin 16, a 150Ω series resistor must be used.

II.10 - Thermal Considerations

In order to ensure reliable device operation, the dissipated power should be accurately determined. Calculation will allow an evaluation of the dissipated power and should be completed by package temperature measurements in actual applications. According to results obtained, a heatsink may or may not be required.

- Power drawn from V_{CC1} supply :

$$P1 = V_{CC1} \cdot I_1$$

Where I_1 is the current through the shunt regulator (Pin 16).

- Power drawn from V_{CC2} supply :

$$P2 = V_{CC2}\left(\frac{I_{PP}}{8} + I_2\right)$$

Where :
- Ipp = peak-to-peak current through the vertical deflection yoke.
- I_2 = Pin 7 quiescent current.
- V_{CC2} = Pin 7 voltage.

- Power dissipated in deflection yoke and the measurement resistor :

$$P_Y = (R_Y + R_M)\frac{I^2pp}{12}$$

Where :
- R_y = Frame deflection yoke resistance
- R_M = Measurement resistor value

Thus, the overall power dissipated in the integrated circuit is :

$$P_D = P1 + P2 - P_Y$$

$$P_D = \left[V_{CC1} \cdot I_1\right] + \left[V_{CC2}\left(\frac{Ipp}{8} + I_2\right)\right] - \left[(R_Y + R_M)\frac{I^2pp}{12}\right]$$

In application using the flyback generator, the V_{CC2} specified above becomes "V_{CC2} - V_D", where V_D is the voltage drop across the series diode.

Figure 26

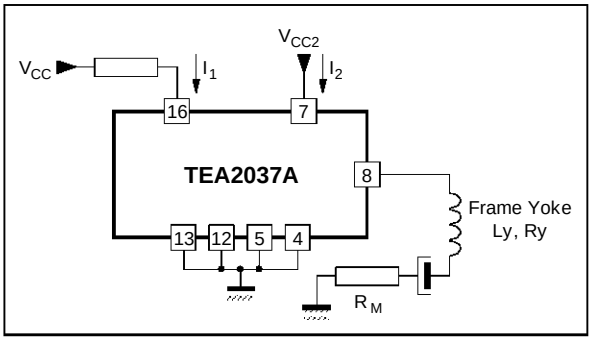
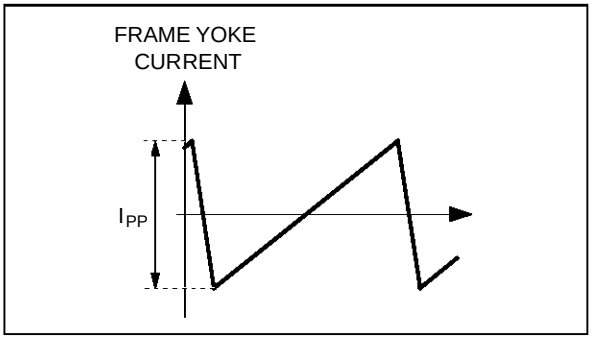


Figure 27



III - APPLICATIONS

III.1 - Monitor Applications

III.1.1 - Low-cost monitor (French Minitel Type) (see Figure 28)

CHARACTERISTICS

- Screen : 9" Monochrome
- Frame deflection yoke : 72mH, 40Ω, 220mA peak-to-peak
- V_{CC} = + 25V without flyback generator
- Frame flyback time : 1.2ms
- Vertical frequency : 50Hz (20ms)
- Vertical free-running period : 24.5ms
- Horizontal frequency : 15 625Hz
- Capture range : ±5µs
- Holding range : ±10µs
- Input signal : composite video
- Dissipated power : 1.15W
- Only one adjustment : vertical amplitude

This is a low-cost application used in French Minitel type configurations and requires minimum number of additional components and adjustments. The input is a composite video signal at line frequency = 15 625Hz and frame frequency of 50Hz.

The free-running horizontal frequency is determined by the component values of RC network on Pin 9. Since no adjustment is available, precision components must be used to ensure correct synchronization :

[R = 35.7kΩ, 1% and C = 2.2nF, 2% for f_H = 15 625Hz]

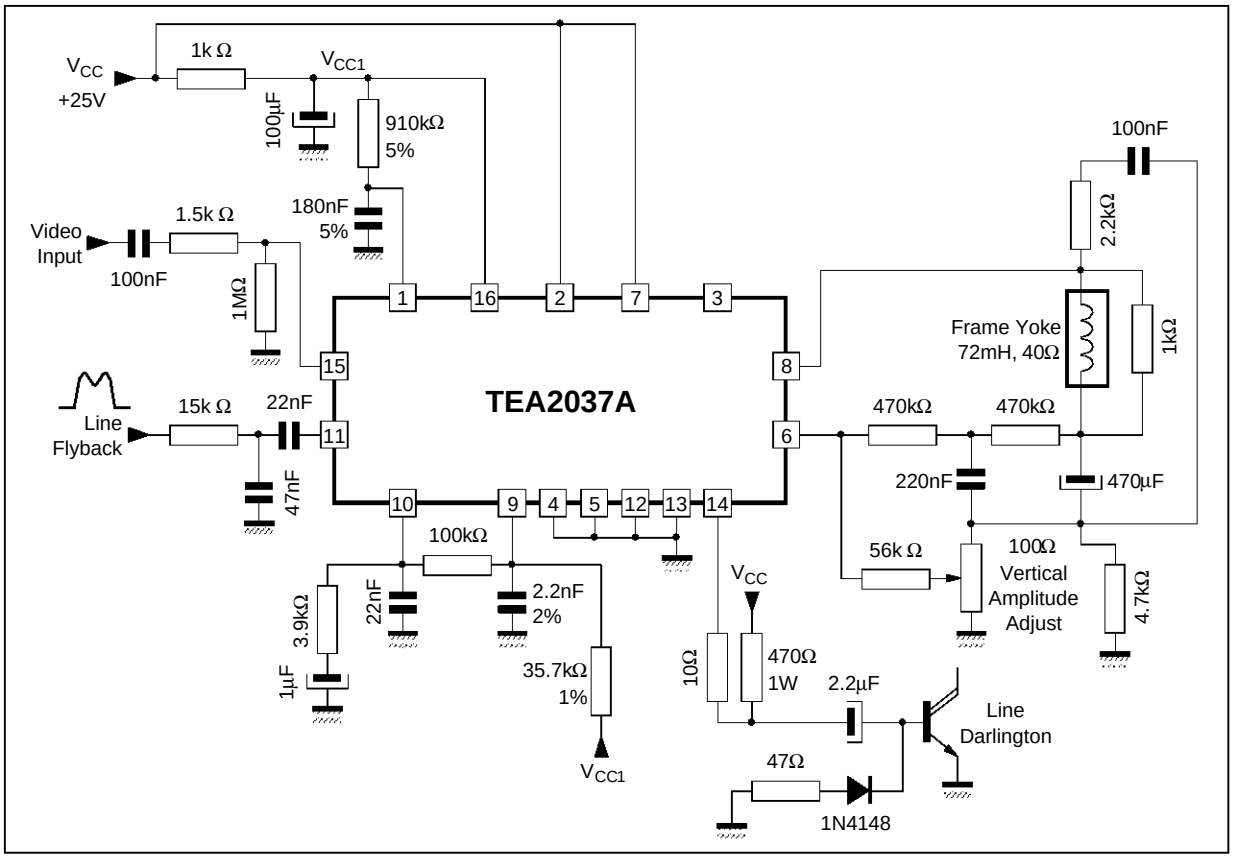
The capture range is large enough to compensate for possible variations.

- Synchronization range of the vertical oscillator is quite large which consequently allows use of less accurate components :

[R = 910 kΩ, 5 % and C = 180 nF, 5 %]

- Since the frame flyback time is short enough at supply voltage used here, the flyback generator is not used in this application.

Figure 28

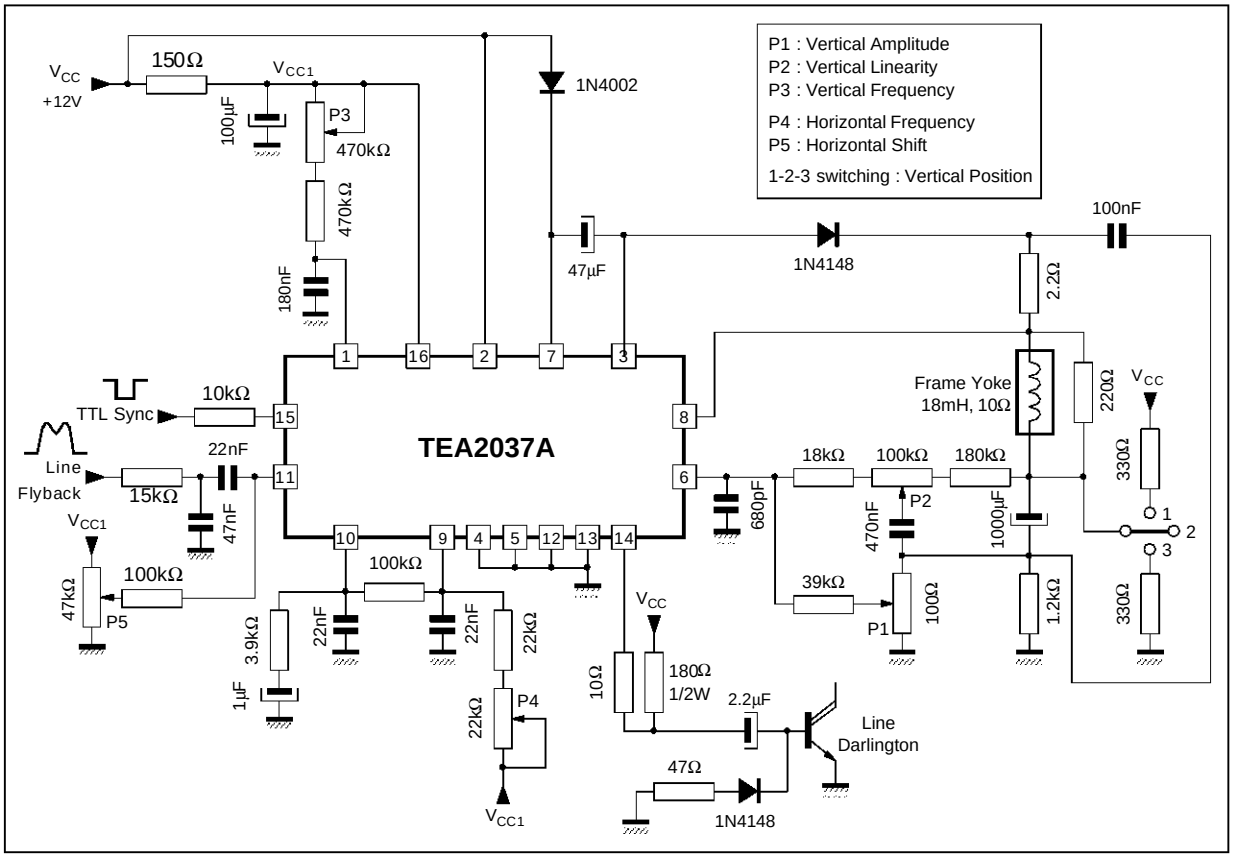


III.1.2 - Monitor with Geometry and Frequency Adjustments (see Figure 29)

CHARACTERISTICS

- Screen : 12" Colour
- Frame deflection yoke : 18mH, 10Ω, 500mA peak-to-peak
- V_{CC} = + 12V with flyback generator
- Frame flyback time : 0.7ms
- Vertical frequency : 50/60Hz
- Vertical free-running period : 23ms (adjustable)
- Horizontal frequency : 15.7kHz (adjustable)
- Capture range : = ±5µs
- Holding range : ±10µs
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 0.9W
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Vertical frequency
  - Horizontal frequency
  - Horizontal phase-shift

Figure 29

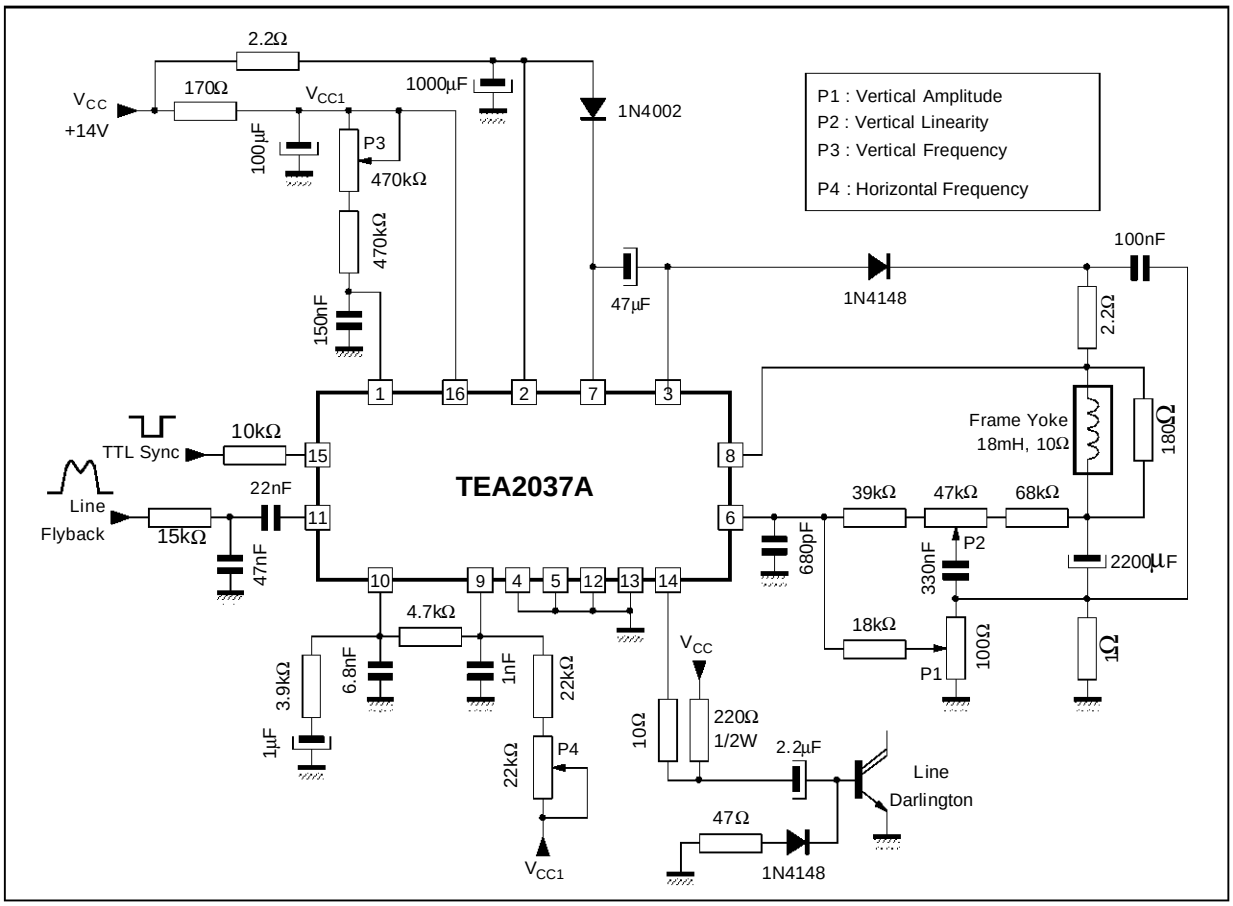


III.1.3 - High Frequency Monitor (see Figure 30)

CHARACTERISTICS

- Screen : 14" Colour
- Frame deflection yoke : 11mH, 7Ω, 750mA peak-to-peak
- V_{CC} = + 14 V with flyback generator
- Frame flyback time : 0.6ms
- Vertical frequency : 72Hz
- Vertical free-running period : 16ms (adjustable)
- Horizontal frequency : 35kHz (adjustable)
- Line flyback time : 5.5µs
- Capture range : 5µs (@sync pulse = 4.7µs)
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 1.4W (heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Vertical frequency
  - Horizontal frequency

Figure 30

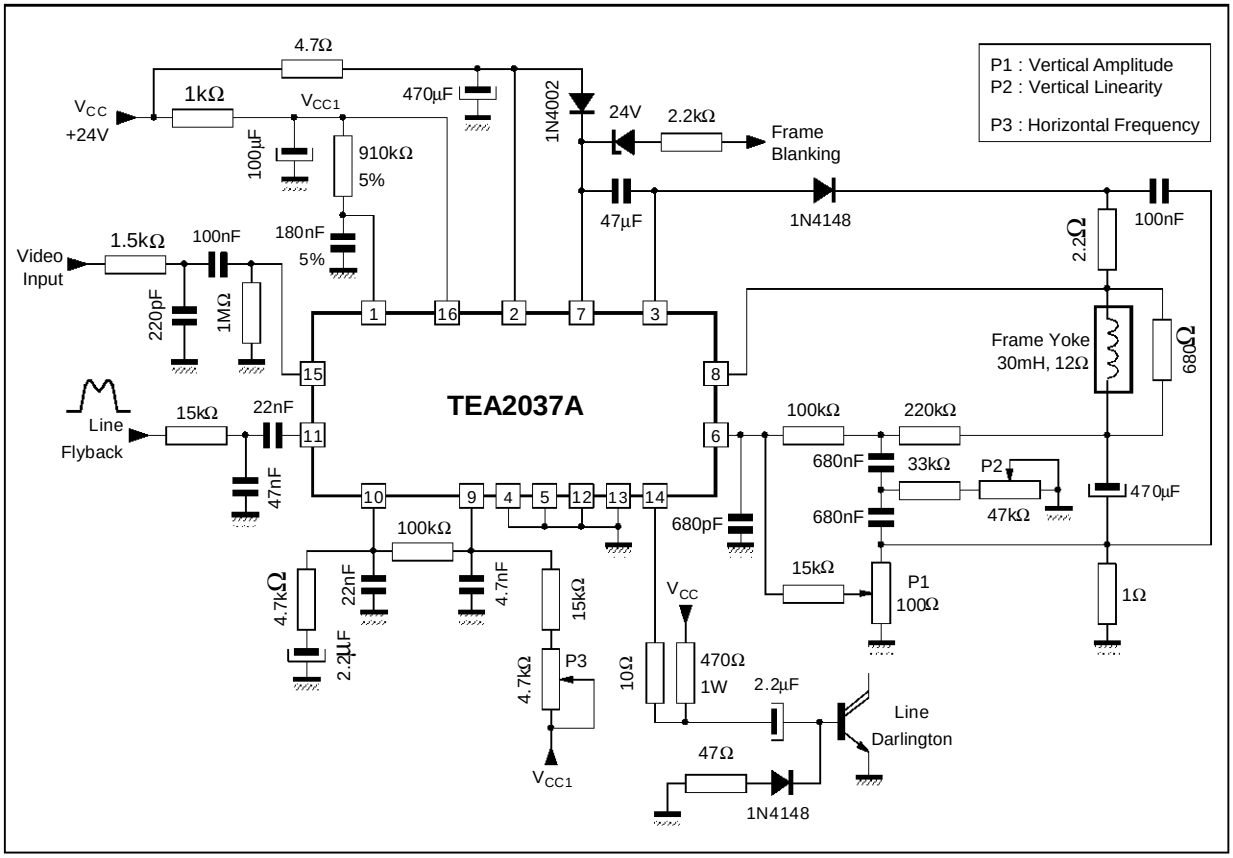


III.2 - Black & White TV Application (see Figure 31)

CHARACTERISTICS

- Screen : 20" B & W 110°
- Frame yoke : 30mH, 12Ω, 850mA peak-to-peak
- V_{CC} = + 24 V with flyback generator
- Frame flyback time : 1ms
- Vertical frequency : 50Hz
- Vertical free-running period : 24.5ms
- Horizontal frequency : 15 625Hz (adjustable)
- Capture range : ±2 µs
- Holding range : ±4.5 µs
- Input signal : composite video
- Dissipated power : 2.3W (10°C/W - heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Horizontal frequency

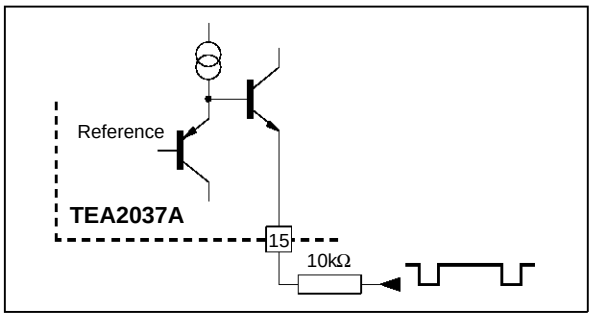
Figure 31



III.3 - Using Composite TTL Synchronization

Since the threshold level on input Pin 15 is internally set at 1.6V, the device can directly accept TTL signals.
However, a series resistor is required to limit the current sunk by the on-chip transistor (Pin 15).

Figure 32



If composite sync signal is not available, line and frame sync signals can be recombined at circuit input as illustrated in Figure 33.

Figure 33

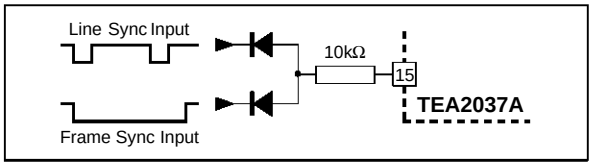
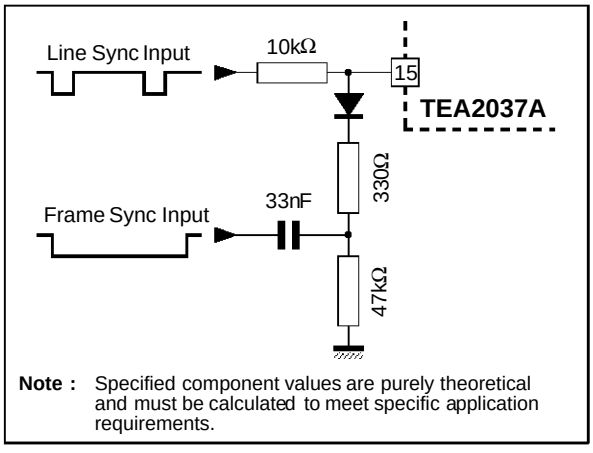


Figure 34 : Application Example



Note : Specified component values are purely theoretical and must be calculated to meet specific application requirements.

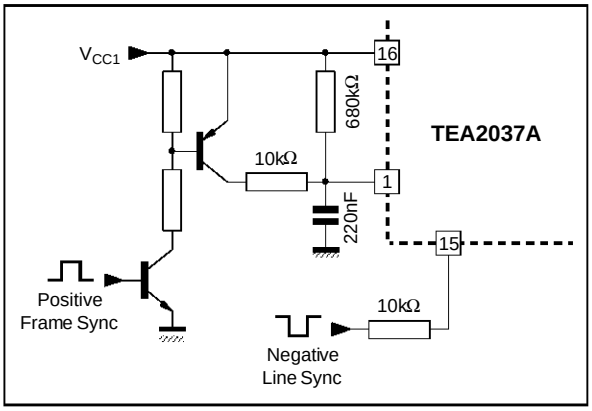
This arrangement is particularly interesting in applications where the available signals differ from those commonly used. An example is the case where the frame signal is of quite long duration (sometimes as long as frame blanking period). In such case, efficient synchronization can be achieved by differentiating the signal so that it will behave as a signal of only few lines duration which is the condition required for appropriate frame and line sync separation and also a picture without flag effect.

III.4 - Direct Frame Synchronization

The vertical scanning can be directly synchronized by the frame oscillator (Pin 1) and without any need of using the synchronization input (Pin 15).

Figure 35 illustrates an example : In this case, only the line sync pulse is applied to Pin 15.

Figure 35



III.5 - Constant Amplitude 50/60Hz Switching

In applications requiring 50/60Hz standard switching feature, the arrangement shown below allows to maintain the amplitude of the oscillator saw-tooth (Pin 1) constant thus yielding uniform vertical scanning.

Figure 36

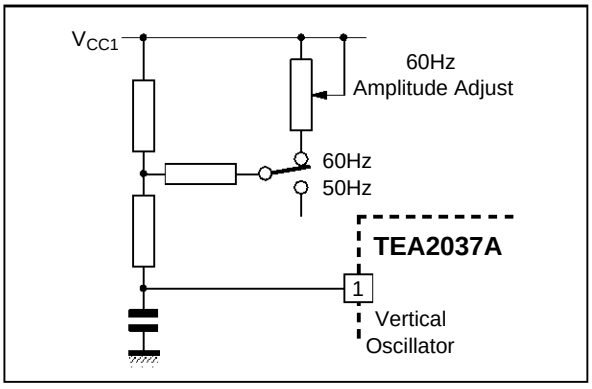
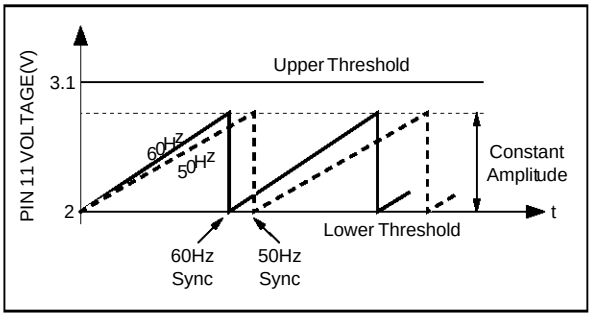
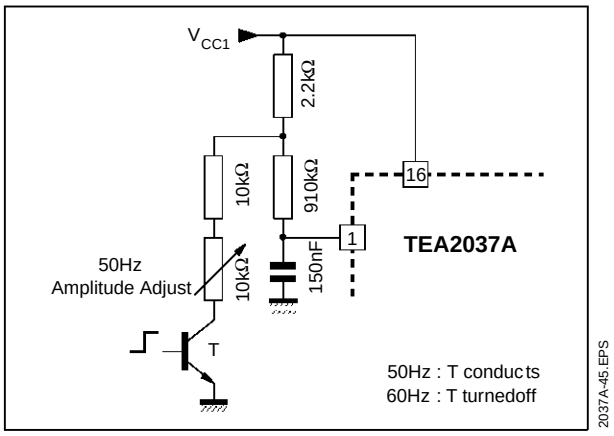


Figure 37



A practical application configuration is illustrated in Figure 38.

Figure 38



III.6 - Modifying the Line Output Duration

(see Figures 39 and 40)

The line output pulse duration is determined by two internally set threshold levels. This interval can be altered by modifying the charge current of the line oscillator (Pin 9).

III.7 - Starting the TEA2037A from a +6V Power Supply

The line oscillator of TEA2037A is capable of starting at a low supply voltage (< 6V). The period of oscillation is practically the same as at nominal operation. It is thus possible to initiate the line scanning at a reduced supply voltage (e.g. +6V) and then supply the overall configuration by the power available on the line transformer (see Figure 41).

Figure 39

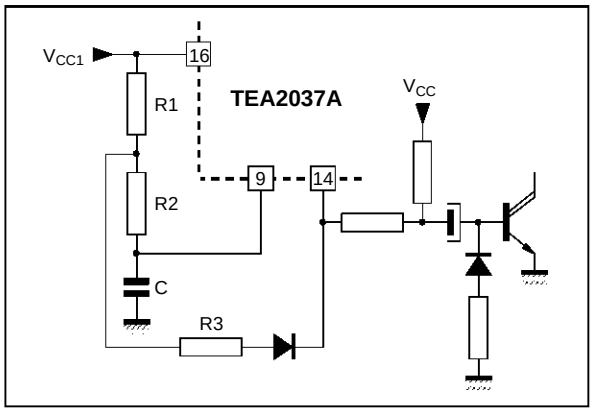


Figure 40

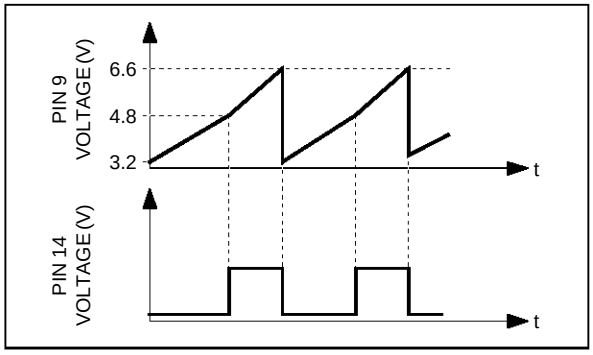
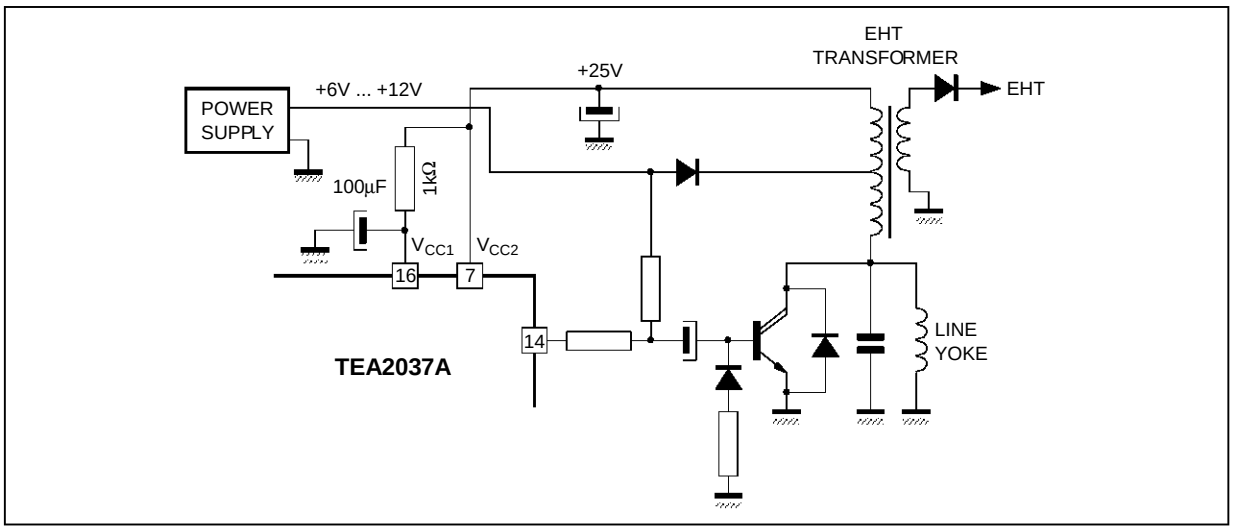


Figure 16



IV - DESIGN CONSIDERATIONS

IV.1 - Precautions for Interlaced Scanning

- The links interconnecting the ground terminals of V_{CC} and V_{CC1} power supplies, as well as those of device decoupling capacitors, must be kept to as short as possible
- A high value decoupling capacitor can be used for V_{CC} supply, provided that a good quality low series resistance capacitor is employed. Interlacing is very sensitive to decoupling quality. The value of the decoupling capacitor can vary from 22µF to 100µF.
- The interconnecting links between the frame oscillator capacitor, the line oscillator capacitor and TEA2037A grounds must be kept to as short as possible.

Perfect line and frame synchronization is achieved by observing the above guidelines and recommendations.

IV.2 - Printed Circuit Board Layout

The usual precautions observed in design of TV timebase pc boards must be employed

The line output stage handles high amounts of voltage and current. Components employed must therefore be appropriately rated, the width of and the clearance between the wiring tracks should be carefully selected. All connections must be as short as possible and all signals at the line frequency gathered at this section.

The supply to the frame scanning section of the circuit must not be influenced by the horizontal scanning function, particularly when interlaced scanning is used.

Generally speaking, interactions on the pc board between the high-gain/low-level and the high-current sections of the output stages must be minimized by as much as possible.

As indicated in previous chapters, the four center pins of the device must be earthed. The pad used for this purpose must be as large as possible since it acts as the heatsink for the device. A cruciform pad underlying the circuit should be employed.

There should be a single connection to the chassis earth terminal.