Common Bus CPU Card (C3) Family for 64-bit MIPS Processors

PRELIMINARY

IDT7M9516 IDT7M9521
IDT7M9518 IDT7M9522
IDT7M9519 IDT7M9523
IDT7M9520

FEATURES:

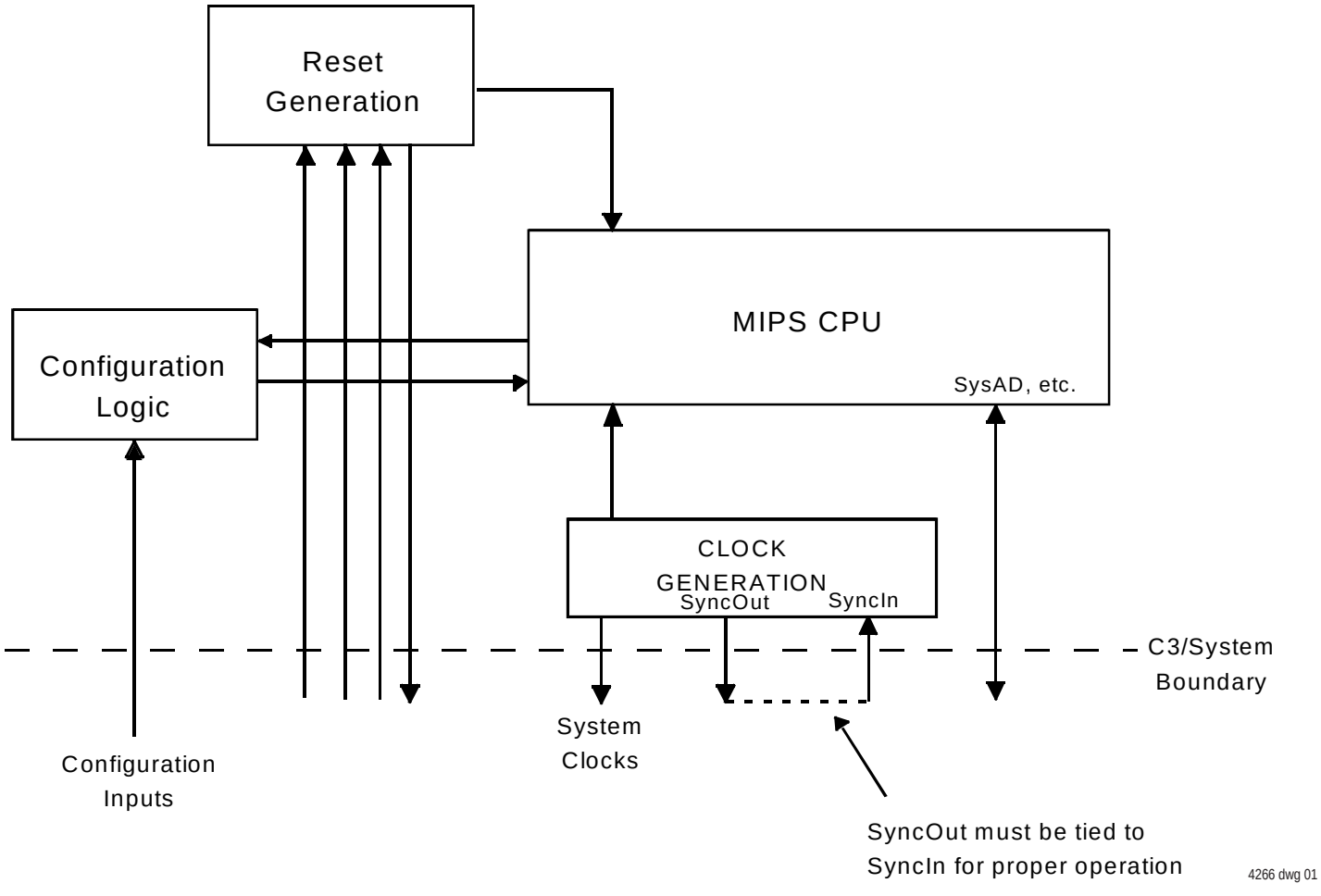
- **Supports IDT Common Bus CPU Card (C3) electrical and mechanical specifications.**
- **C3 Card family supports IDT 64bit MIPS family including R4650, R4700, R64475, R5000, R64575 for easy scaling of performance.**
- **Low profile, mezzanine form-factor. Ideal daughtercard for:**
  - *Compact PCI*
  - *VME*
  - *Ethernet / ATM switches*
- **Utilizes SAMTEC CLP connectors**
  - *100 pin Conn. A: part number: CLP-150-02-L-D-PA*
  - *96 pin Conn. B: part number: CLP-148-02-L-D-PA*
- **Onboard clock generation circuitry for processor/system clocks**
- **Onboard processor reset and configuration circuitry.**
- **5V Tolerance**

DESCRIPTION:

The C3 family are CPU mezzanine daughtercards based on IDT's MIPS processors. The C3 Card family is designed to replace the CPU and specific support circuitry around the CPU in a system design. The goal of the C3 is to provide the system designer a seamless hardware migration path through IDT's family of 64-bit MIPS processors(R4650, R4700, R64475, R5000, R64575), and to simplify the overall system implementation requirements of those processors.

Each of the above processors has a unique pin configuration/package; therefore, a system designer would normally be required to implement a unique board design for each of the processors. The goal of the C3 is to eliminate the differences between these processors at the system interface level, and to allow the system designer to implement a single baseboard design which will support C3 cards featuring the R4650, R4700, R64475, R5000, R64575 or future processors.

FUNCTIONAL BLOCK DIAGRAM



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JULY 1999

BOARD OVERVIEW

The C3 processor cards consist of the following functional blocks: 64bit MIPS CPU, clock generation circuitry for the processor/system clocks, processor reset and configuration circuitry, and an optional L2 cache subsystem.

RESET CONFIGURATION

The C3 contains on board reset generation logic that provides all of the reset requirements of the processor. This reset logic handles all Power On Reset requirements, as well as handling two system hard reset sources (S_HardRST*, A_HardRST*) and a system soft reset source (SoftRST*). In addition, the reset logic of the C3 also provides a reset output (RSTOut*) to the system that is asserted whenever there is a processor hard reset.

C3 CONFIGURATION

The C3 is configured through a set of static configuration inputs. The configuration inputs are used for both C3 clock configuration and processor configuration. The clock configuration inputs are used to set the system bus clock frequency and the CPU core to system bus clock multiplier. The processor configuration inputs are used to configure the following: endianess (big/little), drive strength (83%/100%), internal timer (enabled/disabled), write type (R4X00/pipelined) and block write data rate (D/Dx/Dxx/Dxxx).

CLOCK GENERATION

The C3 provides nine clock outputs that are associated with system bus clock generation, as well as a 20MHz clock output and a 24MHz clock output. The ten bus clock outputs consist of nine identical buffered system clocks and one dedicated output for processor to system clock synchronization. The system clocks - SysCLK(0:8) - are provided to drive devices on the system bus, as well as other devices that need to operate at the system clock frequency. The processor synchronization clock output (SyncOut) must be connected to the processor synchronization clock input (SyncIn) through a delay path that matches the delay path of the system clocks to ensure proper operation of the C3 in the system. The 20MHz and 24MHz clocks are provided for system peripherals that have fixed frequency requirements.

WATCHDOG TIMER

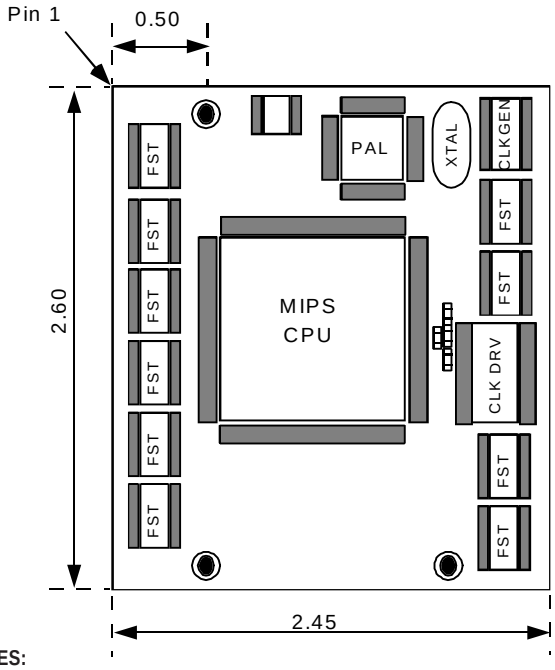
The watchdog timer input (WDStrb pin B-172) of the C3 must be strobed periodically to prevent the watchdog timer output (WDO* pin B-173) from being asserted. If the input is not strobed within 1 second of the previous strobe, the output will be asserted. Note that if the watchdog timer functionality is not required, these pins can be left unconnected.

5V TOLERANCE CIRCUITRY

5V tolerance is provided by running the signals through bus switches. All inputs and I/O's are 5V tolerant except for SYNCIN. The input voltage on SYNCIN must not exceed VCC3 + 0.3V. (Not available on 7M9521 and 7M9522).

PACKAGE DIMENSIONS

TOP VIEW



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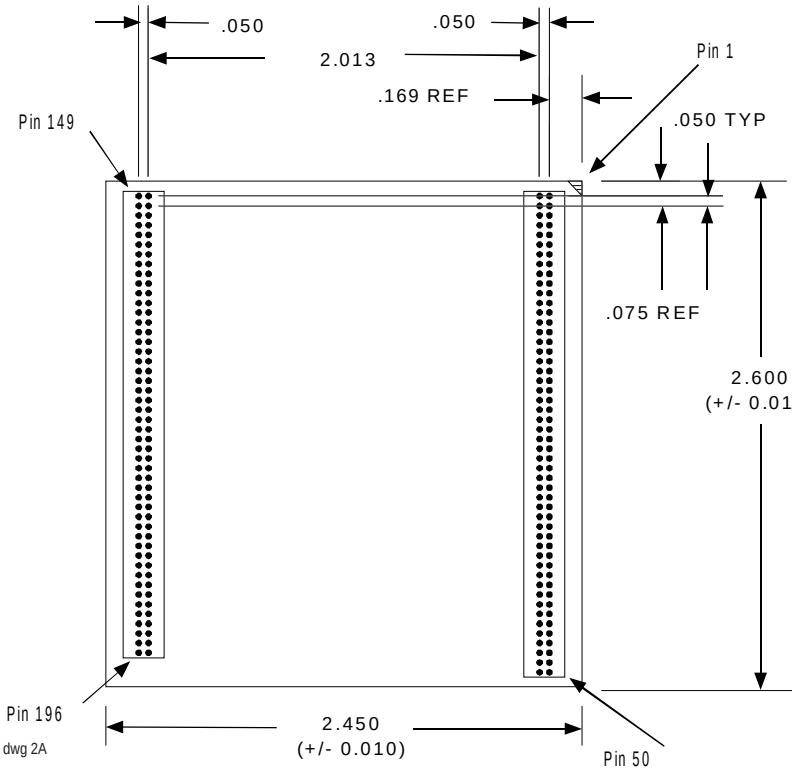
BOTTOM VIEW



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NOTES:
1. All dimensions in inches.
2. Actual component placement may differ from those shown in the diagram.

PINOUT(1)

Connector A

VCC5	1	51	VCC5
SysAD(10)	2	52	SysCMD(7)
SysAD(41)	3	53	GND
SysCMD(6)	4	54	SysAD(9)
GND	5	55	SysAD(40)
SysAD(8)	6	56	SysCMD(5)
ClkMult(0)	7	57	ScTCE*
ClkMult(1)	8	58	A_HardRst*
GND	9	59	ClkMult(2)
SysADP(4)	10	60	SysADC(0)
RSVD	11	61	SysAD(39)
SysCMD(4)	12	62	GND
GND	13	63	RSVD
SysAD(7)	14	64	SysCMD(3)
SysAD(38)	15	65	SysAD(6)
WrRdy*	16	66	VCC3
GND	17	67	SysAD(37)
SysAD(5)	18	68	SysCMD(2)
SysAD(36)	19	69	SysAD(4)
GND	20	70	GND
SysCMD(1)	21	71	SysAD(35)
SysAD(3)	22	72	SysCMD(0)
GND	23	73	SysAD(2)
SysAD(34)	24	74	VCC3
INT5*	25	75	INT4*
SysAD(33)	26	76	SysAD(1)
GND	27	77	SysAD(32)
SysAD(0)	28	78	VCC3
INT2*	29	79	INT3*
GND	30	80	SysAD(16)
SysAD(48)	31	81	INT1*
SysAD(17)	32	82	VCC3
GND	33	83	SysAD(49)
INT0*	34	84	SysAD(18)
SysAD(50)	35	85	ValidIn*
GND	36	86	GND
SysAD(19)	37	87	RSVD
SysAD(20)	38	88	SysAD(51)
GND	39	89	SysAD(52)
SysAD(21)	40	90	VCC3
RELEASE*	41	91	ValidOut*
GND	42	92	RSVD
RdRdy*	43	93	GND
SysAD(54)	44	94	SysAD(53)
GND	45	95	SysAD(22)
SysAD(23)	46	96	SysAD(55)
NMI*	47	97	VCC3
GND	48	98	SysADP(2)
SysAD(24)	49	99	SysADP(6)
VCC5	50	100	VCC5

Connector B

VCC5	101	149	VCC5
S_HardRst*	102	150	CLKFreq(0)
OutDrv	103	151	CLKFreq(1)
SoftRst*	104	152	CLKFreq(2)
GND	105	153	ScDOE*
20MHzOut	106	154	GND
GND	107	155	ScWord(0)
24MhzOut	108	156	ScWord(1)
GND	109	157	L2_Hit
SysAD(42)	110	158	SysCMD(8)
SysAD(11)	111	159	GND
SysAD(12)	112	160	SysAD(43)
VCC3	113	161	SysAD(44)
SysAD(13)	114	162	SysAD(45)
BlkWr(0)	115	163	GND
BlkWr(1)	116	164	TimerEn*
VCC3	117	165	WrType
SysAD(14)	118	166	RSVD
SysAD(15)	119	167	GND
SysADP(1)	120	168	SysAD(46)
GND	121	169	SysAD(47)
SysClk(8)	122(2)	170	SysADP(5)
Endian	123	171	GND
VCC3	124	172	WD_Strb
SyncIn	125	173	WDO*
VCC3	126	174	RstOut*
SysClk(1)	127	175	GND
VCC3	128	176	SysCLK(0)
SyncOut	129	177	GND
VCC3	130	178	SysCLK(2)
SysCLK(3)	131	179	GND
VCC3	132	180	SysCLK(4)
SysCLK(5)	133	181	GND
VCC3	134	182	SysCLK(6)
SysCLK(7)	135	183	GND
VCC3	136	184	ExtReq*
SysADP(7)	137	185	SysADC(3)
GND	138	186	SysAD(31)
SysAD(63)	139	187	SysAD(30)
SysAD(62)	140	188	GND
SysAD(29)	141	189	SysAD(61)
VCC3	142	190	SysAD(60)
SysAD(28)	143	191	SysAD(59)
SysAD(27)	144	192	GND
SysAD(26)	145	193	SysAD(58)
GND	146	194	SysAD(57)
SysAD(56)	147	195	SysAD(25)
VCC5	148	196	VCC5

NOTE:
1. The pinout of the C3 card is from a top view.
2. This pin is not connected (NC) on the 7M9516.

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PIN DEFINITIONS

Signal Name	Signal Definition	Type	Description
SysAD(63:0)	System (CPU) Address/Data Bus	I/O	64-bit multiplexed address/data bus. This bus is driven by the C3 during the address phase (SysCMD(8)=0) of a bus transaction. Valid data is driven by the C3 during the data phase (SysCMD(8)=1) for writes when ValidOut* is asserted. The C3 receives data on this bus during the data phase for reads when ValidIn* is sampled low.
SysADP(7:0)	SysAD Parity	I/O	Even parity is generated during the data phase for writes. Even parity is checked during the data phase for reads if SysCMD(4) is low. Timing and valid sample windows match SysAD(63:0). SysADP(0) is assosciated with SysAD(7:0), SysADP(1) is associated withSysAD(15:8).
SysCMD(8:0)	System (CPU) command/data	I/O	This is the 9-bit processor command bus.
SysCLK(8:0)	System (CPU) Clocks	Output	Nine identical clocks for devices residing on the C3 processor bus. All processor transitions/transactions are referenced with respect to these clocks.
SyncOut	Synchronization Clock Output	Output	The C3 system clock generator synchronization output must be connected to SyncIn through an interconnect scheme that matches that used on SysCLK(8:0).
SyncIn Clock Input	Synchronization	Input	C3 system clock generator synchronization input. This pin must be connected to SyncOut for the C3 to operate.
RdRdy*	Read Ready	Input	This pin is driven low by the system to indicate that the system is ready to accept a C3 read request.
WrRdy*	Write Ready	Input	This pin is driven low by the system to indicate that the system is ready to accept a C3 write request.
ValidOut*	Valid Output	Output	This pin is driven low by the C3 to indicate that it is driving a valid address/data on the SysAD, SysADP and SysCMD busses.
ValidIn*	Valid Input	Input	This pin in driven low by the system to indicate that it is presenting valid address/data on the SysAD, SysADP and SysCMD busses.
Endian	Endian	Config Input	Endian configuration input. 0=big, 1=little
OutDrv	Output Drive	Config Input	Output drive strength configuration input. 0=100%, 1=83%
TimerEn*	Timer Enable	Config Input	CPU internal timer interrupt enable configuration input. 0=enable timer, 1=disable timer
WrType	Write Type	Config Input	Write Type configuration input. 0=R4X00 compatible, 1=Pipelined
ClockMult(2:0)	Clock Multiplier	Config Input	000=x2 001=x3 010=x4 011=x5 100-101=reserved 110=SmartClock mode 0 (max CPU core frequency) 111=SmartClock mode 1(max CPU bus frequency)
BlkWr(1:0)	Block Write	Config Input	Block Write data rate 00=DDDD 01=DxDxDxD 10=DxxDxxDxxD 11=DxxxDxxxDxxxD
RELEASE*	Release Interface	Output	This pin is driven low to signal to the requesting device that the system interface is available.
ExtReq*	External Request	Intput	This pin is driven low to request the use of the system interface.

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PIN DEFINITIONS (CONTINUED)

Signal Name	Signal Definition	Type	Description
ClkFreq(2:0)	SysCLK Frequency	Config Input	In normal mode these inputs specify the system bus clock frequency. In SmartClock mode, these inputs specify the maximum system clock frequency. 000=45MHz (includes 43.75/44) 100=75MHz 001=50MHz 101=83MHz 010=60MHz (includes 58.33) 110=90MHz 011=66MHz 111=100MHz
INT*(5:0)	Interrupts	Input	General processor interrupts.
NMI*	Non-Maskable Interrupt	Input	Non-maskable interrupt
SoftRST*	Soft Reset	Input	Asserting this input causes a processor soft (or warm) reset.
S_HardRST* Hard Reset	Synchronous	Input	Asserting this input causes a processor hard (or cold) reset.
A_HardRST* Hard Reset	Asynchronous	Input	Asserting this input causes a processor hard (or cold) reset.
RSTOut*	Reset Output	Output	This pin is asserted by the C3 to reset system logic. This output is asserted during power-on reset, and whenever HardRST* is asserted.
WDO*	Watch Dog Output	Output	This pin asserted by the C3 whenever there is a timeout of the watchdog timer.
WD_Strb	Watch Dog	Input	This pin must be strobed periodically by the system to prevent the Strobe watchdog timer from timing out.
L2_HIT (ScMatch)	L2 Cache Hit	Output	This pin indicates to the system that a hit has occurred in the on board L2 cache. This pin is a no connect on the 7M9516/18/19/20/23.
ScDOE*	Secondary Cache Data OE*	Input	Only used when a secondary cache is implemented with the R5K internal cache controller. This pin is a no connect on the 7M9516/18/19/20/23.
ScWord(1:0)	Secondary Cache Word	I/O	Only used when a secondary cache is implemented with the R5K internal cache controller
ScTCE*	Secondary Cache Tag Chip Enable	Output	This pin indicates to the system when the L2 cache controller of the R5K is accessing the Tag RAM. This pin is driven high by the 7M9516/18/19/20/23.
20MHz Out	20MHz Clock	Output	20MHz Clock
24MHz Out	24MHz Clock	Output	24MHz Clock
GND	Ground	Supply	System Ground
VCC3	+3.3V	Supply	System 3.3V Supply
VCC5	+5V	Supply	System 5V Supply

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ENVIRONMENTAL

	Temp. (°C)		Humidity (1)	Condition
	Min	Max	Min	Max
Operating	0	55	20%	80%
Non-Op.	-10	60	10%	90%
Storage	-25	60	10%	90%

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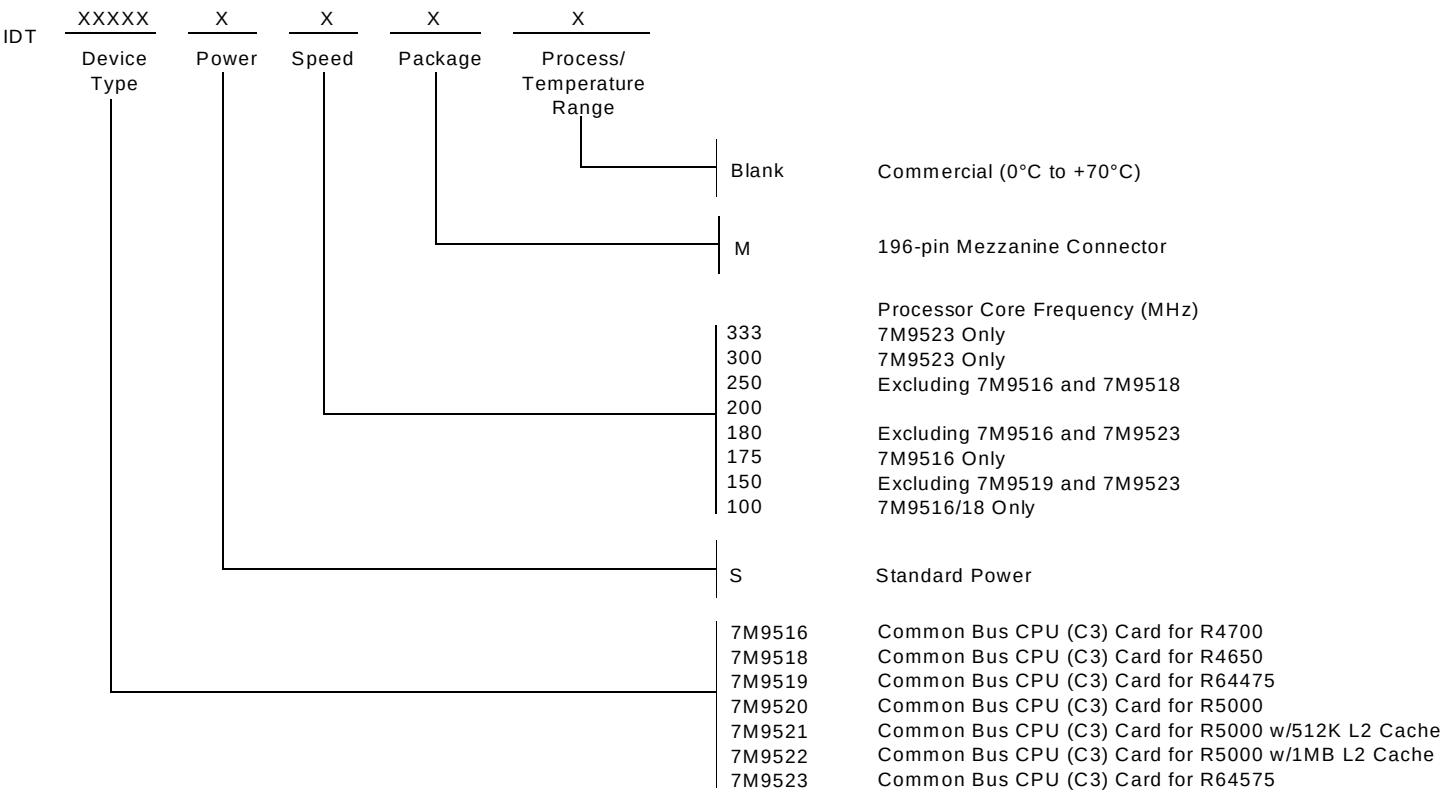
NOTE:
1. Non-Condensing

ORDERING INFORMATION



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CORPORATE HEADQUATERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015
fax: 408-492-8674
www.idt.com

for Tech Support:
408-988-5647
ssdhelp@idt.com