Elan Microelectronics Crop.

EM65168/EM65168A

80 COM/SEG LCD DRIVER

DEC 18, 2003

Version 0.8

EM65168/EM65168A Specification Revision History		
Version	**Content**	**Date**
0.1	Initial version	December 23, 2002
0.2	1. Add Pin configurations 2. COB bonding diagram	March 28,2003
0.3	Add BF,DON,HPM,RES control registers	March 31,2003
0.4	1. Modify the DC characteristic 2. The RF register on page 19 3. Modify some descriptions on page 20	April 29, 2003
0.5	1. Modify EM65168 to EM65168/EM65168A. 2. Add the description of compatibility of EM65168A and EM83040A on page 4. 3. Add the attention about EM65168A control registers on page 19. 4. Add the resistor value level limitation of Ra and Rb when using external resistor on page 17 and 19. 5. Add FIG. 10_1 and description of adding a capacitor across V1 and Vreg, and its recommended value on page16 & 17.	May 28,2003
0.6	1. Modify LCD waveform(Fig.9) on page15. 2. Add the description of all COM/SEG voltage state when EN=1 on page 9. 3. Add note about RAMW and RAMR control on page 9.	SEP 17,2003
0.7	1. Modify IOH1 and IOL1 DC values on page 23	Nov 5,2003
0.8	1. Modify VEV value and REG[5:0] setting value of DC spec. on page 23 2. Modify VEV values of REG[5:0] vs VEV table on page 16.	Dec 18,2003

Contents

1. General description

The EM65168/EM65168A is a dot matrix LCD driver, which is fabricated by low power CMOS technology. This chip includes 80-bits shift register, 80 bits data latch and 80 bits level driver. A LCD RAM inside can be mapping to LCD signal. It converts RAM data to parallel data and output waveform to LCD.

2. Features

(1) Supply power: 2.5~5.5V

(2) LCD drive voltage: 3.6 to 15V

(3) Internal RAM: 6,400 bits

(4) RAM can be controlled by eight signals including 4/8 bits bus.

(5) Duty: 1/32, 1/48, 1/64, 1/80

(6) Build in DC/DC converter: double, triple, quad and five times.

(7) Modularized function: connect to another EM65168/EM65168A to extent LCD matrix

(8) One DC converter enabled and other EM65168/EM65168A can share with this.

(9) Internal regulator output for DC/DC converter controlled by control register.

(10) Bias Selectable: 1/5, 1/6, 1/7, 1/8, 1/9

(11) Internal RC clock about 24 KHz.

(12) CMOS process (P-type silicon substrate)

(13) EM65168A is compatible with EM83040A.

(14) Package (Ordering information):

Part Number	Versions	Description	Package information
EM65168H	Bare chip	NA	Page 30
EM65168AH	Bare chip	NA	Page 30

Note: The EM65168 series has the following sub-codes depending on their shapes.

H: Bare chip (Aluminum pad without bumped); **GH**: Gold bumped chip;

F: COF package; **T**: TAB (TCP) package

Example EM65168H → EM65168: Elan number ; H: Bare chip

3. Application

- Data Bank
- LCD toy
- Education computer

4. Pin configurations

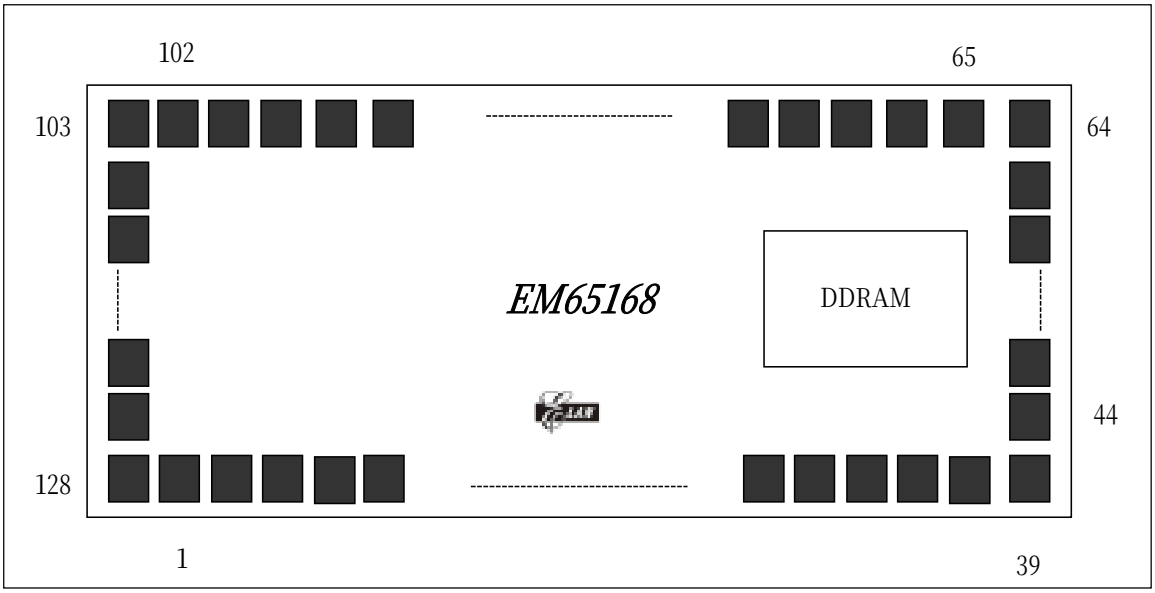


Figure 1. Pin configuration

Note: With the Elan logo in the center (as shown figure) and DDRAM (black color) on the right side the pin 1 is in the down left corner.

PIN DIMENSIONS

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	4260	2150	μm
Pad size (min.)		85	90	
Pad pitch (min.)	100			
Coordinate Origin	Chip center			

PAD Coordinates Table

(Total 114 pins)

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
1	GND	-1880.0 ,-948.8	51	O33	2003.8 ,-100.0
2	CA	-1770.0 ,-948.8	52	O34	2003.8 ,0.0
3	VSS2+	-1660.0 ,-948.8	53	O35	2003.8 ,100.0
4	VSS2-	-1555.0 ,-948.8	54	O36	2003.8 ,200.0
5	V2	-1450.0 ,-948.8	55	O37	2003.8 ,300.0
6	V3	-1350.0 ,-948.8	56	O38	2003.8 ,400.0
7	VREG	-1250.0 ,-948.8	57	O39	2003.8 ,500.0
8	V1	-1150.0 ,-948.8	58	O40	2003.8 ,605.0
9	V4	-1050.0 ,-948.8	59	O41	2003.8 ,715.0
10	V5	-950.0 ,-948.8	60	O42	2003.8 ,825.0
11	O1	-850.0 ,-948.8	61		
12	VOUT	-750.0 ,-948.8	62		
13	O2	-650.0 ,-948.8	63		
14	VSS4	-550.0 ,-948.8	64	O47	2003.8 ,948.8
15	O3	-450.0 ,-948.8	65	O48	1880.0 ,948.8
16	VSS3	-350.0 ,-948.8	66	O49	1770.0 ,948.8
17	O4	-250.0 ,-948.8	67	O50	1660.0 ,948.8
18	CB	-150.0 ,-948.8	68	O51	1555.0 ,948.8
19	O5	-50.0 ,-948.8	69	O52	1450.0 ,948.8
20	O6	50.0 ,-948.8	70	O53	1350.0 ,948.8
21	O25	150.0 ,-948.8	71	O54	1250.0 ,948.8
22	O7	250.0 ,-948.8	72	O55	1150.0 ,948.8
23	O24	350.0 ,-948.8	73	O56	1050.0 ,948.8
24	O8	450.0 ,-948.8	74	O57	950.0 ,948.8
25	O23	550.0 ,-948.8	75	O58	850.0 ,948.8
26	O9	650.0 ,-948.8	76	O46	750.0 ,948.8
27	O22	750.0 ,-948.8	77	O59	650.0 ,948.8
28	O10	850.0 ,-948.8	78	O45	550.0 ,948.8
29	O11	950.0 ,-948.8	79	O60	450.0 ,948.8
30	O12	1050.0 ,-948.8	80	O44	350.0 ,948.8
31	O13	1150.0 ,-948.8	81	O61	250.0 ,948.8
32	O14	1250.0 ,-948.8	82	O43	150.0 ,948.8
33	O15	1350.0 ,-948.8	83	O62	50.0 ,948.8
34	O16	1450.0 ,-948.8	84	O63	-50.0 ,948.8
35	O17	1555.0 ,-948.8	85	O80	-150.0 ,948.8
36	O18	1660.0 ,-948.8	86	O64	-250.0 ,948.8
37	O19	1770.0 ,-948.8	87	O79	-350.0 ,948.8
38	O20	1880.0 ,-948.8	88	O65	-450.0 ,948.8
39	O21	2003.8 ,-948.8	89	O78	-550.0 ,948.8
40			90	O66	-650.0 ,948.8
41			91	O77	-750.0 ,948.8
42			92	O67	-850.0 ,948.8
43			93	O68	-950.0 ,948.8
44	O26	2003.8 ,-825.0	94	O69	-1050.0 ,948.8
45	O27	2003.8 ,-715.0	95	O70	-1150.0 ,948.8
46	O28	2003.8 ,-605.0	96	O71	-1250.0 ,948.8
47	O29	2003.8 ,-500.0	97	O72	-1350.0 ,948.8
48	O30	2003.8 ,-400.0	98	O73	-1450.0 ,948.8
49	O31	2003.8 ,-300.0	99	O74	-1555.0 ,948.8
50	O32	2003.8 ,-200.0	100	O75	-1660.0 ,948.8

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
101	O76	-1770.0 ,948.8			
102	MAIN	-1880.0 ,948.8			
103	MD	-2003.8 ,948.8			
104					
105					
106					
107	M1	-2003.8 ,825.0			
108	M0	-2003.8 ,715.0			
109	EN	-2003.8 ,605.0			
110	RAMENB	-2003.8 ,500.0			
111	RAMADS	-2003.8 ,400.0			
112	RAMW	-2003.8 ,300.0			
113	RAMR	-2003.8 ,200.0			
114	RAMD7	-2003.8 ,100.0			
115	RAMD6	-2003.8 ,0.0			
116	RAMD5	-2003.8 ,-100.0			
117	RAMD4	-2003.8 ,-200.0			
118	RAMD3	-2003.8 ,-300.0			
119	RAMD2	-2003.8 ,-400.0			
120	RAMD1	-2003.8 ,-500.0			
121	RAMD0	-2003.8 ,-607.5			
122	VDD	-2003.8 ,-715.0			
123	LOAD	-2003.8 ,-825.0			
124					
125					
126					
127					
128	FR	-2003.8 ,-948.8			

Note : For PCB layout, IC substrate must be connected to GND.

5. Block diagram

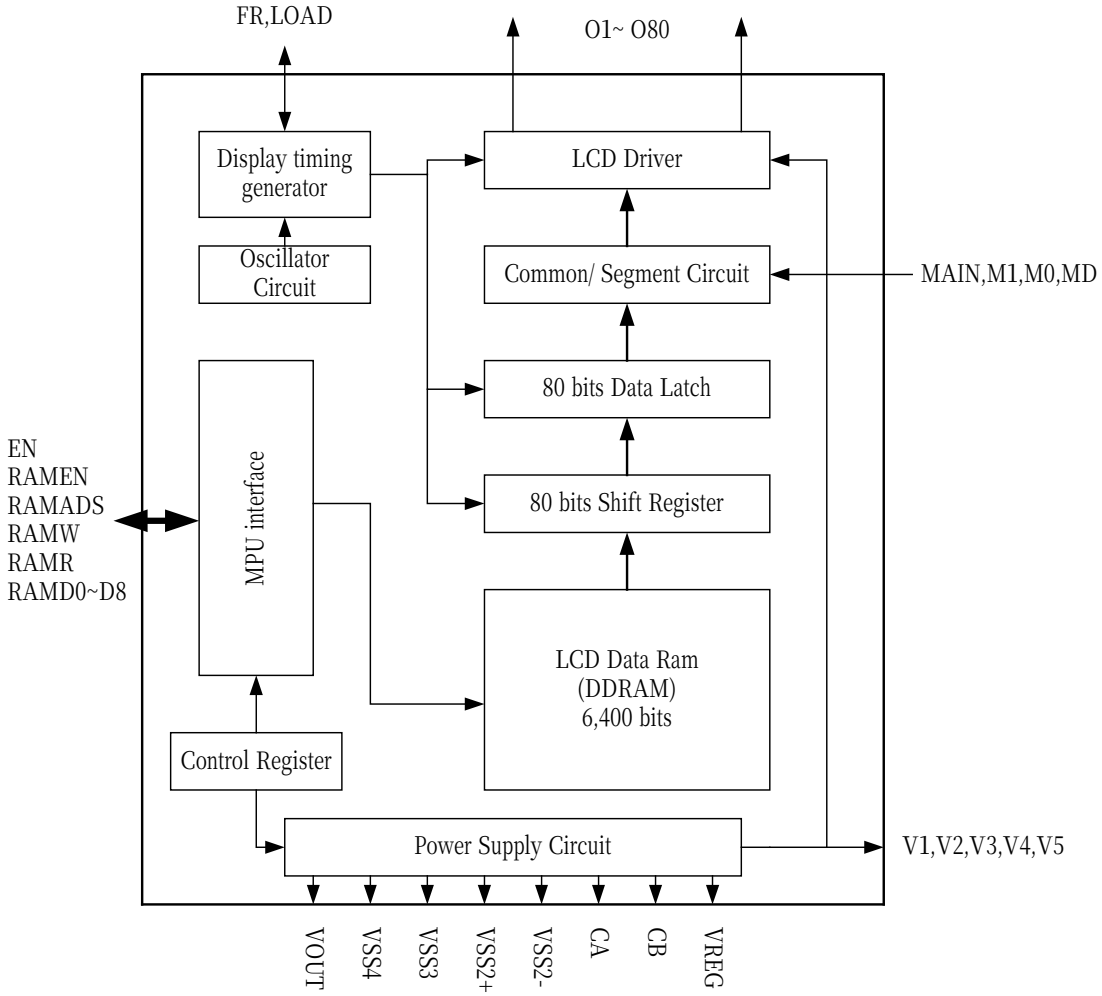


FIG. 2 Block Diagram

6. Pin description

Pin name	*I/O*	*Function*	*PIN No.*
VDD	Power	System power supply	1
GND	Power	Ground	1
VOUT	Power	Voltage converter input/output pin Connect this pin to GND through capacitor EN=1,VOUT=VDD-Vt	1
VSS4	Power	Step-up capacitor	1
VSS3	Power	Step-up capacitor	1
VSS2+	Power	Step-up capacitor	1
VSS2-	Power	Step-up capacitor	1
VREG	Power	Output voltage regulator terminal. Provides the voltage between V1 and GND through a resistive voltage divider.	1
MAIN	I	Master or slave control signal. MAIN=1, master unit MAIN=0, slave unit	1
EN	I	This pin control whole chip power. This chip will work when this pin is connected to ground. And whole chip will disable when connect to VDD voltage. **EN=0 and MAIN=1 the chip will generate VSS2+, VSS2-VSS3, VSS4, VOUT, LOAD, FR signal and internal RC clock.** EN=1, standby mode **(all COM/SEG output to GND level)**	1
MD	I	MD=0: 4-bit bus mode, the RAMD3~RAMD0 is valid, RAMD7~DAMD4 must be connected to VDD or GND level MD=1: 8-bit bus mode, the RAMD7~RAMD0 is valid	1
M1	I	Mode select	1
M0	I	Mode select	1
RAMEN	I	RAM read and write control signal. 1 => can not read and write. 0=> can read and write.	1
RAMADS	I	RAM bus (RAMD[7:0]) select signal 1=> RAM Data bus, 0=>RAM Address bus	1
RAMW	I	RAM write signal, low active	1
RAMR	I	RAM read signal, low active RAMW 1 1 0 0 RAMR 1 0 1 0 RAMD[7:0] Tri-state Output Input Tri-state	1
RAMD[7:0]	I/O	RAM data or address bus For 4-bits bus mode, RAMD[3:0] is valid and RAMD[7:4] is not used, it must be connected to VDD or VSS level. For 8-bits bus mode, RAMD[7:0] is valid	8
LOAD	I/O	LCD load signal between one common signal to another. MAIN=1: The master unit will output LOAD signal. MAIN=0: The slave will accept the signal from master unit.	1
FR	I/O	This is the liquid crystal alternating current signal I/O terminal. MAIN=1: The master unit will output FR signal. MAIN=0: The slave will accept the signal from master unit.	1
CA	I	Step-up capacitor	1
CB	I	Step-up capacitor	1
V1~V5	I	Reference voltage input, V1≧V2≧V3≧V4≧V5	5
O1~O80	O	LCD waveform output	80

7. Function description

(1) User can use MAIN pin to choose master unit or slave unit.

MAIN	*Unit*	*Function*
1	MASTER	Generate these signals: FR, LOAD, V1, V2, V3, V4, V5 Internal RC clock
0	SLAVE	Accept these Master unit signals: FR, LOAD, V1, V2, V3, V4, V5 No internal RC clock

(2) User can use M1, M2 to choose four modes. As followed

MASTER	*MAIN*	*M1*	*M0*	*Segment*	*Common*	*BIAS*
Mode1	1	0	0	O(16:1)=S(16:1)	O(80:17)=C(64:1)	1/9
Mode2	1	0	1		O(80:1)=C(80:1)	1/9
Mode3	1	1	0	O(32:1)=S(32:1)	O(80:33)=C(48:1)	1/7
Mode4	1	1	1	O(48:1)=S(48:1)	O(80:49)=C(32:1)	1/5
SLAVE	*MAIN*	*M1*	*M0*	*Segment*	*Common*	*BIAS*
Mode1	0	0	0	O(80:1)=S(80:1)		1/9
Mode2	0	0	1	O(80:1)=S(80:1)		1/9
Mode3	0	1	0	O(80:1)=S(80:1)		1/7
Mode4	0	1	1	O(80:1)=S(80:1)		1/5

* S=Segment, C=Common, * (M1, M0) for Master must same as Slave unit

(3) The relationship of F_{OSC}、LOAD and FR frequency

MAIN	*M1*	*M0*	*Description*	f_{osc}	*LOAD*	*FR*
1	0	0	64 common (1/64 duty)	24KHz	f_{OSC}/5=4.8K	LOAD/64=75.0 Hz
1	0	1	80 common (1/80 duty)	24KHz	f_{OSC}/4=6.0K	LOAD/80=75.0 Hz
1	1	0	48 common (1/48 duty)	24KHz	f_{OSC}/7=3.4K	LOAD/48=71.4 Hz
1	1	1	32 common (1/32 duty)	24KHz	f_{OSC}/10=2.4K	LOAD/32=75.0 Hz

(4) RAM control

LCD RAM can be read or written via control signal. When #RAMEN pin is at low state, the RAM can be read or written in data. The RAMADS can be set as RAMD[7:4] to be used as address bus or data bus. When it used as Address and in 4-bit mode, the #RAMEN pin should remain low and users need to set three times Address as RAMD[3:0] by following the Address setting sequence: Address[11:8] (A11, A10, A9, A8), Address[7:4] (A7, A6, A5, A4), and Address[3:0] (A3, A2, A1. A0). If the Address bus is in 8-bit mode, users need to set two times Address as RAMD[7:0] by following the Address setting sequence: Address[10:8] (x,x,x,x,A10, A9, A8), Address[7:0] (A7, A6, A5, A4, A3, A2, A1. A0).

When it used as Data bus, the #RAMEN pin will be at high state, users can read or write single data or continuously read or write multiple data. When read or write data from RAM, the

Address will plus 1, and once #RAMEN pin become at high state, users cannot read or write to RAM.

LCD RAM Write mode

4-bit bus mode

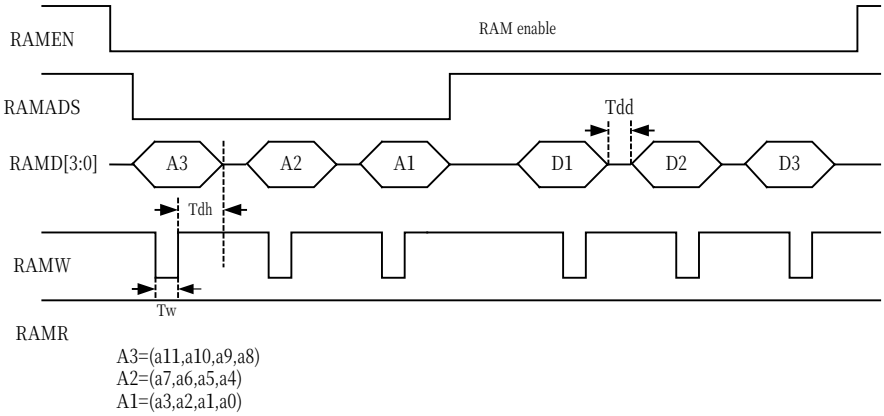


FIG. 3 LCD RAM write mode for 4-bit bus

8-bit bus mode

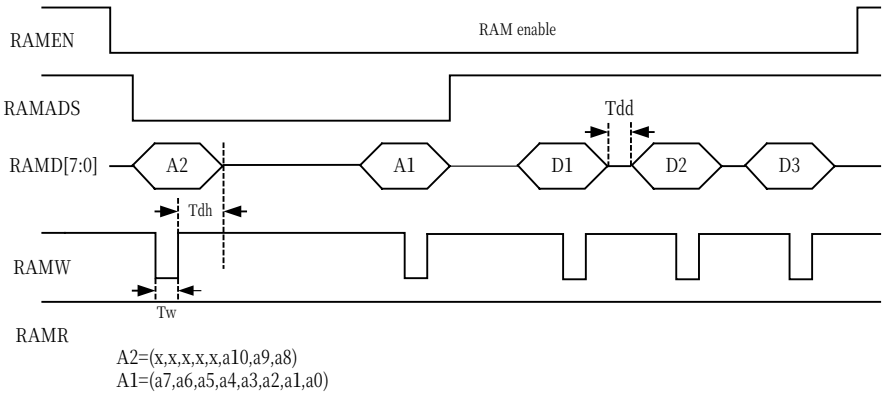


FIG. 4 LCD RAM write mode for 8-bit bus

LCD RAM Read mode

4-bit bus mode

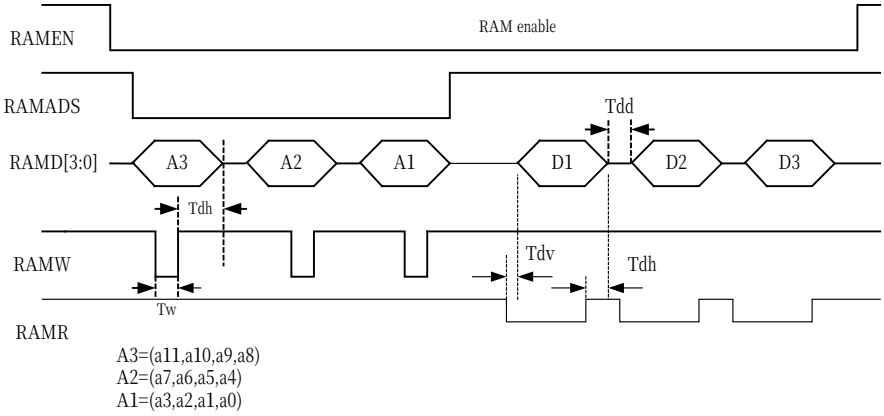


FIG. 5 LCD RAM read mode for 4-bit bus

8-bit bus mode

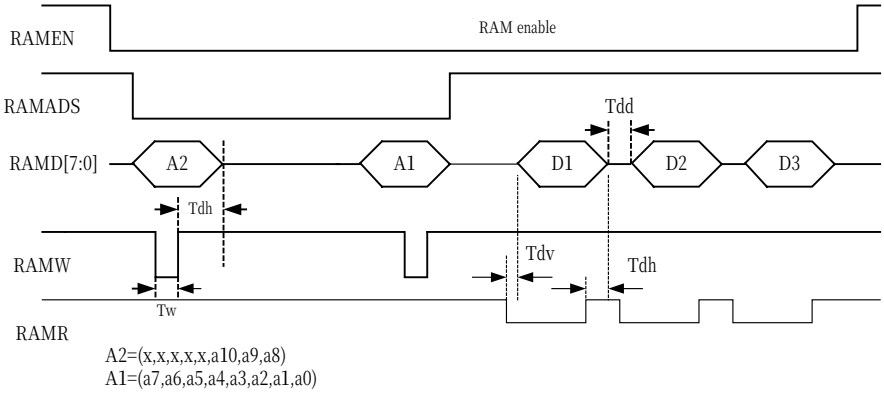


FIG. 6 LCD RAM read mode for 8-bit bus

(5) RAM mapping

4-bit bus mode: RAM address is from 000H to address A05H, control register is from A00H to A05H

8-bit bus mode: RAM address is from 000H to address 503H, control register is from 500H to 502H

User fill “1” to LCD RAM, LCD driver will generate “light” waveform. Otherwise, it will generate a “dark” waveform. The LCD RAM area is mapped to segment 1 to segment 80. And user can refer to FIG. 7,8 and Table 1 to get the idea of LCD ram mapping. The other RAM(Area11) is prohibited.

Table 1: LCD mapping RAM area

Master/slave	*Master Common No.*	*Segment N0.*	*LCD Display area*
Master	32	48	1,2,3
Master	48	32	1,2,5,6
Master	64	16	1,5,8
Master	80	0	No mapping RAM
Slave	32	80	1,2,3,4
Slave	48	80	1,2,3,4,5,6,7
Slave	64	80	1,2,3,4,5,6,7,8,9
Slave	80	80	1,2,3,4,5,6,7,8,9,10
Any	Any	Any	Area 11 is prohibited

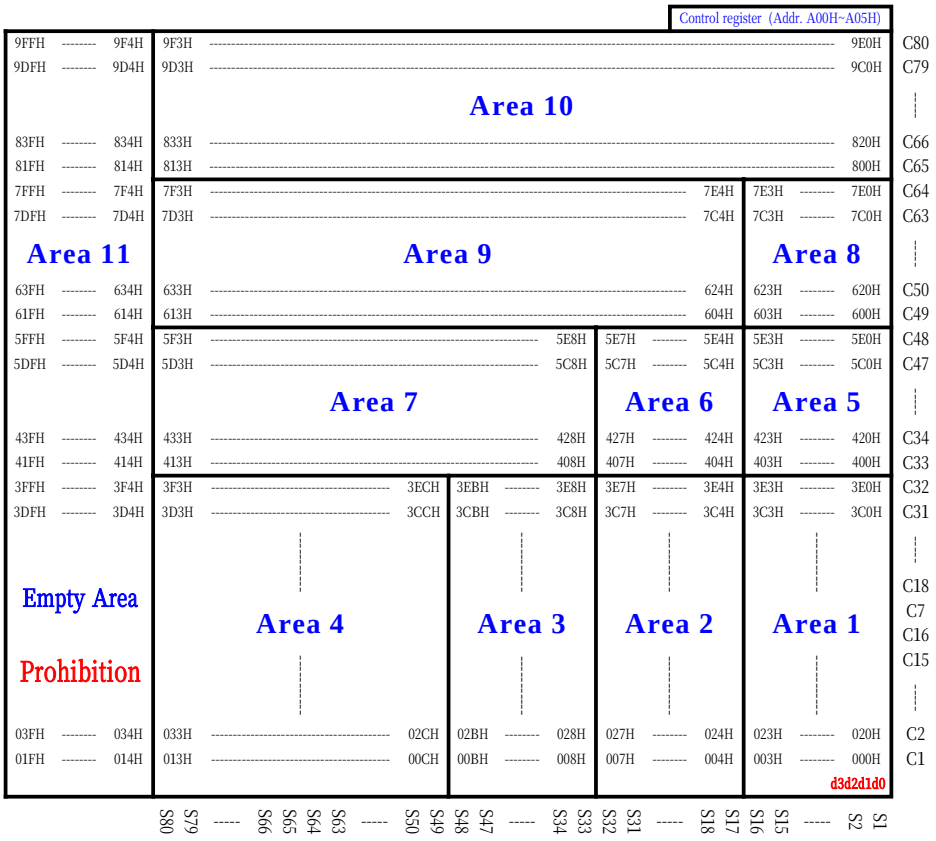


FIG. 7 RAM mapping of LCD display for 4 bits bus mode

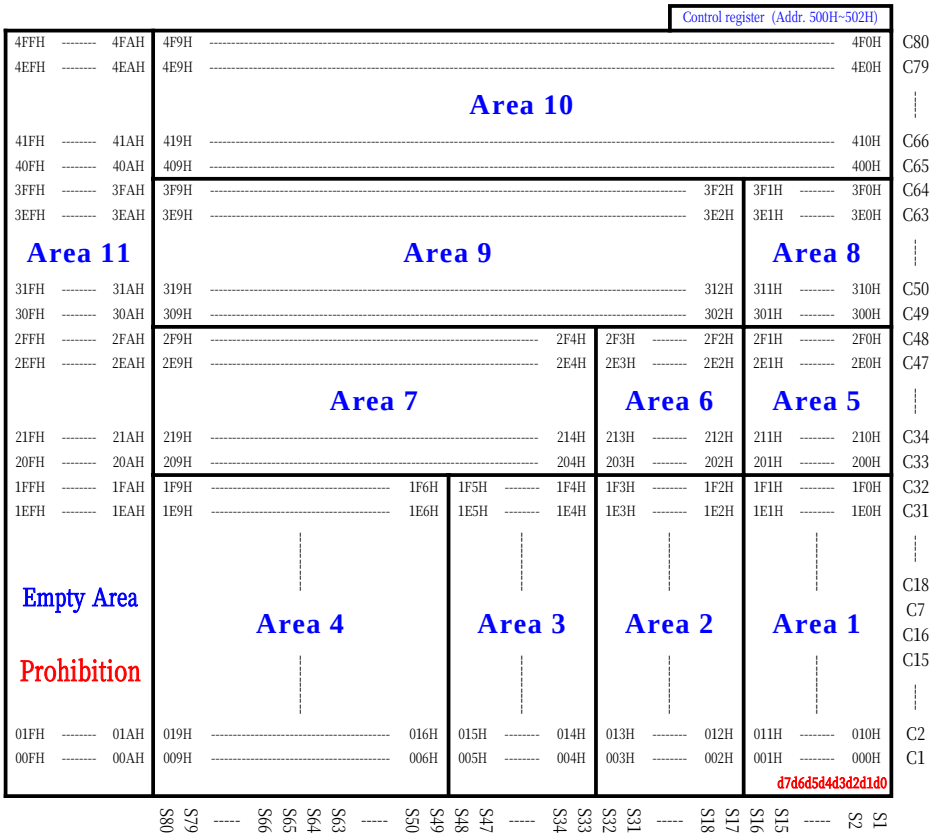


FIG. 8 RAM mapping of LCD display for 8bits bus mode

(6) LCD waveform

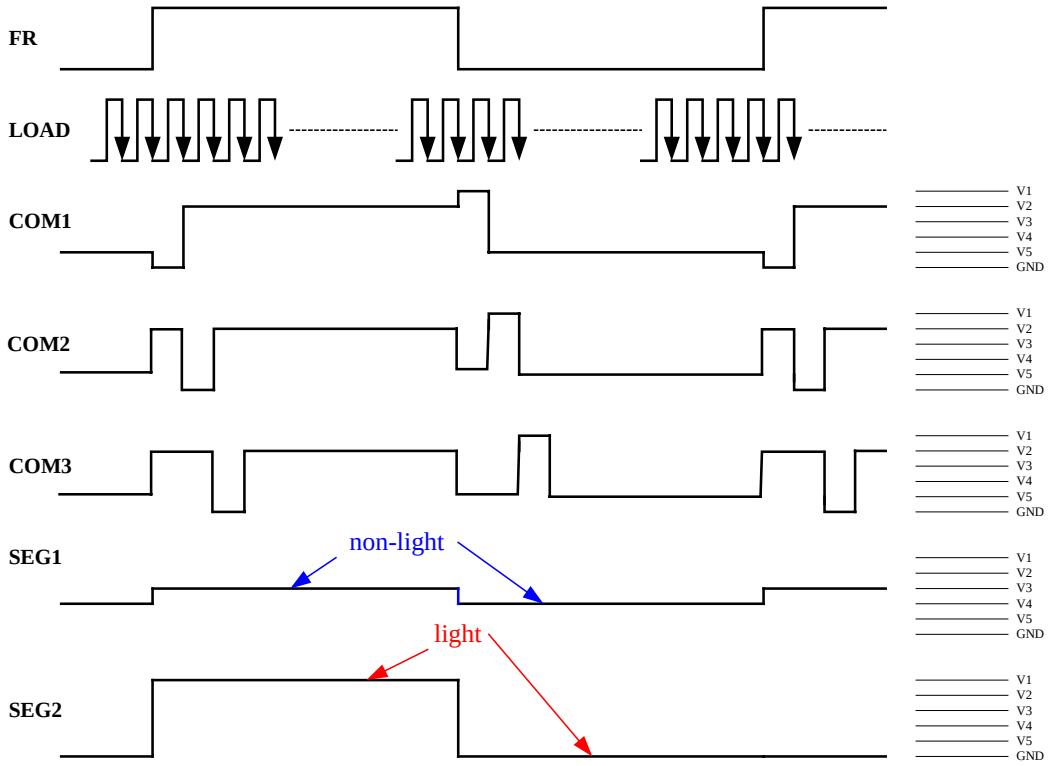


FIG. 9 LCD Waveform

(7) Control register

4-bit mode data bus

Address	Bit3	Bit2	Bit1	Bit0	Initial state
A00H	REG3	REG2	REG1	REG0	0000 (0H)
A01H	PMS1	PMS0	REG5	REG4	0000 (0H)
A02H	IRS	IR2	IR1	IR0	0010 (2H)
A03H	BSE	BS2	BS1	BS0	0000 (0H)
A04H	X	DON	HPM	RES	0000 (0H)
A05H	BF	RF2	RF1	RF0	0000 (0H)

8-bit mode data bus

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Initial state
500H	PMS1	PMS0	REG5	REG4	REG3	REG2	REG1	REG0	00000000 (00H)
501H	BSE	BS2	BS1	BS0	IRS	IR2	IR1	IR0	00000010 (02H)
502H	BF	RF2	RF1	RF0	X	DON	HPM	RES	00000000 (00H)

The power supply circuit mode select (PMS1, PMS0)

Use settings	*PMS1*	*PMS0*	*Step-up circuit*	*V regulator circuit*	*V/F circuit*	*External voltage input*
Only the internal power supply is used	1	1	O	O	O	X
Only the V regulator circuit and the V/F circuit are used	1	0	X	O	O	VOUT
Only the V/F circuit is used	0	1	X	X	O	V1
Only the external power supply is used	0	0	X	X	X	V1 to V5

The Voltage Regulator Circuit, (REG5~REG0) is selected the voltage of V_{EV}

REG5	*REG4*	*REG3*	*REG2*	*REG1*	*REG0*	*V_{EV}*	*V_{EV} step*
0	0	0	0	0	0	1.2 V	0.0127V
0	0	0	0	0	1	1.212 V	
			↓			↓	
0	1	1	1	1	1	1.593 V	
1	0	0	0	0	0	1.606 V	
			↓			↓	
1	1	1	1	1	0	1.987 V	
1	1	1	1	1	1	2.0 V	

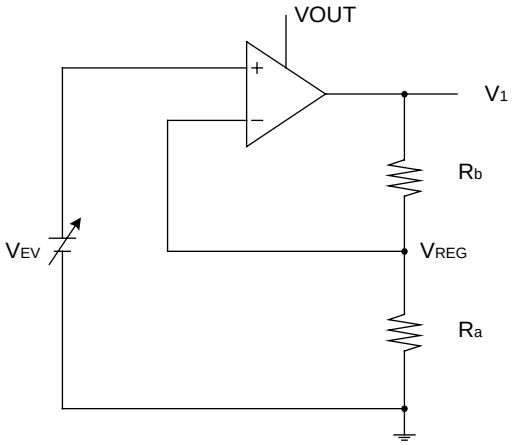


FIG. 10

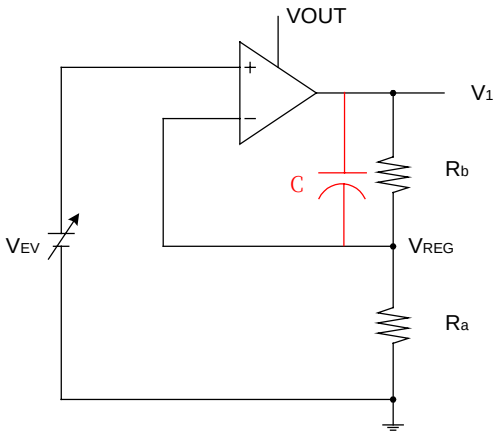


FIG. 10_1

The internal resistor select (IRS) and (IR2, IR1, IR0) is selected for the V1 voltage regulator internal resistance ratio.

IRS=0: internal regulator resistor is used.

IRS=1: internal regulator resistor is not used. (External resistor is used)

IR2	*IR1*	*IR0*	*Resistor ratio (1+Rb/Ra)*
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

The V1 voltage can be calculated using equation A over the range where **VDD<V1≦VOUT**

$V1=(1+Rb/Ra)\bullet V_{EV}*(97\sim103\%)$ (Equation A)

Example: Default: IRS=0 (internal regulator resistor is used), (IR2, IR1, IR0)=(0, 1, 0), and (REG5~0)=(000000)

$V1=(1+Rb/Ra)\bullet V_{EV}*(0.97\sim1.03)=4.0\bullet1.2*(0.97\sim1.03)=4.656\sim4.944$ V

When IRS=0 (internal regulator resistor is used), (IR2, IR1, IR0)=(0, 1, 1), and (REG5~0)=(100000)

$V1=(1+Rb/Ra)\bullet V_{EV}*(0.97\sim1.03)=4.5\bullet1.606*(0.97\sim1.03)=7.01\sim7.44$ V

The output voltage of V1 is determined by function of the V1 voltage regulator ratio register (1+Rb/Ra), and the electric volume resister (REG5~REG0).

Note: When external resistor is used(FIG. 10_1),

1. **Ra and Rb values must to be MΩ level, for example, if the desired value of (1+Rb/Ra) is 3.0, we give Ra=1 MΩ and Rb=2 MΩ.**
2. **Add a capacitor across V1 and Vreg, and the recommended value of C is 10nF~100nF.**

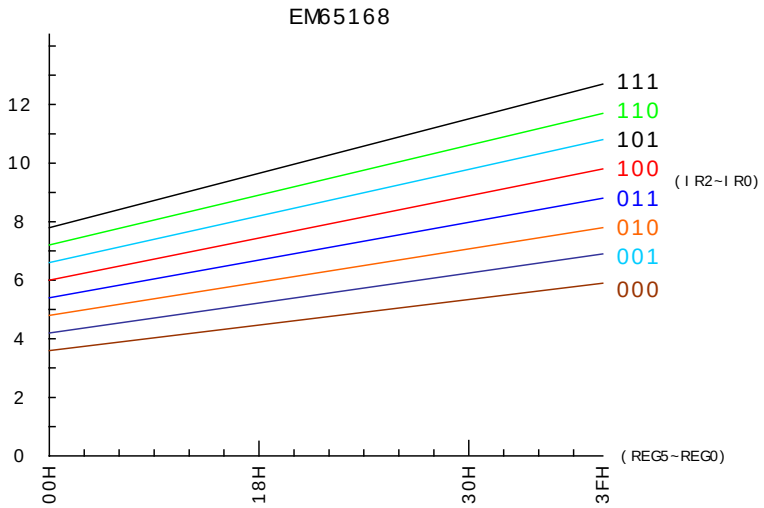


FIG. 11 The output voltage curve of V1

LCD Bias set

BSE=0: The LCD bias is not selectable

M1	*M0*	*BIAS*
0	0	1/9
0	1	1/9
1	0	1/7
1	1	1/5

BSE=1: The LCD bias is selectable by setting BS2, BS1, BS0

BS2	*BS1*	*BS0*	*BIAS*
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	Prohibit (1/9)
1	1	0	Prohibit (1/9)
1	1	1	Prohibit (1/9)

RES

The internal circuit can be initialized. This register is effective only at Master operation mode. (This register is a read-only bit.)

RES = “0”: Normal operation

RES = “1”: Initialization ON

When the reset operation begins internally after RES register sets to “1”, the RES register is automatically cleared to “0”.

[Caution: It needs to wait for more than 20 ms after setting RES bit]

HPM

The HPM register is the power control for the power supply circuit for liquid crystal drive.

HPM = “0”: Normal mode

HPM = “1”: High power mode

DON

The DON register controls the LCD display turning on or off.

DON= “0”: Display OFF (All COM/SEG output GND level)

DON= “1”: Display ON

The RF registers (RF2, RF1, RF0) can control resistance ratio of CR oscillator. Therefore frame frequency can change RF registers setting.

RF2	RF1	RF0	Operation
0	0	0	Initial resistance ratio
0	0	1	1.2 times initial resistance ratio
0	1	0	0.9 times initial resistance ratio
0	1	1	Initial resistance ratio
1	0	0	0.8 times initial resistance ratio
1	0	1	Initial resistance ratio
1	1	0	1.1 times initial resistance ratio
1	1	1	Initial resistance ratio

BF

The BF register controls the operating frequency of the booster.

BF	Operating clock frequency in the booster
0	1.5K Hz * 4
1	1.5 K Hz

Note: IF Step-up capacitor (C2 showed as Fig. 12) is less 1 uF, BF control register must be set "0".

Attention: EM65168A have fixed some control bits of Control Register, so original user using EM83040A can use external resistor and set V_{EV}=1.56V, to get $V_1 = (1+\frac{Rb'}{Ra'}) \cdot V_{EV} = 1.56 \cdot (1+\frac{Rb'}{Ra'})$ by adding external resistors, Ra', Rb', but Ra' and Rb' values must to be MΩ level; the fixed control bits are shown below:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Fixed bits
500H	PMS1	PMS0	REG5	REG4	REG3	REG2	REG1	REG0	11011110
501H	BSE	BS2	BS1	BS0	IRS	IR2	IR1	IR0	0xxx1xxx
502H	BF	RF2	RF1	RF0	X	DON	HPM	RES	0000x100

Note:

1. The control register(500H) is fixed to **11011110**
2. The **BSE** bit is fixed to **0**, and the **IRS** bit is fixed to **1**
3. The control register(502H) is fixed to **0000x100**

(8) The step-up voltage circuit

Placing capacitor C2 in different configurations in Fig 12 and across VOUT and VSS boosts the voltage coming from VDD and VSS n-times and outputs the boosted voltage to VOUT pin.

(a) Double step-up, (b) Triple step-up, (c) Quad step-up (d) five times step-up

C1=0.47 to 3.3μf, C2=0.1 to 2.2uf

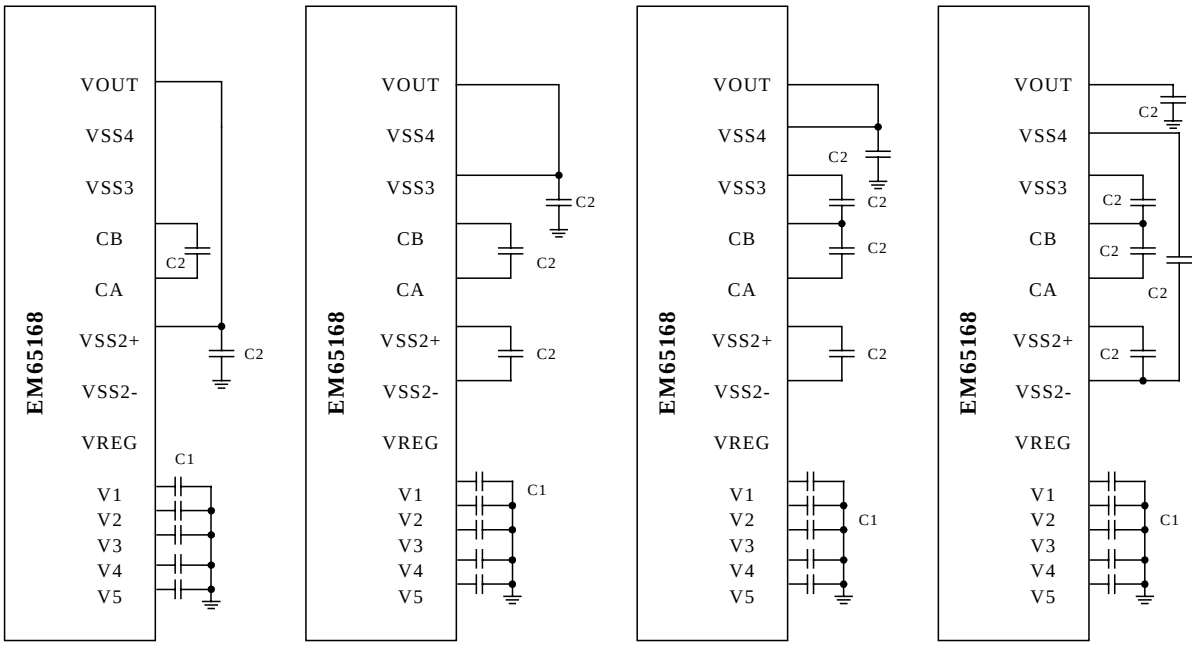


FIG. 12

(9)Reference circuit examples are as following FIG. 13

(a)Only the internal power supply is used, control register (PS1, PS0, IRS)=(1,1,0)

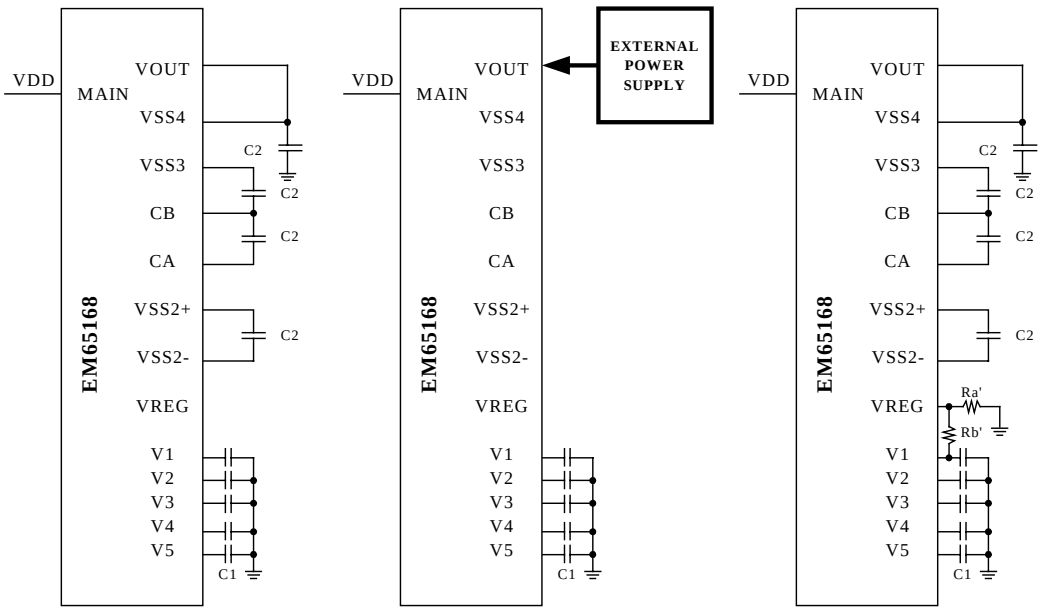
(b)Only the V regulator circuit and the V/F circuit are used, control register (PS1, PS0, IRS)=(1,0,0)

(c)Only the internal power supply is used, control register (PS1, PS0, IRS)=(1,1,1) When internal regulator resistor is not used (external resistor is used), V1=VREG*(1+Rb'/Ra')

(d)Only the V regulator circuit and the V/F circuit are used, control register (PS1, PS0, IRS)=(1,0,1), When internal regulator resistor is not used (external resistor is used), V1=VREG*(1+Rb'/Ra')

(e)Only the V/F circuit is used, control register (PS1, PS0)=(0,1)

(f)Only the external power supply is used, control register (PS1, PS0)=(0,0)



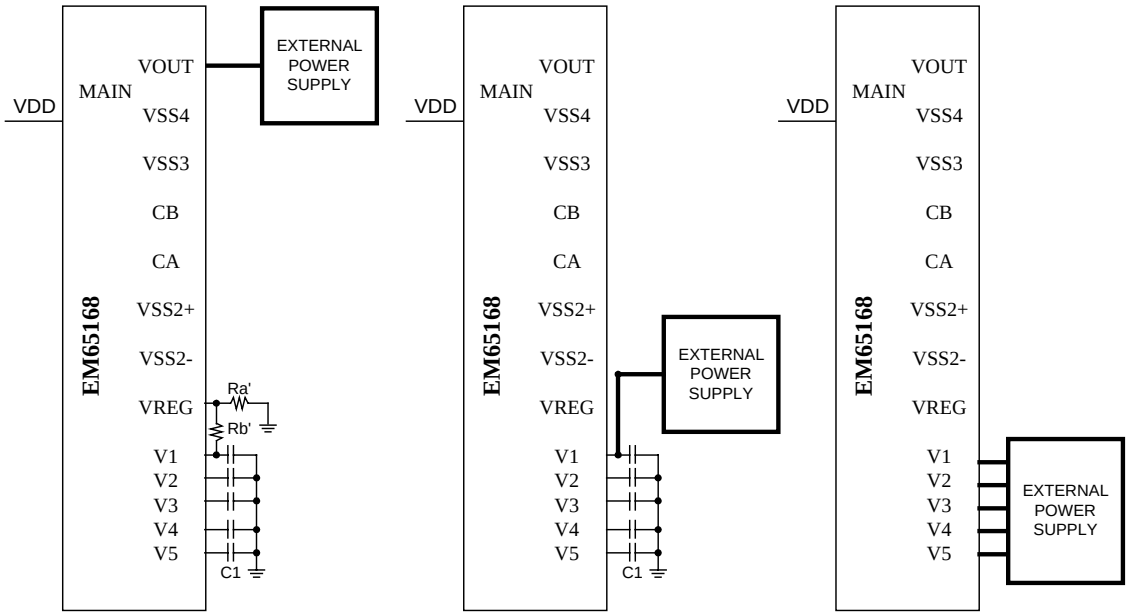

VDD
MAIN
VOUT
VSS4
VSS3
CB
CA
VSS2+
VSS2-
VREG
V1
V2
V3
V4
V5
EM65168
EXTERNAL POWER SUPPLY
Ra'
Rb'
C1
(d)
(e)
(f)

FIG. 13

8. Absolute rating

Rating	*Symbol*	*Value*	*Unit*
DC Supply Voltage	VDD	<6	V
INPUT VOLTAGE	Vin	-0.5 TO Vdd +0.5	V
OPERATING TEMPERATURE RANGE	Ta	-30 TO 80	℃

9. DC characteristic

(Test condition: If not specified, Ta=25°C ;VDD=3V, VSS=0V)

Symbol	*Parameter*	*Condition*	*Min*	*Typ*	*Max*	*Unit*
VDD	Input voltage	With double step-up	2.5		5.5	V
		With triple step-up	2.5		5.5	
		With quad step-up	2.5		4.0	
		With five times step-up	2.5		3.3	
VIH	High level input voltage	※1	0.8VDD	0.9VDD	VDD	V
VIL	Low level input voltage	※1	0	0.1VDD	0.2VDD	V
IOH1	High level output current	VOH = VDD-0.4V ※2	-2.4	-3.2	-4.5	mA
IOL1	Low level output current	VOL= 0.4V ※2	2.4	3.2	4.5	mA
IOH2	High level output current	VOH = VDD-0.4V ※*3	-0.8	-1.0	-1.2	mA
IOL2	Low level output current	VOL= 0.4V ※3	0.8	1.0	1.2	mA
ILI	Input leakage current	VI = VSS or VDD ※4	-2	0	2	μA
ILO	Output leakage current	VI = VSS or VDD ※5	-2	0	2	μA
Iop	Operating current	EN=0. MAIN =1 (MASTER), DC converter enable, Five times step-up ;Display all on pattern (M1, M0)=(1,1), V1=11V 24KHz clock, No load	-	110	160	μA
		EN=0. MAIN =1 (MASTER), DC converter enable, Three times step-up ;Display all on pattern (M1, M0)=(1,1), V1=11V 24KHz clock, No load		85	135	μA
Isb	Standby mode	EN=1	-	1	2	μA
V_{EV}	Voltage variation of regulator	Ta=0℃; REG[5:0]=111111	0.97*V_{EV}	TBD	1.03*V_{EV}	V
		Ta=25℃; REG[5:0]=111111	1.94	2.0	2.06	V
		Ta=40℃; REG[5:0]=111111	0.97*V_{EV}	TBD	1.03*V_{EV}	V
VOUT	Step-up circuit output voltage	x2/x3/x4/x5 R_L=500k (Step-up Capacitor =1 uF)	95	99	100	%
Cv	LCD voltage capacitor	V1,V2,V3,V4,V5	0.47	1	3.3	μF
Cs	Step-up capacitor	CA,CB,VSS2+,VSS2-,VSS3,VSS4	0.1	1	2.2	μF
fosc	Internal oscillator frequency	Ta=25℃	20	24	28	kHz
R_{ON}	LCD ON resistance	V1=9V, 1/9bias |ΔV|=0.5V		1.2	2	KΩ

Note:

※ **1** RAMD[7:0], MAIN, EN,M1,M0,RAMEN,RAMADS, RAMW,RAMR pins.

※ **2** RAMD[7:0] pins

※ **3** FR,LOAD pins

※ **4** MAIN, EN,M1,M0,RAMEN,RAMADS,RAMW,RAMR pins

※ **5** Applied when RAMD[7:0], FR and LOAD are in the state of high impedance.

10. AC Characteristic

(Ta= -30°C ~ 80°C, VDD=3V, VSS=0V)

Symbol	*Parameter*	*Min.*	*Typ.*	*Max.*	*Unit*
Vrc	RC clock variable	-20		+20	%
Tframe	Frame period	1/60	1/75	1/90	S
Tw	Write low pulse	700			nS
Tdh	Data hold time	100			nS
Tdd	Data to data time	100			nS
Tdv	Data valid time	700			nS

11. AC timing

4-bits data bus mode

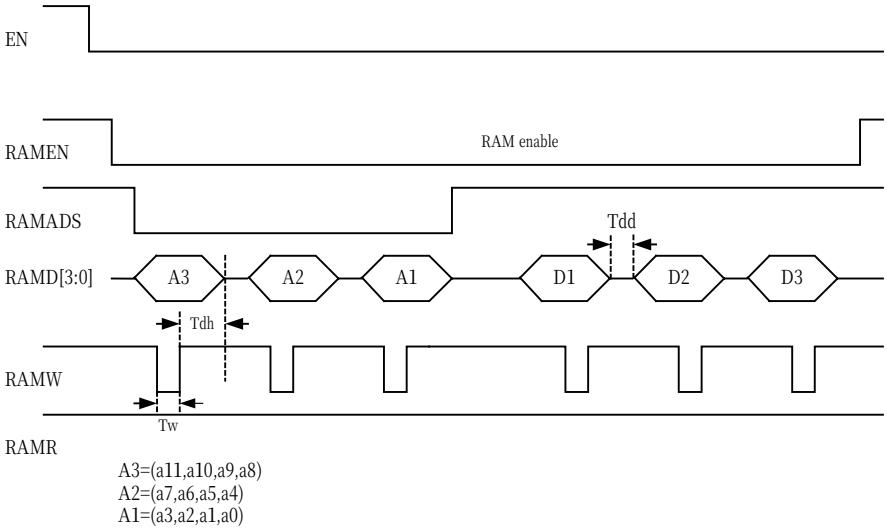


FIG 14 LCD RAM write mode

8-bits data bus mode

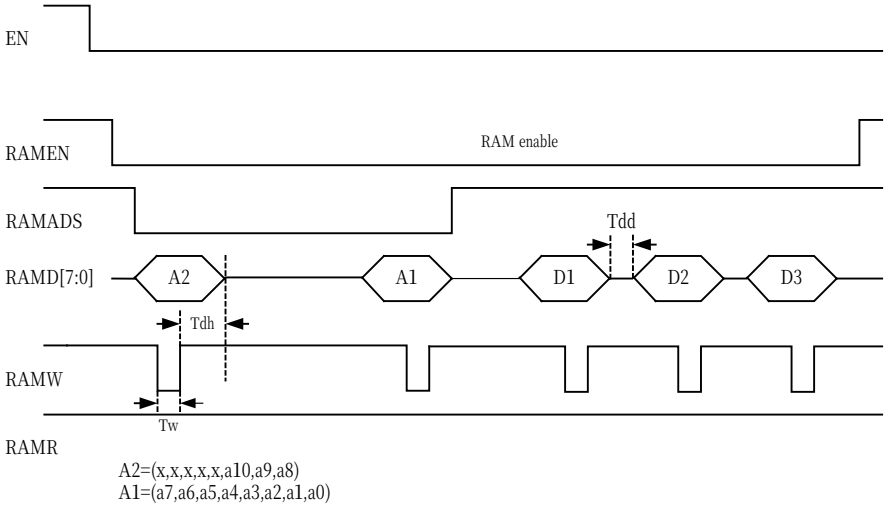


FIG 15 LCD RAM write mode

4-bits data bus mode

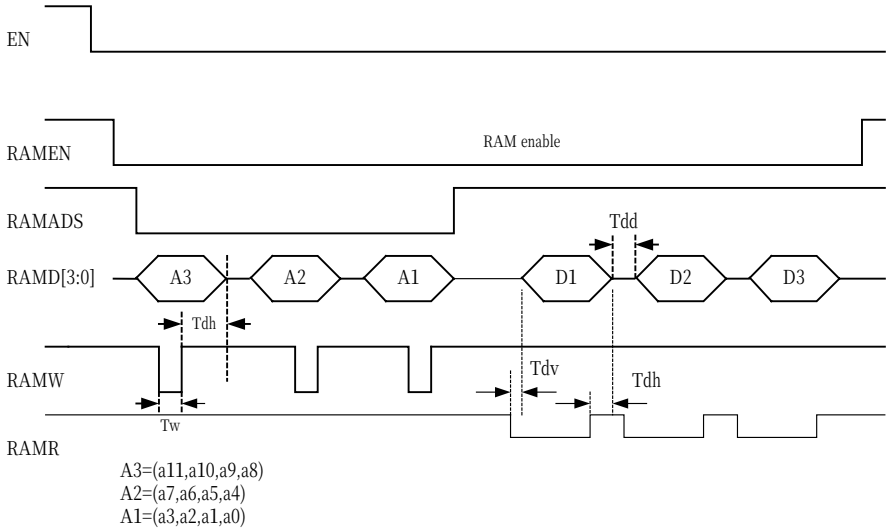


FIG 16 LCD RAM read mode

8-bits data bus mode

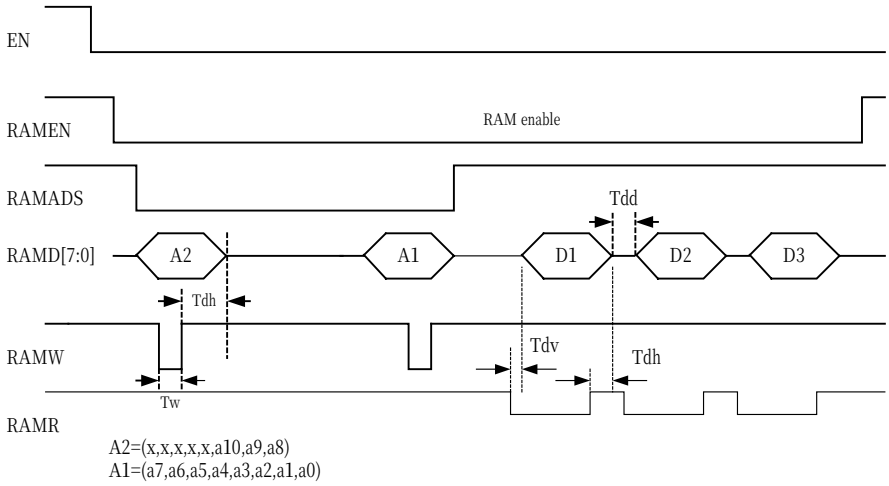


FIG 17 LCD RAM read mode

12. Application circuit

(1) C32 x S48

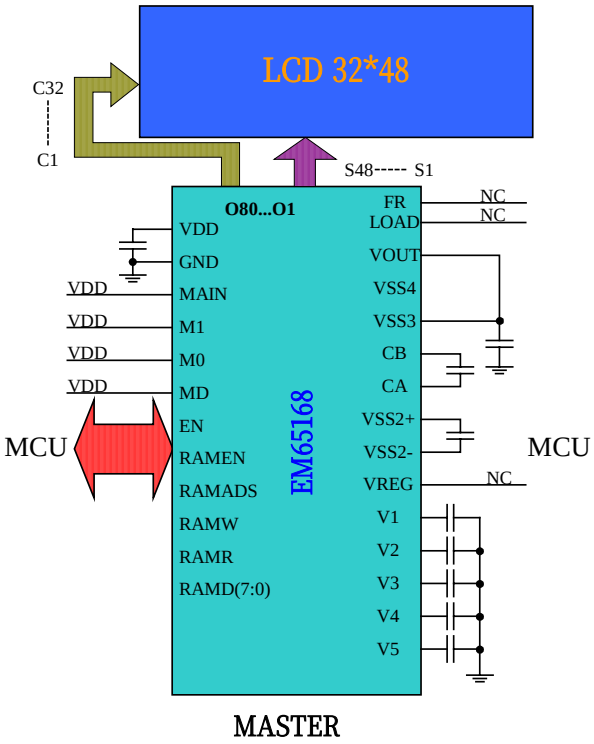


FIG. 18 32common*48segment application circuit

(2) C32 x S128

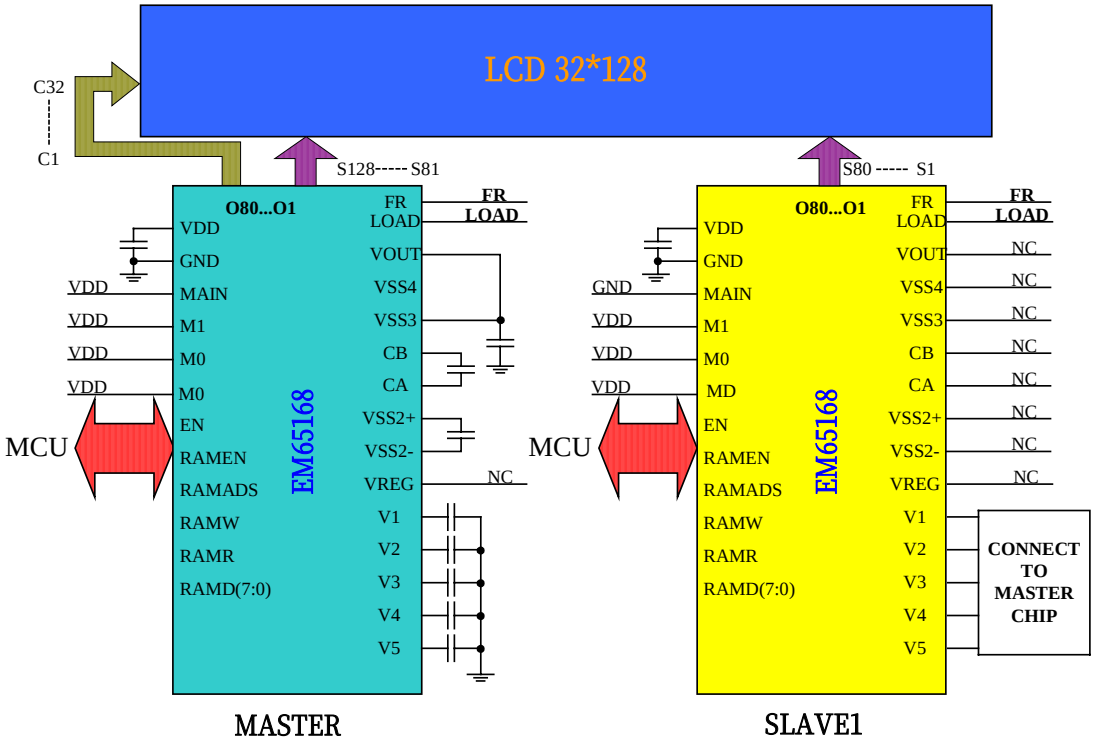


FIG. 19 32common*128segment application circuit

(3) C48 x S112

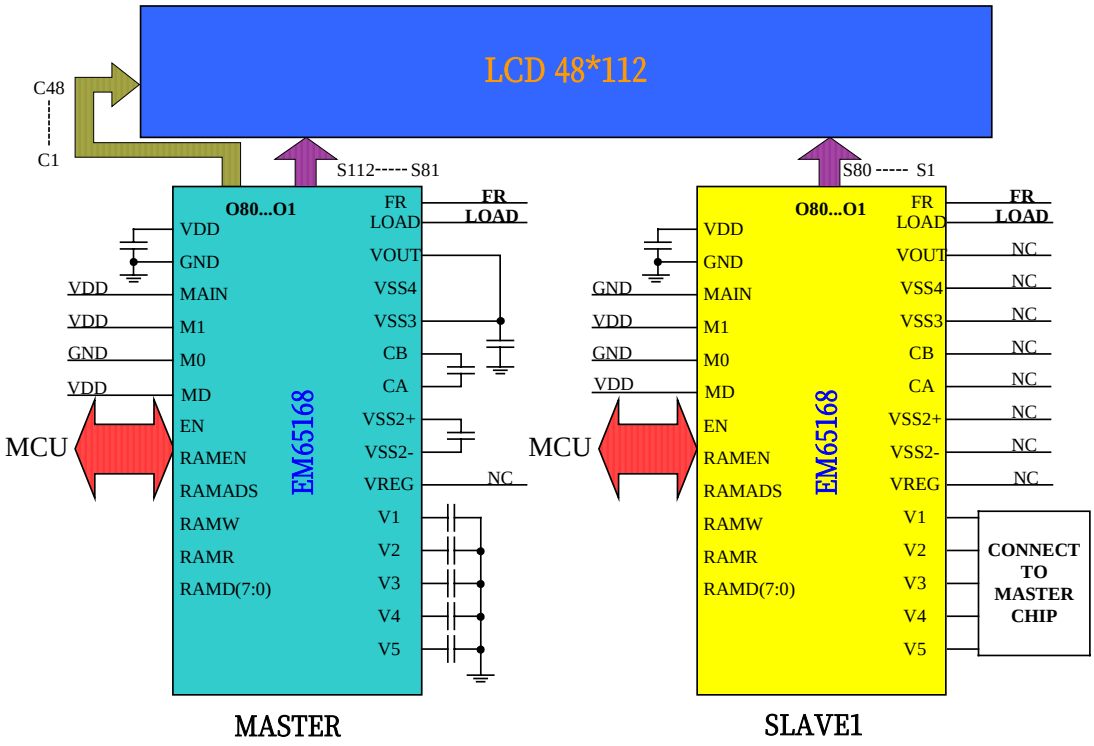


FIG. 20 48common*112segment application circuit

(4) C64 x S96

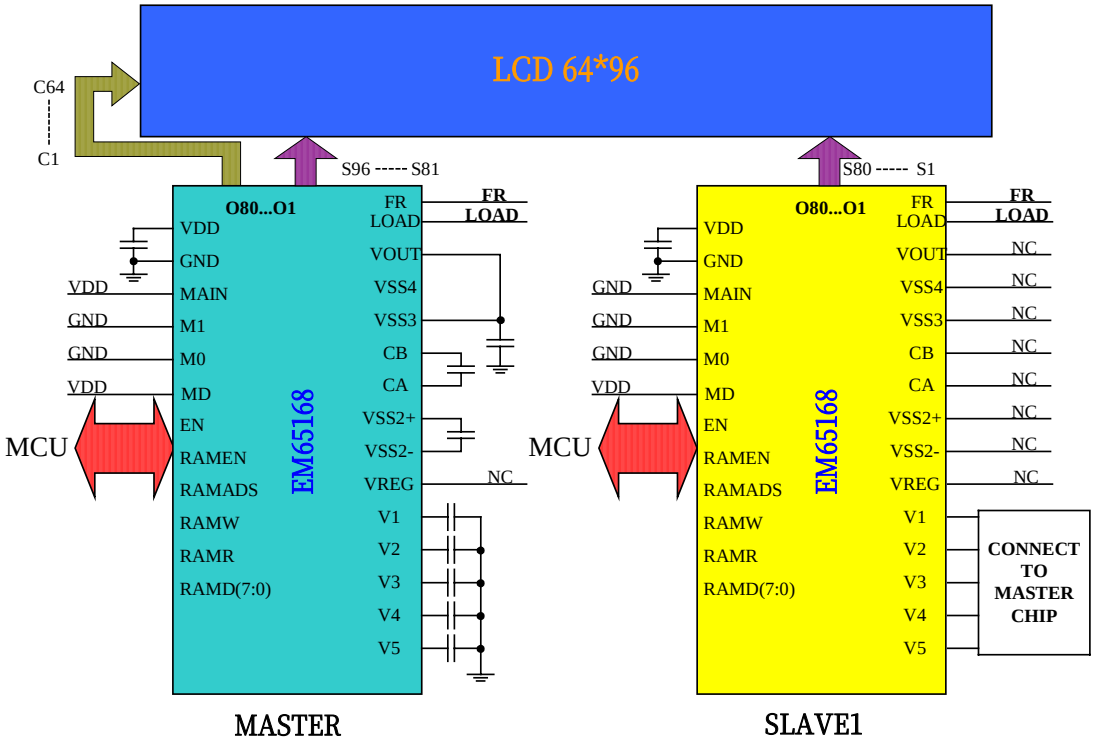


FIG. 21 64common*96segment application circuit

(5) C80*S160

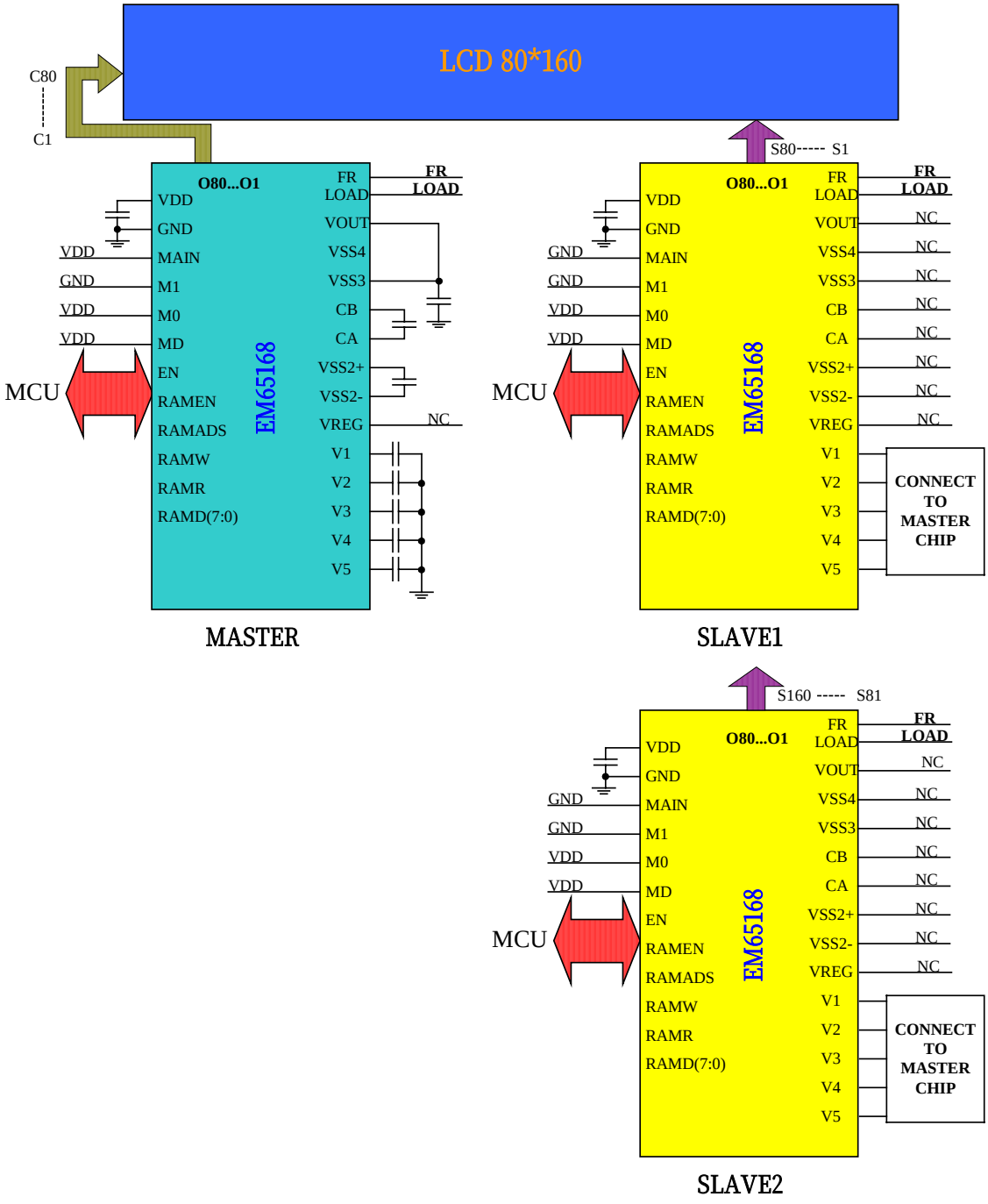


FIG. 22 80common*160segment application circuit

13. Package information

EM65168/EM65168A COB bonding diagram

(Recommend using the following method to improve the bonding yield)