# 10-Bit high-speed multiplying D/A converter NE/SE5410

## DESCRIPTION

The NE5410/SE5410 are 10-bit Multiplying Digital-to-Analog Converters pin- and function-compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost effective D/A systems.

The NE/SE5410 provides complete 10-bit accuracy and differential non-linearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC, provide the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

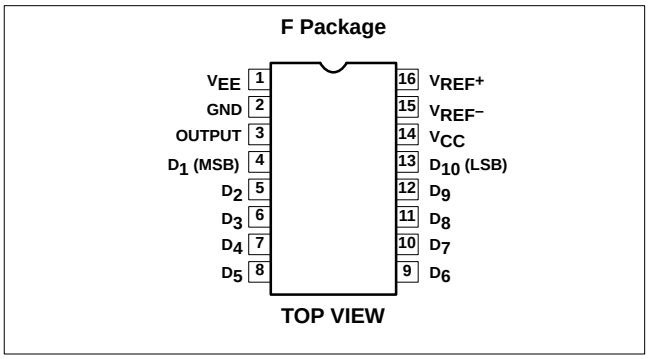
## FEATURES

- Pin- and function-compatible with MC3410
- 10-bit resolution and accuracy (±0.05%)
- Guaranteed differential non-linearity over temperature
- Wide compliance voltage range—-2.5 to +2.5V
- Fast settling time—250ns typical
- Digital inputs are TTL- and CMOS-compatible
- High-speed multiplying input slew rate—20mA/µs
- Reference amplifier internally-compensated
- Standard supply voltages +5V and -15V

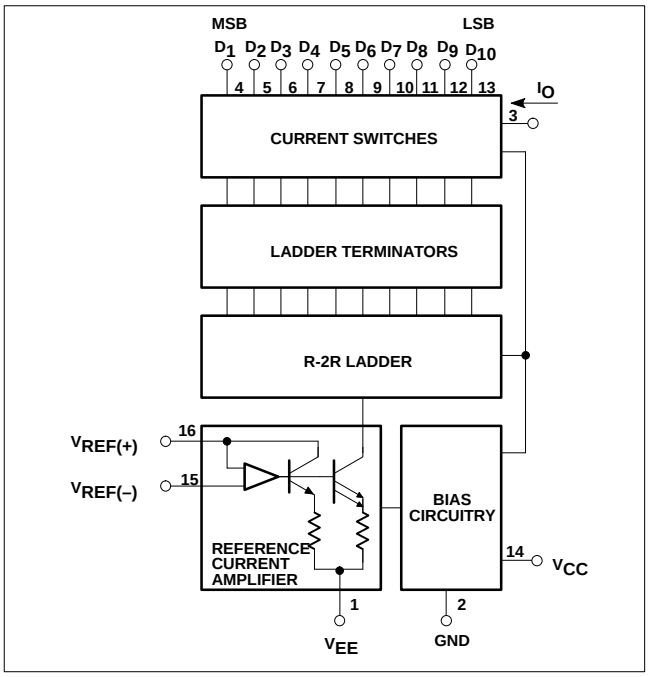
## APPLICATIONS

- Successive approximation A/D converters
- High-speed, automatic test equipment
- High-speed modems
- Waveform generators
- CRT displays
- Strip CHART and X-Y plotters
- Programmable power supplies
- Programmable gain and attenuation

## PIN CONFIGURATION




## BLOCK DIAGRAM




## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG # |
|---|---|---|---|
| 16-Pin Ceramic Dual In-Line Package (CERDIP) | 0 to +70°C | NE5410F | 0582B |
| 16-Pin Ceramic Dual In-Line Package (CERDIP) | -55 to +125°C | SE5410F | 0582B |

## ABSOLUTE MAXIMUM RATINGS

$T_A$=+25°C, unless otherwise specified.

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Power supply | +7.0 | $V_{DC}$ |
| $V_{EE}$ | | -18 | $V_{DC}$ |
| $V_I$ | Digital input voltage | +15 | $V_{DC}$ |
| $V_O$ | Applied output voltage | +4, -5.0 | $V_{DC}$ |
| $I_{REF(16)}$ | Reference current | 2.5 | mA |
| $V_{REF}$ | Reference amplifier inputs | $V_{CC}$, $V_{EE}$ | $V_{DC}$ |
| $V_{REF(D)}$ | Reference amplifier differential inputs | 0.7 | $V_{DC}$ |
| $T_A$ | Operating temperature range | | |
| | SE5410 | -55 to +125 | °C |
| | NE5410 | 0 to +70 | °C |
| $T_J$ | Junction temperature | | |
| | Ceramic package | +150 | °C |
| $T_{STG}$ | Storage temperature | -65 to +150 | °C |
| $P_D$ | Maximum power dissipation $T_A$=25°C (still-air)[1] | 1190 | mW |

**NOTES:**
1. Derate above 25°C at the following rate:
   F package at 9.5mW/°C

## DC ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}$=+5.0$V_{DC}$, $V_{EE}$=-15$V_{DC}$, $I_{REF}$=2.0mA, all digital inputs at high logic level. SE5410: $T_A$=-55°C to +125°C, NE5410 Series: $T_A$=0°C to +70°C, unless otherwise noted.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $\in_R$ | Relative accuracy | Over Temperature | | ±0.025 | ±0.05 | % |
| | (Error relative to full scale $I_O$) | | | ±1/4 | ±1/2 | LSB |
| | Differential non-linearity | Over temperature | | ±0.025 | ±0.05 | % |
| | | | | ±1/4 | ±1/2 | LSB |
| $t_S$ | Settling time to within ±1/2 LSB (all bits low to high) | $T_A$ = 25°C | | 250 | | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay time | $T_A$ = 25°C | | 35<br>20 | | ns |
| $TCI_O$ | Output full-scale current drift | | | 20 | 40 | ppm/°C |
| $V_{IH}$ | Digital input logic levels (all bits)<br>High level, Logic "1"<br>Low level, Logic "0" | | 2.0 | | 0.8 | $V_{DC}$ |
| $I_{IH}$<br>$I_{IL}$ | Digital input current (all bits)<br>High level, $V_{IH}$ = 5.5V<br>Low level, $V_{IL}$ = 0.8V | | | | 20<br>–20 | µA |
| $I_{REF(15)}$ | Reference input bias current (Pin 15) | | | –1.0 | –5.0 | µA |
| $I_{OH}$ | Output current (all bits high) | $V_{REF}$ = 2.000V, R16 = 1000Ω | 3.937 | 3.996 | 4.054 | mA |
| $I_{OL}$ | Output currents (all bits low) | $T_A$ = 25°C | | 0 | 0.4 | µA |
| $V_O$ | Output voltage compliance | $T_A$ = 25°C<br>$\in_R$ < 0.050%<br>relative to full-scale | | | –2.5<br>+2.5 | $V_{DC}$ |
| SR $I_{REF}$ | Reference amplifier slew rate | | | 20 | | mA/µs |
| ST $I_{REF}$ | Reference amplifier settling time | 0 to 4.0mA, ±0.1% | | 2.0 | | µs |
| PSRR(–) | Output current power supply sensitivity | | | 0.003 | 0.01 | %/% |
| $C_O$ | Output capacitance | $V_O$ = 0 | | 25 | | pF |

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$=+5.0$V_{DC}$, $V_{EE}$=-15$V_{DC}$, $I_{REF}$=2.0mA, all digital inputs at high logic level. SE5410: $T_A$=-55°C to +125°C, NE5410 Series: $T_A$=0°C to +70°C, unless otherwise noted.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_I$ | Digital input capacitance (all bits high) | | | 4.0 | | pF |
| $I_{CC}$<br>$I_{EE}$ | Power supply current (all bits low) | | | +2<br>–12 | +4<br>–18 | mA |
| $V_{CC}$<br>$V_{EE}$ | Power supply voltage range | $T_A$ = 25°C<br>$V_O$ = 0 | +4.75<br>–14.25 | +5.0<br>–15 | +5.25<br>–15.75 | $V_{DC}$ |
| | Power consumption | | | 190 | 300 | mW |

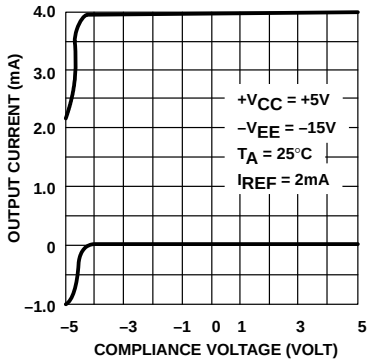



**Figure 1. Output Current vs Output Compliance Voltage**

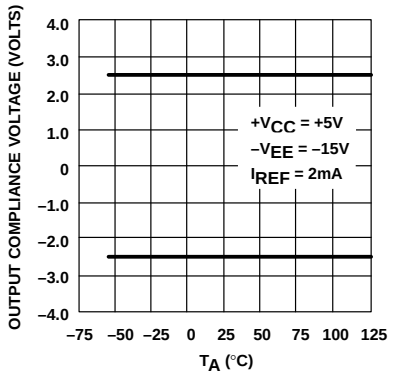



**Figure 2. Maximum Output Compliance Voltage vs Temperature**

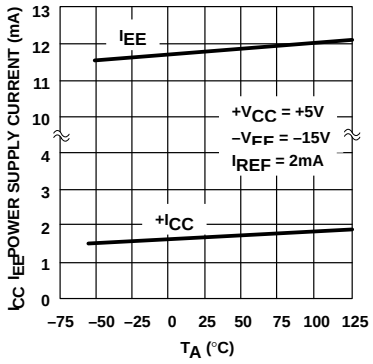



**Figure 3. Power Supply Currents vs Temperature**

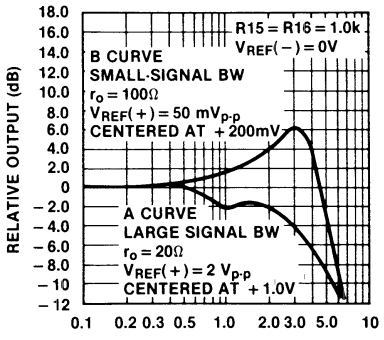



**Figure 4. Reference Amplifier Frequency Response**

## CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion-implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs) (see Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully-differential current switches. The switches use current steering for speed.

An on-chip high slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is

approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the $V_{EE}$ supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16=1.0kΩ, and settling time is ±10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

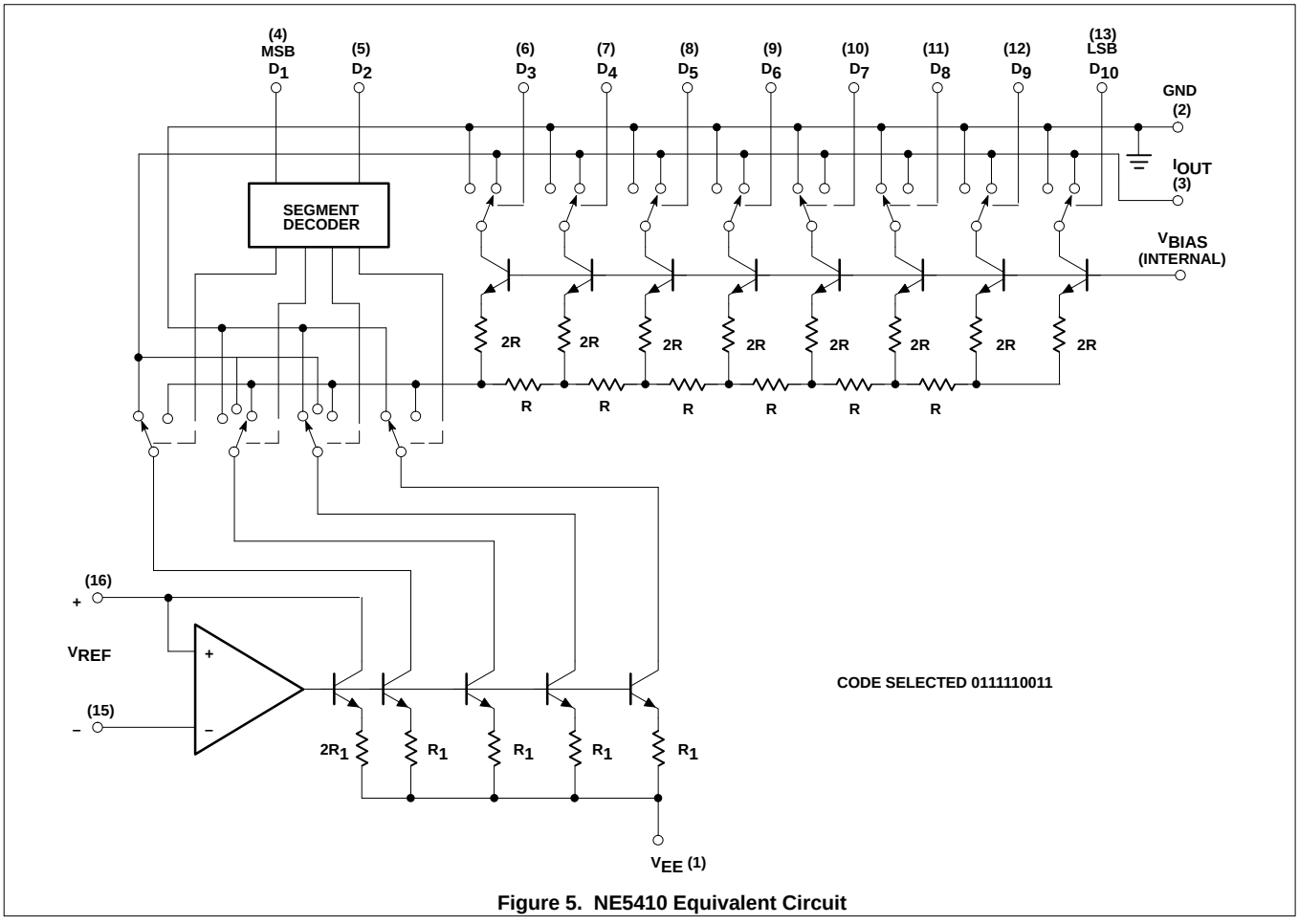



**Figure 5. NE5410 Equivalent Circuit**

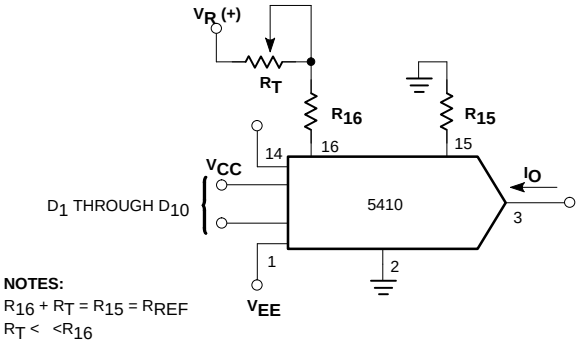



**Figure 6. Basic Connections**

## OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from -2.5 to +2.5V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE}$>-15V.

## ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full-scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ± LSB at 25°C with a reference current of 2.0mA on Pin 16.

## MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

## SETTLING TIME

The worst-case switching condition occurs when all bits are switched “on,” which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for the output to settle to within ± 1/2LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to -2.5V, the settling time increases to 1.5µs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100µF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor $R_L$.

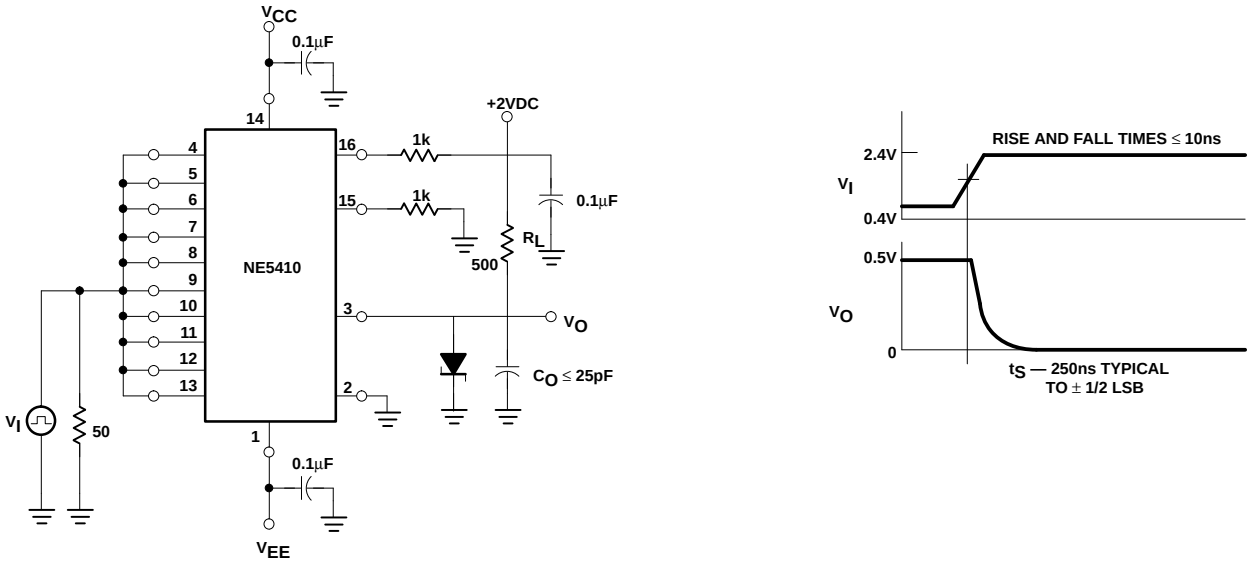



**Figure 7. Settling Time**

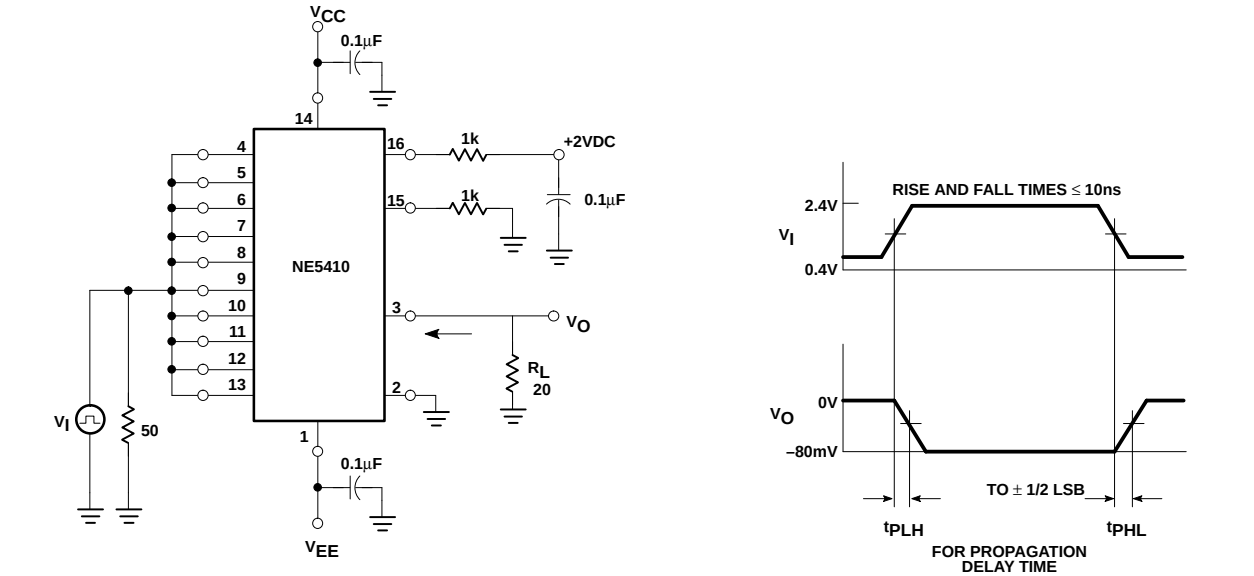



**Figure 8. Propagation Delay Time**

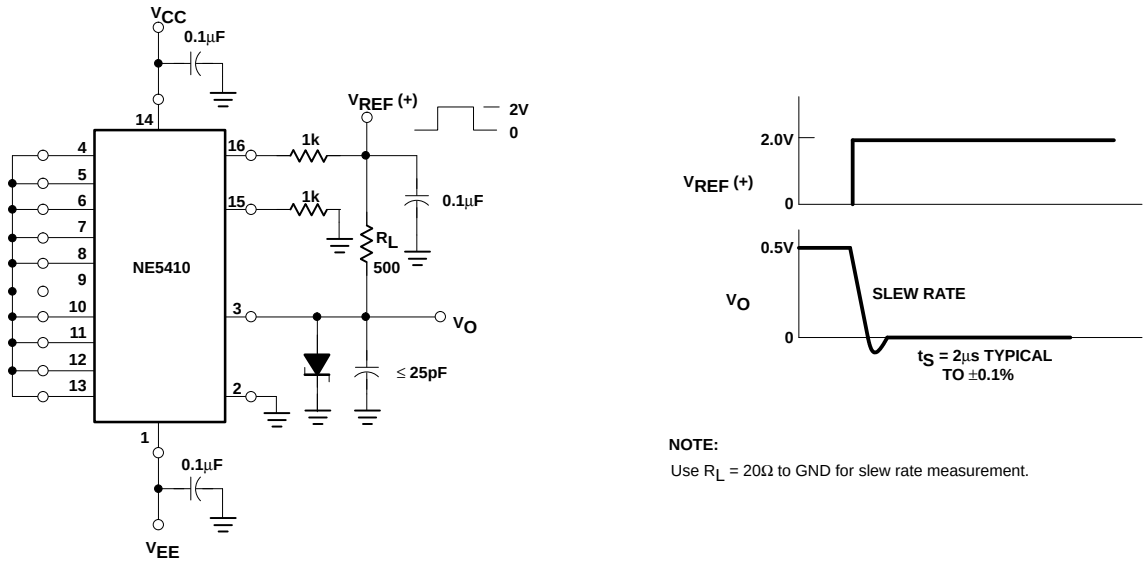



**Figure 9. Reference Amplifier Settling Time and Slew Rate**

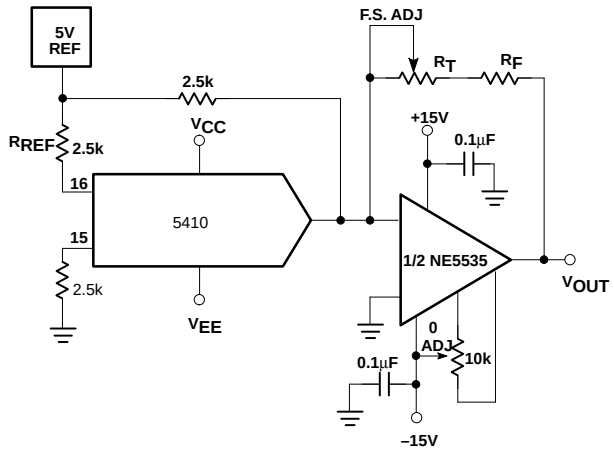
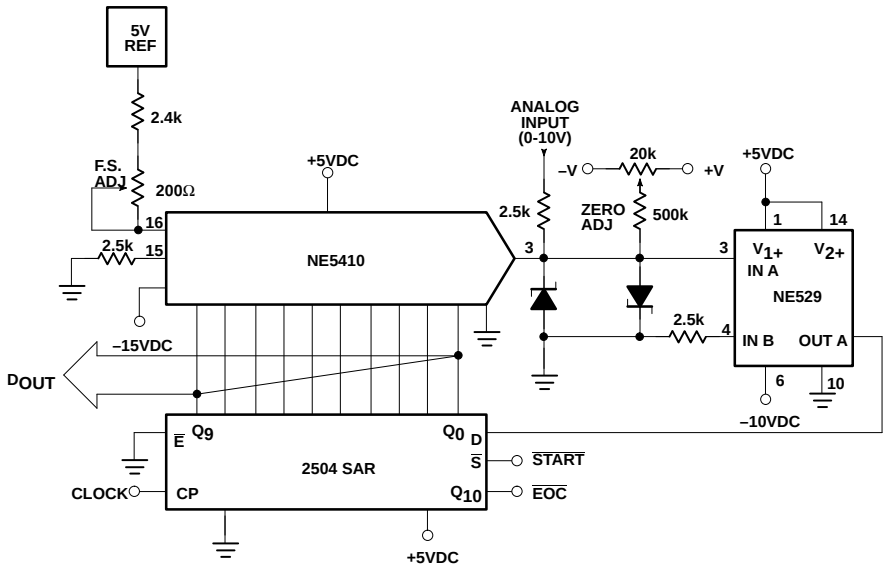
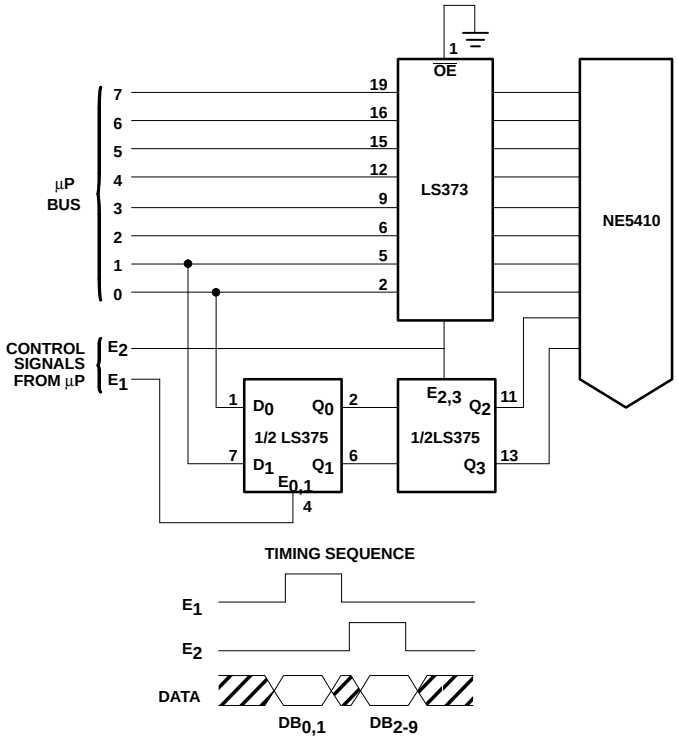



**Figure 10. Bipolar Voltage Output Circuits (-10V to +10V)**




**NOTES:**
10-bit conversion time = 3.3µs with 3MHz clock.
This converter uses a 2504 12-bit successive approximation register in the short cycle operating mode where the end of conversion signal is taken from the first unused bit of the SAR ($Q_{10}$).

**Figure 11. Successive Approximation A/D Converter**

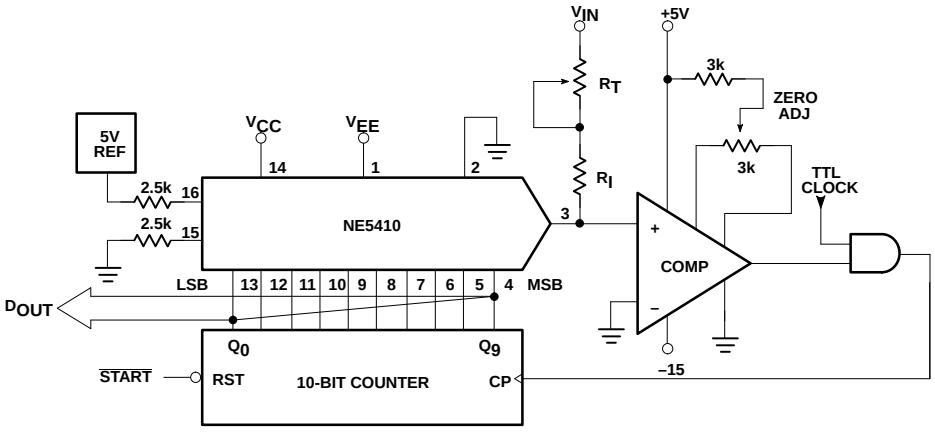






**NOTES:**
With this double latch technique, valid data will be latched to the DAC until updated with the $E_2$ pulse. Timing will depend on the processor used.

**Figure 12. 8-Bit µP Bus Interface**




**NOTE:**

$V_{IN}$ FULL SCALE = 4mA $(R_1 + R_T)\left(\frac{1023}{1024}\right)$

**Figure 13. Staircase A/D**