Ordering number :EN5452A

Monolithic Digital IC

# LB1955

## Three-Phase Brushless Motor Driver

## Functions

- The LB1955 is a 3-phase brushless motor driver IC that is optimal for applications such as driving the drum motor in VCRs.

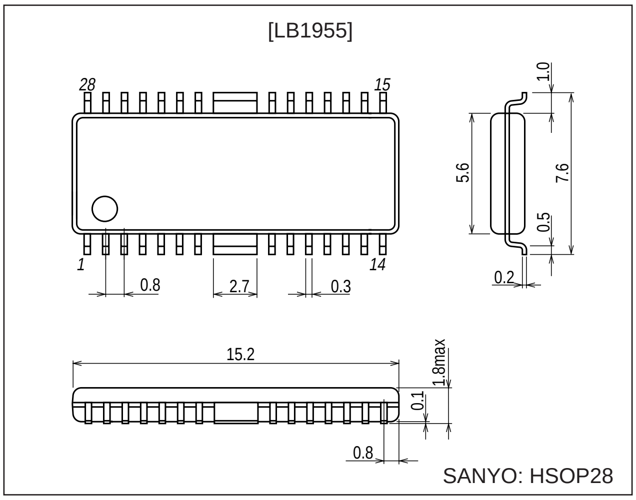
## Features

- Current linear drive
- FG and PG free
- Single-voltage power supply
- Built-in AGC circuit
- Built-in thermal shutdown circuit

## Package Dimensions

unit: mm

**3222-HSOP28**




## Specifications

### Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$max | | 14.5 | V |
| Maximum output current | $I_{OUT}$ | | 1.0 | A |
| Allowable power dissipation | Pdmax | Independent device | 0.60 | W |
| Operating temperature | Topr | | –20 to +75 | °C |
| Storage temperature | Tstg | | –55 to +150 | °C |

### Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 10.2 to 13.8 | V |
| Hall input amplitude | Vhall | At the input | 70 to 500 | mVp-p |
| VC input voltage | $V_C$ | | 0 to 5 | V |

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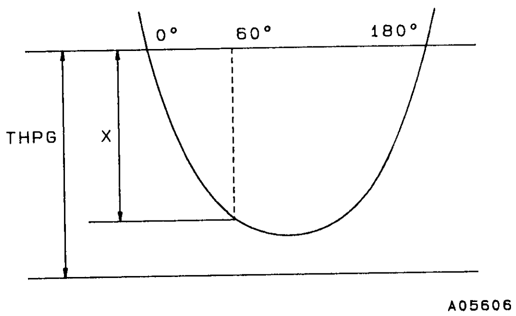
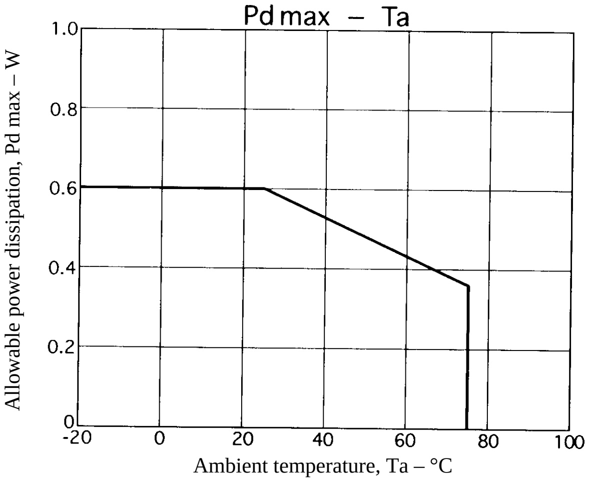
## Electrical Characteristics at Ta = 25°C, $V_{CC}$ = 12 V

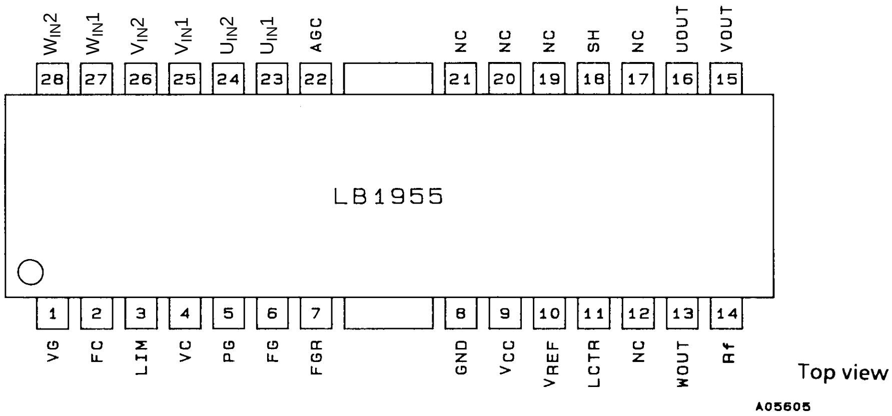
| Parameter | Symbol | Conditions | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| [Power Supply] | | | | | | | |
| Current drain | $I_{CC}$ | $V_C$ = 0 V, LCTR = 6 V | | 7.0 | 10.0 | 13.0 | mA |
| IC internal power supply | $V_{REF}$ | | | 4.75 | 5.0 | 5.25 | V |
| [Output] | | | | | | | |
| Output saturation voltage | $V_{O(sat)}1$ | $I_O$ = 400 mA | Sink side | | | 0.4 | V |
| | | $V_C$ = 5 V, $R_f$ = 0 Ω | Source side | | | 1.5 | V |
| Output saturation voltage 2 | $V_{O(sat)}2$ | $I_O$ = 800 mA | Sink side | | | 0.7 | V |
| | | $V_C$ = 5 V, $R_f$ = 0 Ω | Source side | | | 2.0 | V |
| 3-phase output current ripple | Ior | $I_O$ = 100 mA, $R_f$ = 0.47 Ω | | –5 | | +5 | % |
| [Hall Amplifier] | | | | | | | |
| Input offset voltage | VHoff | | | –20 | | +20 | mV |
| Input bias current | IHb | $V_{AGC}$ = 1.4 V | $U_{IN}$ | | | 10 | μA |
| | | | $V_{IN}$, $W_{IN}$ | | | 5 | μA |
| Common-mode input voltage range | $V_{HCM}$ | | | 2.2 | | 5.0 | V |
| [Control] | | | | | | | |
| VC pin input bias current | $I_{VCb}$ | $V_C$ = 0 V | | –10 | –1.3 | | μA |
| Control start voltage | $V_{THVC}$ | $R_f$ = 0.47 Ω, $I_O$ ≥ 10 mA<br>With the Hall input logic fixed | | 2.25 | 2.5 | 2.75 | V |
| Open-loop control gain | $G_{MVC}$ | $R_f$ = 0.47 Ω, $\Delta I_O$ = 200 mA<br>With the Hall input logic fixed and VG shorted to RF | | 0.72 | 0.9 | 1.08 | A/V |
| [PG] | | | | | | | |
| PG Hall amplifier input offset voltage | $V_{PGoff}$ | Design target | | –10 | | +10 | mV |
| Peak hold charge current | $I_{SHCHG}$ | (U, V, W) = (L, L, H) | | | 30 | | μA |
| PG comparator threshold | THPG | SH = 1000pF, Design target* | | 113 | 117 | 121 | % |
| PG output high-level voltage | $V_{PGH}$ | | | 4.5 | | 5.2 | V |
| PG leakage current | $I_{LEAKPG}$ | | | –10 | 0 | +10 | μA |
| [FG] | | | | | | | |
| Back emf Schmitt input hysteresis width | $V_{SCHG}$ | In the back emf Schmitt input increasing direction, Design target | | | 100 | | mV |
| | | In the back emf Schmitt input decreasing direction, Design target | | | 0 | | mV |
| Ringing canceller Schmitt input hysteresis width | $V_{SCHR}$ | In the Schmitt input increasing direction, Design target | | | 180 | | mV |
| | | In the Schmitt input decreasing direction, Design target | | –20 | 0 | +20 | mV |
| FG output high-level voltage | $V_{FGH}$ | FGR = 0 V | | 4.5 | | 5.2 | V |
| FG leakage current | $I_{LEAKFG}$ | | | –10 | 0 | +10 | μA |
| [TSD] | | | | | | | |
| Thermal shutdown operating temperature | TTSD | Design target | | | 180 | | °C |
| Thermal shutdown temperature hysteresis width | ΔTSD | Design target | | | 15 | | °C |

Note: * is provided for when X is the peak value at the 60° position of the lower side of the $U_{IN}1$ Hall amplifier input: THPG = 1.17X.
However, note that the THPG level may be reduced if the value of the capacitor (SH) used for the sample-and-hold circuit is too small since a discharge current of a few nA will result.






## Pin Assignment




## Pin Functions

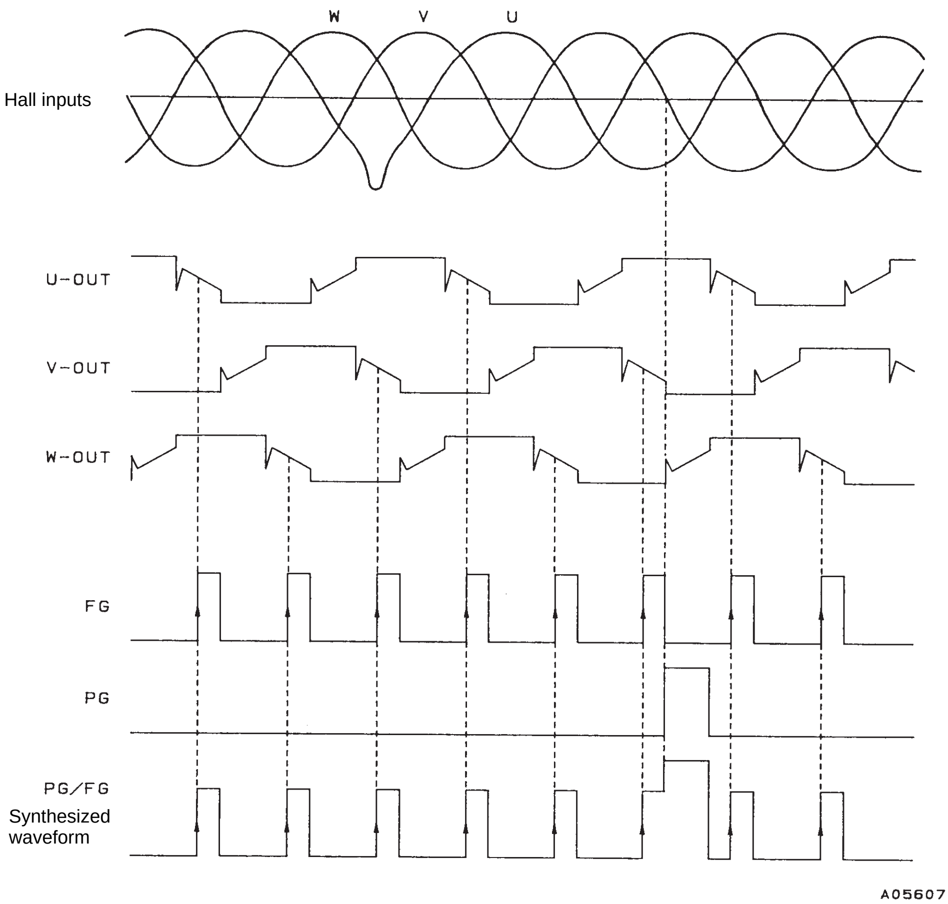
| Pin No. | Pin | Function |
|---|---|---|
| 23, 24<br>25, 26<br>27, 28 | $U_{IN}1$, $U_{IN}2$<br>$V_{IN}1$, $V_{IN}2$<br>$W_{IN}1$, $W_{IN}2$ | U phase Hall element input<br>V phase Hall element input<br>W phase Hall element input |
| 16<br>15<br>13 | UOUT<br>VOUT<br>WOUT | U phase output<br>V phase output<br>W phase output |
| 11 | LCTR | Pin connected to the center points of the coils that are Y-connected to the U, V, and W outputs. |
| 9 | $V_{CC}$ | Power supply |
| 10 | $V_{REF}$ | Reference voltage output |
| 8 | GND | GND |
| 14 | Rf | Output current detection |
| 1 | VG | Closed loop control gain switching |
| 2 | FC | Speed control loop frequency characteristics correction |
| 3 | LIM | Output current limit setting |
| 4 | VC | Speed control |
| 5 | PG | PG waveform output |
| 6 | FG | FG waveform output (FGR shorted to GND) |
| 7 | FGR | PG/FG synthesized output (FGR shorted to PG) |
| 18 | SH | PG waveform sample-and-hold circuit capacitor connection |
| 22 | AGC | Connection for the capacitor used by the AGC circuit, which holds the input gain at a fixed level. |
| 12, 17, 19<br>20, 21 | NC | No connection |

## Truth Table

| | Source → sink | Hall input logic | | |
|---|---|---|---|---|
| | | U | V | W |
| 1 | W phase → V phase | H | H | L |
| 2 | W phase → U phase | H | L | L |
| 3 | V phase → U phase | H | L | H |
| 4 | V phase → W phase | L | L | H |
| 5 | U phase → W phase | L | H | H |
| 6 | U phase → V phase | L | H | L |

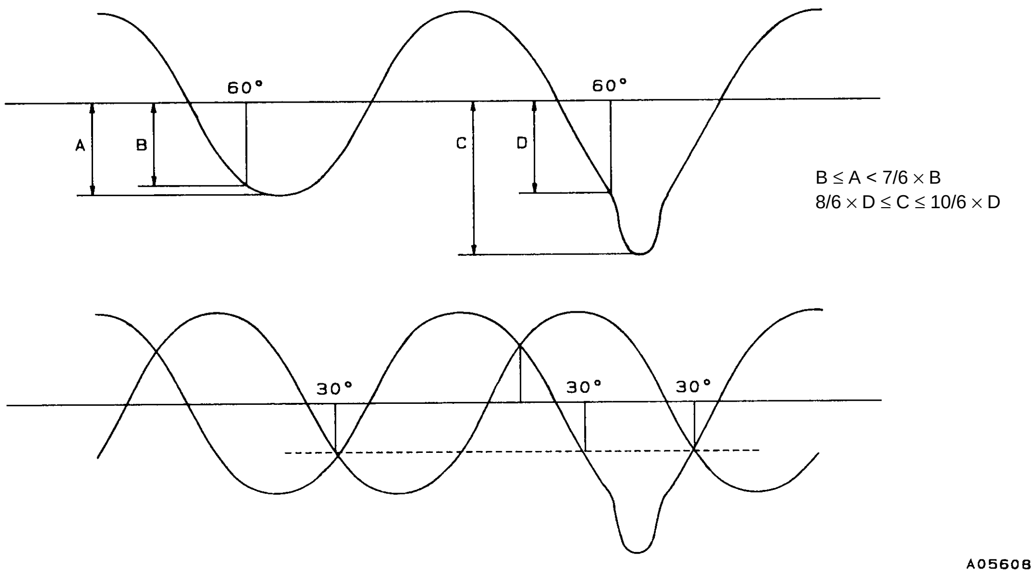
Note: The Hall input "H" and "L" values are defined as follows: "H" means that for that phase the (+) input is higher than the (-) input, and "L" means that for that phase the (+) input is lower than the (-) input. However, note that an input potential difference corresponding to the Hall to output gain is required.

## Timing Charts



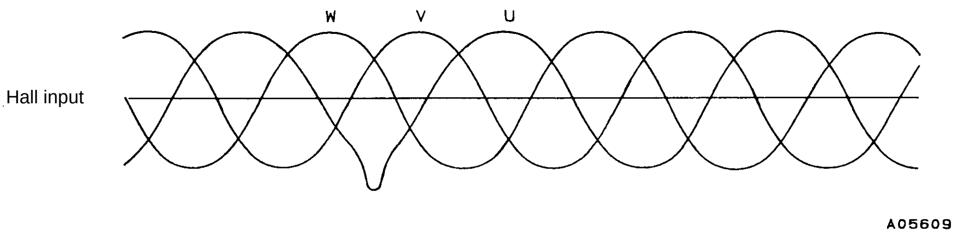

Note: The Hall inputs are defined as follows: $U = U_{IN}1 - U_{IN}2$, $V = V_{IN}1 - V_{IN}2$, and $W = W_{IN}1 - W_{IN}2$.
Inputs to the Hall input pins must be applied in the phase order shown in the timing chart.

## Recommended Special Magnetization Waveforms



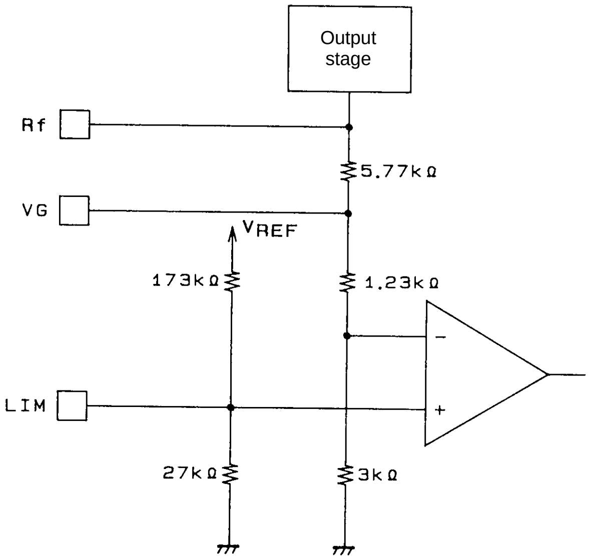

Note: Note that the intersections between the special magnetization and general waveforms and the intersections between pairs of general waveforms must be set up to be 30° apart.

## Hall Input Order




Note: The Hall input order must be set up to be W → V → U.

## VG and LIM Pin Usage

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LIM pin: Open
- VG – Rf: Shorted
- Gm = 0.423/Rf (A/V) (Closed loop control gain)
- Ilim = ($V_{REF}$ × 27/200 – 0.2) × 4.23/3/Rf (Current limit)

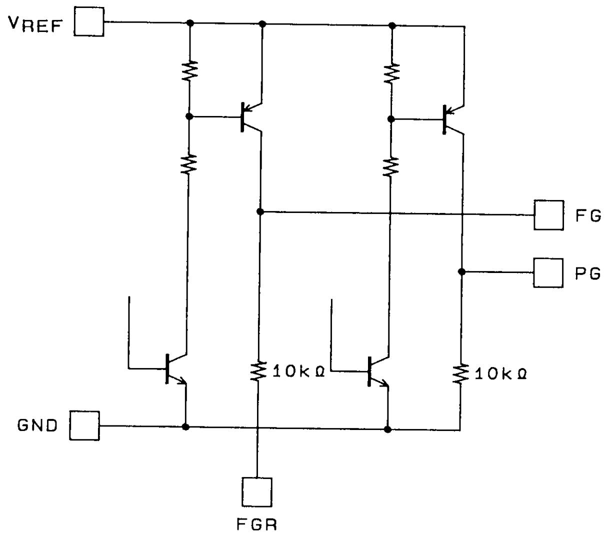
VG pin: Open
- Gm = 1/Rf (A/V) (Closed loop control gain)
- Ilim = ($V_{REF}$ ×27/200 – 0.2) ×10/3/Rf (Current limit)

LIM – $V_{REF}$: Shorted
- No current limit.

Note: This current limiting function is for protection against unusual and abnormal currents. If a current limit level below the rated current is set, this will, inversely, result in heat generation within the IC.

When the LIM pin is open, VG is shorted to Rf, and Rf = 0.47 Ω, this will result in a current limit level of about 1.3 to 1.4 A. If this limit falls under the rated value due to mode changes or changes in the value of the Rf resistor, set the current limit to an appropriate value by applying to the LIM pin a voltage that is divided from the $V_{REF}$ to ground potential by resistors of a few kΩ. Alternatively, short the LIM pin to $V_{REF}$ to defeat the current limit function.

## PG and FG Pin Output Circuits

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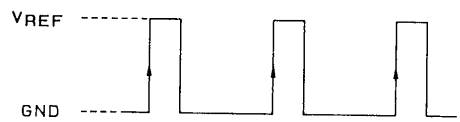
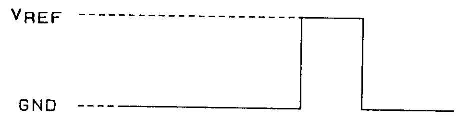
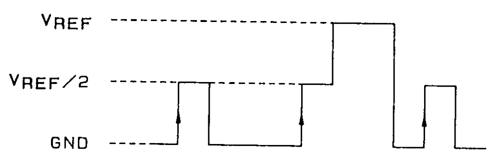
## FG (FGR shorted to ground)




PG




## PG (FGR shorted to PG)

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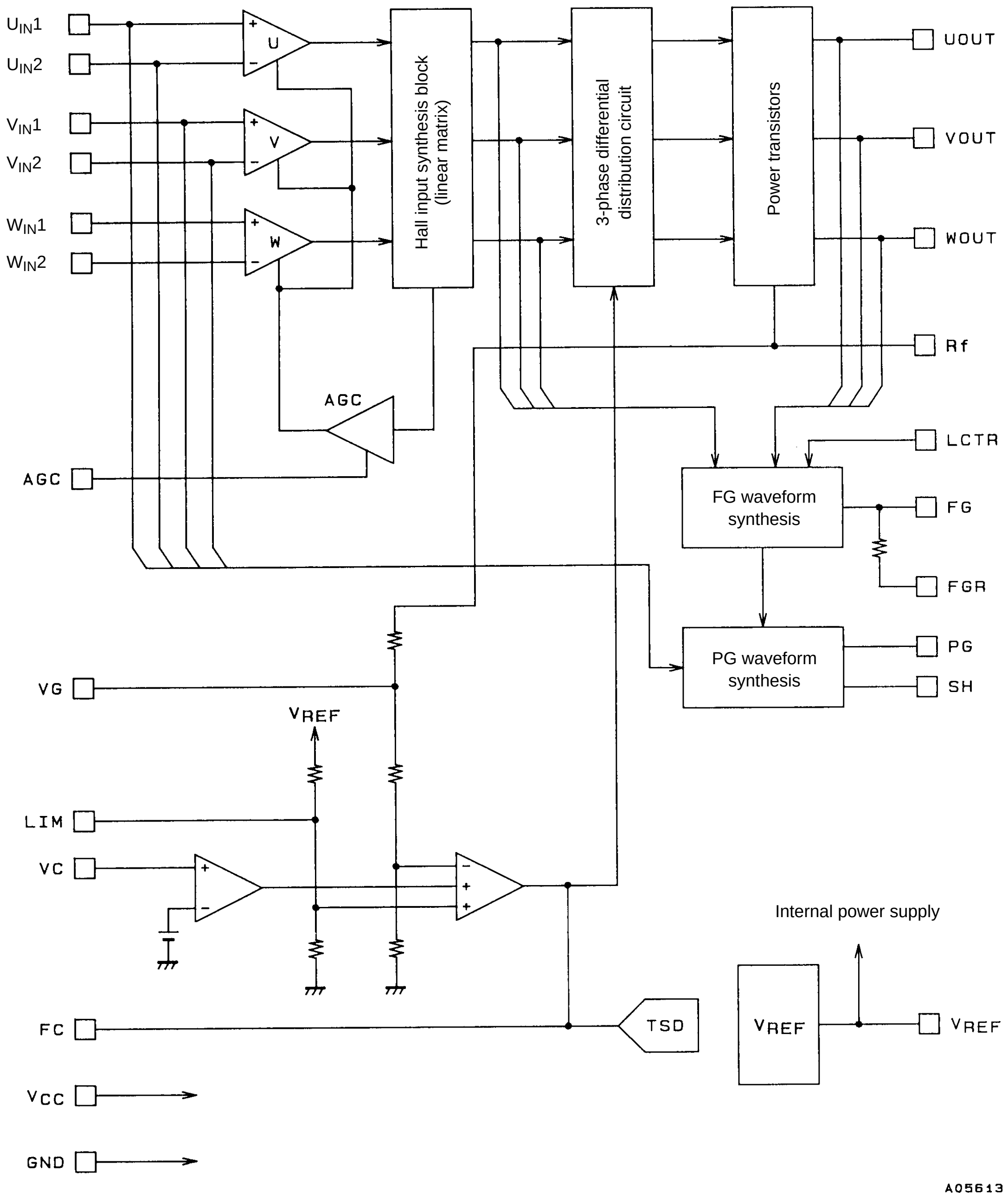
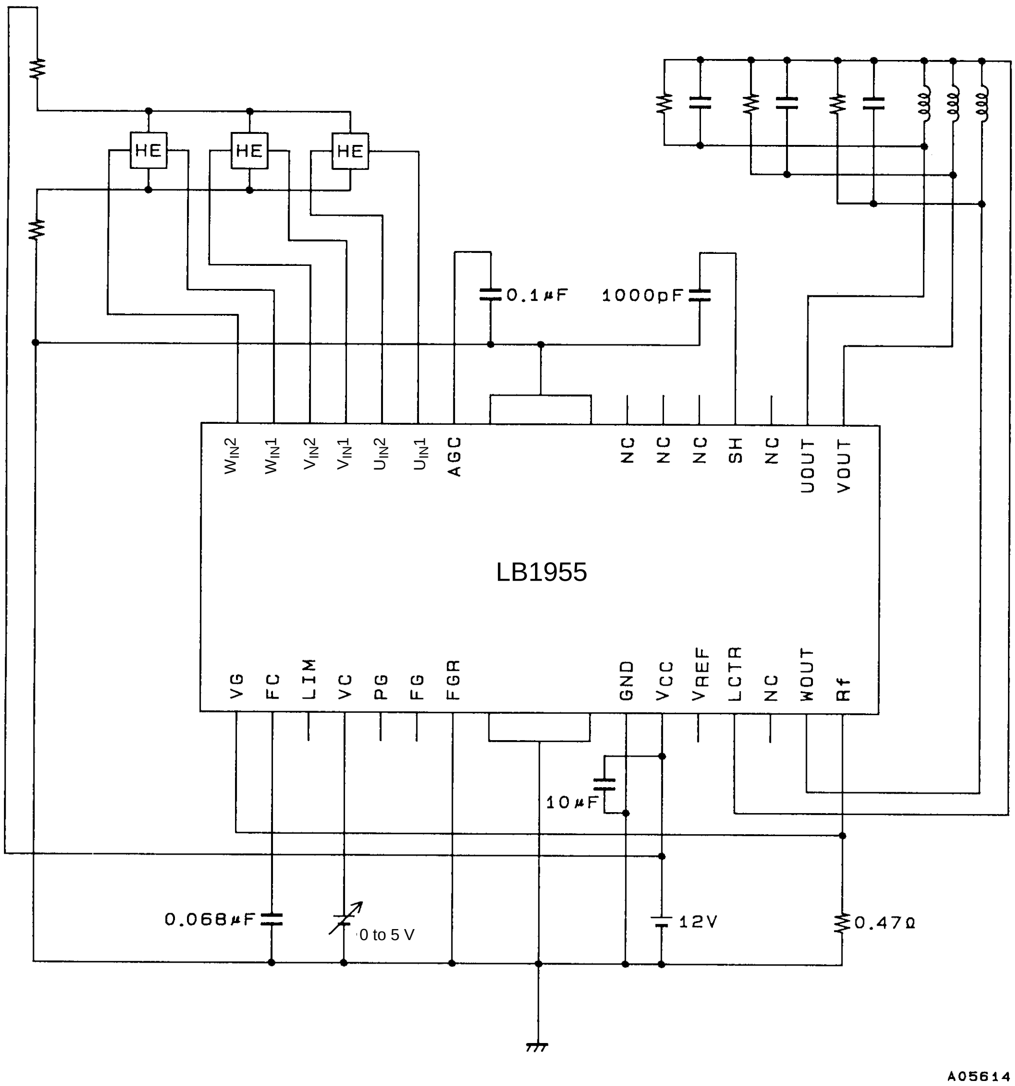
## Block Diagram



## Sample Application Circuit



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