Dual Channel, High CMR, High Speed, TTL Compatible Optocouplers 8 Pin DIP and SOIC-8

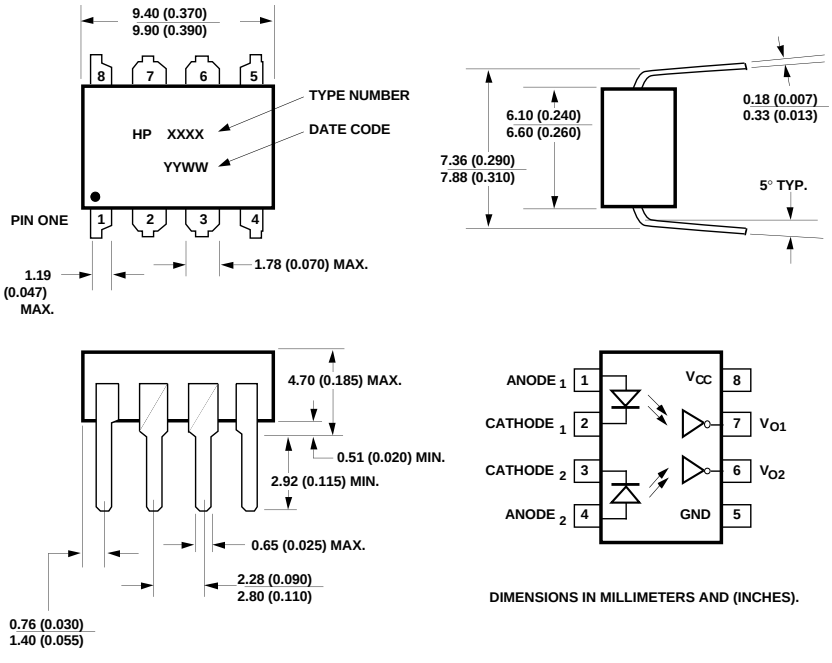
Technical Data

HCPL-2630 HCPL-0630
HCPL-2631 HCPL-0631
HCPL-4661 HCPL-0661

Features

- **Available in 8 Pin DIP and SOIC-8**
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2631/0631: 10,000 V/µs @ V_{CM} = 50 V
  HCPL-4661/0661: 15,000 V/µs @ V_{CM} = 1000 V
- **High Density Packaging**
- **Low Input Current Capability: 5 mA**
- **High Speed: 10 MBd**
- **LSTTL and TTL Compatible**
- **Guaranteed AC and DC Performance Over Temperature: -40°C to 85°C**
- **Recognized Under the Component Program of UL1577 (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vrms, 1 Minute**
- **5000 Vrms, 1 Minute (Option 020) (HCPL-2630/2631/4661)**
- **CSA Approved Under Component Acceptance Notice No. 5 (File No. CA 88324) (HCPL-2630/2631/4661)**
- **Hermetic Equivalent Device Available (HCPL-5630/31)**
- **Surface Mount Gull Wing Option Available for 8 Pin DIP (Option 300)**

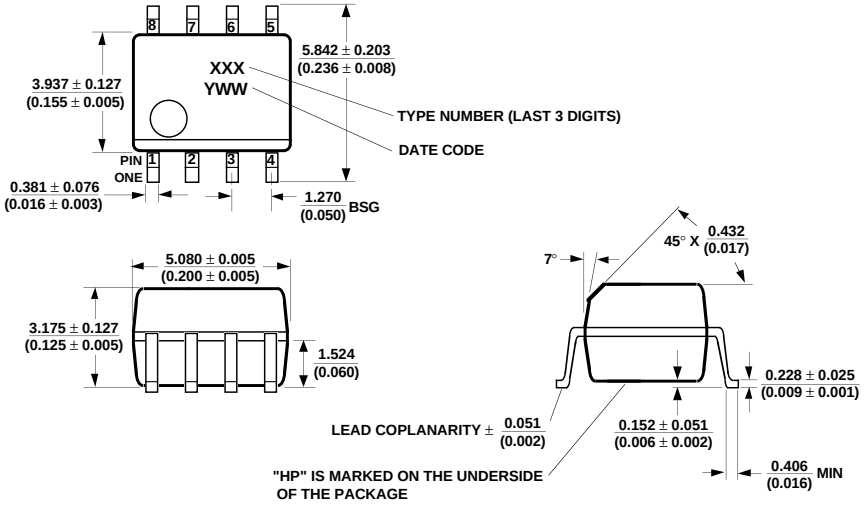
Outline Drawing - 8 Pin DIP



DIMENSIONS IN MILLIMETERS AND (INCHES).

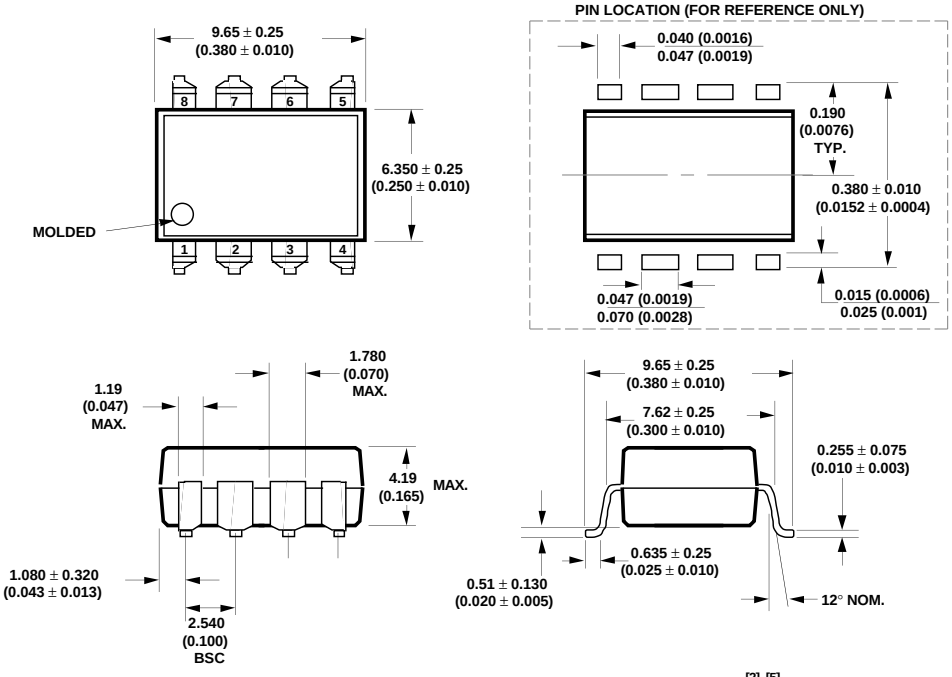
CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Outline Drawing - SO-8



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline Drawing - Option 300



DIMENSIONS IN mm (IN.)
TOLERANCES: xx.xx = 0.01
xx.xxx = 0.005
(unless otherwise specified)

LEAD COPLANARITY [2] [5]
MAXIMUM: 0.102 (0.004)

Description

These dual channel devices are optically coupled logic gates that combine GaAsP light emitting diodes and integrated high gain photodetectors. The photons are collected in the detector by a photodiode and the current is amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated. The internal shield provides a guaranteed common mode transient immunity specification of 5000 V/µs for the HCPL-2631/0631, and 10,000 V/µs for the HCPL-4661/0661.

These dual channel optocouplers are available in an 8 Pin DIP and in an industry standard SOIC-8 package. The following is a cross reference table listing the 8 Pin DIP part number and the electrically equivalent SOIC-8 part number.

8 Pin DIP	SOIC-8 Package
HCPL-2630	HCPL-0630
HCPL-2631	HCPL-0631
HCPL-4661	HCPL-0661

The SOIC-8 does not require “through holes” in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

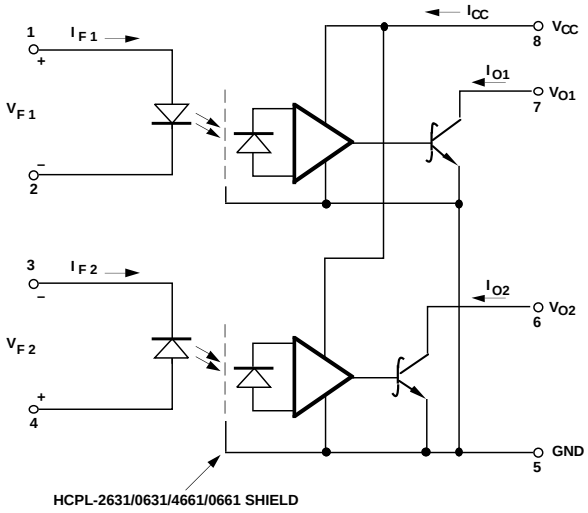
The unique design provides maximum ac and dc circuit isolation while achieving LSTTL and TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to +85°C. The dual channel design minimizes PCB space.

These devices are recommended for high speed logic interfacing, input/output buffering, and for use as line receivers in environments that conventional line receivers cannot tolerate. They can be used for the digital programming of machine control systems, motors and floating power supplies. The internal shield makes the HCPL-2631/0631/4661/0661 ideal for use in extremely high ground or induced noise environments.

Applications

- **Isolation of High Speed Logic Systems**
- **Microprocessor System Interfaces**
- **Isolated Line Receiver**
- **Computer-Peripheral Interfaces**
- **Ground Loop Elimination**
- **Digital Isolation for A/D, D/A Conversion**
- **Power Transistor Isolation in Motor Drives**

Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 1).

Recommended Operation Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}*	0	250	μA
Input Current, High Level Each Channel	I_{FH}	5	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (@ R_L = 1 kΩ) Each Channel	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω
Operating Temperature	T_A	-40	85	°C

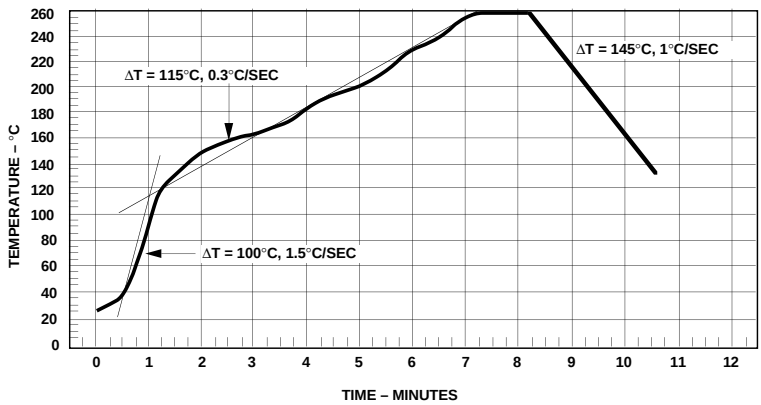
*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.

Absolute Maximum Ratings

(No Derating Required up to 85°C)
Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature (8 Pin DIP) ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current
(each channel, See note 2)..... 15 mA
Reverse Input Voltage (each channel) ..... 5 V
Supply Voltage – V_{CC} (1 Minute Maximum) ..... 7 V
Output Collector Current – I_O (each channel) ..... 50 mA
Output Collector Voltage – V_O (each channel)** ..... 7 V
Output Collector Power Dissipation (each channel) ..... 60 mW[17]
Infrared and Vapor Phase Reflow
Temperature (SOIC-8 & Option #300) ..... See Thermal Profile

**Selection for higher output voltages up to 20 V is available.

Thermal Profile



Maximum Solder Reflow Thermal Profile. (Note: Use of non-chlorine activated fluxes is highly recommended.)

Electrical Characteristics

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. (See note 1.)

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input Threshold Current	I_{TH}		2.5	5.0	mA	V_{CC} = 5.5 V, $I_O \geq$ 13 mA, V_O = 0.6 V	5, 15	
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA	2	3
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	3, 5, 6, 15	3
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC} = 5.5 V, I_F = 0 mA (Both Channels)		
Low Level Supply Current	I_{CCL}		13	21	mA	V_{CC} = 5.5 V, I_F = 10 mA (Both Channels)		
Input Forward Voltage	V_F	1.4	1.5	1.75	V	T_A = 25°C, I_F = 10 mA	4	3
		1.3		1.80				
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA,		3
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		3
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA	13	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min T_A = 25°C		4, 12
Opt. 020**	V_{ISO}	5000						4, 15
Input-Input Leakage Current	I_{I-I}		0.005		µA	RH ≤ 45% t = 5 s, V_{I-I} = 500 V		5
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω			5
Capacitance (Input-Input)	C_{I-I}		0.03**		pF	f = 1 MHz		5
			0.25***					
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	RH ≤ 45% V_{I-O} = 500 V, t = 5 s		3, 16
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		

*All typical values are at V_{CC} = 5 V, T_A = 25°C.
**For HCPL-2630/2631/4661 only.
***For HCPL-0630/0631/0661 only.

Switching Specifications

Over recommended temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75	ns	T_A = 25°C	R_L = 350 Ω C_L = 15 pF	7, 8, 9	3, 6
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75	ns	T_A = 25°C		7, 8, 9	3, 7
					100	ns				
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			3.5	35	ns			10	13
Propagation Delay Skew	t_{PSK}				40	ns				13,14
Output Rise Time (10-90%)	t_r			24		ns			11	3
Output Fall Time (90-10%)	t_f			10		ns			11	3
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	HCPL-2630/0630		10,000		V/µs	V_{CM} = 10 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	12	3, 8, 10
		HCPL-2631/0631	5,000	10,000			V_{CM} = 50 V			
		HCPL-4661/0661	10,000	15,000			V_{CM} = 1000 V			
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	HCPL-2630/0630		10,000		V/µs	V_{CM} = 10 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA T_A = 25°C	12	3, 9, 10
		HCPL-2631/0631	5,000	10,000			V_{CM} = 50 V			
		HCPL-4661/0661	10,000	15,000			V_{CM} = 1000 V			

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
10. For sinusoidal voltages, $(\lvert dV_{CM} \rvert/dt)_{max} = \pi f_{CM} V_{CM}(p\text{-}p)$.
11. As illustrated in Figure 15 the V_{CC} and GND traces can be located between the input and the output leads to provide additional noise immunity at the compromise of insulation capability.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for 1 second (Leakage detection current limit, $I_{I\text{-}O} \le 5$ µA).
13. See application section; “Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew” for more information.
14. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
15. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (Leakage detection current limit, $I_{I\text{-}O} \le 5$ µA). This option is valid for HCPL-2630/2631/4661 only.
16. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
17. Derate linearly above 80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.

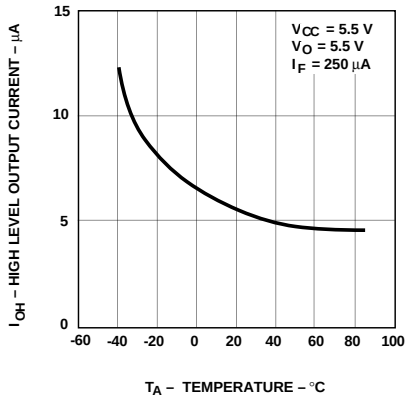


Figure 2. High Level Output Current vs. Temperature.

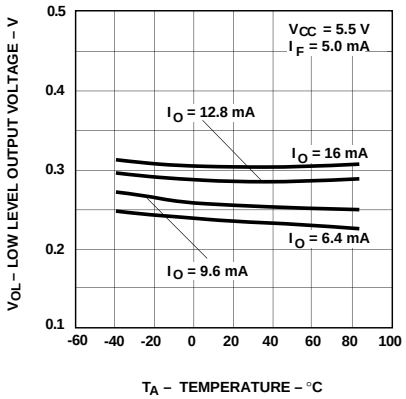


Figure 3. Low Level Output Voltage vs. Temperature.

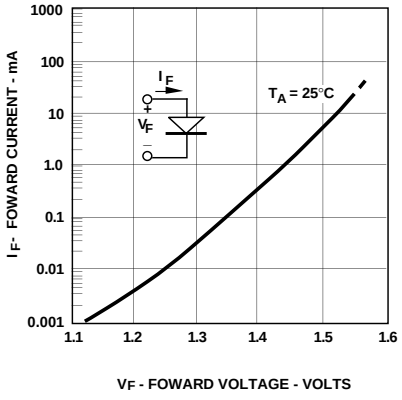


Figure 4. Input Diode Forward Characteristic.

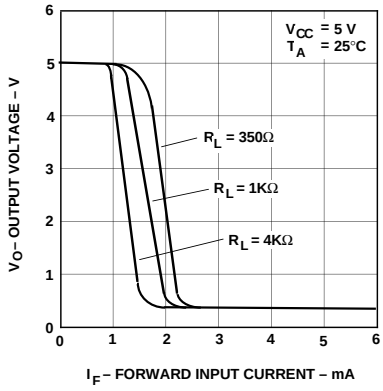


Figure 5. Output Voltage vs. Forward Input Current.

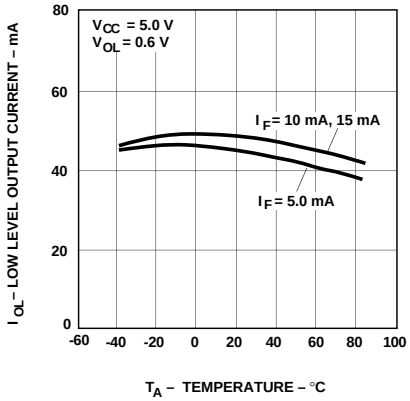


Figure 6. Low Level Output Current vs. Temperature.

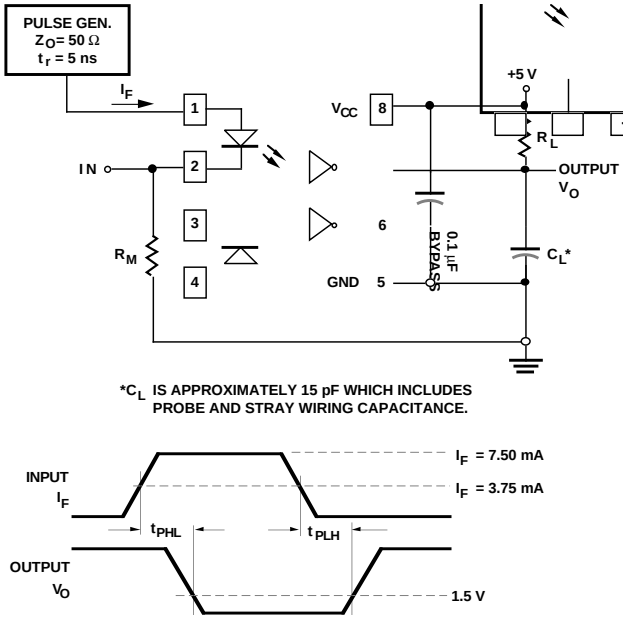


Figure 7. Test Circuit for t_{PHL} and t_{PLH} (See Note 3).

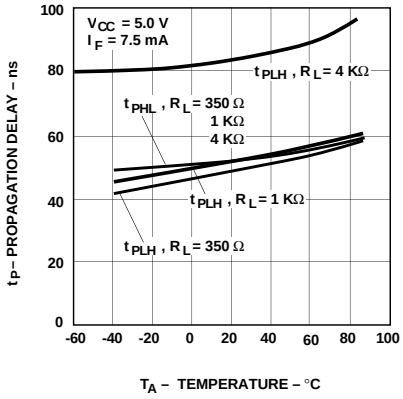


Figure 8. Propagation Delay vs. Temperature.

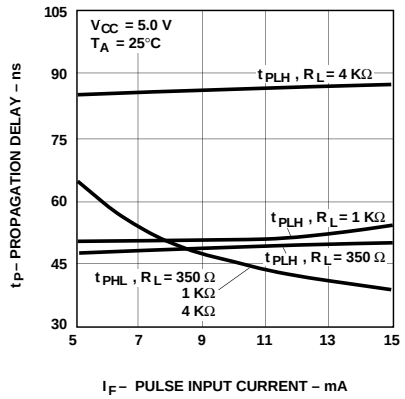


Figure 9. Propagation Delay vs. Pulse Input Current.

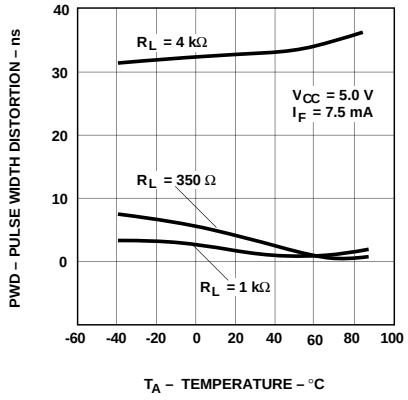


Figure 10. Pulse Width Distortion vs. Temperature.

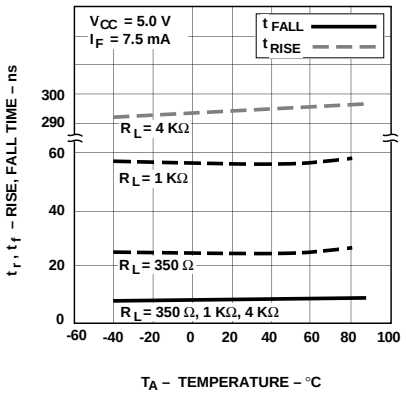


Figure 11. Rise and Fall Time vs. Temperature.

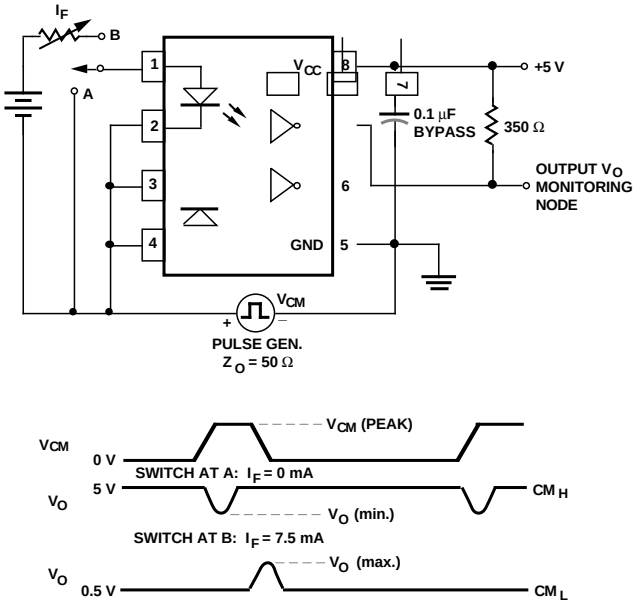


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

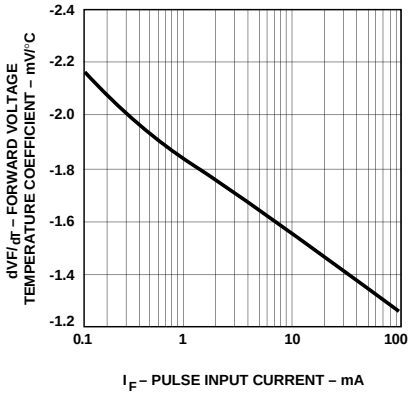
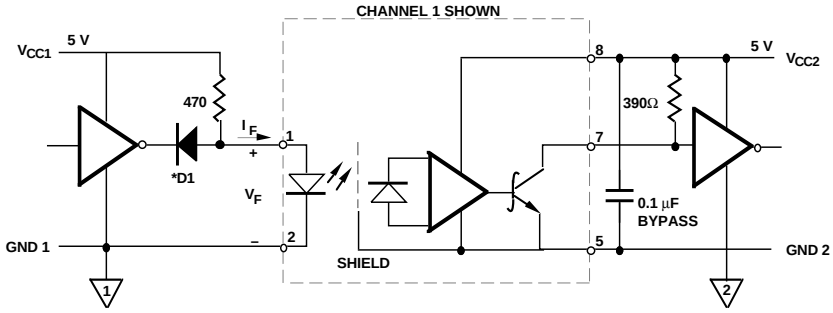


Figure 13. Temperature Coefficient of Forward Voltage vs. Input Current.



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 14. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.

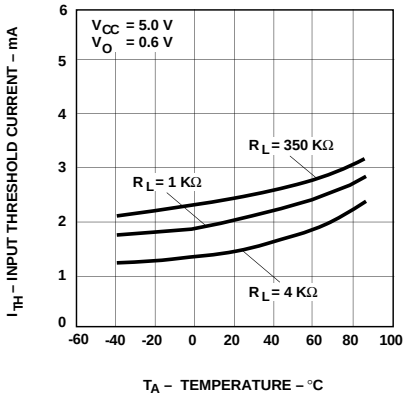


Figure 15. Input Threshold Current vs. Temperature.

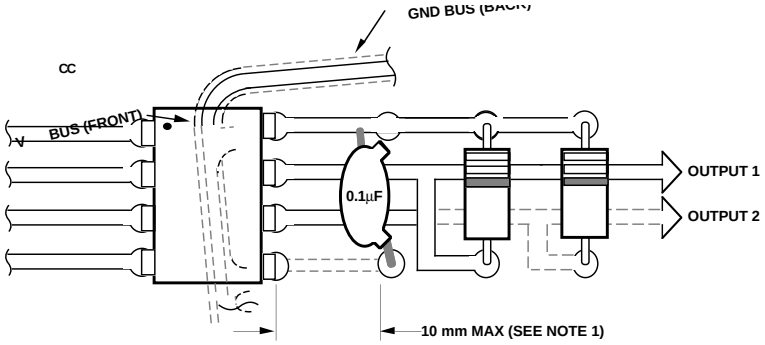


Figure 16. Recommended Printed Circuit Board Layout.

Insulation Related Specifications

Parameter	Symbol	DIP Value	SOIC-8 Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	≥4	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	≥4	mm	Measured from input terminals to output tminals
Min. Internal Plastic Gap (Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	200	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0110)		IIIa	IIIa		Material group (DIN VDE 0110)

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given

group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 17, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PHL} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 18 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 18 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

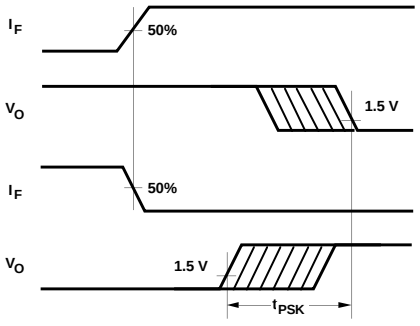


Figure 17. Illustration of Propagation Delay Skew - t_{PSK}.

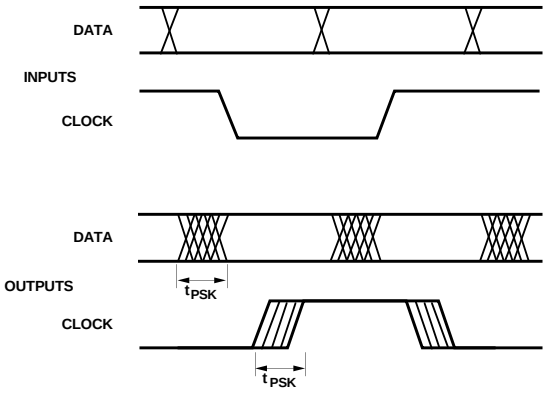


Figure 18. Parallel Data Transmission Example.

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Printed in U.S.A. Data Subject to Change Obsoletes 5954-1031 (1/86), 5954-0960 (12/83) 5091-9125E (12/93)