



# Z08617

## NMOS Z8® 8-BIT MCU KEYBOARD CONTROLLER

### FEATURES

- Low Power Consumption - 750 mW
- 32 Input/Output Lines
- Digital Inputs NMOS Levels with Internal Pull-Up Resistors
- 4 Kbytes ROM
- Four Direct Connect LED Drive Pins
- 124 Bytes of RAM
- Hardware Watch-Dog Timer (WDT)
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- On-Chip RC Oscillator
- Clock Frequency: Up to 5MHz
- Low EMI Emission

### GENERAL DESCRIPTION

The Z08617 Keyboard Controller is a member of the Z8® single-chip microcontroller family with 4 Kbytes of ROM. The device is housed in a 40-pin DIP package, and is manufactured in NMOS technology. The Z08617 microcontroller offers fast execution, efficient use of memory, sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z08617 architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z08617 provides 32 pins dedicated to input and output. These lines are grouped into four ports, each port consists of 8 lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z08617 offers low EMI emission which is achieved by means of several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces which are available to support this wide range of configurations: Program Memory and 124 General-Purpose Registers.

The Z08617 offers two on-chip counter/timers with a large number of user-selectable modes. This unburdens the program from coping with real-time problems such as counting/timing (Figure 1).

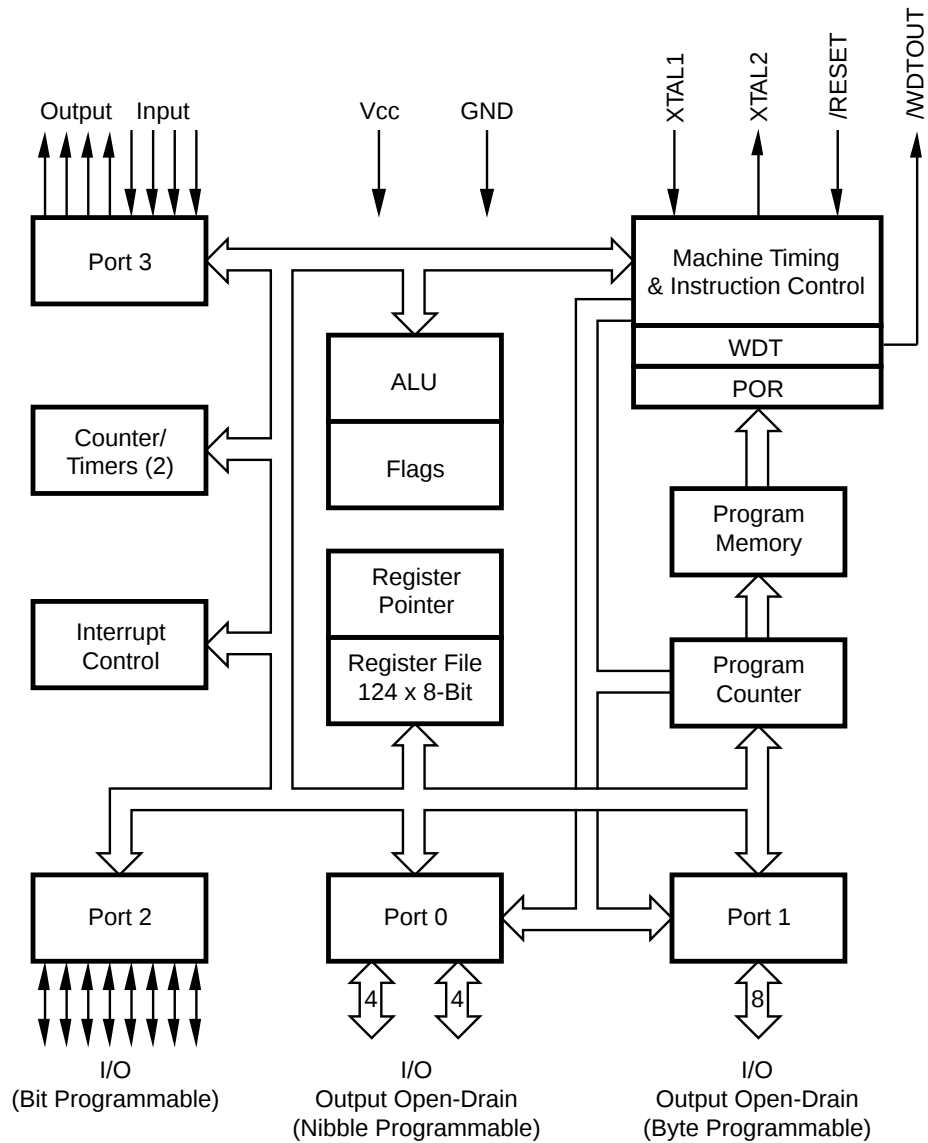
#### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

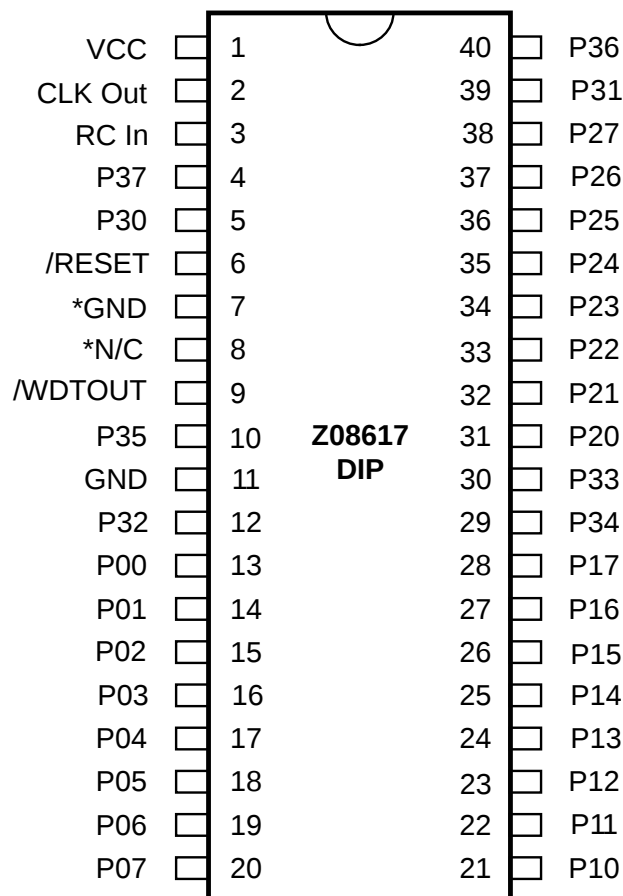
| Connection | Circuit  | Device   |
|------------|----------|----------|
| Power      | $V_{CC}$ | $V_{DD}$ |
| Ground     | GND      | $V_{SS}$ |

## GENERAL DESCRIPTION (Continued)



**Figure 1. Z08617 Functional Block Diagram**

## PIN IDENTIFICATION



### Note:

- \* Pin 8 is connected to the chip, although used only for testing. This pin **must** float. Pin 7 is a test pin and **must** be grounded.

Figure 2. 40-Pin DIP Pin Configuration

Table 1. 40-Pin DIP Pin Identification

| Pin # | Symbol          | Function        | Direction | Pin # | Symbol  | Function                     | Direction |
|-------|-----------------|-----------------|-----------|-------|---------|------------------------------|-----------|
| 1     | V <sub>CC</sub> | Power Supply    | Input     | 11    | GND     | Ground                       |           |
| 2     | CLK Out         | Clock Out       | Output    | 12    | P32     | Port 3, Pin 2                | Input     |
| 3     | RC In           | Z8 Clock        | Input     | 13-20 | P07-P00 | Port 0, Pins 0,1,2,3,4,5,6,7 | In/Output |
| 4     | P37             | Port 3, Pin 7   | Output    | 21-28 | P17-P10 | Port 1, Pins 0,1,2,3,4,5,6,7 | In/Output |
| 5     | P30             | Port 3, Pin 0   | Input     | 29    | P34     | Port 3, Pin 4                | Output    |
| 6     | /RESET          | Reset           | Input     | 30    | P33     | Port 3, Pin 3                | Input     |
| *7    | GND             | Ground          |           | 31-38 | P27-P20 | Port 2, Pins 0,1,2,3,4,5,6,7 | In/Output |
| *8    | N/C             | Not Connected   |           | 34-38 | P24-P20 | Port 2, Pins 0, 1, 2, 3, 4   | In/Output |
| 9     | /WDTOUT         | Watch-Dog Timer | Output    | 39    | P31     | Port 3, Pin 1                | Input     |
| 10    | P35             | Port 3, Pin 5   | Output    | 40    | P36     | Port 3, Pin 6                | Output    |

## ABSOLUTE MAXIMUM RATINGS

| Symbol    | Description       | Min  | Max  | Units |
|-----------|-------------------|------|------|-------|
| $V_{CC}$  | Supply Voltage*   | -0.3 | +7.0 | V     |
| $T_{STG}$ | Storage Temp      | -65  | +150 | C     |
| $T_A$     | Oper Ambient Temp | †    | †    |       |

### Notes:

\* Voltage on all pins with respect to GND.

† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 17).

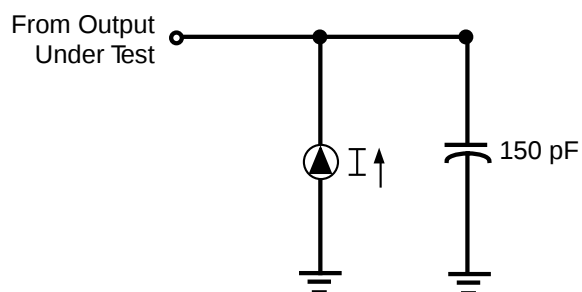


Figure 17. Test Load Diagram

## STANDARD TEST CONDITIONS

$T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ ,  $f = 1.0 \text{ MHz}$ , unmeasured pins returned to ground.

| Parameter          | Max   |
|--------------------|-------|
| Input capacitance  | 12 pF |
| Output capacitance | 12 pF |
| I/O capacitance    | 12 pF |

## DC CHARACTERISTICS

 $V_{CC} = 4.75V \text{ to } 5.25V @ 0^{\circ}C \text{ to } -55^{\circ}C$ 

| Sym      | Parameter                | Min  | Max      | Typ* | Unit    | Condition                                        |
|----------|--------------------------|------|----------|------|---------|--------------------------------------------------|
| $V_{IH}$ | Input High Voltage       | 2.0  | $V_{CC}$ |      | V       |                                                  |
| $V_{IL}$ | Input Low Voltage        | -0.3 | 0.8      |      | V       |                                                  |
| $V_{RH}$ | Reset Input High Voltage | 3.8  | $V_{CC}$ |      | V       |                                                  |
| $V_{RL}$ | Reset Input Low Voltage  | -0.3 | 0.8      |      | V       |                                                  |
| $V_{OH}$ | Output High Voltage      | 2.0  |          |      | V       | $I_{OH} = -250 \mu A$ (Port 2 only)              |
|          | Output High Voltage      | 2.4  |          |      | V       | $I_{OH} = -250 \mu A$ (Port 3 only)              |
| $V_{OL}$ | Output Low Voltage       |      | 0.8      |      | V       | $I_{OL} = 10.0 \text{ mA}$ (See note [1] below.) |
| $I_{IL}$ | Input Leakage            | -10  | 10       |      | $\mu A$ | $V_{IN} = 0V, 5.25V$ (See note [3] below.)       |
| $I_{OL}$ | Output Leakage           | -10  | 10       |      | $\mu A$ | $V_{IN} = 0V, 5.25V$ (See note [2] below.)       |
| $I_{IR}$ | Reset Input Current      | -335 | -775     | -477 | $\mu A$ | $V_{IN} = 0V, 5.25V$                             |
| $I_{R1}$ | Input Current            | -335 | -775     |      | $\mu A$ | Pull-up resistor=10.4 Kohms, $V_{IN}=0.0V$       |
| $I_{R2}$ | Input Current            | -1.6 | -2.9     |      | mA      | Pull-up resistor = 2.4 Kohms, $V_{IN}=0.0V$      |
| $I_{CC}$ | $V_{CC}$ Supply Current  |      | 160      |      | mA      |                                                  |
| WDT      | Watch-Dog Timer          |      | 2.0      |      | mA      | $V_{OL}=0.4 \text{ Volt}$                        |

### Notes:

\* Typical @ 25°C

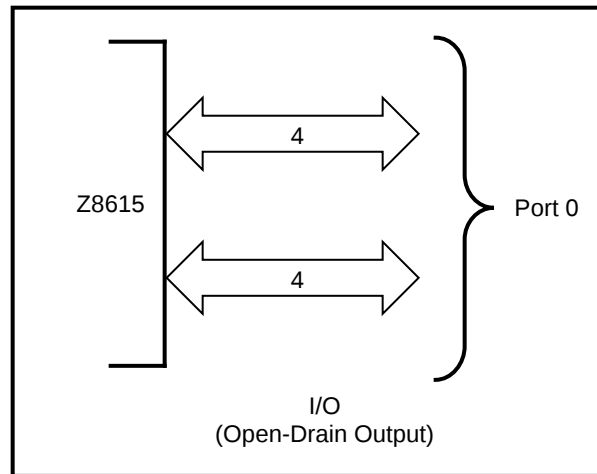
- [1] Ports P37-P34 may be used to sink 12 mA. These may be used for LEDs or as general-purpose outputs requiring high sink current.
- [2] P00-P07, P10-P17, P20-P25, P30-P33 as output mode open-drain as a logic one.
- [3] P00-P07, P10-P17, P20-P25, P30-P33 as output mode open-drain as a logic one.

## PIN FUNCTIONS

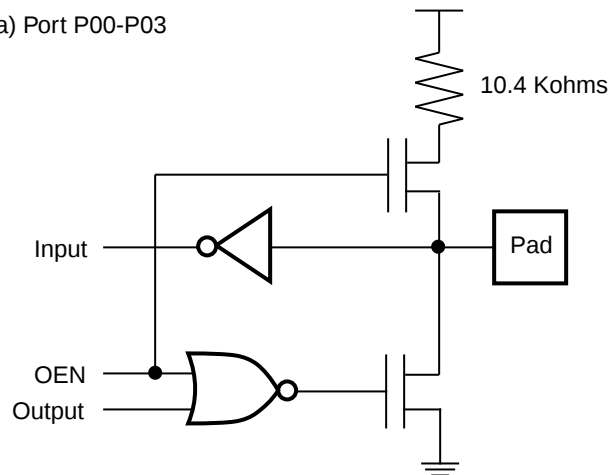
**RCIN** This pin is connected between a precision resistor on the power supply from the precision RC Oscillator.

**CLK Out** This pin is the system clock of the Z8 and runs at the frequency of the RC Oscillator. Any load on this pin will effect the RC Oscillator frequency.

**Port 0** (P07-P00). Port 0 is an 8-bit, nibble programmable, bi-directional, NMOS compatible I/O port. These eight I/O lines can be configured under software control as a nibble input port, or as a nibble open-drain output port. When used as an I/O port, inputs are standard NMOS (Figure 5). Port P03-P00 has 10.4 Kohms ( $\pm 35\%$ ) pull-up resistors when configured as inputs.



(a) Port P00-P03



(b) Port P04-P07

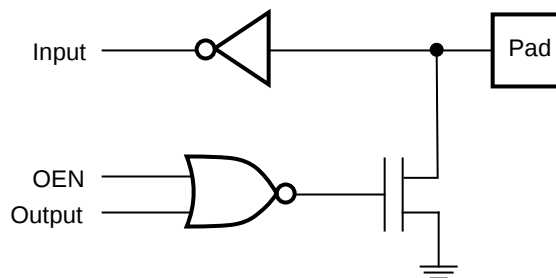
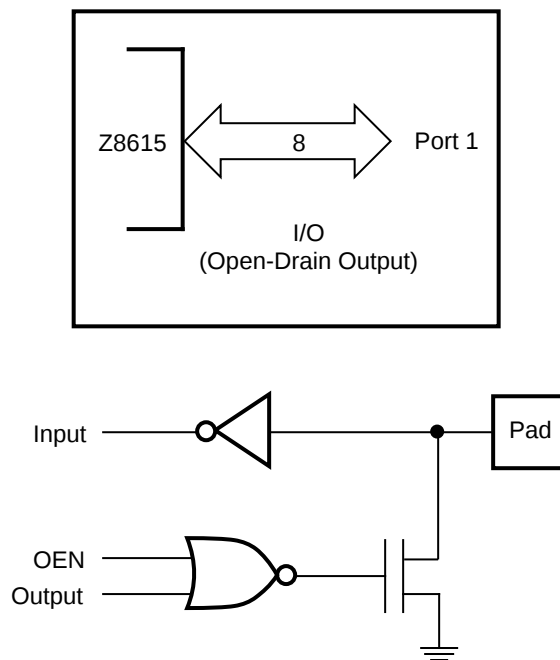


Figure 5. Port 0 Configuration

## PIN FUNCTIONS (Continued)

**Port 1** (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, NMOS compatible I/O port. These eight I/O lines are configured under software control program as a

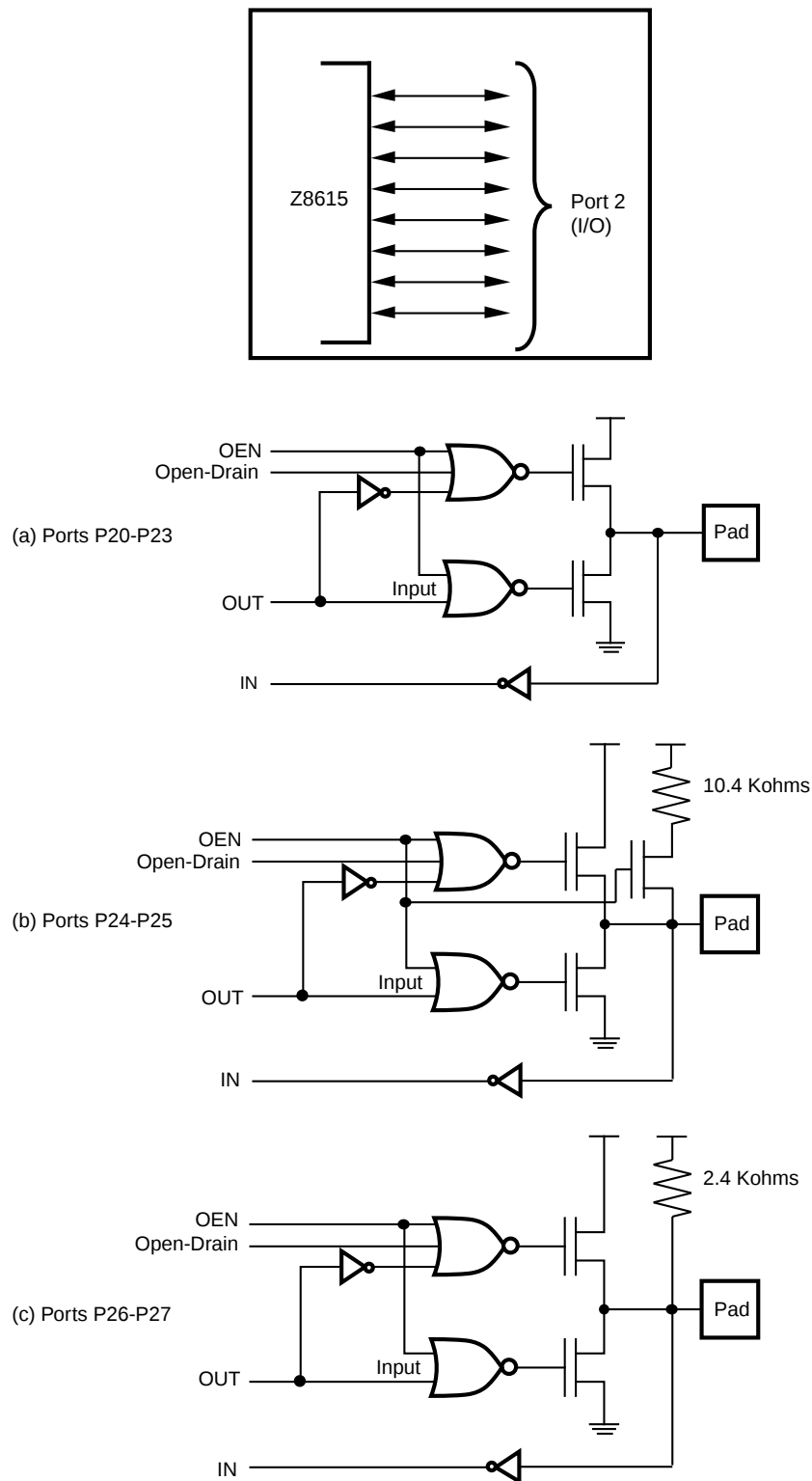
byte input port or as an open-drain output port. When used as an I/O port, inputs are standard NMOS (Figure 6).



**Figure 6. Port 1 Configuration**

**Port 2** (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, NMOS compatible I/O port. These eight I/O lines are configured under the software control program for I/O. Port 2 can be programmed as bit-by-bit independently, as input or output, or configured to provide open-

drain outputs (Figure 7). P26 and P27 have 2.4 Kohms ( $\pm 25\%$ ) pull-up resistors and are capable of sourcing 2.4 mA. P24 and P25 have 10.4 Kohms ( $\pm 35\%$ ) pull-up resistors when configured as inputs.



**Figure 7. Port 2 Configuration**

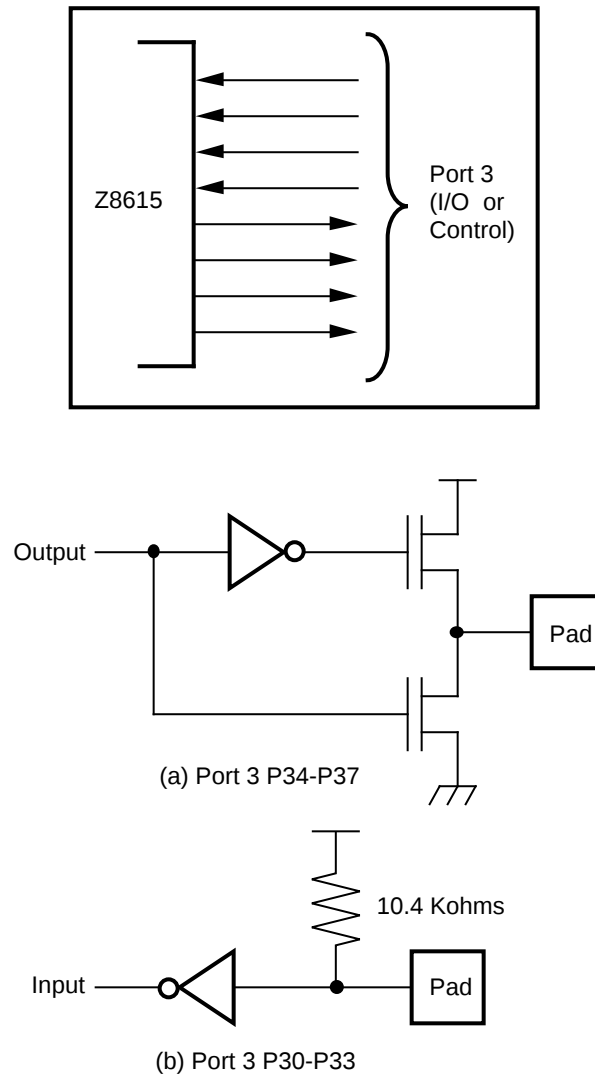
## PIN FUNCTIONS (Continued)

**Port 3** (P37-P30). Port 3 is an 8-bit, NMOS compatible four-fixed-input and four-fixed-output I/O port. These eight I/O lines have four-fixed-input (P33-P30) and four-fixed-output (P37-P34) ports. Port 3 inputs have 10.4 Kohms ( $\pm 35\%$ ) pull-up resistors and port 3 outputs are capable of driving up to four LEDs.

Port 3 is configured under software control to provide the following control functions: four external interrupt request signals (IRQ3-IRQ0); timer input and output

signals ( $T_{IN}$  and  $T_{OUT}$  - Figure 8).

**/RESET** (input, active Low). When activated, /RESET initializes the Z08617. When /RESET is deactivated, program execution begins from the internal program location at 000CH. Reset pin has a 10.4 Kohms pull-up resistor. Once this pin is pulled Low, it takes about 150 ms for microcon-troller initialization.



**Figure 8. Port 3 Configuration**

## FUNCTIONAL DESCRIPTION

The device incorporates special functions to enhance Zilog's Z8 applications as a keyboard controller, scientific research and advanced technologies applications.

**Program Memory.** The 16-bit program counter addresses 4 Kbytes of program memory space at internal locations (Figure 9).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have six 16-bit vectors that correspond to the six available interrupts.

Byte 12 to byte 4095 consists of on-chip, mask programmed ROM. Addresses 4096 and greater are reserved.

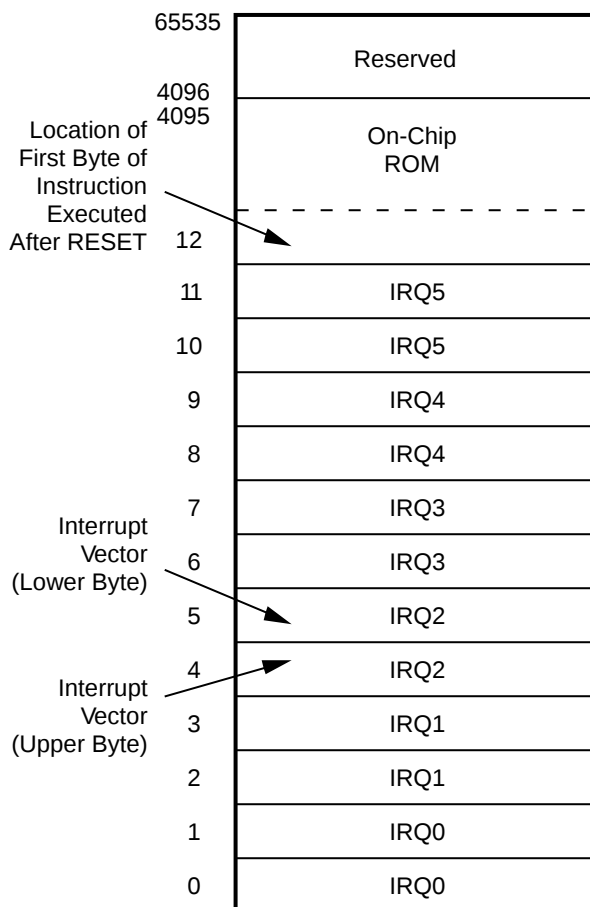


Figure 9. Program Memory Map

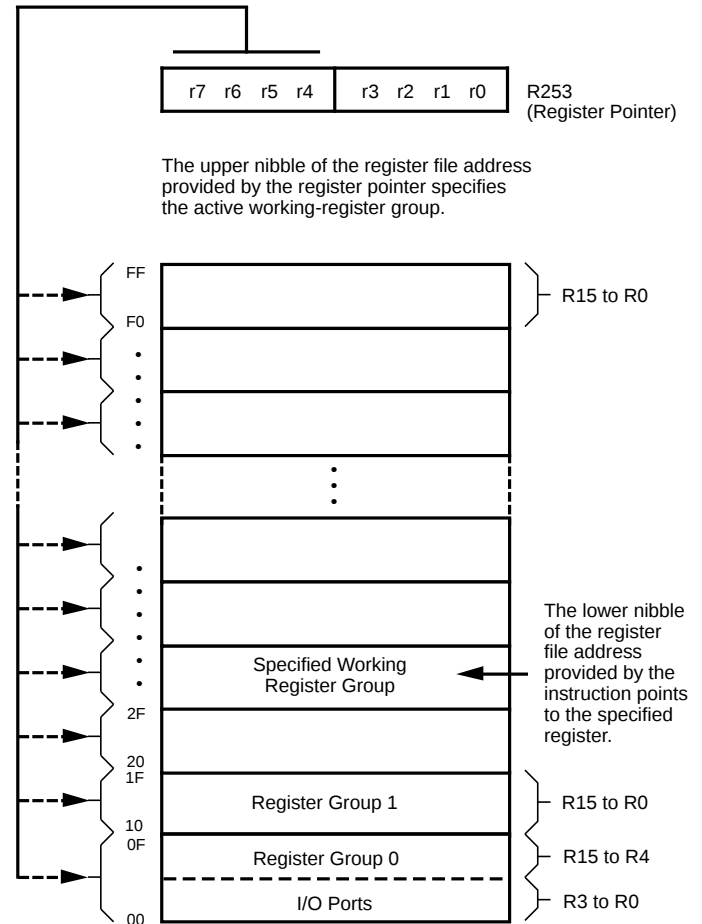
## FUNCTIONAL DESCRIPTION (Continued)

**Register File.** The register file (Figure 10) consists of four I/O port registers, 124 general-purpose registers and 16 control and status registers (R3-R0, R127-R4, and R255-R240, respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register

Pointer (Figure 11). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

| LOCATION |                                     | IDENTIFIERS |
|----------|-------------------------------------|-------------|
| R255     | Stack Pointer (Bits 7-0)            | SPL         |
| R254     | General-Purpose Register (Bits 7-0) | GPR         |
| R253     | Register Pointer                    | RP          |
| R252     | Program Control Flags               | FLAGS       |
| R251     | Interrupt Mask Register             | IMR         |
| R250     | Interrupt Request Register          | IRQ         |
| R249     | Interrupt Priority Register         | IPR         |
| R248     | Ports 1-0 Mode                      | P01M        |
| R247     | Port 3 Mode                         | P3M         |
| R246     | Port 2 Mode                         | P2M         |
| R245     | T0 Prescaler                        | PREQ        |
| R244     | Timer/Counter0                      | T0          |
| R243     | T1 Prescaler                        | PRE1        |
| R242     | Timer/Counter1                      | T1          |
| R241     | Timer Mode                          | TMR         |
| R240     | Reserved                            |             |
|          | Not Implemented                     |             |
| R127     | General-Purpose Registers           |             |
| R4       |                                     |             |
| R3       | Port 3                              | P3          |
| R2       | Port 2                              | P2          |
| R1       | Port 1                              | P1          |
| R0       | Port 0                              | P0          |

**Figure 10. Register File Configuration**



**Figure 11. Register Pointer Configuration**

**Stack.** The Z08617 internal register files are used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 124 general-purpose registers.

**Counter/Timers.** There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 12).

The 6-bit prescalers can further divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its own counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo- $n$  continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and are either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input as an external clock, a trigger input that can be retriggerable or non-triggerable, or as a gate input for the internal clock. The counter/timers can be programmable cascaded by connecting the T0 output to the input of T1. Port 3 lines P36 also serves as a timer output ( $T_{OUT}$ ) through which T0, T1 or the internal clock are output.

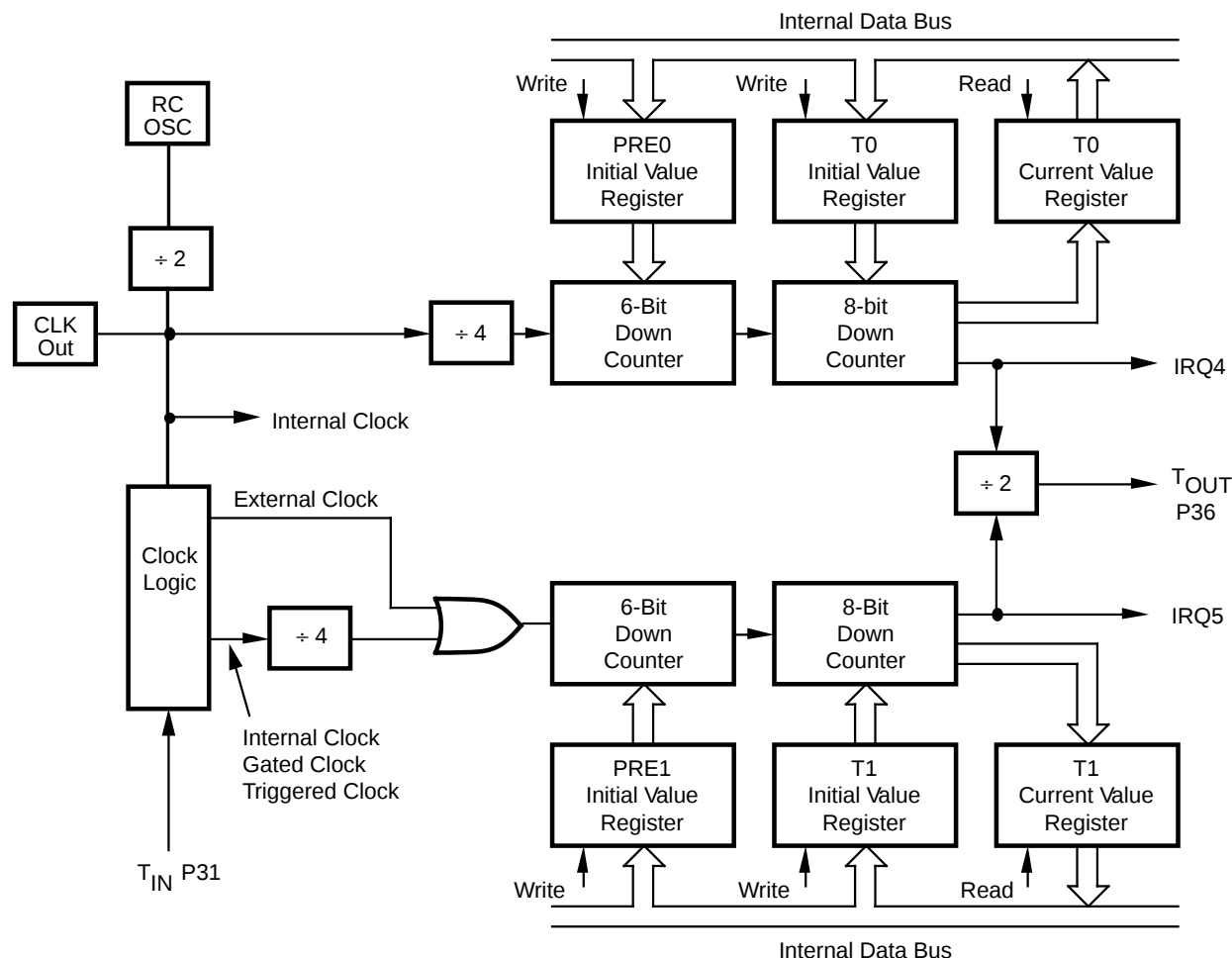


Figure 12. Counter/Timers Block Diagram

## FUNCTIONAL DESCRIPTION (Continued)

**Interrupts.** The Z08617 has six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 13). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two are claimed by the counter/timers. The Interrupt Masked Register globally or individually enables or disables the six interrupts requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an

interrupt request is granted. This disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.

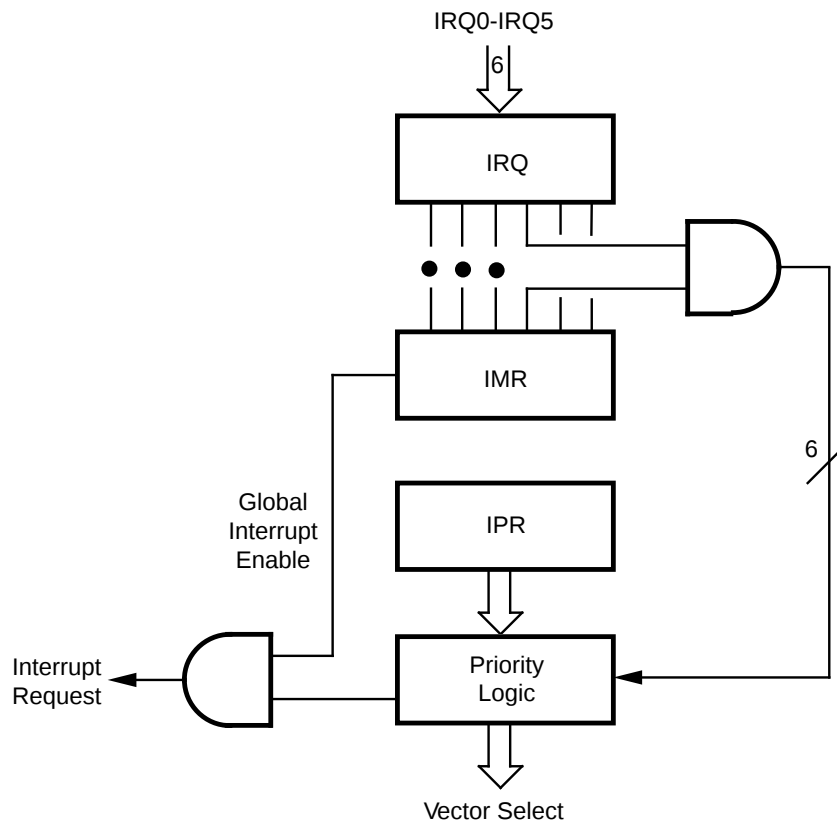
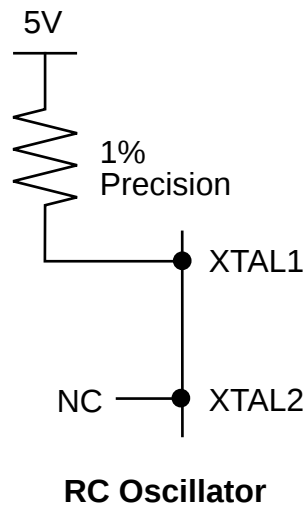


Figure 13. Interrupt Block Diagram

**RC Oscillator.** The Z08617 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor is necessary to achieve  $\pm 10\%$  accurate frequency oscillation.

**EMI.** The Z08617 offers low EMI emission due to circuit modifications to improve EMI performance. The internal divide-by-two circuit has been removed to improve EMI performance.



**Figure 14. Oscillator Configuration**

## FUNCTIONAL DESCRIPTION (Continued)

**Watch-Dog Timer.** The Z08617 is equipped with a hardware Watch-Dog Timer which will be turned on automatically by power-on (Figure 15). The Watch-Dog Timer must be refreshed at least once every 50 ms by executing the instruction WDT (Opcode = %5F), otherwise the Z08617 will reset itself if /WDTOUT pin 9 is connected to /RESET (Pin 6). Figure 16 shows the block diagram of WDT.

The Watch-Dog Timer is automatically enabled upon power-up of the microcontroller and /RESET going High. The /WDTOUT pin can be connected to the /RESET pin to provide an automatic reset upon WDT time-out. Dur-

ing WDT time-out, the /WDTOUT pin goes Low for approximately 8-15  $\mu$ s.

**WDT Hot Bit.** Bit 7 of the Interrupt Request Register (IRR register FAH) determines whether a hot start or cold start occurred. A cold start is defined as a reset occurring from the power-up of the Z08617 (bit 7 is set to zero upon power-up). A hot start occurs when a WDT time-out has occurred (bit 7 is set to 1). Bit 7 of the IRQ register is read-only and is automatically reset to 0 when accessed.

**Power-On Reset.** Upon power-up of the microcontroller, a reset condition is enabled. A delay of 150 ms  $\pm$ 20% is used to assist in initializing the microcontroller.

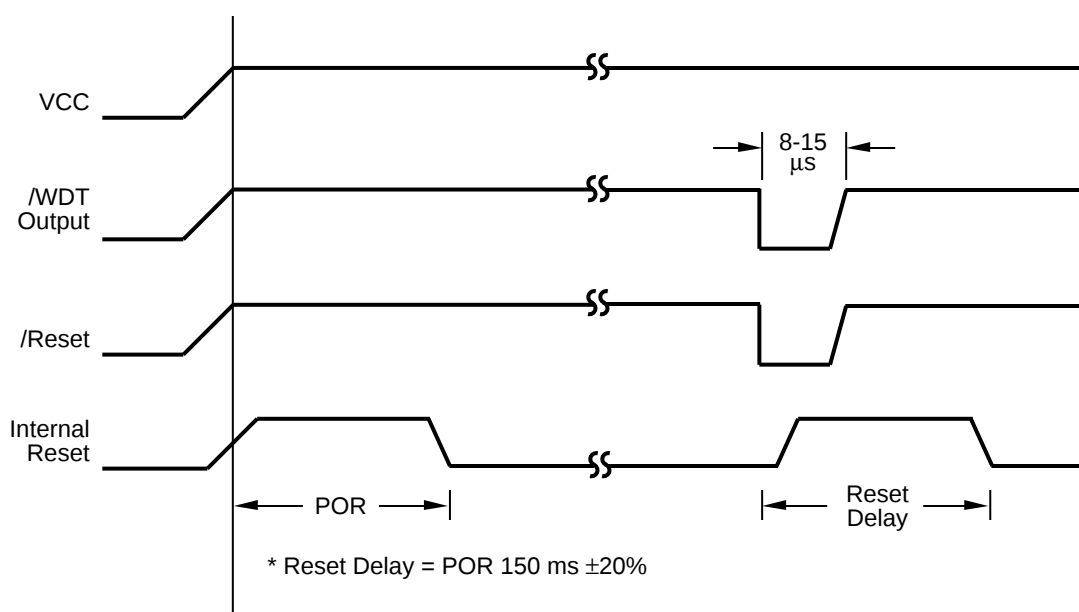


Figure 15. WDT Turn-On Timing After Reset

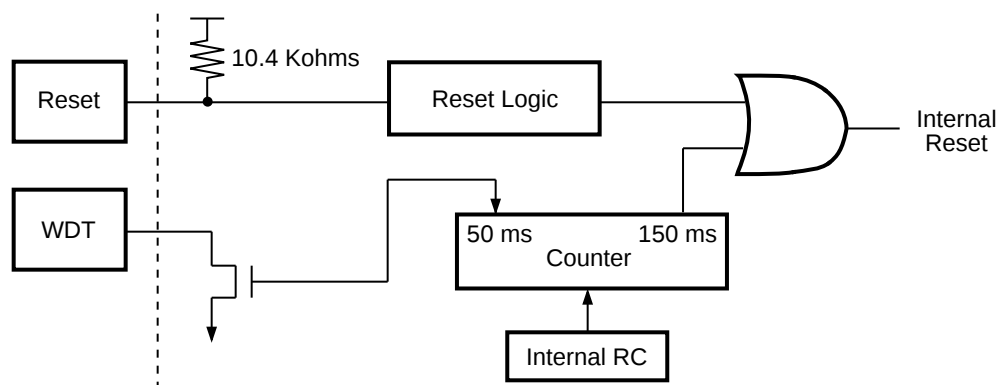
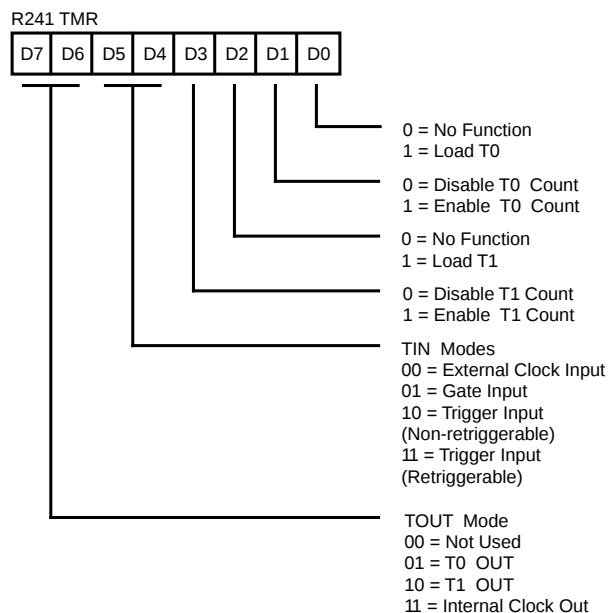
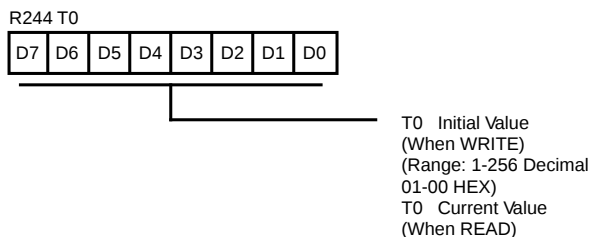


Figure 16. WDT Block Diagram

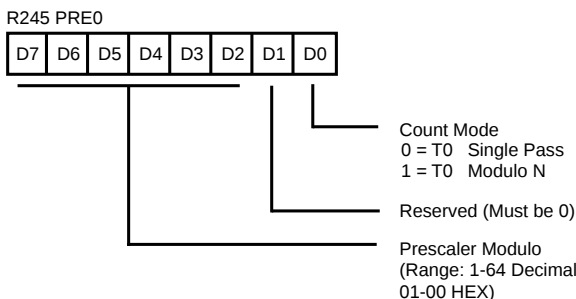
## Z8® CONTROL REGISTER DIAGRAMS



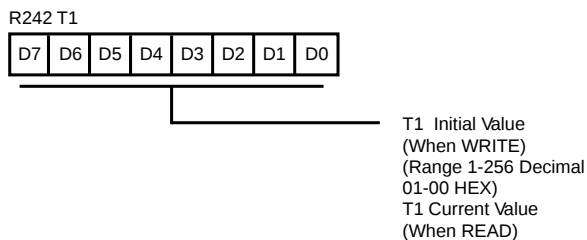
**Figure 18. Timer Mode Register (F1H: Read/Write)**



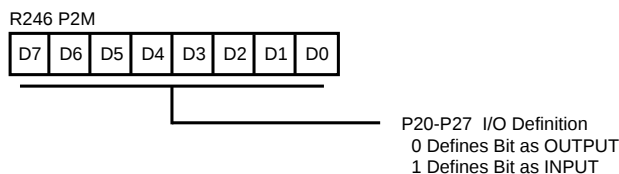
**Figure 21. Counter/Timer 0 Register (F4H: Read/Write)**



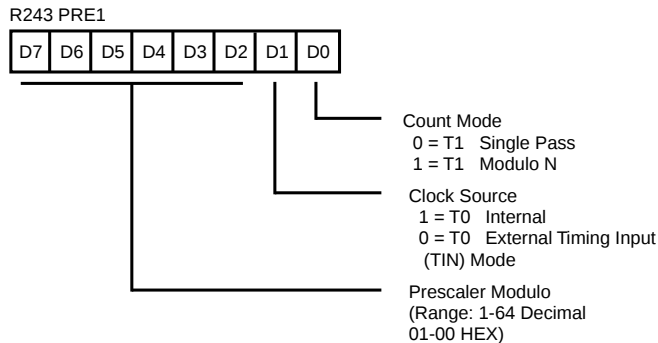
**Figure 22. Prescaler 0 Register (F5H: Write Only)**



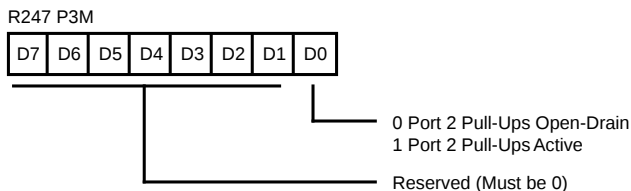
**Figure 19. Counter Timer 1 Register (F2H: Read/Write)**



**Figure 23. Port 2 Mode Register (F6H: Write Only)**



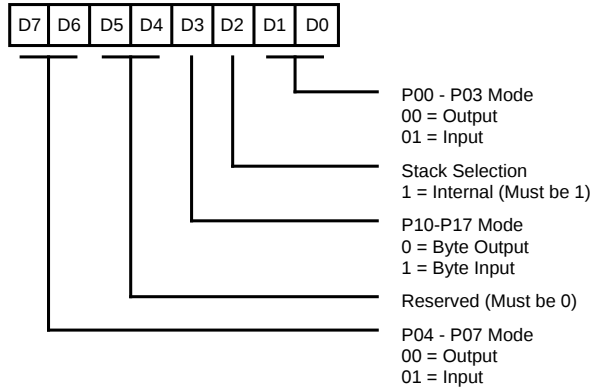
**Figure 20. Prescaler 1 Register (F3H: Write Only)**



**Figure 24. Port 3 Mode Register (F7H: Write Only)**

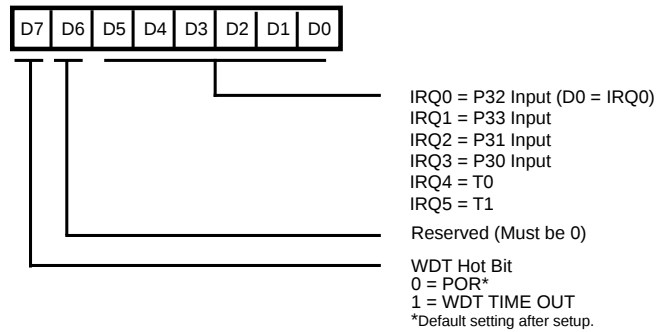
## Z8® CONTROL REGISTER DIAGRAMS (Continued)

R248 P01M



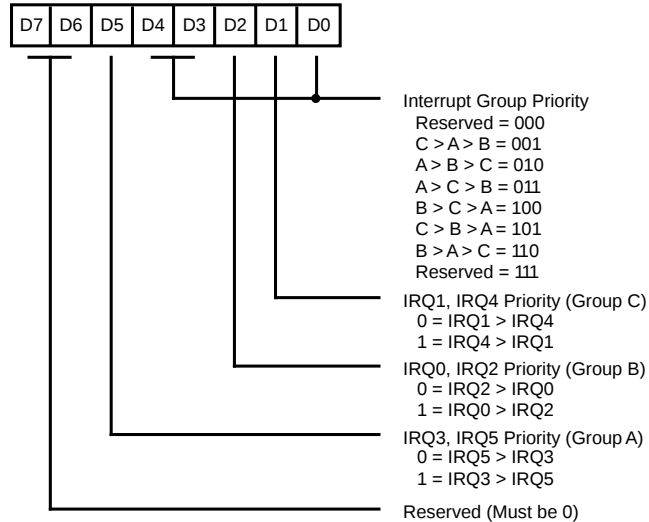
**Figure 25. Port 0 and 1 Mode Register**  
(F8H: Write Only)

R250 IRQ



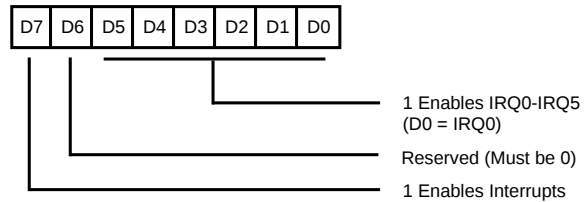
**Figure 27. Interrupt Request Register**  
(FAH: Read/Write)

R249 IPR



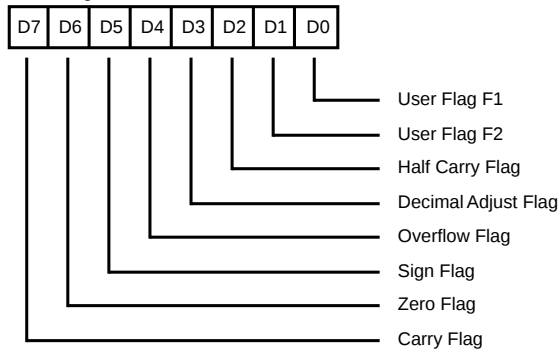
**Figure 26. Interrupt Priority Register**  
(F9H: Write Only)

R251 IMR



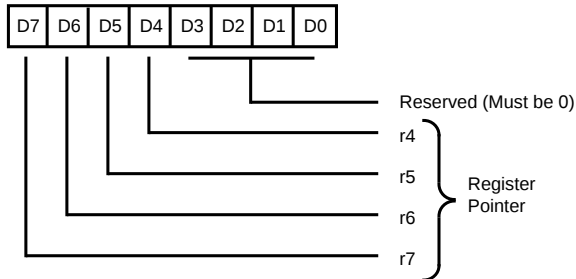
**Figure 28. Interrupt Mask Register**  
(FBH: Read/Write)

R252 Flags



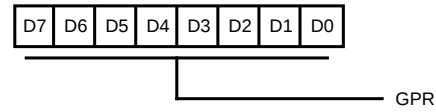
**Figure 29. Flag Register**  
(FCH: Read/Write)

R253 RP



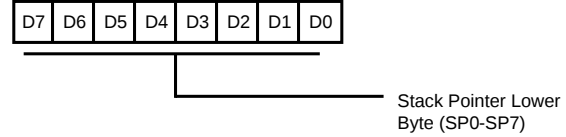
**Figure 30. Register Pointer**  
(FDH: Read/Write)

R254 GPR



**Figure 31. General-Purpose Register**  
(FEH: Read/Write)

R255 SPL



**Figure 32. Stack Pointer**  
(FFH: Read/Write)

## INSTRUCTION SET NOTATION

**Addressing Modes.** The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

| Symbol | Meaning                                                          |
|--------|------------------------------------------------------------------|
| IRR    | Indirect register pair or indirect working-register pair address |
| Irr    | Indirect working-register pair only                              |
| X      | Indexed address                                                  |
| DA     | Direct address                                                   |
| RA     | Relative address                                                 |
| IM     | Immediate                                                        |
| R      | Register or working-register address                             |
| r      | Working-register address only                                    |
| IR     | Indirect-register or indirect working-register address           |
| Ir     | Indirect working-register address only                           |
| RR     | Register pair or working register pair address                   |

**Symbols.** The following symbols are used in describing the instruction set.

| Symbol | Meaning                              |
|--------|--------------------------------------|
| dst    | Destination location or contents     |
| src    | Source location or contents          |
| cc     | Condition code                       |
| @      | Indirect address prefix              |
| SP     | Stack Pointer                        |
| PC     | Program Counter                      |
| FLAGS  | Flag register (Control Register 252) |
| RP     | Register Pointer (R253)              |
| IMR    | Interrupt mask register (R251)       |

**Flags.** Control register (R252) contains the following six flags:

| Symbol                           | Meaning                             |
|----------------------------------|-------------------------------------|
| C                                | Carry flag                          |
| Z                                | Zero flag                           |
| S                                | Sign flag                           |
| V                                | Overflow flag                       |
| D                                | Decimal-adjust flag                 |
| H                                | Half-carry flag                     |
| Affected flags are indicated by: |                                     |
| 0                                | Clear to zero                       |
| 1                                | Set to one                          |
| *                                | Set to clear according to operation |
| -                                | Unaffected                          |
| x                                | Undefined                           |

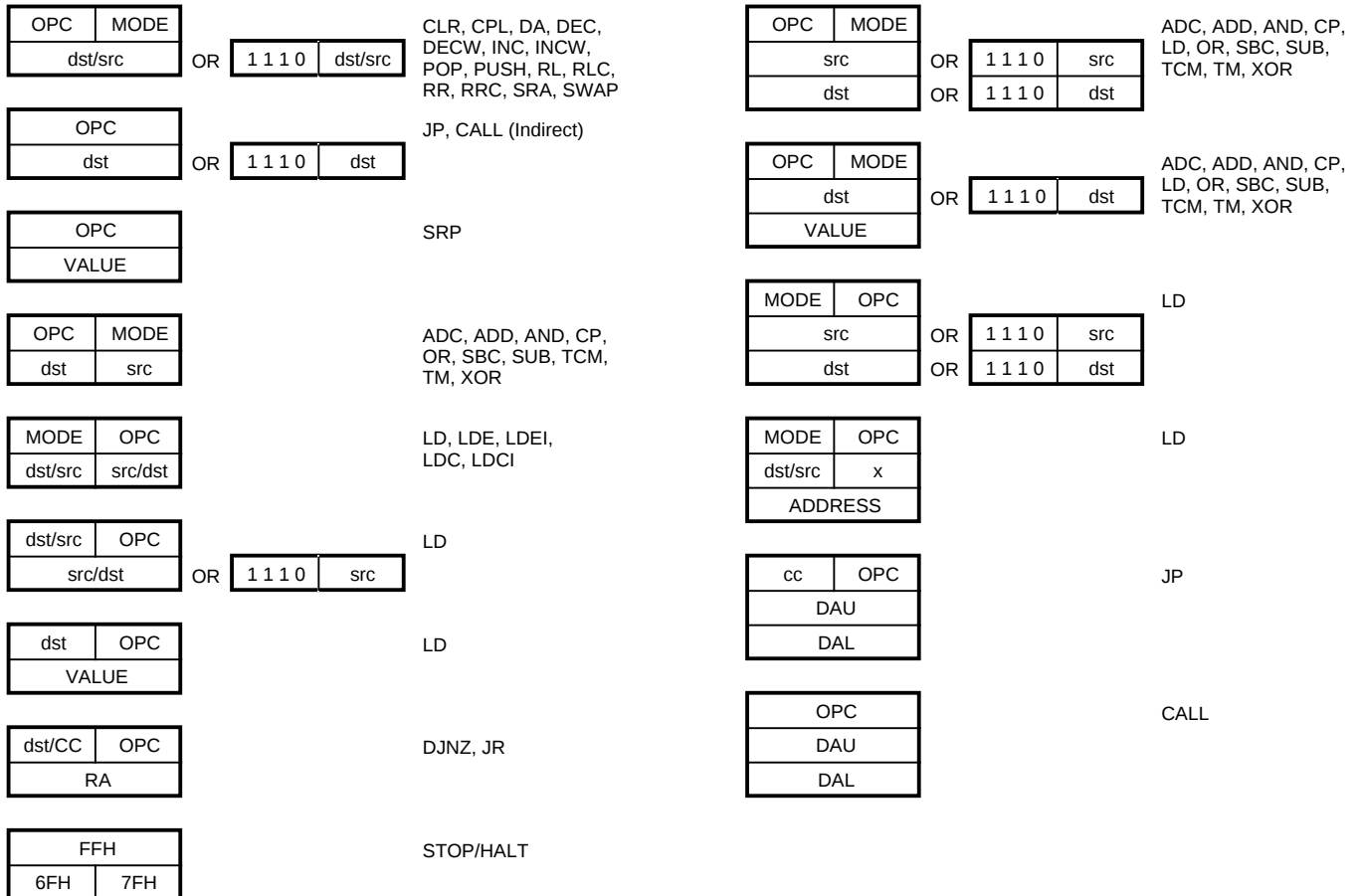
## CONDITION CODES

| Value | Mnemonic | Meaning                        | Flags Set             |
|-------|----------|--------------------------------|-----------------------|
| 1000  | —        | Always True                    | —                     |
| 0111  | C        | Carry                          | C = 1                 |
| 1111  | NC       | No Carry                       | C = 0                 |
| 0110  | Z        | Zero                           | Z = 1                 |
| 1110  | NZ       | Not Zero                       | Z = 0                 |
| 1101  | PL       | Plus                           | S = 0                 |
| 0101  | MI       | Minus                          | S = 1                 |
| 0100  | OV       | Overflow                       | V = 1                 |
| 1100  | NOV      | No Overflow                    | V = 0                 |
| 0110  | EQ       | Equal                          | Z = 1                 |
| 1110  | NE       | Not Equal                      | Z = 0                 |
| 1001  | GE       | Greater Than or Equal          | (S XOR V) = 0         |
| 0001  | LT       | Less than                      | (S XOR V) = 1         |
| 1010  | GT       | Greater Than                   | [Z OR (S XOR V)] = 0  |
| 0010  | LE       | Less Than or Equal             | [Z OR (S XOR V)] = 1  |
| 1111  | UGE      | Unsigned Greater Than or Equal | C = 0                 |
| 0111  | ULT      | Unsigned Less Than             | C = 1                 |
| 1011  | UGT      | Unsigned Greater Than          | (C = 0 AND Z = 0) = 1 |
| 0011  | ULE      | Unsigned Less Than or Equal    | (C OR Z) = 1          |
| 0000  | F        | Never True (Always False)      | —                     |

## INSTRUCTION FORMATS



### One-Byte Instructions



### Two-Byte Instructions

### Three-Byte Instructions

## INSTRUCTION SUMMARY

**Note:** Assignment of a value is indicated by the symbol “←”. For example:

dst ← dst + src

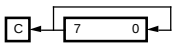
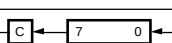
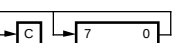
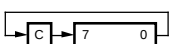
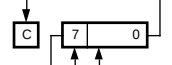
indicates that the source data is added to the destination data and the result is stored in the destination location. The notation “addr (n)” is used to refer to bit (n) of a given operand location.

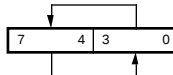
## INSTRUCTION SUMMARY (Continued)

| Instruction<br>and Operation                                                     | Address<br>Mode |     | Opcode<br>Byte (Hex) | Flags<br>Affected |   |   |   |   |   |  |
|----------------------------------------------------------------------------------|-----------------|-----|----------------------|-------------------|---|---|---|---|---|--|
|                                                                                  | dst             | src |                      | C                 | Z | S | V | D | H |  |
| <b>ADC</b> dst, src<br>dst ← dst + src + C                                       | †               |     | 1[ ]                 | *                 | * | * | * | 0 | * |  |
| <b>ADD</b> dst, src<br>dst ← dst + src                                           | †               |     | 0[ ]                 | *                 | * | * | * | 0 | * |  |
| <b>AND</b> dst, src<br>dst ← dst AND src                                         | †               |     | 5[ ]                 |                   | * | * | 0 | - | - |  |
| <b>CALL</b> dst<br>SP ← SP - 2<br>@SP ← PC,<br>PC ← dst                          | DA<br>IRR       |     | D6<br>D4             | -                 | - | - | - | - | - |  |
| <b>CCF</b><br>C ← NOT C                                                          |                 |     | EF                   | *                 | - | - | - | - | - |  |
| <b>CLR</b> dst<br>dst ← 0                                                        | R<br>IR         |     | B0<br>B1             | -                 | - | - | - | - | - |  |
| <b>COM</b> dst<br>dst ← NOT dst                                                  | R<br>IR         |     | 60<br>61             | -                 | * | * | 0 | - | - |  |
| <b>CP</b> dst, src<br>dst - src                                                  | †               |     | A[ ]                 | *                 | * | * | * | - | - |  |
| <b>DA</b> dst<br>dst ← DA dst                                                    | R<br>IR         |     | 40<br>41             | *                 | * | * | X | - | - |  |
| <b>DEC</b> dst<br>dst ← dst - 1                                                  | R<br>IR         |     | 00<br>01             | -                 | * | * | * | - | - |  |
| <b>DECW</b> dst<br>dst ← dst - 1                                                 | RR<br>IR        |     | 80<br>81             | -                 | * | * | * | - | - |  |
| <b>DI</b><br>IMR(7) ← 0                                                          |                 |     | 8F                   | -                 | - | - | - | - | - |  |
| <b>DJNZ</b> r, dst<br>r ← r - 1<br>if r ≠ 0<br>PC ← PC + dst<br>Range: +127,-128 | RA              |     | rA<br>r = 0 - F      | -                 | - | - | - | - | - |  |
| <b>EI</b><br>IMR(7) ← 1                                                          |                 |     | 9F                   | -                 | - | - | - | - | - |  |

| Instruction<br>and Operation                                                          | Address<br>Mode                                             |                                                                   | Opcode<br>Byte (Hex)                                                              | Flags<br>Affected |   |   |   |   |   |  |
|---------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------------|-----------------------------------------------------------------------------------|-------------------|---|---|---|---|---|--|
|                                                                                       | dst                                                         | src                                                               |                                                                                   | C                 | Z | S | V | D | H |  |
| <b>INC</b> dst<br>dst ← dst + 1                                                       | r<br>R<br>IR                                                |                                                                   | rE<br>r = 0 - F<br>20<br>21                                                       | -                 | * | * | * | - | - |  |
| <b>INCW</b> dst<br>dst ← dst + 1                                                      | RR<br>IR                                                    |                                                                   | A0<br>A1                                                                          | -                 | * | * | * | - | - |  |
| <b>IRET</b><br>FLAGS ← @SP;<br>SP ← SP + 1<br>PC ← @SP;<br>SP ← SP + 2;<br>IMR(7) ← 1 |                                                             |                                                                   | BF                                                                                | *                 | * | * | * | * | * |  |
| <b>JP</b> cc, dst<br>if cc is true<br>PC ← dst                                        | DA<br>IRR                                                   |                                                                   | CD<br>C = 0 - F<br>30                                                             | -                 | - | - | - | - | - |  |
| <b>JR</b> cc, dst<br>if cc is true,<br>PC ← PC + dst<br>Range: +127,-128              | RA                                                          |                                                                   | CB<br>C = 0 - F                                                                   | -                 | - | - | - | - | - |  |
| <b>LD</b> dst, src<br>dst ← src                                                       | r<br>r<br>R<br>r<br>X<br>r<br>Ir<br>R<br>R<br>R<br>IR<br>IR | Im<br>R<br>r<br>X<br>r<br>Ir<br>r<br>R<br>R<br>R<br>IM<br>IM<br>R | rC<br>r8<br>r9<br>r = 0 - F<br>C7<br>D7<br>E3<br>F3<br>E4<br>E5<br>E6<br>E7<br>F5 | -                 | - | - | - | - | - |  |
| <b>LDC</b> dst, src                                                                   | r                                                           | lrr                                                               | C2                                                                                | -                 | - | - | - | - | - |  |
| <b>LDCI</b> dst, src<br>dst ← src<br>r ← r + 1;<br>rr ← rr + 1                        | lr                                                          | lrr                                                               | C3                                                                                | -                 | - | - | - | - | - |  |

# INSTRUCTION SUMMARY (Continued)

| Instruction<br>and Operation                                                                          | Address<br>Mode |         | Opcode<br>Byte<br>(Hex) | Flags<br>Affected |   |   |   |   |   |   |
|-------------------------------------------------------------------------------------------------------|-----------------|---------|-------------------------|-------------------|---|---|---|---|---|---|
|                                                                                                       | dst             | src     |                         |                   | C | Z | S | V | D | H |
| <b>NOP</b>                                                                                            |                 |         | FF                      |                   | - | - | - | - | - | - |
| <b>OR</b> dst, src<br>dst ← dst OR src                                                                | †               |         | 4[ ]                    |                   | - | * | * | 0 | - | - |
| <b>POP</b> dst<br>dst ← @SP;<br>SP ← SP + 1                                                           | R<br>IR         |         | 5 0<br>5 1              |                   | - | - | - | - | - | - |
| <b>PUSH</b> src<br>SP ← SP - 1;<br>@SP ← src                                                          |                 | R<br>IR | 7 0<br>7 1              |                   | - | - | - | - | - | - |
| <b>RCF</b><br>C ← 0                                                                                   |                 |         | CF                      |                   | 0 | - | - | - | - | - |
| <b>RET</b><br>PC ← @SP;<br>SP ← SP + 2                                                                |                 |         | AF                      |                   | - | - | - | - | - | - |
| <b>RL</b> dst<br>  | R<br>IR         |         | 9 0<br>9 1              |                   | * | * | * | * | - | - |
| <b>RLC</b> dst<br> | R<br>IR         |         | 1 0<br>1 1              |                   | * | * | * | * | - | - |
| <b>RR</b> dst<br>  | R<br>IR         |         | E 0<br>E 1              |                   | * | * | * | * | - | - |
| <b>RRC</b> dst<br> | R<br>IR         |         | C 0<br>C 1              |                   | * | * | * | * | - | - |
| <b>SBC</b> dst, src<br>dst ← dst — src - C                                                            | †               |         | 3[ ]                    |                   | * | * | * | * | 1 | * |
| <b>SCF</b><br>C ← 1                                                                                   |                 |         | DF                      |                   | 1 | - | - | - | - | - |
| <b>SRA</b> dst<br> | R<br>IR         |         | D 0<br>D 1              |                   | * | * | * | 0 | - | - |
| <b>SRP</b> src<br>RP ← src                                                                            |                 | Im      | 3 1                     |                   | - | - | - | - | - | - |

| Instruction<br>and Operation                                                                          | Address<br>Mode |     | Opcode<br>Byte<br>(Hex) | Flags<br>Affected |   |   |   |   |   |   |
|-------------------------------------------------------------------------------------------------------|-----------------|-----|-------------------------|-------------------|---|---|---|---|---|---|
|                                                                                                       | dst             | src |                         |                   | C | Z | S | V | D | H |
| <b>SUB</b> dst, src<br>dst ← dst - src                                                                | †               |     | 2[ ]                    |                   | [ | [ | [ | [ | 1 | [ |
| <b>SWAP</b> dst<br> | R<br>IR         |     | F 0<br>F 1              |                   | X | * | * | X | - | - |
| <b>TCM</b> dst, src<br>(NOT dst)<br>AND src                                                           | †               |     | 6[ ]                    |                   | - | * | * | 0 | - | - |
| <b>TM</b> dst, src<br>dst AND src                                                                     | †               |     | 7[ ]                    |                   | - | * | * | 0 | - | - |
| <b>WDT</b>                                                                                            |                 |     | 5F                      |                   | - | X | X | X | - | - |
| <b>XOR</b> dst, src<br>dst ← dst XOR src                                                              | †               |     | B[ ]                    |                   | - | * | * | 0 | - | - |

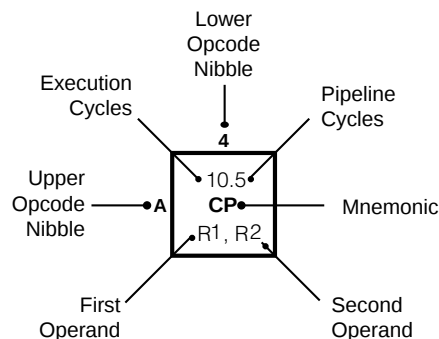
† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

| Address Mode |     | Lower<br>Opcode Nibble |
|--------------|-----|------------------------|
| dst          | src |                        |
| r            | r   | [2]                    |
| r            | Ir  | [3]                    |
| R            | R   | [4]                    |
| R            | IR  | [5]                    |
| R            | IM  | [6]                    |
| IR           | IM  | [7]                    |

# OPCODE MAP

|                    |   | Lower Nibble (Hex)    |                        |                         |                           |                       |                        |                       |                        |                       |                     |                           |                         |                     |                         |                  |              |            |
|--------------------|---|-----------------------|------------------------|-------------------------|---------------------------|-----------------------|------------------------|-----------------------|------------------------|-----------------------|---------------------|---------------------------|-------------------------|---------------------|-------------------------|------------------|--------------|------------|
|                    |   | 0                     | 1                      | 2                       | 3                         | 4                     | 5                      | 6                     | 7                      | 8                     | 9                   | A                         | B                       | C                   | D                       | E                | F            |            |
| Upper Nibble (Hex) | 0 | 6.5<br>DEC<br>R1      | 6.5<br>DEC<br>IR1      | 6.5<br>ADD<br>r1, r2    | 6.5<br>ADD<br>r1, lr2     | 10.5<br>ADD<br>R2, R1 | 10.5<br>ADD<br>IR2, R1 | 10.5<br>ADD<br>R1, IM | 10.5<br>ADD<br>IR1, IM | 6.5<br>LD<br>r1, R2   | 6.5<br>LD<br>r2, R1 | 12/10.5<br>DJNZ<br>r1, RA | 12/10.0<br>JR<br>cc, RA | 6.5<br>LD<br>r1, IM | 12.10.0<br>JP<br>cc, DA | 6.5<br>INC<br>r1 |              |            |
|                    | 1 | 6.5<br>RLC<br>R1      | 6.5<br>RLC<br>IR1      | 6.5<br>ADC<br>r1, r2    | 6.5<br>ADC<br>r1, lr2     | 10.5<br>ADC<br>R2, R1 | 10.5<br>ADC<br>IR2, R1 | 10.5<br>ADC<br>R1, IM | 10.5<br>ADC<br>IR1, IM |                       |                     |                           |                         |                     |                         |                  |              |            |
|                    | 2 | 6.5<br>INC<br>R1      | 6.5<br>INC<br>IR1      | 6.5<br>SUB<br>r1, r2    | 6.5<br>SUB<br>r1, lr2     | 10.5<br>SUB<br>R2, R1 | 10.5<br>SUB<br>IR2, R1 | 10.5<br>SUB<br>R1, IM | 10.5<br>SUB<br>IR1, IM |                       |                     |                           |                         |                     |                         |                  |              |            |
|                    | 3 | 8.0<br>JP<br>IRR1     | 6.1<br>SRP<br>IM       | 6.5<br>SBC<br>r1, r2    | 6.5<br>SBC<br>r1, lr2     | 10.5<br>SBC<br>R2, R1 | 10.5<br>SBC<br>IR2, R1 | 10.5<br>SBC<br>R1, IM | 10.5<br>SBC<br>IR1, IM |                       |                     |                           |                         |                     |                         |                  |              |            |
|                    | 4 | 8.5<br>DA<br>R1       | 8.5<br>DA<br>IR1       | 6.5<br>OR<br>r1, r2     | 6.5<br>OR<br>r1, lr2      | 10.5<br>OR<br>R2, R1  | 10.5<br>OR<br>IR2, R1  | 10.5<br>OR<br>R1, IM  | 10.5<br>OR<br>IR1, IM  |                       |                     |                           |                         |                     |                         |                  |              |            |
|                    | 5 | 10.5<br>POP<br>R1     | 10.5<br>POP<br>IR1     | 6.5<br>AND<br>r1, r2    | 6.5<br>AND<br>r1, lr2     | 10.5<br>AND<br>R2, R1 | 10.5<br>AND<br>IR2, R1 | 10.5<br>AND<br>R1, IM | 10.5<br>AND<br>IR1, IM |                       |                     |                           |                         |                     |                         |                  | 6.0<br>WDT   |            |
|                    | 6 | 6.5<br>COM<br>R1      | 6.5<br>COM<br>IR1      | 6.5<br>TCM<br>r1, r2    | 6.5<br>TCM<br>r1, lr2     | 10.5<br>TCM<br>R2, R1 | 10.5<br>TCM<br>IR2, R1 | 10.5<br>TCM<br>R1, IM | 10.5<br>TCM<br>IR1, IM |                       |                     |                           |                         |                     |                         |                  |              |            |
|                    | 7 | 10/12.1<br>PUSH<br>R2 | 12/14.1<br>PUSH<br>IR2 | 6.5<br>TM<br>r1, r2     | 6.5<br>TM<br>r1, lr2      | 10.5<br>TM<br>R2, R1  | 10.5<br>TM<br>IR2, R1  | 10.5<br>TM<br>R1, IM  | 10.5<br>TM<br>IR1, IM  |                       |                     |                           |                         |                     |                         |                  |              |            |
|                    | 8 | 10.5<br>DECW<br>RR1   | 10.5<br>DECW<br>IR1    |                         |                           |                       |                        |                       |                        |                       |                     |                           |                         |                     |                         |                  |              | 6.1<br>DI  |
|                    | 9 | 6.5<br>RL<br>R1       | 6.5<br>RL<br>IR1       |                         |                           |                       |                        |                       |                        |                       |                     |                           |                         |                     |                         |                  |              | 6.1<br>EI  |
|                    | A | 10.5<br>INCW<br>RR1   | 10.5<br>INCW<br>IR1    | 6.5<br>CP<br>r1, r2     | 6.5<br>CP<br>r1, lr2      | 10.5<br>CP<br>R2, R1  | 10.5<br>CP<br>IR2, R1  | 10.5<br>CP<br>R1, IM  | 10.5<br>CP<br>IR1, IM  |                       |                     |                           |                         |                     |                         |                  | 14.0<br>RET  |            |
|                    | B | 6.5<br>CLR<br>R1      | 6.5<br>CLR<br>IR1      | 6.5<br>XOR<br>r1, r2    | 6.5<br>XOR<br>r1, lr2     | 10.5<br>XOR<br>R2, R1 | 10.5<br>XOR<br>IR2, R1 | 10.5<br>XOR<br>R1, IM | 10.5<br>XOR<br>IR1, IM |                       |                     |                           |                         |                     |                         |                  | 16.0<br>IRET |            |
|                    | C | 6.5<br>RRC<br>R1      | 6.5<br>RRC<br>IR1      | 12.0<br>LDC<br>r1, lrr2 | 18.0<br>LDCI<br>lr1, lrr2 |                       |                        |                       |                        | 10.5<br>LD<br>r1,x,R2 |                     |                           |                         |                     |                         |                  |              | 6.5<br>RCF |
|                    | D | 6.5<br>SRA<br>R1      | 6.5<br>SRA<br>IR1      |                         |                           | 20.0<br>CALL*<br>IRR1 |                        | 20.0<br>CALL<br>DA    | 10.5<br>LD<br>r2,x,R1  |                       |                     |                           |                         |                     |                         |                  |              | 6.5<br>SCF |
|                    | E | 6.5<br>RR<br>R1       | 6.5<br>RR<br>IR1       |                         | 6.5<br>LD<br>r1, IR2      | 10.5<br>LD<br>R2, R1  | 10.5<br>LD<br>IR2, R1  | 10.5<br>LD<br>R1, IM  | 10.5<br>LD<br>IR1, IM  |                       |                     |                           |                         |                     |                         |                  |              | 6.5<br>CCF |
|                    | F | 8.5<br>SWAP<br>R1     | 8.5<br>SWAP<br>IR1     |                         | 6.5<br>LD<br>lr1, r2      |                       | 10.5<br>LD<br>R2, IR1  |                       |                        |                       |                     |                           |                         |                     |                         |                  |              | 6.0<br>NOP |
|                    |   | 2                     |                        | 3                       |                           |                       | 2                      |                       | 3                      |                       |                     | 1                         |                         |                     |                         |                  |              |            |
|                    |   | Bytes per Instruction |                        |                         |                           |                       |                        |                       |                        |                       |                     |                           |                         |                     |                         |                  |              |            |



## Legend:

R = 8-bit Address  
r = 4-bit Address  
R1 or r1 = Dst Address  
R2 or r2 = Src Address

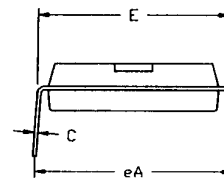
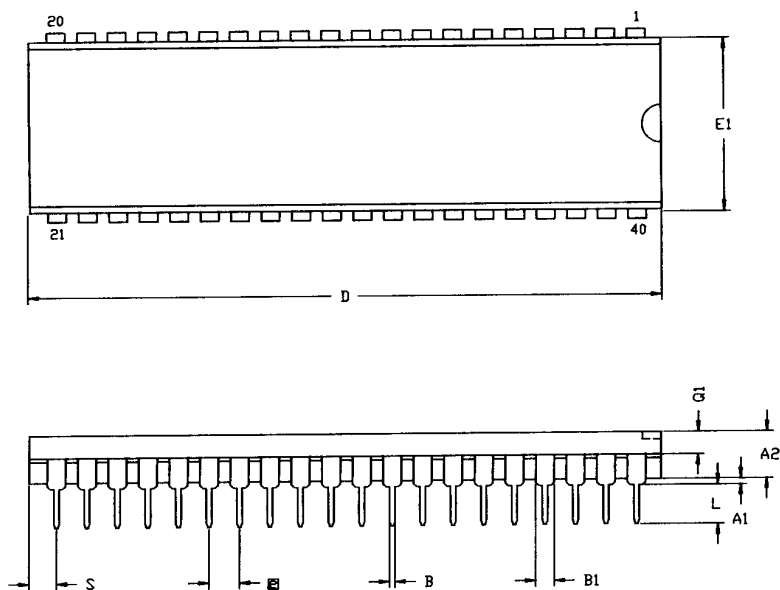
## Sequence:

Opcode, First Operand,  
Second Operand

**Note:** Blank areas not defined.

\*2-byte instruction appears as  
a 3-byte instruction

# PACKAGE INFORMATION



| SYMBOL | MILLIMETER |       | INCH     |       |
|--------|------------|-------|----------|-------|
|        | MIN        | MAX   | MIN      | MAX   |
| A1     | 0.51       | 0.81  | .020     | .032  |
| A2     | 3.25       | 3.43  | .128     | .135  |
| B      | 0.38       | 0.53  | .015     | .021  |
| B1     | 1.02       | 1.52  | .040     | .060  |
| C      | 0.23       | 0.38  | .009     | .015  |
| D      | 52.07      | 52.58 | 2.050    | 2.070 |
| E      | 15.24      | 15.75 | .600     | .620  |
| E1     | 13.59      | 14.22 | .535     | .560  |
| ⌀      | 2.54 TYP   |       | .100 TYP |       |
| eA     | 15.49      | 16.51 | .610     | .650  |
| L      | 3.18       | 3.81  | .125     | .150  |
| Q1     | 1.52       | 1.91  | .060     | .075  |
| S      | 1.52       | 2.29  | .060     | .090  |

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram

## ORDERING INFORMATION

**5 MHz**  
**Z0861705PSC**

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

### Package

P = Plastic DIP

V = Plastic Leaded Chip Carrier

### Speed

05 = 5 MHz

### Environmental

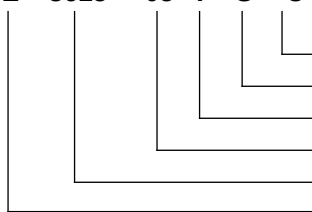
C = Plastic Standard

### Temperature

S = 0°C to +70°C (standard temp for the Z8615 is 0 to –55°C)

### Example:

**Z 8615 05 P S\* C** is a Z8615, 5 MHz, DIP, 0°C to –55°C, Plastic Standard Flow



Environmental Flow  
Temperature (standard temp for the Z8615 is 0 to –55°C)  
Package  
Speed  
Product Number  
Zilog Prefix