NEC

BiCMOS INTEGRATED CIRCUIT

μPC1934

DC-DC CONVERTER CONTROL IC

DESCRIPTION

The μPC1934 is an IC that controls a low-voltage input DC-DC converter. This IC is suitable for an operation with 3-V, 3.3-V input or a lithium ion secondary battery input, because the minimum operation supply voltage is 2.5 V. Because of its wide operating voltage range, it can also be used to control DC-DC converters that use an AC adapter for input.

FEATURES

- Low supply voltage: 2.5 V (MIN.)
- Operating voltage range: 2.5 to 20 V (breakdown voltage: 30 V)
- Timer latch circuit for short-circuit protection.
- Ceramic capacitor with low capacitance (0.1 μF) can be used for short-circuit protection.
- Open drain outputs (Each of the outputs can be used to control a step-down converter, a step-up converter and an inverted converter.)
- Can control two output channels.

ORDERING INFORMATION

Part Number	Package
μPC1934GR-1JG	16-pin plastic SSOP (5.72 mm (225))
μPC1934GR-PJG	16-pin plastic TSSOP (5.72 mm (225))

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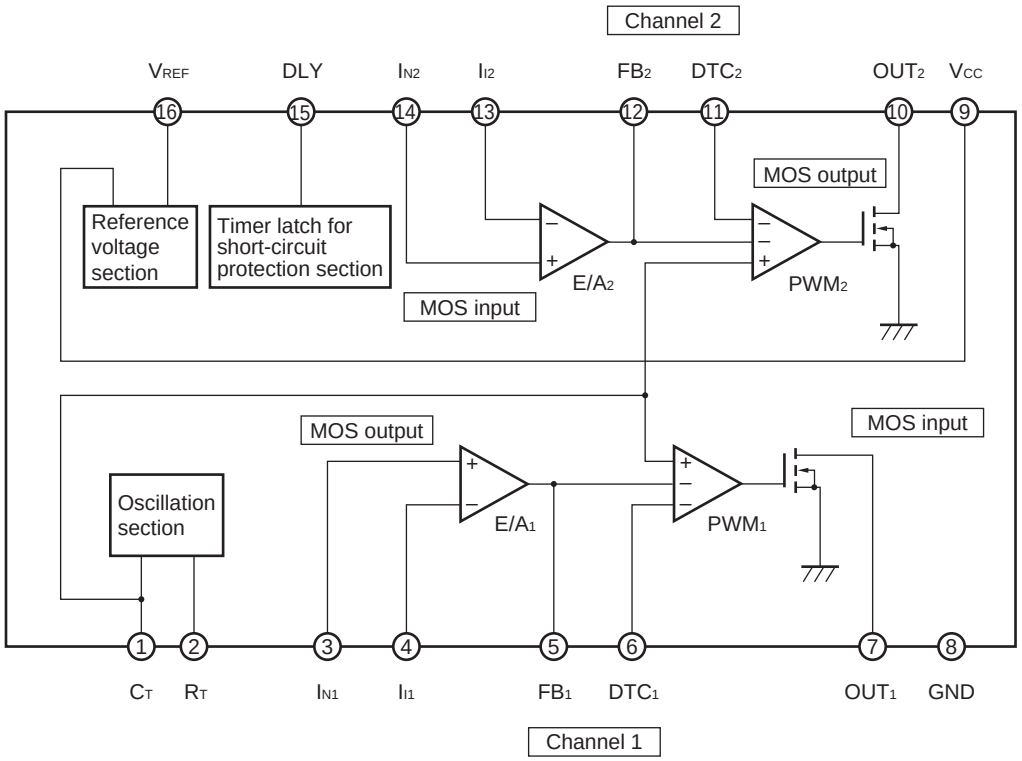
Printed in Japan

The mark ★ shows major revised points.

BLOCK DIAGRAM



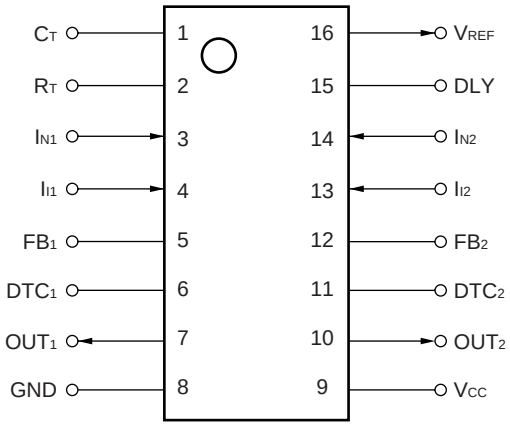
PIN CONFIGURATION (Top View)

16-pin plastic SSOP (5.72 mm (225))

- **μPC1934GR-1JG**

16-pin plastic TSSOP (5.72 mm (225))

- **μPC1934GR-PJG**



PIN FUNCTIONS

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	C_T	Frequency setting capacitor connection	9	V_{CC}	Power supply
2	R_T	Frequency setting resistor connection	10	OUT_2	Channel 2 open drain output
3	I_{N1}	Channel 1 error amplifier non-inverted input	11	DTC_2	Channel 2 dead time setting
4	I_{I1}	Channel 1 error amplifier inverted input	12	FB_2	Channel 2 error amplifier output
5	FB_1	Channel 1 error amplifier output	13	I_{I2}	Channel 2 error amplifier inverted input
6	DTC_1	Channel 1 dead time setting	14	I_{N2}	Channel 2 error amplifier non-inverted input
7	OUT_1	Channel 1 open drain output	15	DLY	Delay capacitor connection of short-circuit protection
8	GND	Ground	16	V_{REF}	Reference voltage output

CONTENTS

1. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (unless otherwise specified, T_A = 25 °C)

Parameter	Symbol	μPC1934GR-1JG	μPC1934GR-PJG	Unit
Supply voltage	V_{CC}	30		V
Output voltage	V_O	30		V
Output current (open drain output)	I_O	21		mA
Total power dissipation	P_T	417	400	mW
Operating ambient temperature	T_A	–20 to + 85		°C
Storage temperature	T_{stg}	–55 to + 150		°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

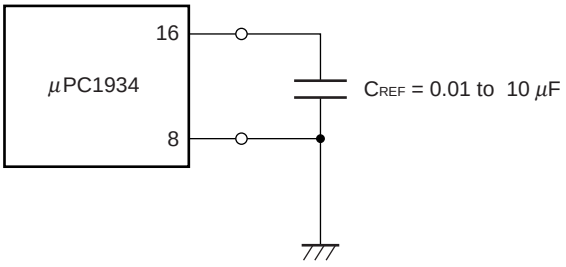
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	2.5		20	V
Output voltage	V_O	0		20	V
Output current	I_O			20	mA
Operating temperature	T_A	–20		+85	°C
Oscillation frequency	f_{OSC}	20		1000	kHz

★ **Caution The recommended operating range may be exceeded without causing any problems provided that the absolute maximum ratings are not exceeded. However, if the device is operated in a way that exceeds the recommended operating conditions, the margin between the actual conditions of use and the absolute maximum ratings is small, and therefore thorough evaluation is necessary. The recommended operating conditions do not imply that the device can be used with all values at their maximum values.**

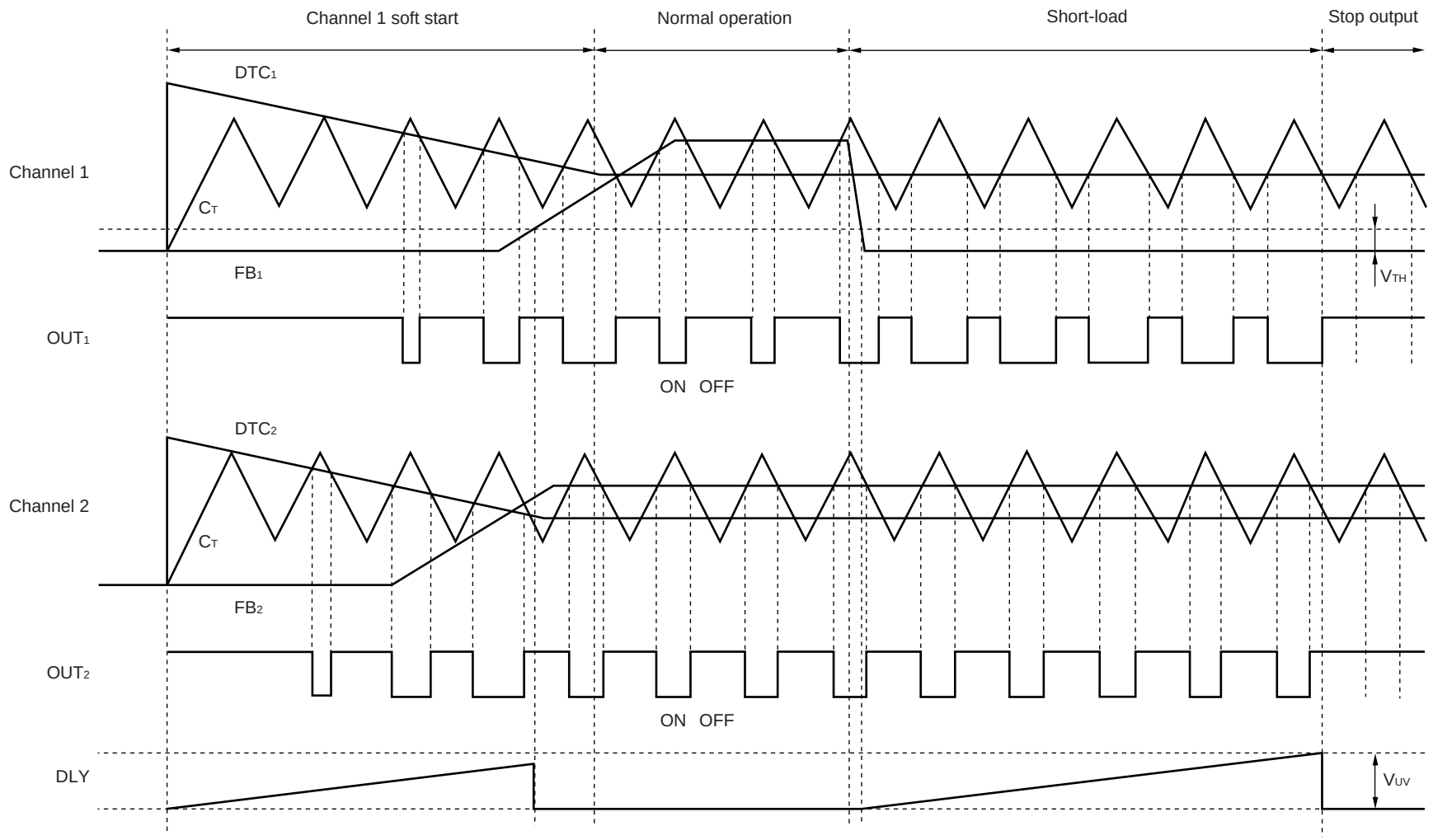
Electrical Characteristics (unless otherwise specified, T_A = 25 °C, V_{CC} = 3 V, f_{OSC} = 100 kHz)

	Block	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Under voltage Lock-out section	Start-up voltage	$V_{CC\ (L\text{-}H)}$	I_{REF} = 0.1 mA		1.57		V
		Operation stop voltage	$V_{CC\ (H\text{-}L)}$	I_{REF} = 0.1 mA		1.5		V
		Hysteresis voltage	V_H	I_{REF} = 0.1 mA	30	70		mV
		Reset voltage (timer latch)	V_{CCR}	I_{REF} = 0.1 mA		1.0		V
	Reference Voltage section	Reference voltage	V_{REF}	I_{REF} = 1 mA	2.0	2.1	2.2	V
★		Line regulation	REG_{IN}	2.5 V≤V_{CC}≤20 V		2	12.5	mV
		Load regulation	REG_L	0.1 mA≤I_{REF}≤1 mA		2	7.5	mV
		Temperature coefficient	$\Delta V_{REF}/\Delta T$	–20 °C≤T_A≤+85 °C, I_{REF} = 0 A		0.5		%
	Oscillation section	f_{OSC} setting accuracy	Δf_{OSC}	R_T = 11 kΩ, C_T = 330 pF	–15		+15	%
		f_{OSC} total stability	Δf_{OSC}	–20 °C≤T_A≤+85 °C, 2.5 V≤V_{CC}≤20 V	–30		+30	%
	Dead time control section	Input bias current	I_{BD}			0.4	1.0	μA
		Low-level threshold voltage	$V_{TH\ (L)}$	Duty = 100 %		1.2		V
		High-level threshold voltage	$V_{TH\ (H)}$	Duty = 0 %		1.6		V
	Error Amplifier section	Input offset voltage	V_{IO}		–10		+10	mV
		Input offset current	I_{IO}		–100		+100	nA
		Input bias current	I_B		–100		+100	nA
		Common mode input voltage range	V_{IMC}		0		0.4	V
		Open loop gain	A_v	V_O = 0.3 V	70	80		dB
		Unity gain	f_{unity}	V_O = 0.3 V		1.5		MHz
		Maximum output voltage (+)	V_{OM}^+	I_O = –45 μA	1.6	2		V
★		Maximum output voltage (–)	V_{OM}^-	I_O = 45 μA		0.02	0.5	V
		Output sink current	I_{Osink}	V_{FB} = 0.5 V	0.8	1.4		mA
		Output source current	$I_{Osource}$	V_{FB} = 1.6 V		–70	–45	μA
	Output section	Drain cutoff current	I_{LEAK}	V_O = 30 V			100	μA
★		Output ON voltage	V_{OL}	R_L = 150 Ω		0.2	0.6	V
		Rise time	t_r	R_L = 150 Ω		50		ns
		Fall time	t_f	R_L = 150 Ω		60		ns
★	Short-circuit Protection section	Input sense voltage	V_{TH}		0.5	0.63	0.75	V
★		UV sense voltage	V_{UV}		0.6	0.8	0.95	V
★		Source current on short-circuiting	I_{OUV}		1.0	1.6	2.5	μA
		Delay time	t_{DLY}	C_{DLY} = 0.1 μF		50		ms
★	Overall	Circuit operation current	I_{CC}	V_{CC} = 3 V	1.4	2.2	3.7	mA

Caution Connect a capacitor of 0.01 to 10 μF to the V_{REF} pin.



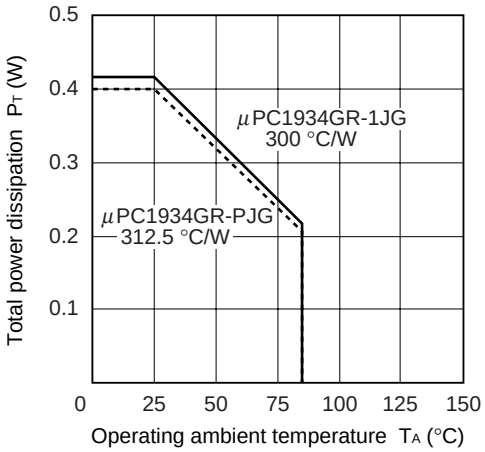
Timing Charts



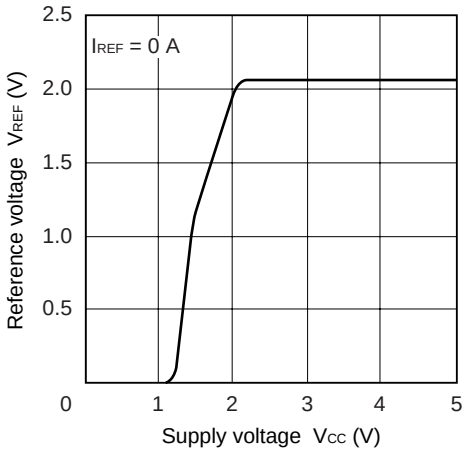
Remark These timings are an example when the channel 1 output has been a short- load. The outputs of channel 1 and 2 are also stopped when a short-circuit protection circuit starts operation by detecting a short- load of channel 2.

Typical Characteristic Curves (unless otherwise specified, V_{CC} = 3 V, f_{OSC} = 100 kHz, T_A = 25 °C) (Nominal)

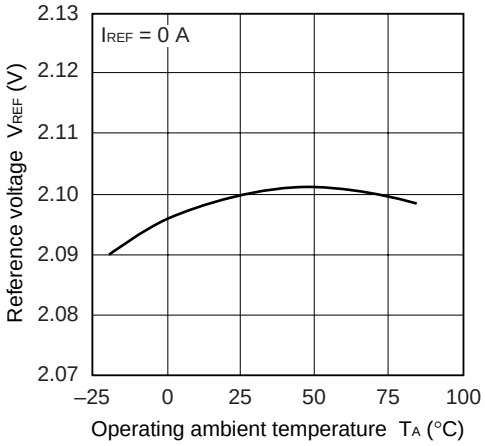
P_T vs T_A



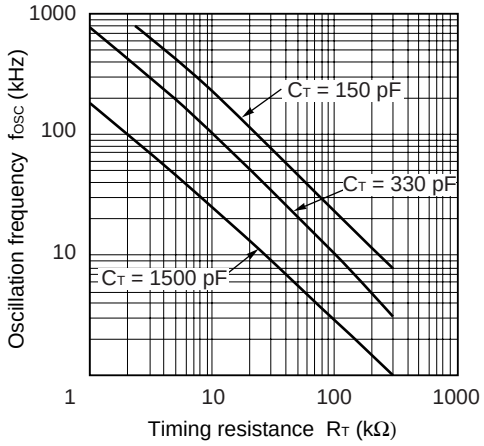
V_{REF} vs V_{CC}



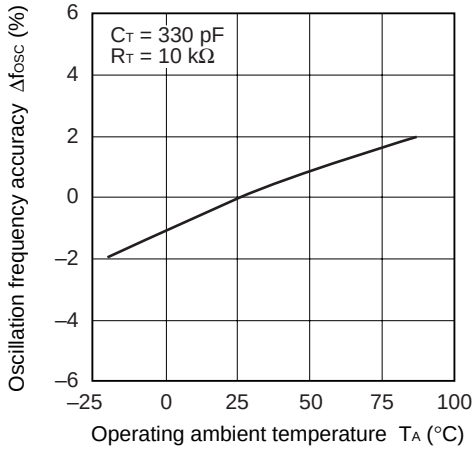
V_{REF} vs T_A



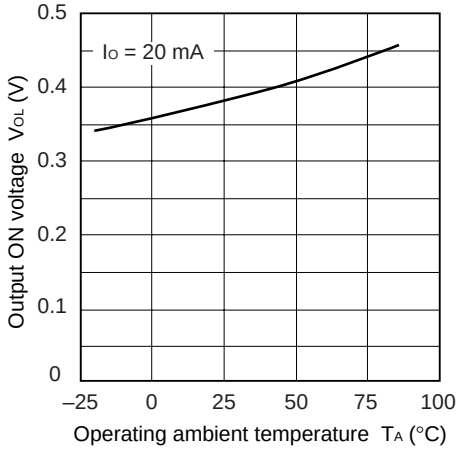
f_{OSC} vs R_T



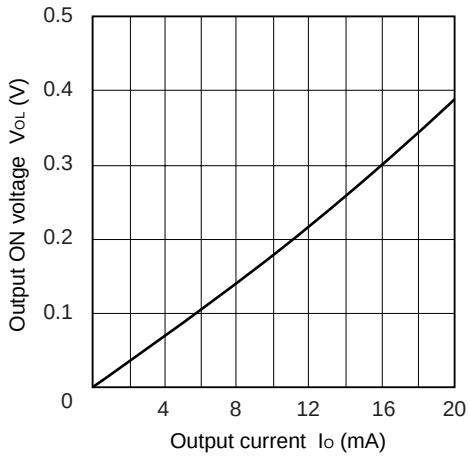
Δf_{OSC} vs T_A



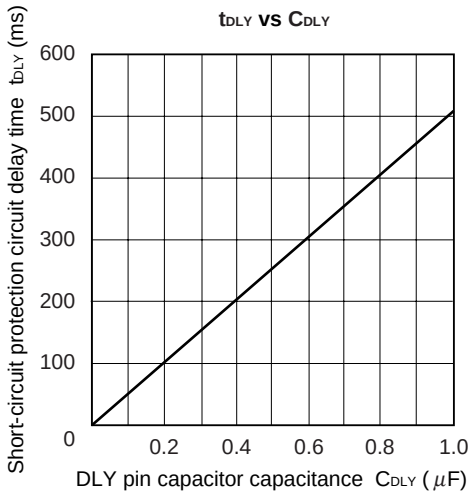
V_{OL} vs T_A



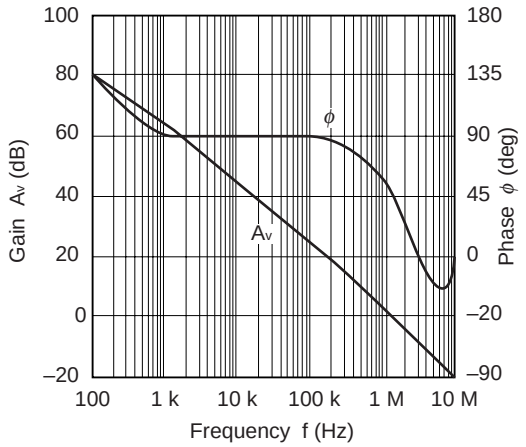
V_{OL} vs I_O



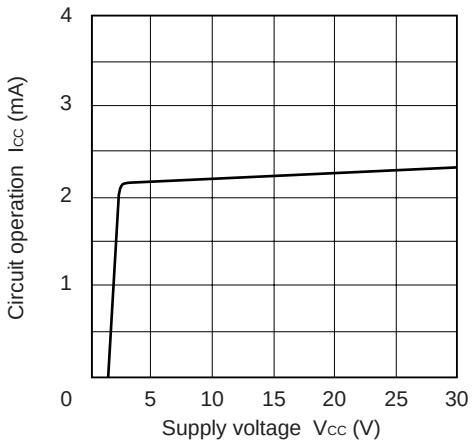
t_{DLY} vs C_{DLY}



A_V, ϕ vs f

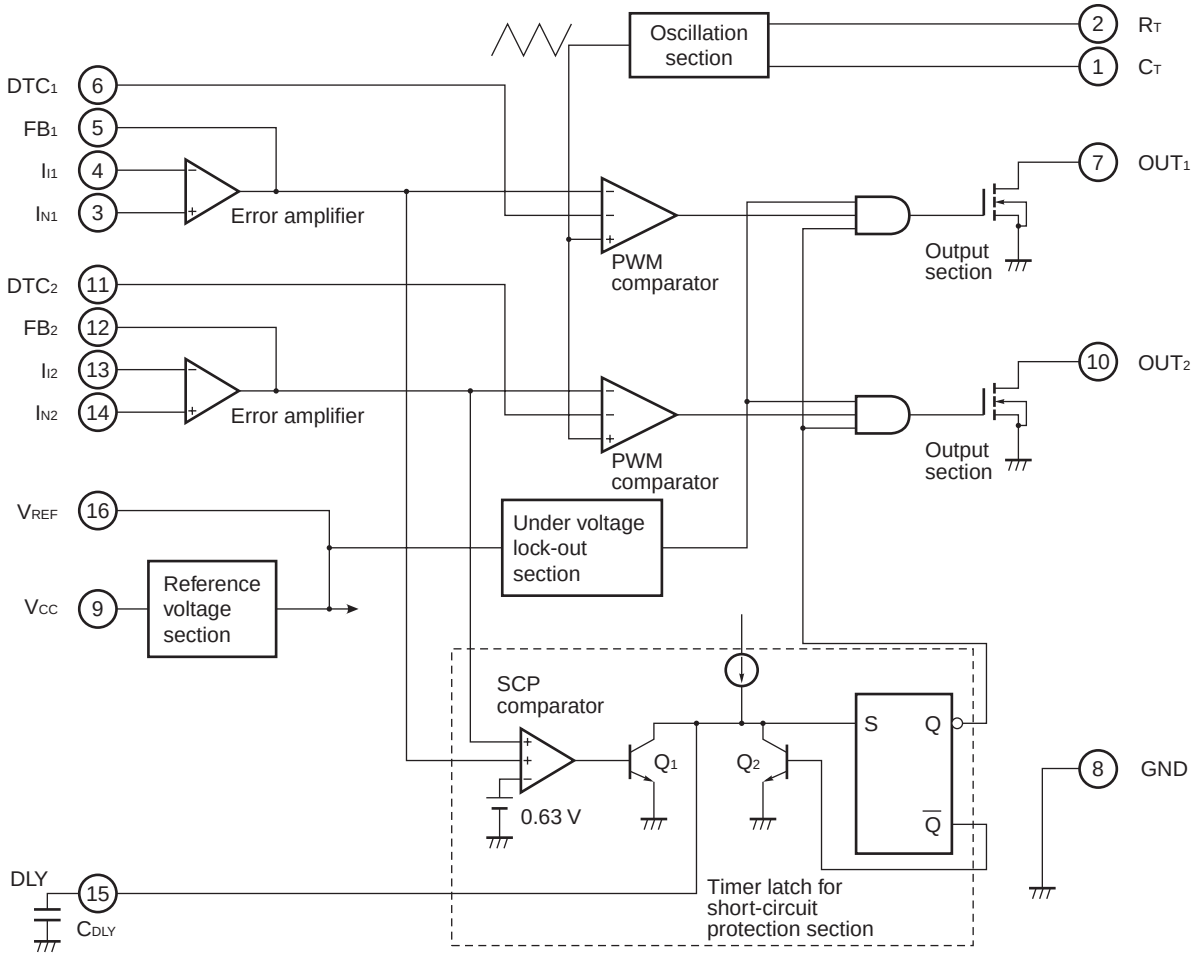


I_{CC} vs V_{CC}



★ 2. CONFIGURATION AND OPERATION OF EACH BLOCK

Figure 2-1 Block Diagram



2.1 Reference Voltage Generator

The reference voltage generator is comprised of a band-gap reference circuit, and outputs a temperature-compensated reference voltage (2.1 V). The reference voltage can be used as the power supply for internal circuits, or as a reference voltage, and can also be accessed externally via the V_{REF} pin (pin 16).

2.2 Oscillator

The oscillator self-oscillates if a timing resistor is attached to the R_T pin (pin 2). Also, the oscillator outputs the symmetrical triangular waveform if a timing capacitor is attached to the C_T pin (pin 1). This oscillator waveform is input to the non-inverted input pins of the two PWM comparators to determine the oscillation frequency.

2.3 Under Voltage Lock-out Circuit

The under voltage lock-out circuit prevents malfunctioning of the internal circuits when the supply voltage is low, such as when the supply voltage is first applied, or when the power supply is interrupted. When the voltage is low, the two output transistors are cut off at the same time.

2.4 Error Amplifiers

The circuits of the error amplifiers E/A_1 and E/A_2 are exactly the same. The first stage of the error amplifier is a P-channel MOS transistor input. Be careful of the input voltage ranges (the common mode input voltage ranges are all 0 to 0.4 V (TYP.)).

2.5 PWM Comparators

The output ON duty is controlled according to the outputs of the error amplifiers and the voltage input to the Dead Time Control pin.

A triangular waveform is input to the non-inverted pin, and the error amplifier output and Dead Time Control pin voltage are input to the inverted pins of the PWM comparators. Therefore, the output transistor ON period is the period when the triangular waveform is higher than the error amplifier output and Dead Time Control pin voltage (refer to **Timing Charts**).

2.6 Timer Latch-Method Short Circuit Protection Circuit

When the converter outputs either a channel or both channels drop, the FB outputs of the error amplifiers of those outputs go low. If the FB output goes lower than the timer latch input detection voltage (V_{TH} = 0.63 V)), then the output of the SCP comparator goes low, and Q_1 goes off.

When Q_1 turns OFF, the constant-current supply charges C_{DLY} via the DLY pin. The DLY pin is internally connected to a flip-flop. When the DLY pin voltage reaches the UV detection voltage (V_{UV} = 0.8 V (TYP.)), the output Q of the flip-flop goes low, and the output stage of each channel is latched to OFF (refer to **Figure 2-1 Block Diagram**).

Make the power supply voltage briefly less than the reset voltage (V_{CCR}, 1.0 V TYP.) to reset the latch circuit when the short-circuit protection circuit has operated.

2.7 Output Circuit

The output circuit has an N-channel open-drain output providing an output withstand voltage of 30 V (absolute maximum rating), and an output current of 21 mA (absolute maximum rating).

★ 3. NOTES ON USE

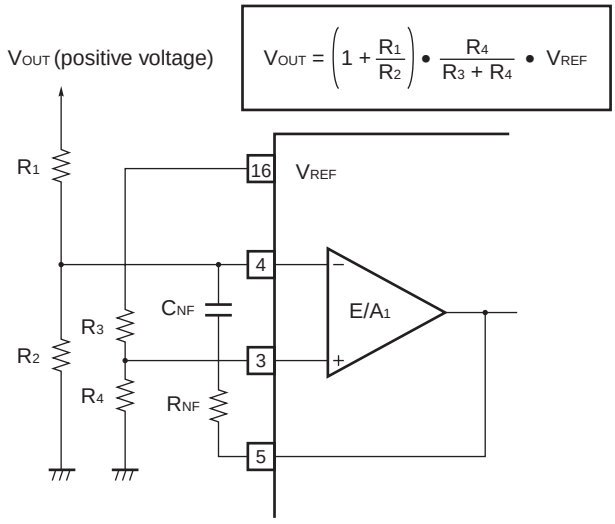
3.1 Setting the Output Voltage

Figure 3-1 illustrates the method of setting the output voltage. The output voltage is obtained using the formula shown in the figure.

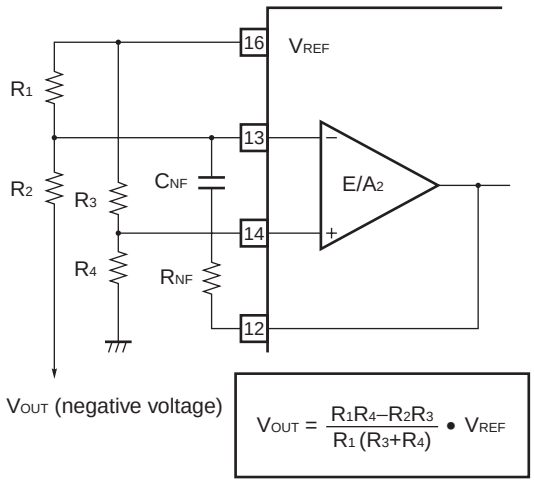
The common mode input voltage range of the error amplifier is 0 to 0.4 V (TYP.) for both the error amplifiers, E/A1 and E/A2. Therefore, select a resistor value that gives this voltage range.

Figure 3-1 Setting the Output Voltage

(1) When setting a positive output voltage using error amplifier E/A1.



(2) When setting a negative output voltage using error amplifier E/A2.



3.2 Setting the Oscillation Frequency

Choose R_T according to the oscillation frequency (f_{OSC}) vs timing resistor (C_T, R_T) characteristics (refer To **Typical Characteristics Curves f_{OSC} vs C_T, R_T**). The formula below (3-1) gives an approximation of f_{OSC}. However, the result of formula 3-1 is only an approximation, and the value must be confirmed in actual operation, especially for high-frequency operation.

$$f_{OSC}\,[Hz] \cong 0.375/(C_T\,[F] \times R_T\,[\Omega]) \quad (3\text{-}1)$$

3.3 Preventing Malfunction of the Timer Latch-Method Short Circuit Protection Circuit

The timer latch short-circuit protection circuit operates when the error amplifier outputs (pin 5 and 12) goes below approximately 0.63 V, and cuts off the output. However, if the rise of the power supply voltage is fast, or if there is noise on the DLY pin (pin 15), the latch circuit may malfunction and cut the output off.

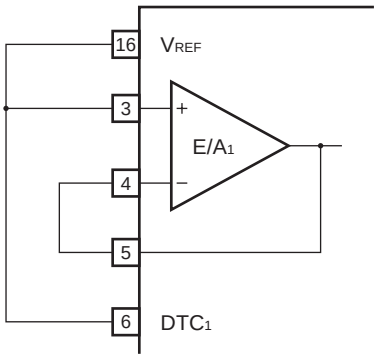
To prevent this, lower the wiring impedance between the DLY pin and the GND pin (pin 8), and avoid applying noise to the DLY pin.

3.4 Connecting Unused Error Amplifiers

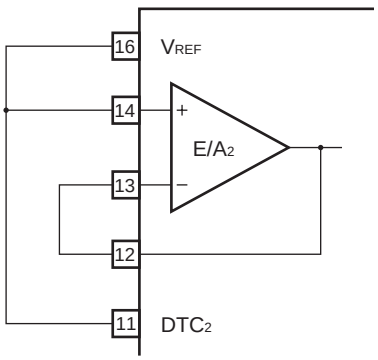
When one of the two control circuits is used, connect the circuit so that the output of the error amplifier of unused circuit is high. Figure 3-2 shows examples of how to connect unused error amplifiers.

Figure 3-2 Examples of Connecting Unused Error Amplifiers

(1) Error amplifier E/A_1



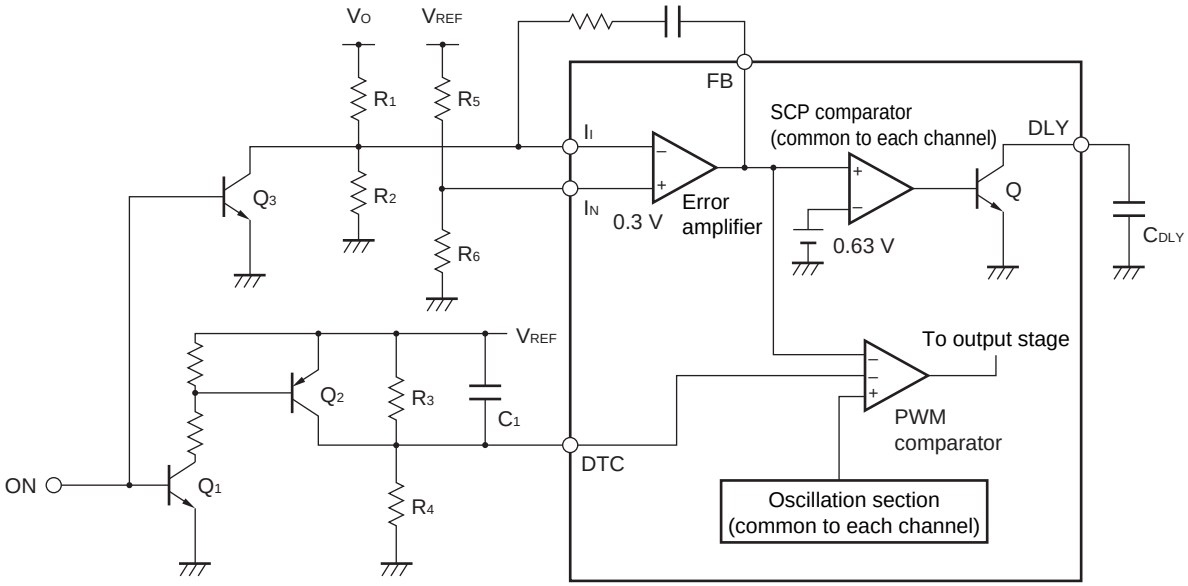
(2) Error amplifier E/A_2



3.5 ON/OFF Control

The ON/OFF control method of the output oscillation is to input the ON/OFF signal from ON as shown in Figure 3-3. The PWM converter can be turned ON/OFF by controlling the level of the DTC pin. However, it is necessary to keep the level of the FB output high so that the timer latch does not start when the PWM converter is OFF. In this circuit example, the FB output level is controlled by controlling the level of the I_I pin.

Figure 3-3 ON/OFF Control



(1) When ON is high: OFF status

Q_1: ON → Q_2: ON → DTC pin: High level → Output duty of PWM comparator: 0 %

Q_3: ON → I_I pin: Low level → FB output: High level → SCP comparator output: High level → Q is ON. → Timer latch stops.

(2) When ON_3 is low: ON status

Q_1: OFF → Q_2 is OFF. → C_1 is charged in the sequence of [V_{REF} → C_1 → R_4] → DTC pin voltage drops. → Soft start

Q_3: OFF → I_I pin: High level → FB output: Low level → SCP comparator output: Low level → Q: OFF

→ Charging C_{DLY} starts (timer latch start).

Caution Keep the high-level voltage of the DTC pin at 1.6 V or higher and the low-level voltage of the I_I pin within (R6/(R5+R6))•V_{REF}. The maximum voltage that is applied to the I_I pin must be equal to or lower than V_{REF}.

3.6 Notes on Actual Pattern Wiring

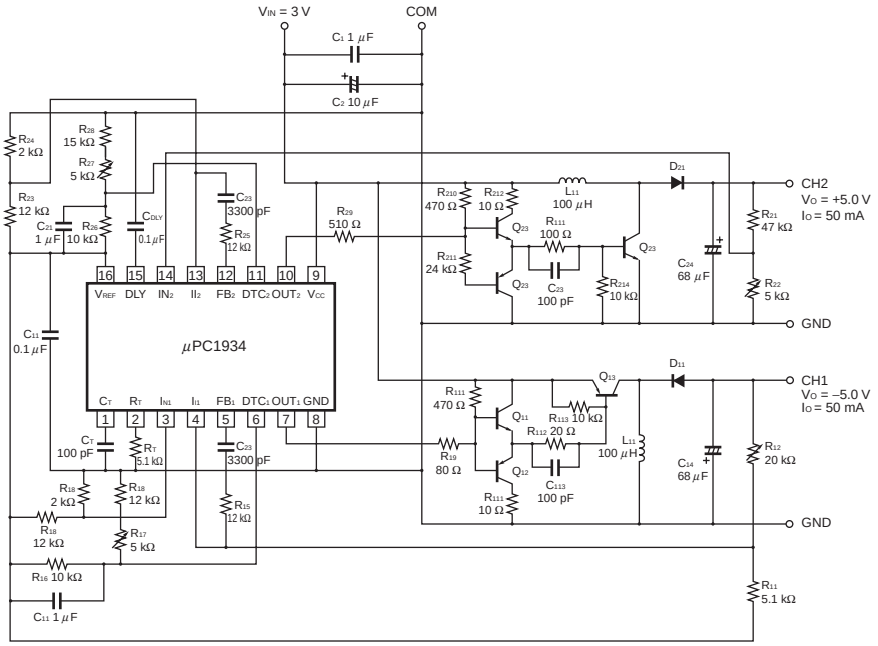
When actually carrying out the pattern wiring, it is necessary to separate control-related grounds and power-related grounds, and make sure that they do not share impedances as far as possible. In addition, make sure the high-frequency impedance is lowered using capacitors and other components to prevent noise input to the V_{REF} pin.

★ 4. APPLICATION EXAMPLE

4.1 Application Example

Figure 4-1 shows an example circuit for obtaining ±5 V/50 mA from a +3 V power supply.

Figure 4-1 Chopper-Method Step-up/Inverting-Type Switching Regulator



4.2 List of External Parts

The list below shows the external parts.

Table 4-1 List of External Parts

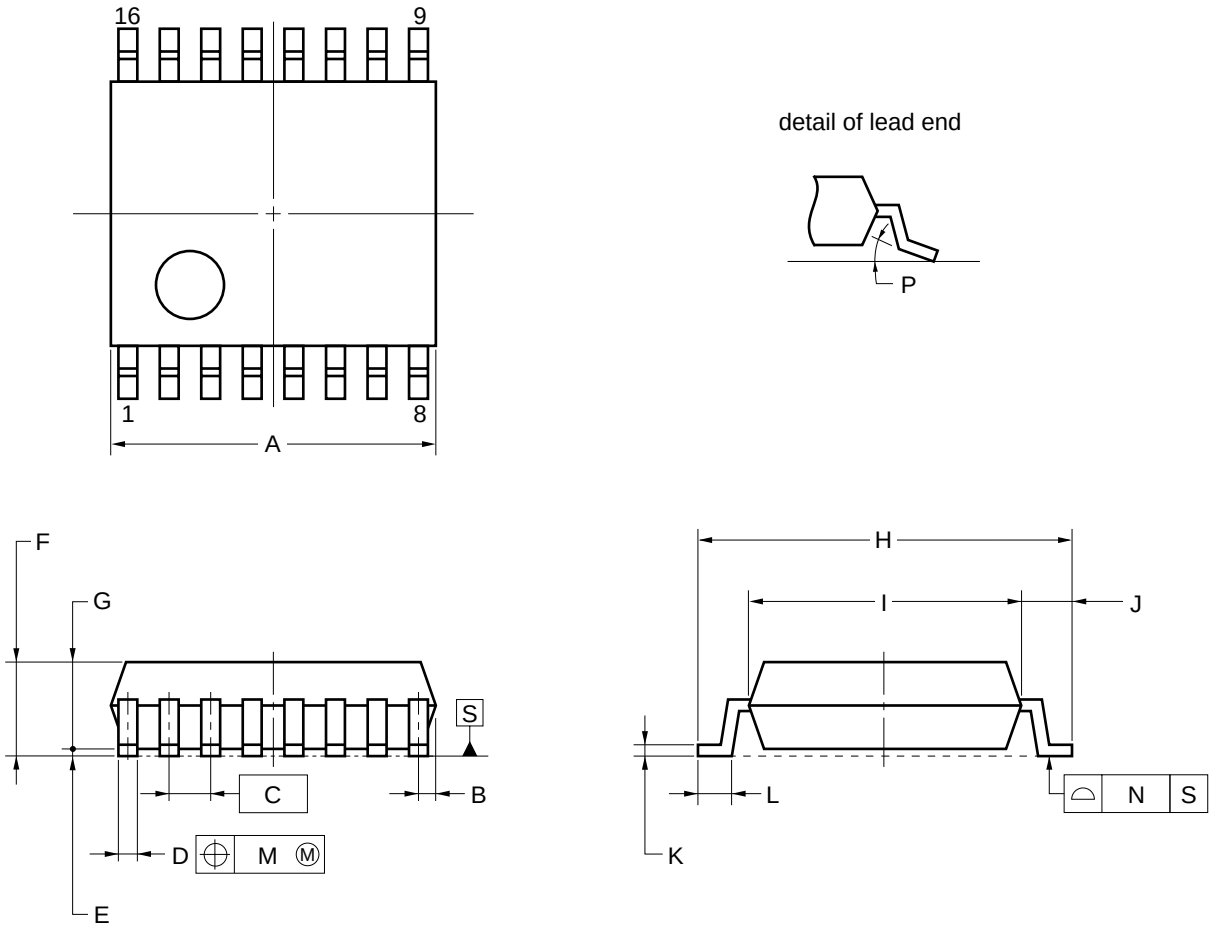
Symbol	Parameter	Function	Part number	Maker	Remark
C_2	10 μF	Input stable capacitor	25SC10M	SANYO	OS-CON, SC series
C_{14}	68 μF	Output capacitor	20SA68M	SANYO	OS-CON, SA series
D_{11}		Schottkey diode	D1FS4	SHINDENGEN	
L_{11}	100 μH	Choke inductor	636FY-101M	TOKO	D73F series
Q_{11}, Q_{12}		Buffer transistor	μPA609T	NEC	Transistor array
Q_{13}		Switching transistor	2SB1572	NEC	
C_{21}	68 μF	Output capacitor	20SA68M	SANYO	OS-CON, SA series
D_{21}		Schottkey diode	D1FS4	SHINDENGEN	
L_{21}	100 μH	Choke inductor	636FY-101M	TOKO	D73F series
Q_{21}, Q_{22}		Buffer transistor	μPA609T	NEC	Transistor array
Q_{23}		Switching transistor	2SD2403	NEC	

Remarks 1. The capacitors that are not specified in the above list are multilayer ceramic capacitors.

2. The resistors that are not specified in the above list are 1/4W resistors.

5. PACKAGE DRAWINGS

16-PIN PLASTIC SSOP (5.72 mm (225))



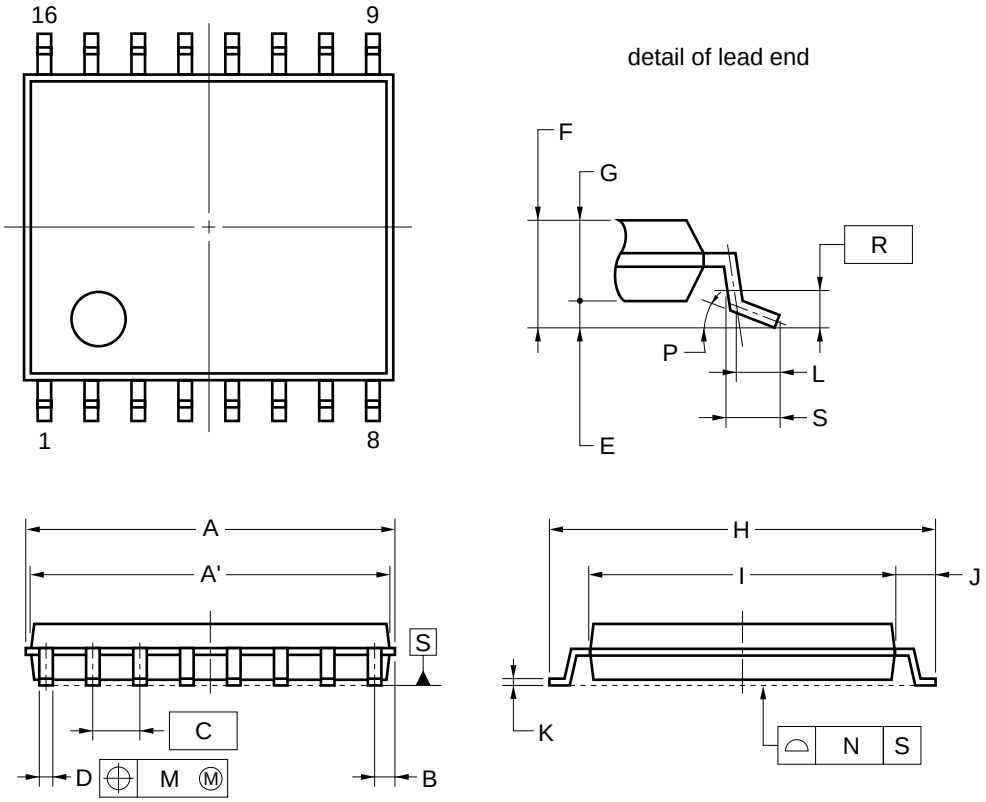
NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2±0.3
B	0.475 MAX.
C	0.65 (T.P.)
D	0.22±0.8
E	0.125±0.075
F	1.565±0.235
G	1.44
H	6.2±0.3
I	4.4±0.2
J	0.9±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.5±0.2
M	0.10
N	0.10
P	5°±5°

P16GM-65-225B-4

16-PIN PLASTIC TSSOP (5.72 mm (225))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.15±0.15
A'	5.0±0.1
B	0.375 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.06}_{-0.04}$
E	$0.09^{+0.06}_{-0.04}$
F	$1.01^{+0.09}_{-0.06}$
G	0.92
H	6.4±0.2
I	4.4±0.1
J	1.0±0.2
K	$0.145^{+0.055}_{-0.045}$
L	0.5
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.6±0.15

S16GR-65-PJG-1

6. RECOMMENDED SOLDERING CONDITIONS

Recommended solder conditions for this product are described below.

For details on recommended soldering conditions, refer to Information Document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Surface Mount Type

μPC1934GR-1JG: 16-pin plastic SSOP (5.72 mm (225))

μPC1934GR-PJG: 16-pin plastic TSSOP (5.72 mm (225))

Soldering Method	Soldering Conditions	Symbol of Recommended Conditions
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.), Number of times: 3 MAX.	IR35-00-3
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.), Number of times: 3 MAX.	VP15-00-3
Wave soldering	Soldering bath temperature: 260 °C MAX., Time: 10 seconds MAX., Number of times: 1, Preheating temperature: 120 °C MAX. (package surface temperature)	WS60-00-1

Caution Do not use two or more soldering methods in combination.

NOTES FOR BiCMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS

Note:

No connection for device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. Input levels of devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF BiCMOS DEVICES

Note:

Power-on does not necessarily define initial status of device. Production process of BiCMOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.