#### 2.7-W MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

#### GENERAL DESCRIPTION

The TMPA2055DM is a mono class-D filter–free audio power amplifier IC. It delivers up to 2.7W power into a 3 ohms load or 2.3W power into a 4 ohm load or 1.5W power into an 8 ohm load. Two patents are pending.

With common mode input structure, TMPA2055DM requires no input or output coupling capacitors. It also features high Common Mode Rejection Ratio and Power Supply Rejection Ratio.

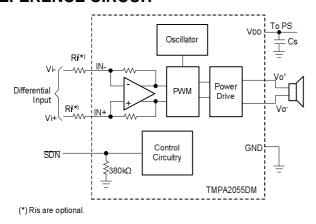
For multiple-input applications, independent gain control and corner frequency can be implemented by summing the input sources through resistor ratio and input capacitor values.

Analog input signal is converted into digital output which drives directly to the speaker. High power efficiency is achieved due to digital output at the load. The audio information is embedded in PWM (Pulse Width Modulation).

#### **APPLICATIONS**

Multimedia application includes Cellular Phones, PDAs, DVD/CD players, TFT LCD TVs/Monitors, 2.1 channel/5.1 channel audio systems, USB audio. It is also ideal for other portable devices like Wireless Radios.

#### REFERENCE CIRCUIT



#### **FEATURES**

- ♦ 4.5V to 5.5V Single Supply
- ♦ Up to 2.7W at 5V, 3 ohms
- ♦ Up to 85% Power Efficiency
- ♦ 2.2mA Quiescent Current at 5V
- ♦ Less Than 0.2uA Shutdown Current
- ◆ Popless Power-Up, Shutdown and Recovery
- ◆ Differential 230 KHz PWM Allows Bridge-Tied Load to

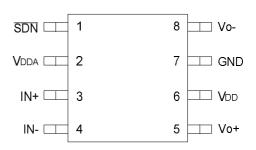
  Doubles Output Power and Eliminates LC Output

  Filter
- ◆ Common Mode Structure Requires No Input Capacitors
- **♦ BTL Output Requires No Output Capacitors**
- ◆ Thermal Shutoff and Automatic Recovery
- ◆ Short-Circuit Protection
- ♦ Differential Signal Processing Improves CMRR
- ♦ Package: TSSOP8, SOP8, MSOP8 Available

For best performance, please refer to

http://www.taimec.com.tw/data/Tmpa2055EVM/tmpa2055 dmEVM.pdf

for PCB layout.



# (Please email <u>david@taimec.com.tw</u> for complete datasheet.)

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Note that the external components or PCB layout should be designed not to generate abnormal voltages to the chip to prevent from latch up which may cause damage to the device.

#### **ABSOLUTE MAXIMUM RATINGS**

Over operating free-air temperature range unless otherwise noted(1)

Supply voltage Vpp	In normal mode	-0.3V to 6V	V	
Supply voltage, VDD	In shutdown mode	-0.3V to 7V	V	
Input voltage, Vı	-0.3V to VDD+0.3V	V		
Continuous total power dissipation	See package dissipation ra	See package dissipation ratings		
Operating free-air temperature, TA	-20 to 85	°C		
Operating junction temperature, TJ	-20 to 150	°C		
Storage temperature, Tstg	-40 to 150	°C		
Lead temperature 1,6mm(1/16 inch)from	260	°C		

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### RECOMMENDED OPERATING CONDITONS

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4.5		5.5	V
High-level input voltage, Vін	SDN	2		VDD	V
Low-level input voltage, V⊩	SDN	0		0.8	V
Input resistor, Ri	Gain ≤ 20 V/V (26dB)	0			kΩ
Common Mode Input Voltage Range	$V_{DD}=V_{DDA}=4.5V\sim5.5V$ , CMRR $\leq$ -55dB	0		VDD	V
Operating free-air temperature, TA		-20		85	°C

#### PACKAGE DISSIPATION RATINGS

PACKGE	DERATING	Ta≤25 °C	TA = 70 °C	TA = 85 °C
	FACTOR	POWER RATING	POWER RATING	POWER RATING
SOP8	6.39mW/ °C	0.799W	0.511W	0.415W

## **ELECTRICAL CHARACTERISTICS**

T<sub>A</sub>=25 °C (unless otherwise noted)

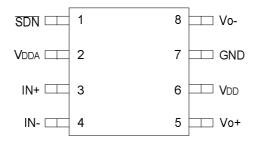
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vos	Output offset voltage (measured differentially)	VI=0V,AV=2, V <sub>DD</sub> =V <sub>DDA</sub> =4.5V to 5.5V		25		mV
PSRR	Power supply rejection ratio	$V_{DD}=V_{DDA}=4.5V$ to 5.5V		-75	-55	dB
CMRR	Common mode rejection ratio	$V_{DD}=V_{DDA}=4.5V$ to 5.5V, $V_{IC}=1V_{PD}$ , $RL=8\Omega$		-55		dB
IIH	High-level input current	$V_{DD}=V_{DDA}=5.5V$ , $V_{I}=5.8V$ ( $\overline{SDN}$ )			20	μΑ
IIL	Low-level input current	$V_{DD}=V_{DDA}=5.5V$ , $V_{I}=-0.3V$ ( $\overline{SDN}$ )			1	μΑ
IQ	Quiescent current	V <sub>DD</sub> =V <sub>DDA</sub> =5V, no load		2	3	mA
IQ (SD)	Shutdown current	V( SDN )=0.8V, V <sub>DD</sub> =V <sub>DDA</sub> =4.5V to 5.5V		0.2	0.5	μΑ
rDS(on)	Static drain-source on-state resistance	$V_{DD}=V_{DDA}=4.5V$		790		mΩ
f(sw)	Switching frequency	$V_{DD}=V_{DDA}=4.5V$ to 5.5V	200	230	260	kHz
Av	BTL Gain	$V_{DD}=V_{DDA}=4.5V$ to $5.5V$	<u>135kΩ</u> Rı+15kΩ	<u>150kΩ</u> Rı+15kΩ	<u>165kΩ</u> Rı+15kΩ	<u>V</u> V
	Resistance from shutdown to GND			380		kΩ

#### **OPERATING CHARACTERISTICS**

 $T_A=25$  °C, Av=2, RL=8 $\Omega$  speaker (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN TYP MA	X UNIT
Ро	Output power	THD+N=10%,f=1kHz, RL=8 $\Omega$	V <sub>DD</sub> =V <sub>DDA</sub> =5V	1.5	W
Ро	Output power	THD+N=10%,f=1kHz, RL=4 $\Omega$	V <sub>DD</sub> =V <sub>DDA</sub> =5V	2.3	W
Ро	Output power	THD+N=10%,f=1kHz, RL=3 $\Omega$	V <sub>DD</sub> =V <sub>DDA</sub> =5V	2.7	W
		$V_{DD}$ = $V_{DDA}$ = $5V$ , Po= $0.85W$ , RL= $8\Omega$ , f= $1kHz$		0.55	
THD+N	Total harmonic distortion plus noise	$V_{DD}=V_{DDA}=5V$ , Po=1.3W, RL=4 $\Omega$ , f=1kHz		0.55	%
		$V_{DD}=V_{DDA}=5V$ , Po=1.5W, RL=3 $\Omega$ , f=1kHz		0.64	
SNR	Signal-to-noise ratio	$V_{DD}$ = $V_{DDA}$ =5V, Po=1W, RL=8 $\Omega$		84	dB
Zı	Input impedance			13.5 15 16.	<sub>5</sub> kΩ

#### **TOP VIEW**



## **TERMINAL FUNCTIONS**

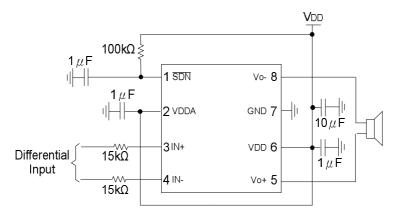
TERMINAL		.,0	DECODURE	
NAME	PIN NO	I/O	DESCRIPTION	
IN-	4	I	Negative differential input	
IN+	3	I	Positive differential input	
Vdd	6	I	Digital Power supply	
Vo+	5	0	Positive BTL output	
GND	7	I	igital ground	
<u>Vo-</u>	8	0	Negative BTL output	
SDN	1	I	Shutdown terminal (active low logic)	
Vdda	2	I	Analog Power supply	

## **TYPICAL CHARACTERISTICS**

Note 1. Input coupling  $1\mu F$  capacitors are used for all measurements.

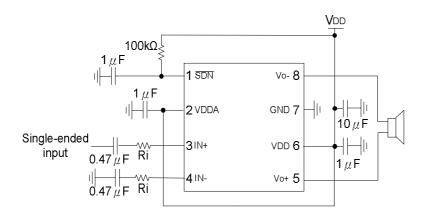
- 2. Differential inputs are applied and BTL outputs are measured.
- 3. Balanced LC filter is used for THD+N measurement and power efficiency measurement.
- 4. Characteristic frequency of the LC filter is set 41KHz unless otherwise specified.

# **APPLICATION INFORMATION**



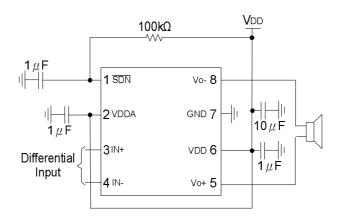
Suppose source impedance of the input is relatively smaller than 15k ohms.

Figure.1 Differential Input With Gain=  $\frac{150k}{15k+15k}$  = 5



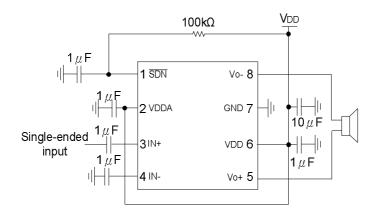
Ri=15k ohms if source impedance of the input is relatively smaller than 15k ohms.

Figure.2 Single-ended Input With Gain=  $\frac{150k}{15k+Ri}$ 



Suppose source impedance of the input is much smaller than 15k.

Figure.3 Differential Input With Gain= 
$$\frac{150k}{15k}$$
 = 10



Suppose source impedance of the input is much smaller than 15k.

Figure.4 Single-ended Input With Gain=
$$\frac{150k}{15k}$$
 = 10

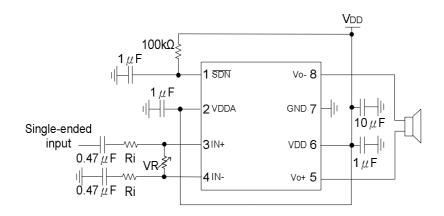


Figure.5 Single-ended Input With Gain Control

Note: Please refer to document 010 APP for more application examples.

Figure 5 ~7 show typical ferrite bead and LC output filters.

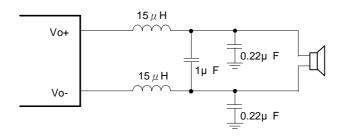


Figure 5. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance= $4\Omega$ 

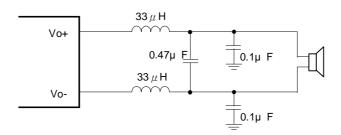


Figure 6. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance= $8\Omega$ 

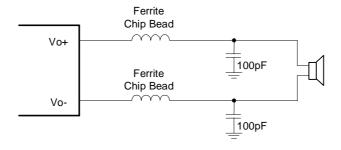
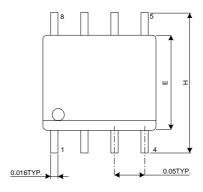
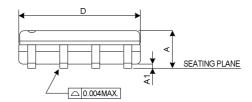


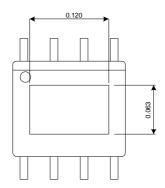
Figure 7. Typical Ferrite Chip Bead Filter (Chip bead example:遠越科技 KML2012Q102N 1kohms@100MHz, DCR=0.2ohms, I=1A)

# I Input Resistors and Gain

# Physical Dimensions (IN MILLIMETERS)



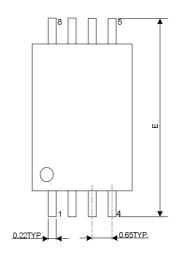


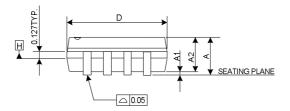


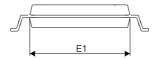
SYMBOLS	MIN.	MAX.
Α	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
Н	0.228	0.244

SOP8

# Physical Dimensions (IN MILLIMETERS)







SYMBOLS	MIN.	NDM.	MAX.	
Α	-	-	1.20	
A1	0.05	-	0.15	
A2	0.96	1.01	1.06	
D	2.90	3.00	3.10	
E	6.40 BSC			
E1	4.30	4.40	4.50	

TSSOP8

May 5, 2005

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