OKI Semiconductor

MSM60801

PCMCIA Card Interface LSI

DESCRIPTION

The MSM60801 is a general purpose, single-chip PCMCIA interface, which integrates all necessary functions to implement a PCMCIA 2.0 socket interface to a wide variety of I/O and memory cards. To ease microcontroller usage and overhead, the MSM60801 controls the PCMCIA interface, serial EEPROM interface, and I/O interfaces directly. Support for UARTs, modems, Ethernet, and other peripheral devices is performed through memory and I/O mapped PCMCIA to local peripheral components.

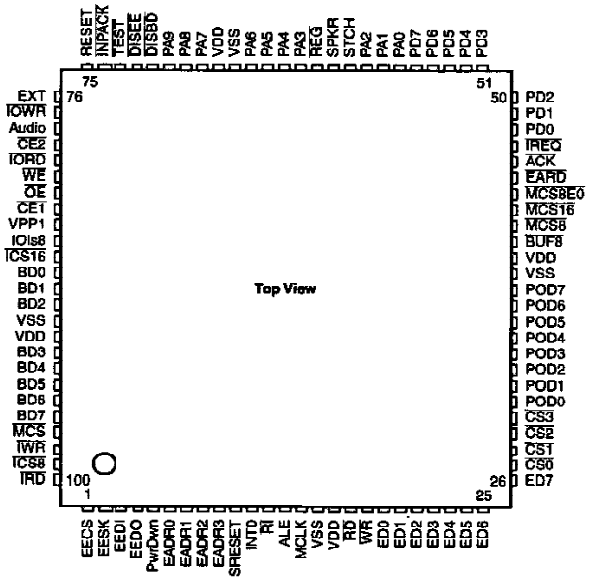
All attribute memory, ranges, interrupts, and Card Configuration Registers (CCR) are controlled via the MSM60801 with processor intervention. A serial EEPROM, holding the Card Information Structure (CIS) data, is loaded into the internal 120-byte attribute memory which provides a buffer for memory read/write operations. Card Configuration Register (CCR) operations, per PCMCIA 2.0, ease firmware considerations. The address decoder and interrupt logic is configurable, based on the application requirements.

The MSM60801 offers an enhanced feature set, including control signals for external drivers, 8-bit port access, and power reduction capabilities. New card designs will greatly benefit from this single chip solution, consuming less than 2 mW during operation. The MSM60801 was design using OKI's high-quality CMOS process, providing unrivaled low-power performance. To minimize board space usage, this new controller is offered in a 100-pin TQFP (TS-K) package.

FEATURES

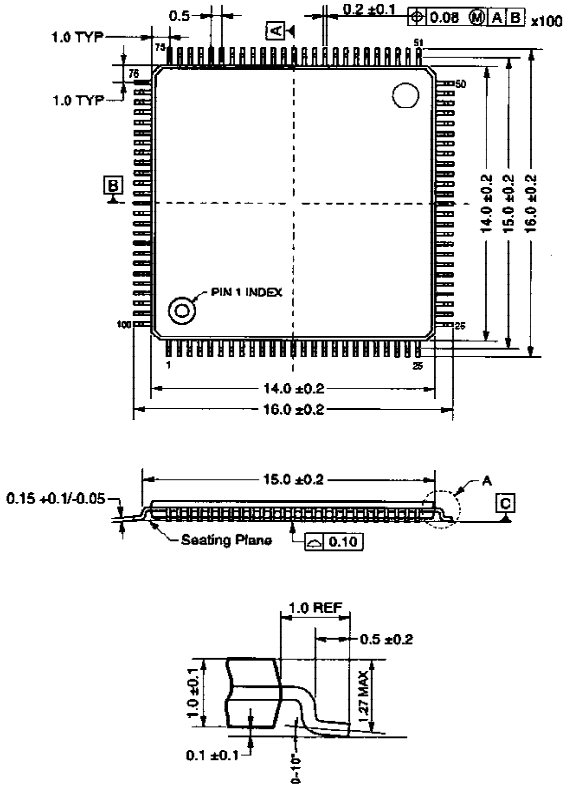
- 120-byte internal memory for tuple information
- Full support of external attribute memory for extended code
- Multiple configuration registers conforming to PCMCIA 2.0
- EXCA register-compatible, allowing direct plug and play
- Automatic loading from EEPROM of register and tuple data reduces costs
- Supports both 8-bit and 16-bit operations, based on peripheral requirements
- Control signals for external drivers
- Latch-up proof for currents on the input and output pins less than 200 mA
- Inputs are protected against electrostatic discharge less than 2 kV (MIL-STD 883C 3015.2)
- Configurable address decoder and interrupt logic eliminate microcomputer involvement
- Extremely low-power consumption (2 mW) increases battery life
- Configurable bidirectional port for read/write operations through periphery data bus speed address mapping
- 100-pin TQFP (TQFP100-P-1420-K) package available

PIN CONFIGURATION

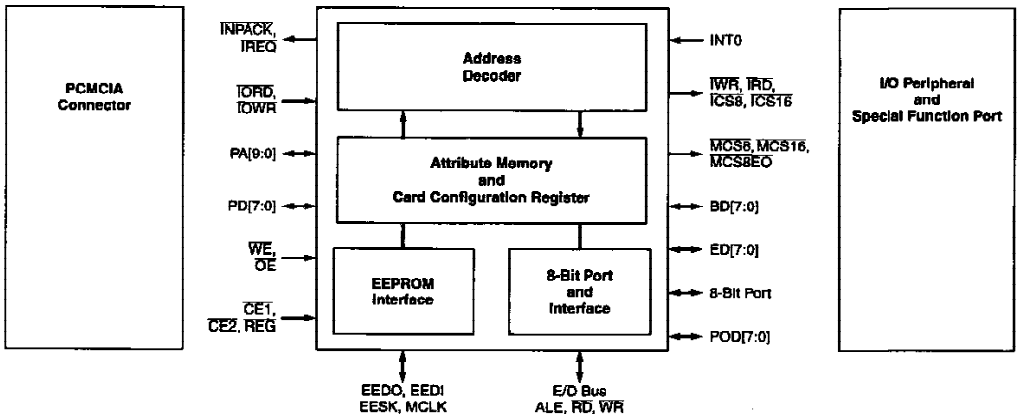


Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	EECS	18	$\overline{WR}$	35	POD4	52	PD4	69	PA8	86	$\overline{ICS16}$
2	EESK	19	ED0	36	POD5	53	PD5	70	PA9	87	BD0
3	EEDI	20	ED1	37	POD6	54	PD6	71	$\overline{DISBD}$	88	BD1
4	EEDO	21	ED2	38	POD7	55	PD7	72	$\overline{DISEE}$	89	BD2
5	PwrDwn	22	ED3	39	VSS	56	PA0	73	$\overline{TEST}$	90	VSS
6	EADR0	23	ED4	40	VDD	57	PA1	74	$\overline{INPACK}$	91	VDD
7	EADR1	24	ED5	41	$\overline{BUF8}$	58	PA2	75	RESET	92	BD3
8	EADR2	25	ED6	42	$\overline{MCS8}$	59	STCH	76	EXT	93	BD4
9	EADR3	26	ED7	43	$\overline{MCS16}$	60	SPKR	77	$\overline{IOWR}$	94	BD5
10	SRESET	27	$\overline{CS0}$	44	$\overline{MCS8E0}$	61	$\overline{REG}$	78	Audio	95	BD6
11	INTO	28	$\overline{CS1}$	45	$\overline{EARD}$	62	PA3	79	$\overline{CE2}$	96	BD7
12	$\overline{RI}$	29	$\overline{CS2}$	46	$\overline{ACK}$	63	PA4	80	$\overline{IORD}$	97	$\overline{MCS}$
13	ALE	30	$\overline{CS3}$	47	$\overline{IREQ}$	64	PA5	81	$\overline{WE}$	98	$\overline{IWR}$
14	MCLK	31	POD0	48	PD0	65	PA6	82	$\overline{OE}$	99	$\overline{ICS8}$
15	VSS	32	POD1	49	PD1	66	VSS	83	$\overline{CET}$	100	$\overline{IRD}$
16	VDD	33	POD2	50	PD2	67	VDD	84	VPP1		
17	$\overline{RD}$	34	POD3	51	PD3	68	PA7	85	IOis8		

TQFP100-P-1420-K PACKAGING



BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Name	Pin Type	Description
EECS	O active-high	**EEPROM Interface.** EECS = high indicates an EEPROM was selected. Chip select line to EEPROM active high.
EESK	O	**EEPROM Interface.** Synchronization clock to EEPROM.
EEDI	O	**EEPROM Interface.** Serial data line to EEPROM.
EEDO	I	**EEPROM Interface.** Serial data line from EEPROM.
PwrDwn	O	**Special Functions Interface.** Indicates the status of PwrDwn in the Card Configuration Register (CCR). PwrDwn = high if PwrDwn is set and all 3-state outputs are 3-stated.
EADR[3:0]	I	**Special Functions Interface.** Address bus for chip select $\overline{CS}$[3:0] port and the Peripheral Configuration Register (M0).
SRESET	O 3-state	**Special Functions Interface.** SRESET = high indicates a reset using RESET or SRESET.
INTO	I Schmitt Trigger	**I/O Interface.** INTO = high indicates the periphery is connected to the I/O interface requires the interface chip (MSM60801) to request an interrupt from the host computer using $\overline{IREQ}$.
$\overline{RI}$	I Schmitt Trigger	**Special Functions Interface.** When RIEN is set in the Card Configuration Register (CCR), STCH reflects the signal $\overline{RI}$.
ALE	I active-high	**Special Functions Interface.** EXT = high multiplexes ED[7:0] from address bus to data bus.
MCLK	I	**I/O Interface.** Clock for state machine and pulsed interrupt: 5 MHz < MCLK < 30 MHz.
V_{SS}		Power supply
V_{DD}		Power supply
$\overline{RD}$	I active-low	**Special Functions** Interface. When $\overline{RD}$ = low, the contents of the register addressed using EADR[3:0] appear (MCS = low) on the data bus ED[7:0].
$\overline{WR}$	I active-low	**Special Functions Interface.** When $\overline{WR}$ = low, the MSM60801 transfers the word on the ED[7:0] data bus to the register addressed using EADR[3:0].
ED[7:0]	I/O	**Special Functions Interface.** Data bus/address bus for special function port.
$\overline{CS}$[3:0]	O 3-state	**Special Functions Interface.** Select outputs dependent on the address at EADR[3:0] and $\overline{MCS}$.
POD[7:0]	I/O	**Special Functions Interface.** Inputs and outputs of special function port.
$\overline{BUF8}$	O 3-state	**Special Functions Interface.** Signal to control external memory buffer.
$\overline{MCS8}$	O 3-state	**Special Functions Interface.** Signal to control external memory buffer.
$\overline{MCS16}$	O 3-state	**Special Functions Interface.** Signal to control external memory buffer.
$\overline{MCS8EO}$	O 3-state	**Special Functions Interface.** Signal control an external memory buffer.
$\overline{EARD}$	O active-low	**Special Functions Interface.** Chip select for external attribute memory.
$\overline{ACK}$	O active-low	**I/O Interface.** When $\overline{ACK}$ = low indicates that the address applied to PA[9:0] is within the configured address range.
$\overline{IREQ}$	O active-low 8 mA driver	**PCMCIA Interface.** $\overline{IREQ}$ = low indicates the host requested an interrupt from the I/O range using the INTO signal. $\overline{IREQ}$ is monitored by the socket service and, dependent on the configuration, is connected to one of the host interrupts, for example a COM1 or COM2 interrupt. $\overline{IREQ}$ is activated from the Card Configuration Register (CCR) which enables either pulsed-interrupt (D6 = low) with minimal pulse length of 1 µs, or a level-interrupt (D6 = high) which is reset when interrupt is processed by the host.

PIN DESCRIPTIONS (Continued)

Pin Name	Pin Type	Description
PD[7:0]	I/O 4 mA driver	**PCMCIA Interface.** Data lines from/to the PCMCIA interface which read attribute memory, read/write the Card Configuration Register (CCR), and exchange data with the I/O interface.
PA[9:0]	I	**PCMCIA Interface.** Address lines which contain the attribute memory address and the Card Configuration Register (CCR), as well as the driving address decoder.
STCH	O 8 mA driver	**PCMCIA Interface.** When RIEN is set in the Card Configuration Register (CCR), the signal at $\overline{RI}$ is reflected on STCH; in all other cases STCH = high.
SPKR	Fan-out 8 mA driver	**PCMCIA Interface.** If Audio is set in the Card Configuration Register (CCR) and the MSM60801 is configured, the inverted signal of Audio is reflected on SPKR; in all other cases SPKR = high.
$\overline{REG}$	I active-low pull-up >10k	**PCMCIA Interface.** $\overline{REG}$ = low indicates a read or write access to the attribute memory range ($\overline{OE}$ and $\overline{WR}$), or to the I/O address range ($\overline{IOWR}$ and $\overline{IORD}$). For access to the common memory, PCMCIA requires $\overline{REG}$ = high.
$\overline{DISBD}$	I active-low pull-up > 10k	**I/O Interface.** When $\overline{DISBD}$ = low and PD[7:0] is configured as inputs for I/O read access, the integrated I/O driver is not used.
$\overline{DISEE}$	I active-low pull-up > 10k	**I/O Interface.** $\overline{DISEE}$ = low disables the $\overline{BUSY}$ signal of the internal state machine. Attribute memory can only be written to or from the Special Function Interface.
$\overline{TEST}$	I pull-up > 10k	**Test Pin.** $\overline{TEST}$ = high indicates the state machine is clocked at CLK/128. $\overline{TEST}$ = low indicates the state machine is clocked at CLK/2.
$\overline{INPACK}$	O active-low 8 mA driver	**PCMCIA Interface.** $\overline{INPACK}$ = low indicates a successful I/O read access. If the MSM60801 is configured independent of the address, it reacts to all I/O read cycles, and activates $\overline{INPACK}$ with $\overline{IORD}$. $\overline{ACK}$ = low indicates the applied address correlates with the configured I/O address range.
RESET	I active-high Schmitt Trigger	**PCMCIA Interface.** RESET = high resets the MSM60801 and clears the Card Configuration Register (CCR). Until configured again, the MSM60801 behaves as a memory-only interface. The EEPROM content is copied into attribute memory, and during copying, $\overline{IREQ}$ is activated by the MSM60801.
EXT	I active-high pull-up > 10k	**I/O Interface.** EXT = high enables writing to attribute memory from the special function port/interface.
$\overline{IOWR}$	I active-low pull-up > 10K	**PCMCIA Interface.** $\overline{IOWR}$ = low indicates a WR signal for write access to the I/O range. $\overline{IOWR}$ is passed on as $\overline{IWR}$ to the I/O range. $\overline{ACK}$ = 0 is the address applied to PA[9:0] within the configured address range.
Audio	I Schmitt-Trigger	**Special Functions Interface.** If Audio is set in the Card Configuration Register (CCR) and the MSM60801 is configured, the inverted signal of Audio is reflected on SPKR; in all other cases SPKR = high.
$\overline{CE2}$	I active-low pull-up > 10k	**PCMCIA Interface.** $\overline{CE2}$ = low enables an odd numbered of address bytes for example, an A0 = high address. If an address is applied with A0 = high, it can be processed only with $\overline{CE2}$ = low. Note that even numbered addresses are not released with $\overline{CE2}$ = low.
$\overline{IORD}$	I active-low pull-up > 10K	**PCMCIA Interface.** $\overline{IORD}$ = low indicates an $\overline{RD}$ signal for read access to the I/O range. $\overline{IORD}$ is passed on as $\overline{IRD}$ to the I/O range. $\overline{ACK}$ = 0 when the address applied to PA[9:0] is within the configured address range.
$\overline{WE}$	I active-low pull-up > 10K	**PCMCIA Interface.** $\overline{WE}$ is used to write data on the data bus PD[7:0] to attribute memory, or to the Card Configuration Register (CCR) addressed via PA[9:0]. $\overline{IREQ}$ = high indicates the interface is configured as a memory-only interface.
$\overline{OE}$	I active-low pull-up > 10k	**PCMCIA Interface.** $\overline{OE}$ = low brings attribute memory or Card Configuration Register (CCR) contents selected via PA[9:0] to the data bus PD[7:0].
$\overline{CE1}$	I active-low pull-up > 10k	**PCMCIA Interface.** When $\overline{CE1}$ = low even numbered address bytes are enabled, for example and address with A0 = low. If an address is applied with A0 = low, it is processed only with $\overline{CE1}$ = low. Note that odd numbered addresses are not released with $\overline{CE1}$ = low. For access to attribute memory and configuration registers, addresses with A0 = low are the only valid addresses.

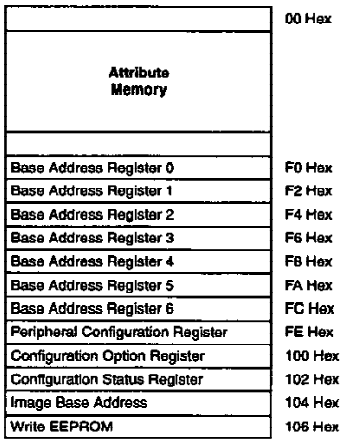
PIN DESCRIPTIONS (Continued)

Pin Name	Pin Type	Description
V_{PP1}	I Schmitt-Trigger	**PCMCIA Interface.** V_{PP1} programming voltage control line which enables a write to attribute memory and to the EEPROM.
IOis8	O	**Special Functions Interface.** Output reflects the IOis8 status in the Card Configuration Register (CCR).
$\overline{ICS16}$	O active-low 3-state	**I/O Interface.** $\overline{ICS16}$ = low indicates an I/O interface for 16-bit access. $\overline{ACK}$ = 0 indicates the PA[9:0] address is within range.
BD[7:0]	I/O	**I/O Interface.** Bidirectional data line to I/O interface
$\overline{MCS}$	I active-low	**Special Functions Interface.** $\overline{MCS}$ = low enables access to registers and ports in the special function range.
$\overline{IWR}$	O active-low 3-state	**I/O Interface.** $\overline{IWR}$ = low indicates the host I/O interface is configured with $\overline{IOWR}$ passed on as $\overline{IWR}$ on the I/O interface, if the PA[9:0] address is within the configured address range. $\overline{ACK}$ = 0 indicates the PA[9:0] address is within the range.
$\overline{ICS8}$	O active-low 3-state	**I/O Interface.** $\overline{ICS8}$ = low indicates the I/O interface for 8-bit access. $\overline{ACK}$ = 0 indicates the PA[9:0] address is within range.
$\overline{IRD}$	O active-low 3-state	**I/O Interface.** $\overline{IRD}$ = low indicates the host I/O interface is configured, with $\overline{IORD}$ passed on as $\overline{IRD}$ on the I/O interface, if the PA[9:0] address is within the configured address range. $\overline{ACK}$ = 0 indicates the PA[9:0] address is within range.

FUNCTIONAL DESCRIPTION

Attribute Memory

Attribute memory contains 120 x 8 bits of RAM, which is normally write protected, and starts at address 00 hex. Additionally, several registers are contained within attribute memory for PCMCIA programming of both the MSM60801 and the Configuration Registers. For additional information on attribute memory, refer to *"Configuration Registers"* and the following figure.



For access to attribute memory, only addresses with PA0 = 0 are valid (even numbered address bytes). Attribute memory is reloaded from the serial EEPROM for hardware resets via RESET or for soft resets via the Card Option Register (COR). Attribute memory stores, among other data, the Card Information Structure (CIS) data the host needs to configure a PCMCIA card. An option is available to access extended external attribute memory. If 200 hex to 3FF hex addresses are accessed, the MSM60801 generates a chip select signal on the $\overline{EARD}$ pins.

Attribute Memory Read

Read accesses to attribute memory are explained in this section. The host applies an address of the attribute memory via the address lines PA[9:0] to the MSM60801, selects an "even-byte" access to the card with $\overline{CE}$ = 0, and pulls $\overline{REG}$ and $\overline{OE}$ low.

Function Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	PA0	$\overline{OE}$	$\overline{WE}$	PD[7:0]
Standby mode	X	H	H	X	X	X	High-Z
8-bit byte access	L	H	L	L	L	H	Even byte
	L	H	L	H	L	H	Not valid
16-bit byte access	L	L	L	X	L	H	Even byte
Odd-byte-only access	L	L	H	X	L	H	High-Z

Attribute Memory Write

Under normal operation, attribute memory is write protected except the Configuration Registers. To write to the CIS-range within the attribute memory, V_{PP1} must be high. The host applies the byte address of the attribute memory via the address lines PA[9:0] to the MSM60801, selects an "even-byte" access to the card with $\overline{CE1}$=0, and pulls $\overline{REG}$ and $\overline{WE}$ low. The last valid condition of the data PD[7:0] before $\overline{WE}$ or before $\overline{CE1}$ returns to high and is stored as a valid data word.

Function Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	PA0	$\overline{OE}$	$\overline{WE}$	PA[7:0]
Standby mode	X	H	H	X	X	X	XXX
8-bit byte access	L	H	L	L	H	L	Even byte
	L	H	L	H	H	L	XXX
16-bit byte access	L	L	L	X	H	L	Even byte
Odd-byte-only access	L	L	H	X	H	L	XXX

For V_{PP1} = high, only the volatile copy of the MSM60801 attribute memory is written to, not to the static attribute memory in the EEPROM. To copy the contents of the MSM60801 attribute memory to the EEPROM, V_{PP1} needs to be set "high," and a write access to address 106 hex must be performed. The MSM60801 starts to erase the EEPROM and copies the attribute memory and the available base addresses to the EEPROM.

I/O Interface

The I/O interface consists of the major MSM60801 functions. The device enables I/O access of the host as an address decoder, according to the PCMCIA standard. The host writes the base address and size (window size) of the address range, acting as I/O address range, to the Configuration Option Register (COR). After configuration, the MSM60801 recognizes I/O accesses to this address range and passes the information to the I/O interface. Reference to $\overline{ACK}$ is made at various places in this data sheet.

Internal signals to the MSM60801 go low when the address applied to PA[9:0] is within the configured address range. The chip selects $\overline{ICS8}$ for 8-bit and $\overline{ICS16}$ for 16-bit access and is active only when a valid when I/O access is performed and the address is within the configured address range.

The BD data bus, $\overline{IWR}$ and $\overline{IRD}$, are used for applications without a bus interface. These signals can also be used to reduce power-consumption in applications with a bus interface when the timing requirements of the BD data bus and the control signals are fulfilled. In other cases, the application has to use the PD bus and the $\overline{IOWR}$ and $\overline{IORD}$ of the PCMCIA interface.

I/O Interface Write

$\overline{IWR}$ is the write signal to the periphery connected to the I/O interface (such as a modem). In case of a valid I/O-write-access to the configured address range the input signal $\overline{IOWR}$ is passed on as $\overline{IWR}$. If the access is not valid, $\overline{IWR}$ remains high:

$$\overline{IWR} = \overline{IOWR} + \overline{REG} + \overline{ACK} + (\overline{CE1} * \overline{CE2})$$

Function Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	PA0	$\overline{IORD}$	$\overline{IOWR}$	$\overline{IRD}$	$\overline{IWR}$	PD[7:0]
Standby mode	X	H	H	X	X	X	H	H	XXXX
8-bit byte access	L	H	L	L	H	L	H	$\overline{IOWR}$	Even byte
	L	H	L	H	H	L	H	$\overline{IOWR}$	Odd byte
16-bit word access	L	L	L	L	H	L	H	$\overline{IOWR}$	Even byte
Odd-byte-only access	H	X	X	X	H	L	H	H	XXXX

I/O Interface Read

$\overline{IRD}$ is the read signal to the periphery connected to the I/O interface (for example, modem). In case of a valid I/O-read-access to the configured address range, $\overline{IORD}$ is passed on as $\overline{IRD}$. If the access is not valid, $\overline{IRD}$ remains high:

$$\overline{IRD} = \overline{IORD} + \overline{REG} + \overline{ACK} + (\overline{CE1} * \overline{CE2})$$

Function Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	PA0	$\overline{IORD}$	$\overline{IOWR}$	$\overline{IRD}$	$\overline{IWR}$	PD[7:0]
Standby mode	X	H	H	X	X	X	H	H	XXXX
8-bit byte access	L	H	L	L	L	H	$\overline{IORD}$	H	Even byte
	L	H	L	H	L	H	$\overline{IORD}$	H	Odd byte
16-bit word access	L	L	L	L	L	H	$\overline{IORD}$	H	Even byte
Odd-byte-only access	H	X	X	X	L	H	H	H	XXXX

Card Reset and Load

After a RESET, the host waits at least 20 ms for setup before MSM60801 access is allowed. The MSM60801 sets $\overline{IREQ}$ low to avoid being accessed. As every PCMCIA card after RESET is unconfigured and seen as a memory-only card, $\overline{IREQ}$ acts as $\overline{BUSY}$. $\overline{IREQ}$ = low tells the host the MSM60801 is not yet capable of reacting to host access.

After a RESET, attribute memory and the available base addresses for the address decoder and the Peripheral Control Register are loaded from an EEPROM connected to the EEPROM interface. When the load procedure is complete, the busy signal is removed, for example $\overline{IREQ}$ goes high again. Time for completion of the load procedure can be calculated as follows:

$$tw_{\overline{IREQ}}\ (ms) = 0.6 / clock\ frequency\ (MCLK/MHz)$$

Attribute memory can now be read by the host, and registers can be accessed.

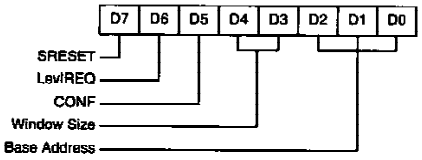
REGISTERS

Configuration Registers

The MSM60801 has two configuration registers for PCMCIA 2.0 standards, the Configuration Option Register (COR) and the Card Configuration Register (CCR), as well as the Chip Version Number Register (CVR) which is used for the version number of the chip.

Configuration Option Register
Index: 100 Hex

The Configuration Option Register (COR), located on one side, is used to configure the MSM60801. On the other side of the Configuration Option Register, a reset can be triggered by setting a particular bit.



Bit(s)	Configuration Option Register Description
D7 SRESET	When SRESET = 1, a reset is initiated. This reset differs from the one forced by a "high" on the RESET input only by not resetting the bit SRESET. The attribute memory is loaded newly. With the SRESET signal the external periphery can be reset, this signal is also active during a hardware RESET.
D6 LevIREQ	When LevIREQ = high, the $\overline{IREQ}$ pin operates as a Level Interrupt. When LevIREQ = low, the interrupt is a pulse. The width of the interrupt pulse is calculated as: $tw_{\overline{IREQ}}$ (µs) = 48/clock frequency (MCLK / MHz).
D5 CONF	When CONF = high, the PCMCIA interface of the MSM60801 is configured as I/O and I/O access is permitted.
D4, D3 Window Size	Window size contains the size of the address window, which is written by the host and used by the address decoder to decode. D4 / D3 / Window Size: 0 / 0 / 8 byte; 0 / 1 / 16 byte; 1 / 0 / 32 byte; 1 / 1 / 64 byte
D2, D1, D0 Base Address	These three bits select the base address register containing the start address of the address window to be decoded. Refer to *"Base Address Registers"* for additional information.

Base Address Registers

The following table lists the start address of the address windows to be decoded.

D3	D2	D0	Base Address Register Selection
0	0	0	Base Address Register 0
0	0	1	Base Address Register 1
0	1	0	Base Address Register 2
0	1	1	Base Address Register 3
1	0	0	Base Address Register 4
1	0	1	Base Address Register 5
1	1	0	Base Address Register 6
1	1	1	Reserved

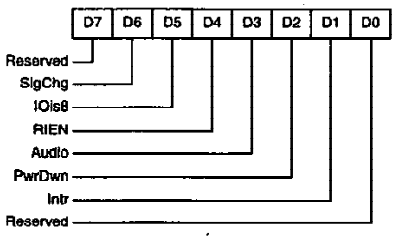
There are seven base address registers whose content is loaded after a RESET from the EEPROM. The base address registers are in the attribute memory range and can only be written to when V_{PP1} = high.

D7 - D0	Base Address
Base Address 0	F0 hex
Base Address 1	F2 hex
Base Address 2	F4 hex
Base Address 3	F6 hex
Base Address 4	F8 hex
Base Address 5	FA hex
Base Address 6	FC hex

The start address is within the 10-bit address range of the MSM60801, selectable in 4-byte steps, where the 2 lower address bits are 0 and the upper 8 bits of the address are stored as the base address in the base address register (e.g., start address 3F8 hex = FE hex in the base address register). If the content of the base address register is "00" hex, and that base address is selected, every I/O access ($\overline{IOWR}$, $\overline{IORD}$, $\overline{ICS}$, etc.) is passed on to the I/O interface (independent address window).

Card Configuration Register
Index: 102 Hex

The Card Configuration Register (CCR) contains information about the status of the card and releases various I/Os of the MSM60801.



Bit(s)	Card Configuration Register Description
D6 SigChg	This bit has no function and has a readable status.
D5 IOis8	When IOis8 = high, this bit provides high output.
D4 RIEN	When RIEN = high this bit is set and the card is configured, and STCH outputs the inverse signal of $\overline{RI}$; otherwise STCH = high.
D3 Audio	When Audio = high this bit is set and the card is configured, and SPKR has the inverse output signal of Audio; otherwise SPKR = high.
D2 PwrDwn	When PwrDwn = high, the contents of this bit is output to the PwrDwn pin.
D1 Intr	The contents of Intr reflect the status of the INTO pin and is read-only.

Chip Version Number Register
Index: 180 Hex ~ 1FE Hex

The Chip Version Number Register (CVR) is an 8-bit code used for the chip version number, and is read only.

Image Base Address Register
Index: 104 Hex

The Image Base Address Register (IBR) is an 8-bit wide code which provides a copy of the configured base address, and is read-only.

Configuration Register Read

Read access to one of the Configuration Registers does not differ from the read access to attribute memory.

Configurations Register Write

Write access to one of the Configuration Registers differs from write access to attribute memory only because it is also possible when V_{PP1} = low.

Peripheral Configuration Register

The Peripheral Configuration Register (M0) is in attribute memory range and can be written to only when V_{PP1} = high. The contents of the Peripheral Configuration Register are stored in the EEPROM. This register can be read from the connected peripheral and the special function data bus ED[7:0] at address EADR[3:0] = 2. The content of the Peripheral Configuration Register is brought to ED[7:0] inverted.

EEPROM INTERFACE

The MSM60801 is connected via a serial EEPROM interface to a 128x8 EEPROM. The serial receive and transmit data transfer is synchronized by the EESK signal, with a square wave of the frequency CLK/128. EESK is generated only when the EEPROM is accessed, such as during initialization after a RESET and a write to the EEPROM (V_{PP1} = high). Data lines EEDO and EEDI are latched with the rising edge of EESK, and start a write access only when V_{PP1} is set to high. Fore additional infomation on the EEPROM interface, refer to the *"MSM60801 PCMCIA Card Interface LSI Application Note"*.

To start a write access, address 106 hex in attribute memory must to be written to. Once attribute memory has been written to, access is not possible until writing is complete. If the MSM60801 is not configured as an I/O interface, $\overline{IREQ}$ becomes active (low) during write access.

EEPROM Read Address

To read data from the EEPROM, EECS must be set to high. The MSM60801 then transmits a 'read' command to the EEPROM on line EEDI. The format is shown in the following table.

Read Op Code 10		
0	Clock idle	0
1	Clock start	1
2	Op code 1B	1
3	Op code 2B	0
4	Address	A6
5	Address	A5
6	Address	A4
7	Address	A3
8	Address	A2
9	Address	A1
10	Address	A0
11	Dummy	0

The next eight clock cycles deliver the data of the addressed EEPROM memory cell via EEDO. The read access is complete by pulling EECS low. The format is shown in the following table.

Read Op Code 10		
12	Data	D7
13	Data	D6
14	Data	D5
15	Data	D4
16	Data	D3
17	Data	D2
18	Data	D1
19	Data	D0
20	Dummy	0

EEPROM Write Address

To write data to the EEPROM it is activated by setting EECS to high. After a 'write' command, the address and the data word to be stored are transmitted via EEDI to the EEPROM. After this sequence a pulse of 1 µs minimum is transmitted on EECS, the EEPROM confirms successful write access with a high signal on EEDO. The format is shown in the following table.

Write Op Code 01		
0	Clock idle	0
1	Clock start	1
2	Op code 1B	1
3	Op code 2B	0
4	Address	A6
5	Address	A5
6	Address	A4
7	Address	A3
8	Address	A2
9	Address	A1
10	Address	A0
11	Data	D7
12	Data	D6
13	Data	D5
14	Data	D4
15	Data	D3
16	Data	D2
17	Data	D1
18	Data	D0
19	Dummy	0
20	Dummy	0

EEPROM Erase Address

To erase the EEPROM, it is activated by setting EECS to high. The 'erase' command is then transmitted via EEDI to the EEPROM. The format is shown in the following table.

Erase Op Code 010		
0	Clock idle	0
1	Clock start	1
2	Op code 1B	0
3	Op code 2B	0
4	Op code 3B	1
5	Op code 4B	0
6	Dummy	0
7	Dummy	0
8	Dummy	0
9	Dummy	0
10	Dummy	0
11	Dummy	0

After this sequence, a low pulse of 1 µs is transmitted via EECS, and the EEPROM answers with a high signal on EEDO upon a successful erase access. The erase process is performed only in conjunction with a write process. For a write access, the whole EEPROM is first erased and then written to.

EEPROM Erase / Write Enable Address

To program the EEPROM, it is first activated by setting EECS to high. EWEN is then transmitted via EEDI to the EEPROM. EWEN is used by the MSM60801, only in conjunction with a write process. The format is shown in the following table.

Erase/write Enable Op Code 011		
0	Clock idle	0
1	Clock start	1
2	Op code 1B	0
3	Op code 2B	0
4	Op code 3B	1
5	Op code 4B	1
6	Dummy	0
7	Dummy	0
8	Dummy	0
9	Dummy	0
10	Dummy	0
11	Dummy	0

SPECIAL FUNCTIONS

Address Mapping

By use of the peripheral data bus ED[7:0], it is possible to read out the Peripheral Configuration Register (M0) and configure a bidirectional port to read or write. The peripheral address bus enables addressing of these functions and generates various chip selects ($\overline{CS}$[3:0]). For each of these accesses, $\overline{MCS}$ is to be pulled low. For read and write access, $\overline{RD}$ is to be pulled low.

EADR[3:0]	Register	$\overline{CS}$[3:0]
0 hex	–	$\overline{CS1}$ = 0
1 hex	–	–
2 hex	Peripheral Configuration Register	–
3 hex	–	–
4 hex	–	$\overline{CS2}$ = 0
5 hex	–	–
6 hex	Bidirectional port	$\overline{CS3}$ = 0
7 hex	Configuration port	–
8 hex	–	$\overline{CS0}$ = 0
9 hex	–	$\overline{CS0}$ = 0
A hex	–	$\overline{CS0}$ = 0
B hex	–	$\overline{CS0}$ = 0
C hex	–	$\overline{CS0}$ = 0
D hex	–	$\overline{CS0}$ = 0
E hex	–	$\overline{CS0}$ = 0
F hex	–	$\overline{CS0}$ = 0

ED[7:0] are data bus connections and POD[7:0] are port I/Os. The direction of the port, address 6 hex, is changed by the Configuration Register of that particular port at address 7 hex (ED[7:0] = low -> POD[7:0] = input). After a RESET, the port is configured as input. When configured as output, the output value can be read back.

Note: Each bit on the port can be programmed independently, either as input or output.

Attribute Memory Description for EXT = 1 Only

If after a RESET and while busy is still set, a logic "1" is written to ED[7:0] at memory location D7 of the Peripheral Configuration Register and can only be written to when EXT = 1. The MSM60801 switches to a special mode where it can be written to attribute memory via data lines ED[7:0]. $\overline{CS0}$ then selects the attribute memory, and the ED[7:0] bus, in this case, is common address bus and data bus.

When ALE = high the address of the attribute memory (00 hex - 7F hex) on the data bus ED[7:0] is stored in which during ALE = low a data word is written with $\overline{WR}$ = low. The attribute memory can not be read out. Resetting bit D7 in the Peripheral Configuration Register brings the MSM60801 back to normal mode. This action must only be performed after some delay to ensure the internal state machine reading the EEPROM has been finished.

The waiting time can be calculated as:

$$tw_{AIT}\ (ms) = 0.6\ /\ clock\ frequency\ (MCLK/MHz)$$

To block write access to the Peripheral Configuration Register (M0), EXT can be set low.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rated Value		Unit
			Min	Max	
Power supply voltage	V_{CC}		-0.5	6.0	V
Operating temperature	T_{OP}		-20	+70	°C
Storage temperature	T_{stg}		-40	+85	

Note: The functionality after a single "reflow" soldering cycle is guaranteed.

Recommended Operating Conditions

Parameter	Symbol	Condition	Rated Value	Unit
Power supply voltage	V_{DD}		+5 V ±10%	V
Operating temperature	T_a		-20 ~ +70	°C

DC Characteristics (V_{DD} = 5.5 V, V_{SS} = 0V)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
"H" level input voltage	V_{IH1}		2.2	–	V_{CC}+0.5	V
	V_{IH2}	Schmitt Trigger	2.3	–	V_{CC}+0.5	
"L" level input voltage	V_{IL1}		-0.5	–	0.8	V
	V_{IL2}	Schmitt Trigger				
"H" level output voltage	V_{OH1}	I_{OH} = -4 mA	3.7	–	–	V
	V_{OH2}	I_{OH} = -8 mA				
"L" level output voltage	V_{OL1}	I_{OL} = 4 mA	–	–	0.4	V
	V_{OL2}	I_{OL} = 8 mA				
"H" level input current	I_{IH}	V_{IL} = 0.8 V	–	–	10	µA
"L" level input current	I_{IL}	V_{IH} = V_{CC}				

Note: Typical condition is 3 V and T_j = 25°C; typical process.

AC Characteristics - Attribute Memory Read

Function	Symbol	Rated Value Min	Rated Value Max	Unit
Read cycle time	$tc_{(R)}$	300	–	ns
Address access time	$ta_{(A)}$	–	250	
Card enable access time	$ta_{(CE)}$	–	100	ns
Output enable access time	$ta_{(OE)}$			
Output disable time from $\overline{OE}$	$tdis_{(OE)}$	–	20	ns
Output disable time from $\overline{CE}$	$tdis_{(CE)}$			
Output enable time from $\overline{OE}$	$ten_{(OE)}$	5	–	ns
Output enable time from $\overline{CE}$	$ten_{(CE)}$			
Data valid from add change	$tv_{(A)}$	0	–	ns
Delay $\overline{EARD}$ from $\overline{OE}$	td_{ERD}	–	10	

Note: $\overline{EARD}$ is only active when the PA[9:0] address is in the range of 200 hex to 3FF hex; the MSM60801 data bus remains 3-state.

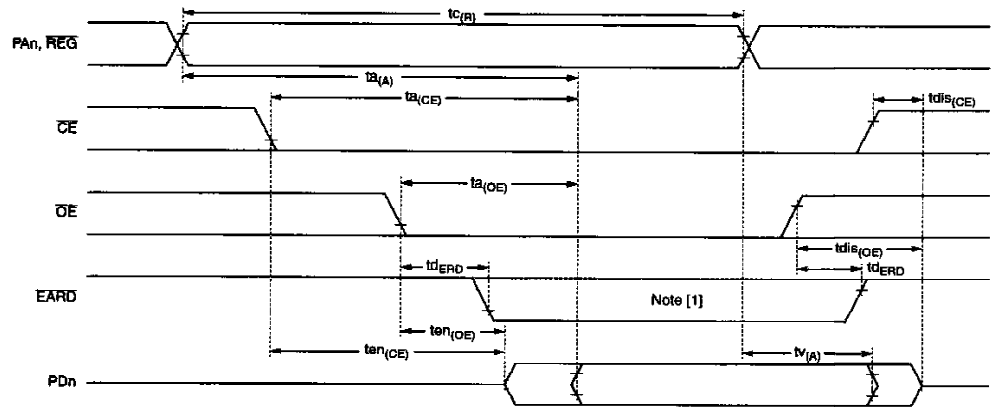


Figure 1. Attribute Memory Read Timing

AC Characteristics - Attribute Memory Write

Function	Symbol	Rated Value		Unit
		Min	Max	
Write cycle time	$tc_{(W)}$	250	–	ns
Address setup time	$ts_{(A)}$	0	–	
Write pulse width	$tw_{(WE)}$	100	–	ns
Data setup time	$ts_{(D)}$	60	–	
Address hold time	$th_{(A)}$	20	–	ns
Data hold time	$th_{(D)}$			

Note: The $\overline{CE}$ timing is identical with the $\overline{WE}$ timing, the write cycle can be controlled by either $\overline{WE}$ or $\overline{CE}$ control.

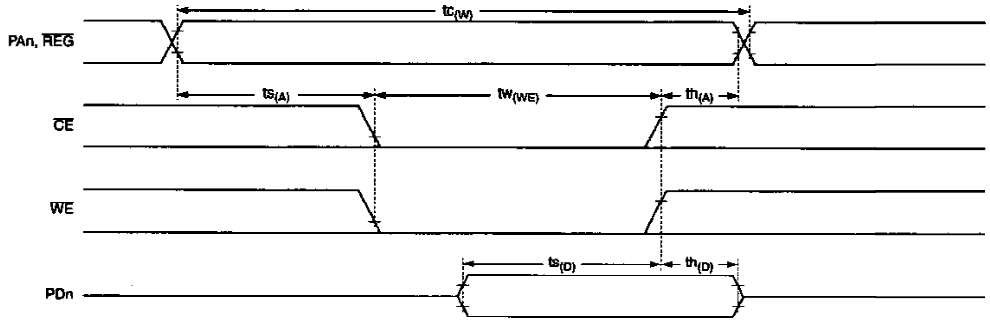


Figure 2. Attribute Memory Write Timing

AC Characteristics - I/O Output

Function	Symbol	Rated Value Min	Rated Value Max	Unit
Address setup before $\overline{IOWR}$	ts_A	70	–	ns
$\overline{ACK}$ delay after address valid	td_{ACK}	–	20	ns
$\overline{REG}$ setup before $\overline{IOWR}$	ts_{REG}	5	–	ns
$\overline{CE}$ setup before $\overline{IOWR}$	ts_{CE}			
$\overline{ICS8}$ / $\overline{ICS16}$ bit after I/O cycle valid	td_{ICS}	–	8	ns
PD data setup before $\overline{IOWR}$	ts_D	60	–	
$\overline{IOWR}$ width time	tw_{IOWR}	165	–	ns
$\overline{IWR}$ delay after $\overline{IOWR}$	td_{IWR}	–	8	
Address hold following $\overline{IOWR}$	th_A	20	–	ns
$\overline{REG}$ hold following $\overline{IOWR}$	th_{REG}	0	–	
$\overline{CE}$ hold following $\overline{IOWR}$	th_{CE}	5	–	ns
PD data hold following $\overline{IOWR}$	th_D	30	–	
BD data delay following $\overline{IOWR}$	td_{BD}	–	15	ns
BD data hold following $\overline{IOWR}$	th_{BD}	4	–	

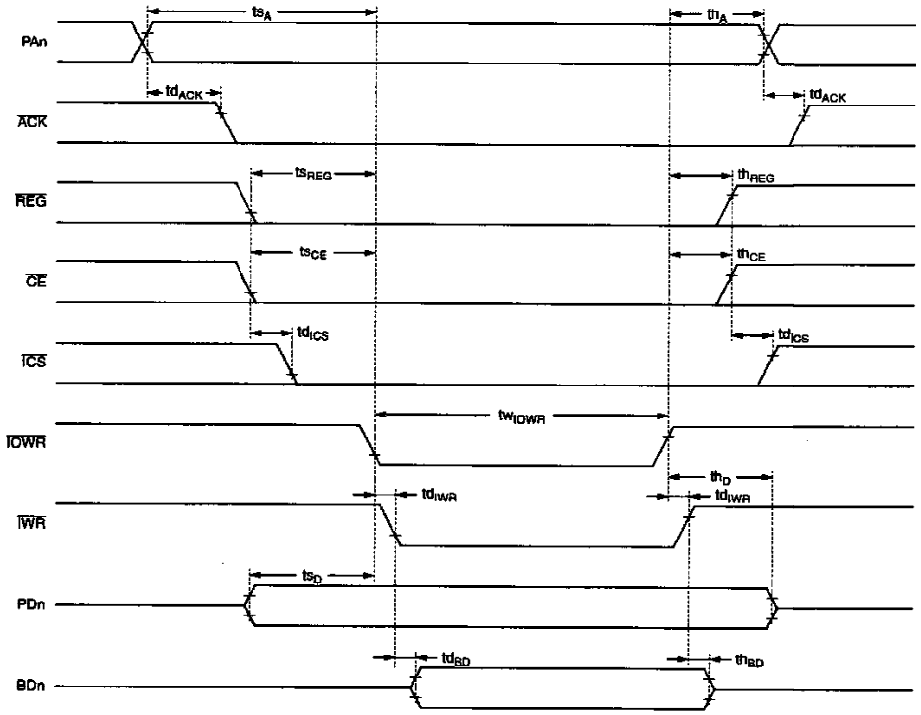


Figure 3. I/O Output Timing

AC Characteristics - I/O Input

Function	Symbol	Rated Value		Unit
		Min	Max	
Address setup before $\overline{IORD}$	ts_A	70	–	ns
Address hold following $\overline{IORD}$	th_A	20	–	
$\overline{ACK}$ delay after address valid	td_{ACK}	–	20	ns
$\overline{IORD}$ width time	tw_{IORD}	165	–	
$\overline{REG}$ setup before $\overline{IORD}$	ts_{REG}	5	–	ns
$\overline{REG}$ hold following $\overline{IORD}$	th_{REG}	0	–	
$\overline{CE}$ setup before $\overline{IORD}$	ts_{CE}	5	–	ns
$\overline{CE}$ hold following $\overline{IORD}$	th_{CE}			
$\overline{IRD}$ delay after $\overline{IORD}$	td_{IRD}	–	8	ns
$\overline{ICS}$ 8/16-bit after I/O cycle valid	td_{ICS}			
$\overline{INPACK}$ delay falling from $\overline{IORD}$	td_{INPACK}	–	10	ns
$\overline{INPACK}$ delay rising from $\overline{IORD}$				
PD data delay after $\overline{IORD}$	td_{IORD}	–	100	ns
PD data hold following $\overline{IORD}$	th_{IORD}	0	–	
BD data delay following $\overline{IORD}$	td_{BD}	–	70	ns
BD data hold following $\overline{IORD}$	th_{BD}	0	–	

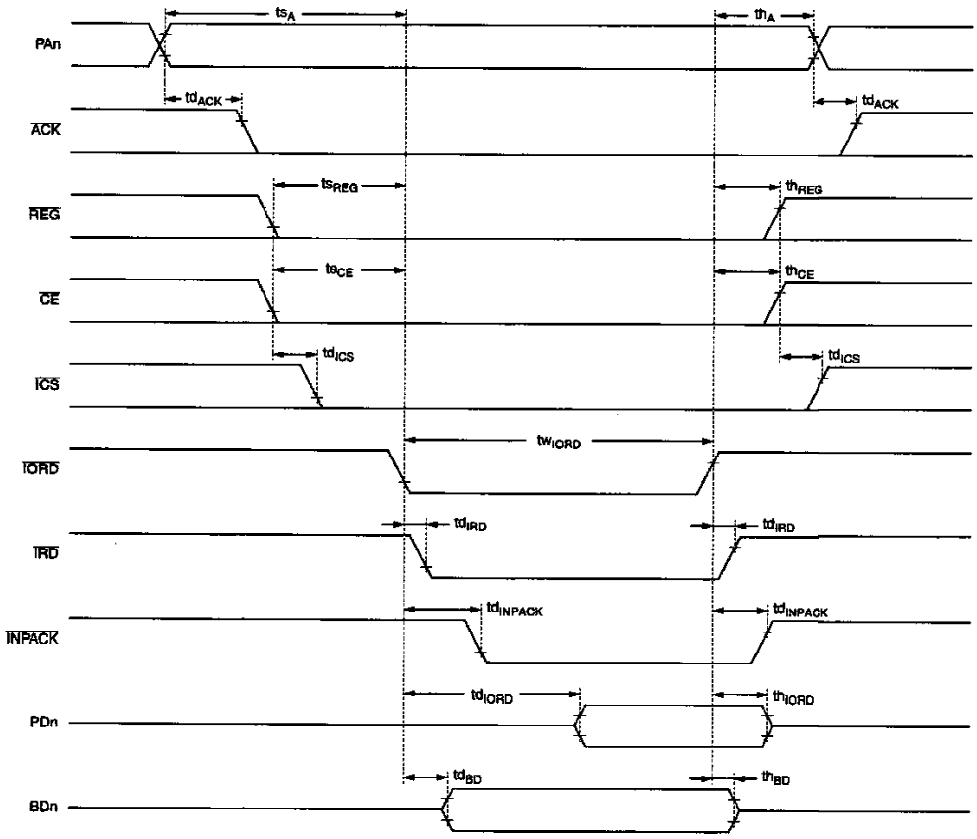


Figure 4. I/O Input Timing

AC Characteristics - Special Functions Write

Function [1]	Symbol	Rated Value Min	Rated Value Max	Unit
Address setup before $\overline{WR}$	ts_{ADR}	10	–	ns
$\overline{CS}$ delay after address valid	td_{ADR}	–	10	
$\overline{CS}$ delay after $\overline{MCS}$ active	td_{MCS}	20	–	ns
ALE width time [2]	tw_{ALE}			
ED address setup time before ALE low	ts_{AD}	5	–	ns
ED address hold after ALE	th_{AD}	2	–	
ED data setup before $\overline{WR}$	ts_{ED}	10	–	ns
ED data hold following $\overline{WR}$	th_{ED}			
$\overline{WR}$ width time	tw_{WR}	20	–	ns
Port data valid following $\overline{WR}$ low	td_{PD}	–	30	

1. Chip selects $\overline{CS}$[3:0] are only active when the EADR[3:0] address is in the specified range and $\overline{MCS}$ is low.
2. ALE and the address on the multiplexed address/data bus is only used in conjuction with the description of the attribute memory.

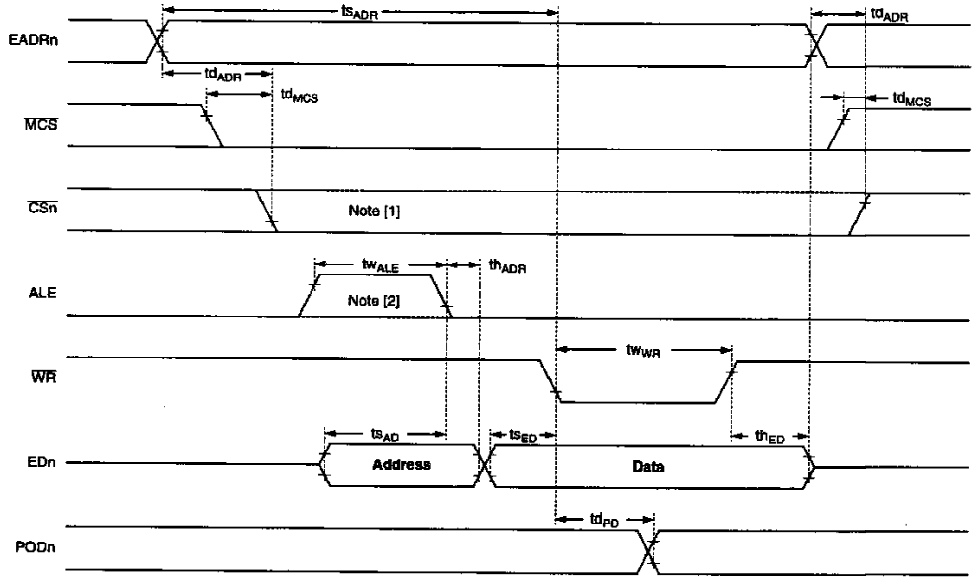


Figure 5. Special Functions Write Timing

AC Characteristics - Special Functions Read

Function	Symbol	Rated Value Min	Rated Value Max	Unit
Address setup before $\overline{RD}$	ts_{ADR}	10	–	ns
$\overline{CS}$ delay after address valid	td_{ADR}			
$\overline{CS}$ delay after $\overline{MCS}$ active	td_{MCS}	–	10	ns
ED data delay following $\overline{RD}$	ts_{ED}	–	30	
$\overline{RD}$ width time	tw_{WR}	40	–	ns
ED data hold following $\overline{RD}$	th_{ED}	4	10	

Note: Chip selects $\overline{CS}$[3:0] are only active when the EADR[3:0] address is in the specified range and $\overline{MCS}$ is low.

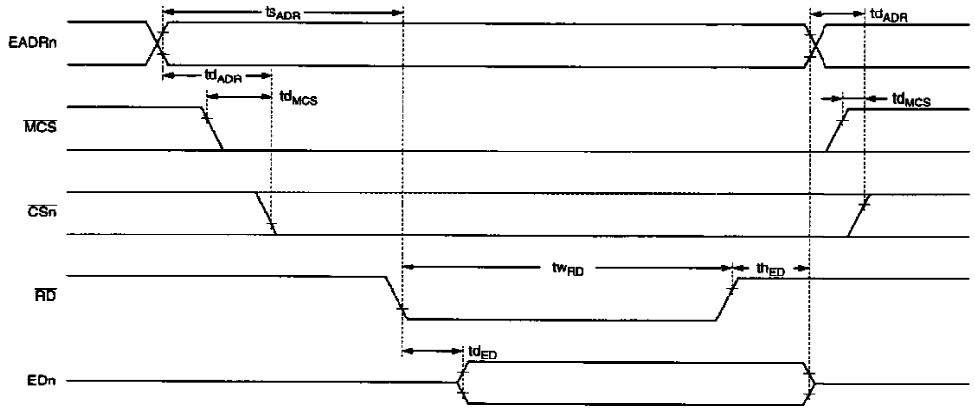


Figure 6. Special Functions Read Timing