MOSEL VITELIC

MS622424
HIGH PERFORMANCE
8K x 24 BIT
CMOS COLOR MAP

Features

- Color Index Mode supports up to 8192 simultaneous colors out of 16.7 million total colors
- 24-bit RGB Mode allows full true color display
- High-speed operation capable of supporting resolutions up 1280 x 1024
- Available in 100-pin PQFP and MQUAD packages
- Unique “Write-Buffer” at MPU port permits dualport-like operation using an economical singleport memory core
- All TTL compatible inputs and outputs
- 60, 70 and 80 MHz pipelined operation
- Standard MPU Interface

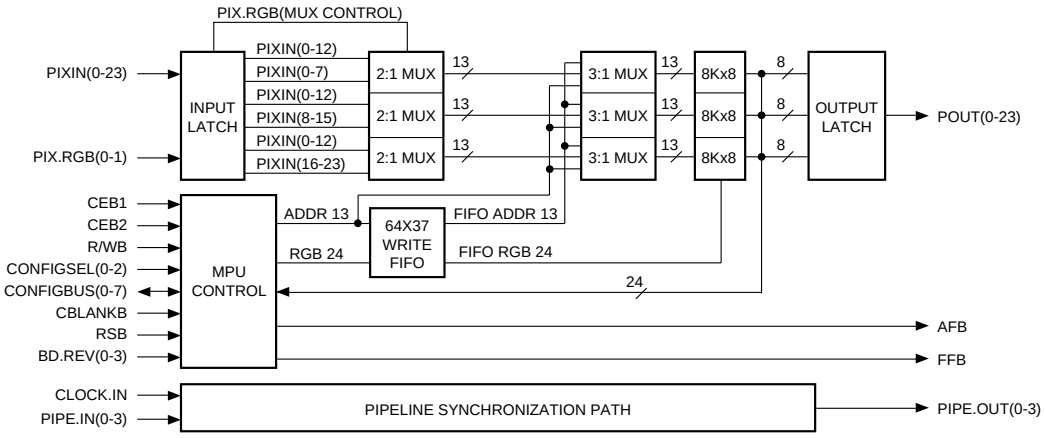
Description

The MS622424 is a high performance, full CMOS, 8K x 24, 192K-bit pipelined static memory. This device is specifically designed for use as a color look-up table in high resolution video display systems. When two of these devices are operated in parallel, the resulting system will be capable of supporting a display of 1280 x 1024 bit mapped color graphics with 13 bits per pixel in the Color Index Mode or 24 bits per pixel in the RGB Mode.

In the Color Index Mode, three internal 8Kx8’s provide 8192 simultaneous colors from a 16.7 million color palette. The palette can be partitioned into several smaller palettes thereby supporting multiple window display. In the RGB Mode, the 24-bit input can be gamma corrected on one of three gamma correction tables. The 24-bit gamma corrected value will then be presented at the output.

This device is implemented in full CMOS for low power consumption, and is available in an 100-pin plastic or metal quad-flat-pack.

Functional Block Diagram



Functional Description

MPU Interface

The MPU interface allows the MPU to access the internal registers and the color map. The CONFIGSEL0–CONFIGSEL2 bits that are latched on the falling edge of CEB define the access mode. The access modes are defined in the table below. The R/WB pin is also latched on the falling edge of CEB and indicates a read operation when high and a write operation when low. These functions are illustrated in the truth table on the next page.

The RGB0 and RGB1 bits are the two bits of a modulo 3 counter, which determine which color (red, green, or blue, in that order) is selected. These two bits are reset by a write to either the high or low Address Register. In writes and reads to and from the color palette, the Address Register is incremented at the end of the RGB cycle.

In order to perform color pallette read without asynchronous problems, initialization is required. This is done by writing a command of configsel(2:0)=111 before the actual read starts. Upon finishing the color palette read operation, a read command of configsel(2:0)=111 should also be issued to switch MPU Access modes.

During a read from the color palette, the color data output at POUT0–POUT23 may be disturbed because the address register will take over addressing of the color map. To prevent random color data from being displayed on the screen, the data at POUT0–POUT23 will be held at the value defined by the last valid pixel address for the duration of the read. A read of the color palette should not be performed while the Write FIFO is not empty because it may contend with the FIFO to color map write. It is recommended that FIFO empty flag status always be checked before issuing color palette read instructions. If such a contention occurs, then the color palette read will be disturbed by the write cycle.

Write FIFO

The Write FIFO stores data and addresses that are written to the Color Palette Buffer and Address Registers. The FIFO is emptied by writing the data to the color map during a blanking period as indicated by CBLANKB. The host can write up to 64 locations that contain a 13-bit address and a 24-bit color before the FIFO becomes full. When the FIFO is full the full flag pin (FFB) goes low until at least one location of the FIFO is transferred to the color map. If the host attempts to write to the Color Palette Buffer while the FFB is active, then the device will transfer 4 locations from the FIFO to the color map in order to make room for the incoming data, regardless of the state of CBLANKB. This process may disturb the data in the pixel stream. To prevent random color data from being displayed on the screen while the device performs these 4 writes, the data at POUT0–POUT23 will be held at the value defined by the last valid pixel address. When Pixel clock is much slower than 70 MHz, the operating frequency of MPU should also be slowed down accordingly in order to maintain the synchronization of FIFO operations

MPU Access Modes

CONFIGSEL<2:0>	MODE
000	Address Register low (R/W)
001	Address Register high (R/W)
010	Color Palette Buffer (R/W)
011	Command Register (R/W)
100	Status Register (read only)
101	Color Buffer Register (read only)
110	Revision register (read only)
111	Color Palette read initialization (R/W)

Color Buffer Register

The Color Buffer Register stores the red and green data that is written to the Color Palette Buffer. Thus if a complete red, green, blue write cycle is not completed (register data is not transferred to the Write FIFO), then the host can recover the red and green data it has written by reading the red and green Color Buffer Registers.

The host can recover the red and green data by first writing to the address register to reset the RGB counter. Then the red and green data can be recovered in two consecutive reads of the Color Buffer Register.

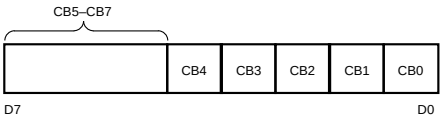
Truth Table

R/WB	CONFIGSEL<2:0>	RGB1[4]	RGB0[4]	FUNCTION
0	000 0	x	x	Write Address Register Low, reset RGB Counter
0	001 1	x	x	Write Address Register High, reset RGB Counter (1)
0	010 2	0	0	Write Red Color Palette Buffer, increment RGB counter
0	010 2	0	1	Write Green Color Palette Buffer, increment RGB counter
0	010 2	1	0	Write Blue Color Data to Write FIFO, transfer register contents to Write FIFO, reset RGB counter, increment Address Register
0	011 3	x	x	Write Command Register
0	100 4	x	x	Invalid Operation
0	101 5	x	x	Invalid Operation
0	110 6	x	x	Invalid Operation
0	111 7	x	x	Initialize color palette read
1	000 0	x	x	Read Address Register Low
1	001 1	x	x	Read Address Register High (2)
1	010 2	0	0	Read Red Color Palette, increment RGB counter (3)
1	010 2	0	1	Read Green Color Palette Buffer, increment RGB counter
1	010 2	1	0	Read Blue Color Palette Buffer, reset RGB counter, increment Address register
1	011 3	x	x	Read Command Register
1	100 4	x	x	Read Status Register
1	101 5	0	0	Read Red Color Buffer Register, increment RGB counter
1	101 5	0	1	Read Green Color Buffer Register
1	101 5	1	0	Invalid Operation
1	110 6	x	x	Read Revision Register
1	111 7	x	x	Terminate color palette read

NOTE:
1. Only CONFIGBUS0–CONFIGBUS4 are recognized; the upper three bits are ignored.
2. Data is output to CONFIGBUS0–CONFIGBUS4 only. The upper three bits will output “0”.
3. Reading the Red Color Palette may disturb the pixel stream.
4. RGB0 and RGB1 are internal RGB couter outputs.

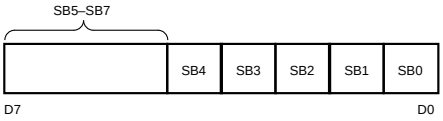
Internal Registers

Command Register ***The Command Register is an 8-bit register.***



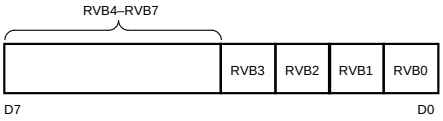
CB0	PIPE.IN0 reset	This bit is internally ANDed with PIPE.IN0 . Thus when CB0 is “0”, then PIPE.OUT0 will always be “0”
CB1	PIPE.IN1 reset	This bit is internally ANDed with PIPE.IN1 . Thus when CB1 is “0”, then PIPE.OUT1 will always be “0”
CB2	PIPE.IN2 set	This bit is internally ORed with PIPE.IN2 . Thus when CB2 is “1”, then PIPE.OUT2 will always be “1”
CB3	PIPE.IN3 set	This bit is internally ORed with PIPE.IN3 . Thus when CB3 is “1”, then PIPE.OUT3 will always be “1”
CB4	HFB/AFB	This bit programs the AFB flag indicator. When this bit is “0” the AFB pin will indicate that the FIFO is half full. When this bit is “1” AFB will indicate almost full.
CB5–CB7	Reserved	Reserved for internal use.

Status Register ***The Status Register is an 8-bit register.***



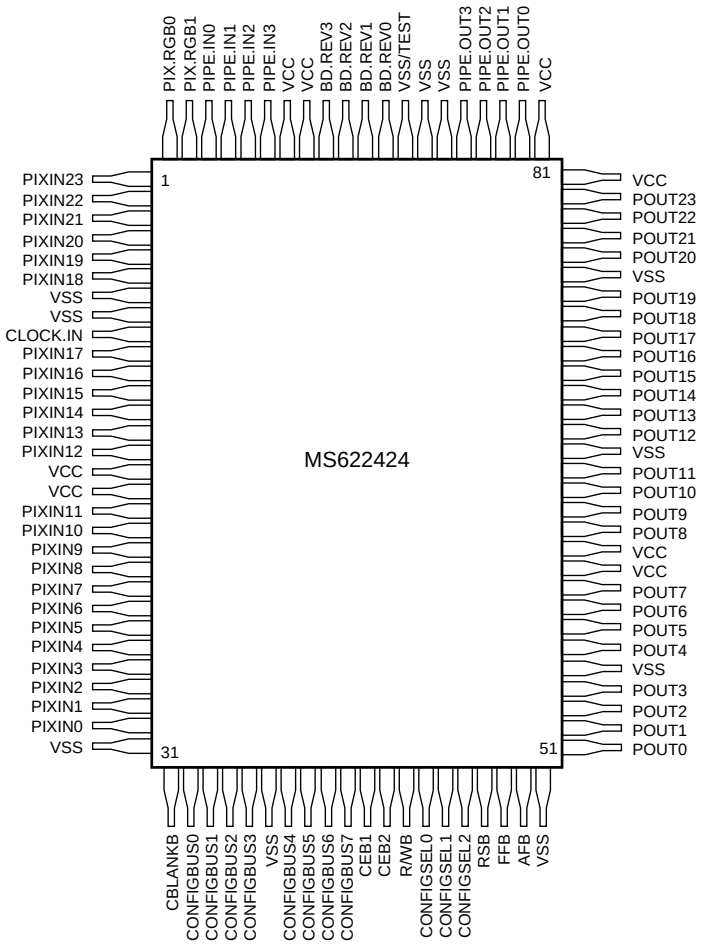
SB0	RGB0	LSB of RGB counter. RGB0 and RGB1 form two bits of a modulo three counter that determines which color is operated on (read only).
SB1	RGB1	MSB of RGB data counter (read only).
SB2	EFB	Empty Flag; Write FIFO is empty when this bit is low.
SB3	HFB/AFB	Half or Almost-Full Flag; Like the external AFB pin, this bit can be programmed by CB4 to indicate that the Write FIFO is at least half full or at least 7/8 full (eight or fewer empty locations left). This pin is active low.
SB4	FFB	Full Flag; Write FIFO is full when this bit is low.
SB5–SB7	Reserved	Reserved for internal use.

Revision Register ***The Revision Register is an 8-bit register.***



RVB0	REV0	LSB of Revision Register. This register is mask programmed to indicate the revision number.
RVB1	REV1	Second bit of Revision Register.
RVB2	REV2	MSB of Revision Register.
RVB3	Reserved	Reserved for internal use.
RVB4–RVB7	REV4–7	Corresponds to board revision input BD.REV0–3

100-pin PQFP/MQUAD
PIN CONFIGURATION
Top View

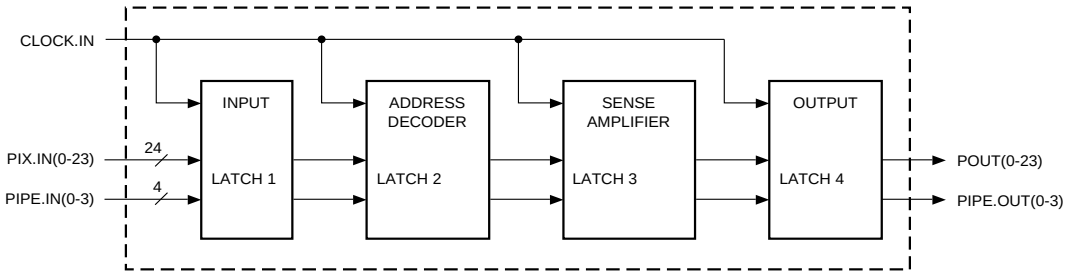


Pin Descriptions

Pin Name	Description
PIXIN0–PIXIN23	These inputs are latched on the rising edge of CLOCK.IN. The PIXIN0–PIXIN23 can be utilized in two different modes. In the Color Index Mode, PIXIN0–PIXIN12 are used to look up a 24 bit color from a palette of 8192 colors; the higher order bits in this mode are ignored. In the RGB Mode, PIXIN0–PIXIN7, PIXIN8–PIXIN15, and PIXIN16–PIXIN23 will address a red, green, or blue color value, respectively, from the 8K color palette. Internally, the five higher order bits are appended to the 8-bit addresses to compose the necessary 13 bits to address 8K locations. The five appended bits can be one of three values:(1)11101, (2)11110, or (3)11111. These binary addresses are expressed with the most significant bit on the left. The RGB Mode and five higher order bits are determined by the values of PIX.RGB0 and PIX.RGB1.
PIX.RGB0–PIX.RGB1	These two input pins select Color Index Mode or RGB mode. The table below defines the selection associated with the values of these two bits. **PIX.RGB1 / PIX.RGB0 / SELECTION** 0 / 0 / Color Index Mode 0 / 1 / RGB Mode, 11101 + 8-bit address 1 / 0 / RGB Mode, 11110 + 8-bit address 1 / 1 / RGB Mode, 11111 + 8-bit address These two bits are latched on the rising edge of CLOCK.IN.
PIPE.IN0–PIPE.IN3	These four input pins are provided for the video timing signals such as CBLANKB and CSYNCB. Internally, these signals will go through the same number of pipeline stages as the pixel data. The video timing signals will subseqently appear at the PIPE.OUT outputs, and synchronized with the appropriate color data. These inputs are also latched by the rising edge of CLOCK.IN.
CLOCK.IN	This is the clock input pin. The CLOCK.IN controls the latching output and subsequent processing of the pixel data and video timing signals.
POUT0–POUT23	Color information output pins. POUT0–POUT7, POUT8–POUT15, and POUT16–POUT23 are the red, green, and blue color data, respectively.
PIPE.OUT0–PIPE.OUT3	Video timing signals output pins. The output data is synchronized with the color data is output on these pins. Fig. 1 describes internal pipeline data path flow.
CEB1, CEB2	The chip enable input pins. MPU read and write cycles are performed by bringing either of these pins low. The falling edge of this signal latches information from the R/WB, CONFIGSEL, and CONFIGBUS pins.
R/WB	Read and write control input pins. When latched by the falling edge of CEB, this signal determines whether the following operation is a read or a write. A read operation is performed when this signal is high, and a write operation is performed when this signal is low.
CONFIGBUS0–CONFIGBUS7	These pins are used for data I/O. RAM and register data are input and output through these pins. These pins are used for read and write to/from RAM and register.
CONFIGSEL0–CONFIGSEL2	The device configuration input pins. These inputs specify the type of read or write operation to perform. The particular RAM or register operation is defined by the truth table. This information is latched on the falling edge of CEB.
CBLANKB	Blanking status input pin. This signal indicates to the device that a blanking period is taking place so it is therefore permissible to change data in the palette RAM. This pin is active low.

Pin Descriptions (Cont'd)

Pin Name	Description
RSB	Reset input pin. This asynchronous system reset initializes state machines and resets the Address, Status, and Color Buffer registers. It also resets the Write FIFO so that it is empty of any contents. It resets command register bits CB2–CB7 and sets bits CB0–CB1. During a reset, CONFIGBUS0–CONFIGBUS7 are in tri-state. This pin is active low.
AFB	The FIFO status output pin. This active low output indicates that the Write FIFO is half or almost full. This active low output can be programmed by a bit in the Command Register to indicate that the FIFO is at least half full or is almost full (eight or less empty locations left).
FFB	The FIFO status output pin. This active low output indicates that the Write FIFO is full.
V_{SS}/TEST	This pin should be grounded for normal operation.
BD.REV(0-3)	Board revision input pins. These input pins can be pull-up to V_{DD} or pull-down to V_{SS}. The BD.REV data can be read though the revision register.



Internal Pipeline Data Path for Pixel and Pipe Input Data

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	–0.5* to +7.0	V
V_T	Terminal Voltage with Respect to V_{SS}	–0.5* to V_{DD} +0.5	V
P_D	Power Dissipation 100% Duty Cycle	TBD	W
t_{OPR}	Operating Temperature	–10 to +85	°C
t_{STG}	Storage Temperature	–65 to +150	°C

*Note: Operation above absolute maximum rating can affect device reliability.

Capacitance*

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance (V_{IN} = 0V)		5	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		8	pF

*Note: These parameters are sampled and not 100% tested.

Recommended DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5.0V ± 5%, V_{SS} = 0V, unless otherwise noted. See package thermal data on pg 10.

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{DD}	Supply Voltage	4.75	5.25	V	
V_{SS}	Supply Voltage	0.0	0.0	V	
V_{IH}	Input High Voltage	2.2	V_{DD}+.3	V	
V_{IL}	Input Low Voltage	–0.5*	+0.8	V	
I_{LI}	Input Leakage Current	–10	10	µA	V_{DD} = 5.25V, V_{IN} = V_{SS} to V_{DD}
I_{LO}	Output Leakage Current	–10	10	µA	V_{OUT} = V_{SS} to V_{DD}
I_{DD}	Dynamic Operating Current		300	mA	Outputs Open, f = fmax
V_{OL}	Output Low Voltage		0.4	V	Active Outputs Open, I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –1.0 mA

* –3.5V for 20 ns pulse.

AC Test Loads

Signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0V to 3.0V, output loading as shown in the diagram below.

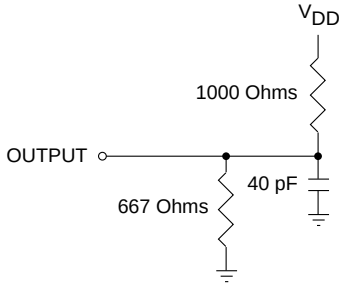


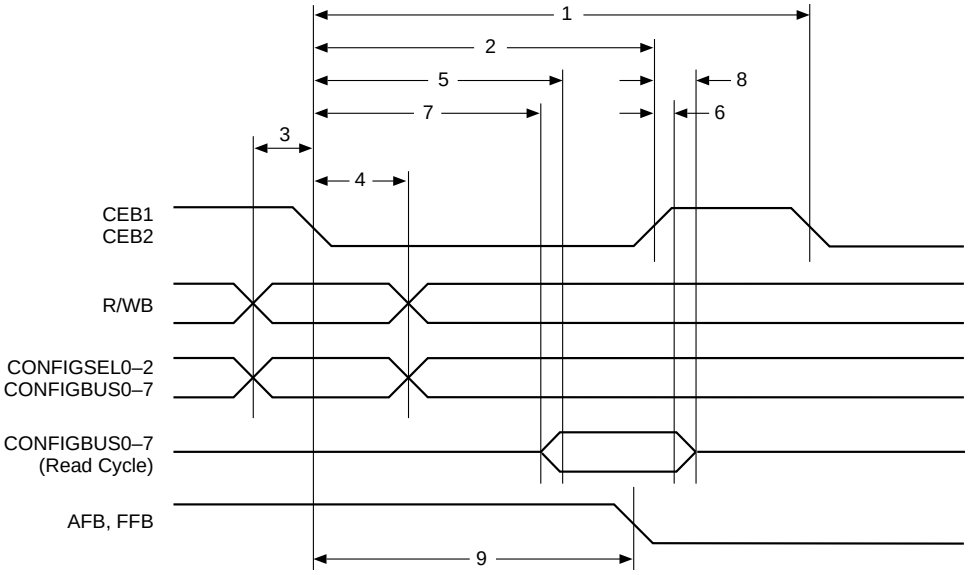
Figure 2. Output Load

AC Test Conditions

(Applies to READ and WRITE Cycle Timing)

Input Pulse High Level	V_{IH} = 3.0V
Input Pulse Low Level	V_{IL} = 0.0V
Input Rise Time	t_R = 3 ns
Input Fall Time	t_F = 3 ns
Input and Output Reference Level	1.5V
Output Load	C_L = 40pF, 1 TTL
V_{DD}	5V ± 5%
T_A	0° to +70°C

Timing Waveforms of MPU Cycle



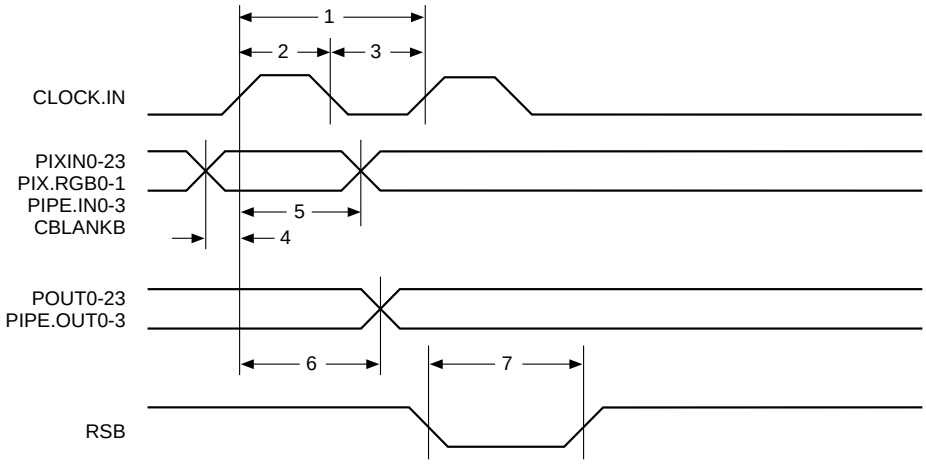
AC Characteristics

At recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	CEB Cycle Time	80			ns	
2	CEB Pulse Width	65			ns	
3	CONFIGSEL/BUS and R/WB Set-up before CEB low	0			ns	
4	CONFIGSEL/BUS and R/WBHold after CEB low	10			ns	
5	CONFIGBUS Data Access			65	ns	
6	CONFIGBUS Data Hold	5			ns	
7	CEB low to CONFIGBUS Lo-Z	10			ns	2, 3
8	CEB high to CONFIGBUS Hi-Z			10	ns	2, 3
9	Write cycle start to AFB, FFB low			65	ns	

NOTES:
1. Applicable to all speed grades.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500mV from low or high voltage with load (see Figure 2).

Timing Waveforms of Pixel Port, CBLANKB, and RESET



AC Characteristics

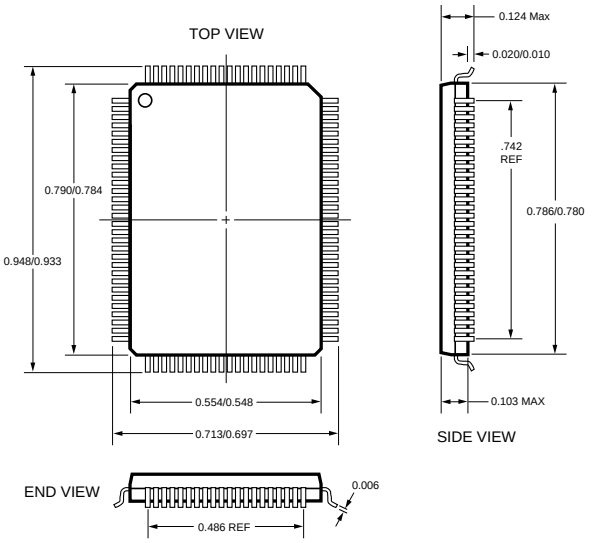
At recommended operating conditions, unless otherwise noted.

Symbol	Parameter	-60			-70			-80			Unit	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
1	CLOCK.IN Cycle Time	16.7			14.3			12.5			ns	
2	CLOCK.IN Pulse Width high	6.0			5.0			4.0			ns	
3	CLOCK.IN Pulse Width low	6.0			5.0			4.0			ns	
4	Pixel Data Set-up before CLOCK.IN high	2.0			1.0			1.0			ns	
5	Pixel Data Hold after CLOCK.IN high											
	PIXIN0-23	4.0			3.0			2.5			ns	
	PIX.RGB0-1	4.0			3.0			2.5			ns	
	PIPE.IN0-3	6.0			5.0			4.0			ns	
	CBLANKB	3.0			1.5			1.5			ns	
6	CLOCK.IN high to Data out	6.0		12.0	5.0		10.0	4.0		9.0	ns	
7	RSB Pulse width Low	35.0			30.0			25.0			ns	1

NOTES:
1. This signal can be completely asynchronous to the Pixel Port and the MPU Port.

PACKAGE OUTLINES

100 pin PQFP



100 pin MQUAD