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Edition 2.0

FUJITSU

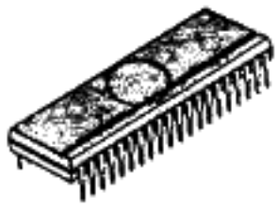
DATA SHEET

MB86041A/MB86043

CMOS PIPELINED DIVIDER WITH 10-BIT DIVIDEND, 8-BIT DIVISOR, AND 10-BIT QUOTIENT

The MB86041A and MB86043 are high-speed CMOS pipe-lined divider featuring integer division or decimal division operating modes and 10-bit dividend, 8-bit divisor, and 10-bit quotient. The remainder is omitted. External divide by zero and overflow signals are provided.
The devices operate at up to 20 MHz for high-speed image signal processing.
The MB86041A is housed in an 40-pin plastic dual in-line package and MB86043 is housed in 48-pin quad flat package.

- Functions
  5-stage, pipelined, high-speed divider
  Operation speed : 20 MHz (Maximum)
- Operation Modes
  (1) Integer division
  (2) Decimal division
- Data Format
  Dividend : 10 bits (TTL Level)
  Divisor : 8 bits (TTL Level)
  Quotient : 10 bits (TTL Level)
  (Note that the remainder is omitted.)
- Detection Function
  (1) Divide by 0 error detection function
  (2) Overflow error detection function



MB86041A
PLASTIC PACKAGE
(DIP-40P-M01)

MB86043
PLASTIC PACKAGE
(FPT-48P-M02)

ABSOLUTE MAXIMUM RATINGS (See NOTE) V_{ss} = 0 V

Ratings	Symbol	Conditions	Value	Unit
Supply voltage	V_{DD}	–	V_{ss}–0.5 to +6.0	V
Input voltage	V_I	–	V_{ss}–0.5 to V_{DD}+0.5	V
Output voltage	V_O	–	V_{ss}–0.5 to V_{DD}+0.5	V
Operating temperature	T_A	–	–25 to +85	°C
Storage temperature	T_{stg}	–	–40 to +125	°C
Output current *1)	I_O	V_O = V_{DD}	+40 (Maximum)	mA
		V_O = 0 V	–40 (Maximum)	

NOTE *1) This is the output current per pin for V_{DD} = 5 V and for a maximum of 1 second.

Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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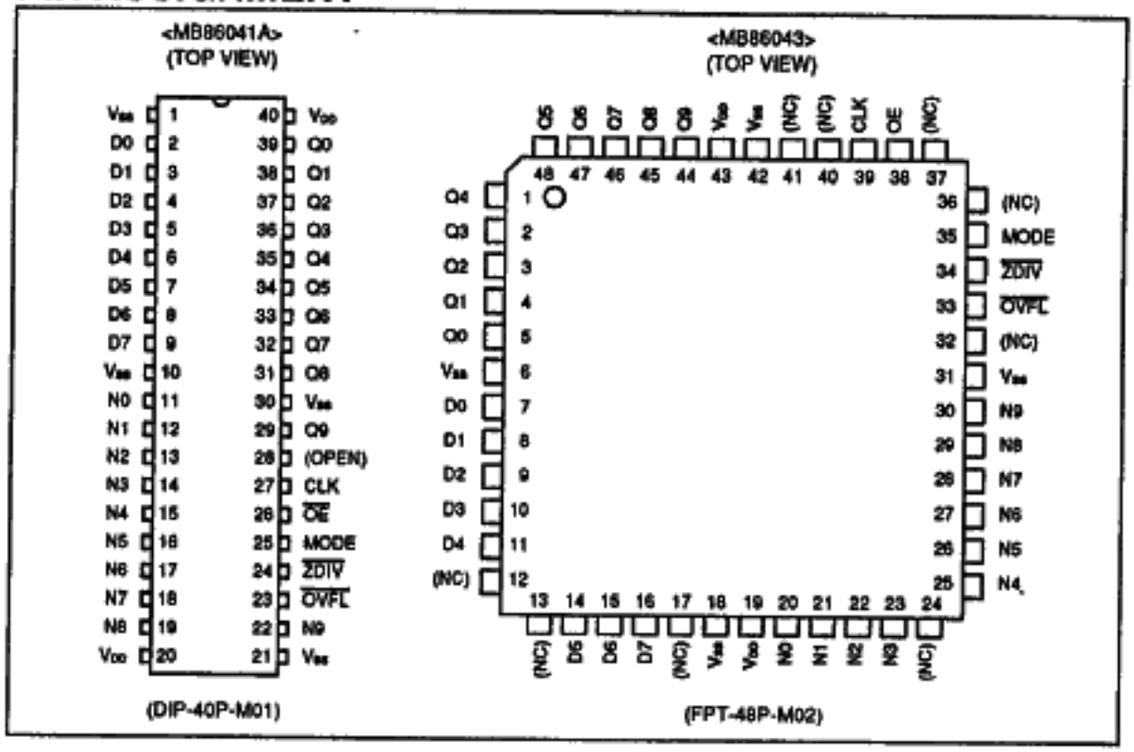
PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin NO.		Symbol	I/O	Function Description
MB86041A	MB86043			
1	6	V_{SS} *1	–	Ground pin (0 V)
2	7	D0	I	Divisor input pin (LSB)
3	8	D1	I	Divisor input pin
4	9	D2	I	Divisor input pin
5	10	D3	I	Divisor input pin
6	11	D4	I	Divisor input pin
–	12, 13	(NC)	–	No connection
7	14	D5	I	Divisor input pin
8	15	D6	I	Divisor input pin
9	16	D7	I	Divisor input pin (MSB)

Pin NO.		Symbol	I/O	Function Description
MB86041A	MB86043			
–	17	(NC)	–	No connection
10	18	V_{ss} *1	–	Ground pin (0 V)
–	19	V_{DD} *2	–	Supply voltage input pin (+5 V)
11	20	N0	I	Dividend input pin (LSB)
12	21	N1	I	Dividend input pin
13	22	N2	I	Dividend input pin
14	23	N3	I	Dividend input pin
–	24	(NC)	–	No connection
15	25	N4	I	Dividend input pin
16	26	N5	I	Dividend input pin
17	27	N6	I	Dividend input pin
18	28	N7	I	Dividend input pin
19	29	N8	I	Dividend input pin
20	–	V_{DD} *2	–	Supply voltage input pin (+5 V)
21	31	V_{ss} *1	–	Ground pin (0 V)
22	30	N9	I	Dividend input pin (MSB)
–	32	(NC)	–	No connection
23	33	$\overline{OVFL}$	O	Overflow error flag output pin Goes low on detection of an overflow in the decimal operation mode.
24	34	$\overline{ZDIV}$	O	Divide by zero error flag output pin Goes low on detection of divide by zero.
25	35	MODE	I	Operation mode selection pin • MODE = L level : integer operation mode • MODE = H level : decimal operation mode Data is latched on the rising edge of clock.
26	38	$\overline{OE}$	I	Output (Q0 to Q9 pins) enable input pin • $\overline{OE}$ = L level : Q0 to Q9 output enabled • $\overline{OE}$ = H level : Q0 to Q9 set to high impedance
–	37, 36	(NC)	–	No connection

*1 : V_{ss} pins : Connect all V_{ss} pins to network ground.
*2 : V_{DD} pins : Connect all V_{DD} pins to the power supply line.

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Pin NO. MB86041A	Pin NO. MB86043	Symbol	I/O	Function Description
–	17	(NC)	–	No connection
10	18	V_{ss} *1	–	Ground pin (0 V)
–	19	V_{DD} *2	–	Supply voltage input pin (+5 V)
11	20	N0	I	Dividend input pin (LSB)
12	21	N1	I	Dividend input pin
13	22	N2	I	Dividend input pin
14	23	N3	I	Dividend input pin
–	24	(NC)	–	No connection
15	25	N4	I	Dividend input pin
16	26	N5	I	Dividend input pin
17	27	N6	I	Dividend input pin
18	28	N7	I	Dividend input pin
19	29	N8	I	Dividend input pin
20	–	V_{DD} *2	–	Supply voltage input pin (+5 V)
21	31	V_{ss} *1	–	Ground pin (0 V)
22	30	N9	I	Dividend input pin (MSB)
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–	37, 36	(NC)	–	No connection

*1 : V_{ss} pins : Connect all V_{ss} pins to network ground.
*2 : V_{DD} pins : Connect all V_{DD} pins to the power supply line.

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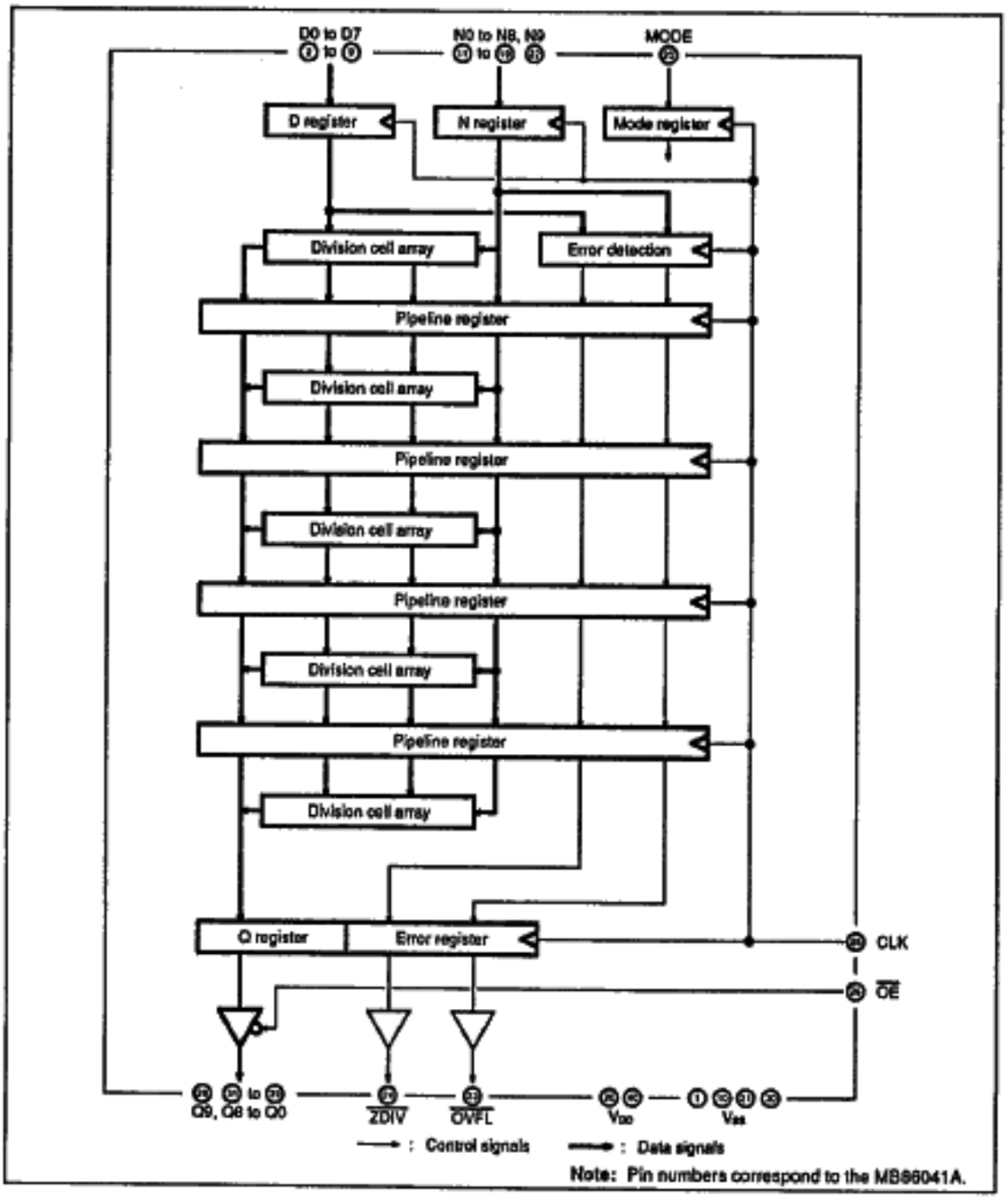
BLOCK DIAGRAM



Note: Pin numbers correspond to the MB86041A.

OPERATION DESCRIPTION

Integer division mode or decimal division mode is selected using the MODE pin.
In the integer division mode, the dividend, divisor, and quotient are operated on as positive integers. In this case, the remainder is omitted.
In the decimal division mode, the decimal point is assumed to be at the left of the MSB. The dividend, divisor, and quotient are operated on as positive fixed-point decimal numbers smaller than 1. Remainder is also omitted in this mode.
The dividend is 10 bits, the divisor 8 bits, and the quotient 10 bits.
Data output status is controlled by the $\overline{OE}$ pin.
Division by zero and overflow detection functions are provided for detection of operational errors.
This device operates at a maximum speed of 20 MHz with a 5-stage pipeline. The output delayed 6 cycles after input. The minimum output delay is 50 ns. (See Figure 1.)
All outputs are unstable for a period of 5 clocks after the device is powered up.

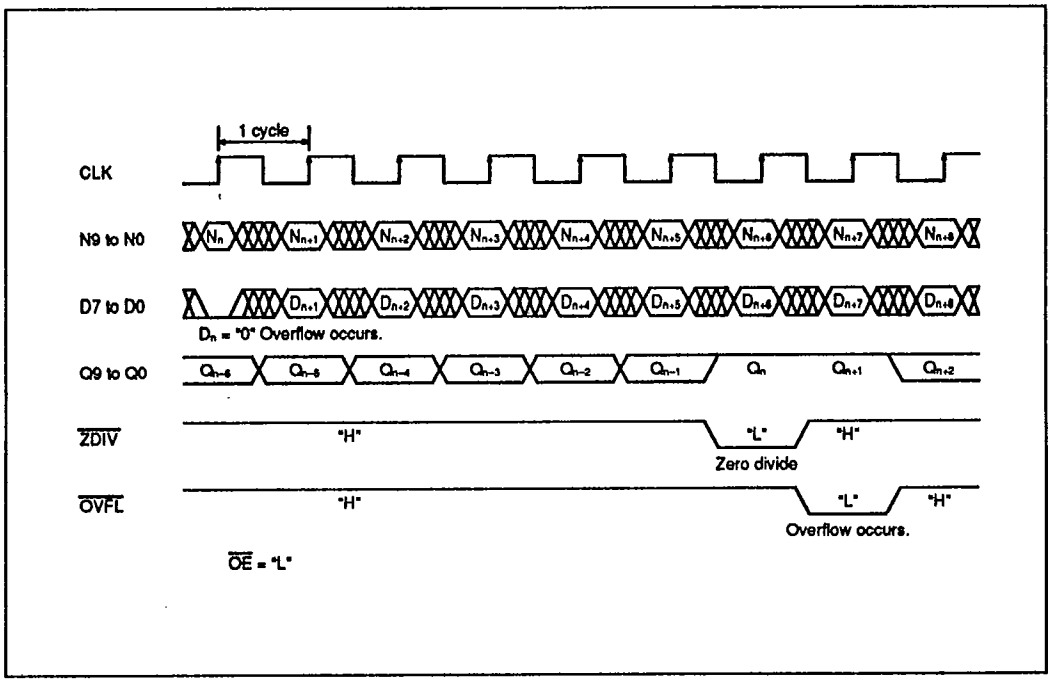


Figure 1 Timing chart

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SETTING OF CONTROL PINS

1. Selection

① Operation mode selection

MODE pin	Operation mode	Type of input data
H-level	Decimal division mode	Data is a positive decimal smaller than 1.
L-level	Integer division mode	Data is a positive integer greater than or equal to 1.

② Data output selection

$\overline{OE}$ pin	Output status of pins Q0 to Q9
H-level	High impedance status
L-level	The quotient is output. The remainder is omitted.

2. Precautions

① Error detection display

- When a divide by zero error is detected:
  All bits of the quotient = 1
  $\overline{ZDIV}$ pin = L-level (for one cycle)
- When an overflow error is detected during decimal operation:
  All bits of the quotient = 1
  $\overline{OVFL}$ pin = L-level (for one cycle)

② Precautions for decimal operation

Values smaller than 1 are used for the dividend (N), divisor (D), and quotient (Q). Therefore, if operation is performed under a condition other than N<D, the result is Q≥1, causing an overflow error.

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MB86041A
MB86043

DATA FORMAT

The dividend is placed on pins N0 to N9 and the divisor on pins D0 to D7 in positive fixed-point format. The quotient is output on pins Q0 to Q9. Remainders are omitted.

1. Integer division mode data format

Dividend (N)

N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

•

(Decimal point)

Divisor (D)

D7	D6	D5	D4	D3	D2	D1	D0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

•

Quotient (Q)

Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

•

2. Decimal division mode data format

Dividend (N)

N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

•

(Decimal point)

Divisor (D)

D7	D6	D5	D4	D3	D2	D1	D0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

•

Quotient (Q)

Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

•

Description of format:

Q9	← Symbol
2^9	← Bit weight

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RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0 V

Parameter	Symbol	Conditions	Value			Unit
			Minimum	Typical	Maximum	
Supply voltage	V_{DD}	–	4.75	5.00	5.25	V
Input voltage	V_I	–	V_{SS}	–	V_{DD}	V
Operating temperature	T_A	–	0	–	70	°C
H-level output current	I_{OH}	–	–	–	–2	mA
L-level output current	I_{OL}	–	–	–	3.2	mA

INPUT AND OUTPUT CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Value			Unit
			Minimum	Typical	Maximum	
Input pin	C_I	f = 1 MHz, V_{DD} = V_I = 0 V	–	–	16	pF
Output pin	C_O	f = 1 MHz, V_{DD} = V_I = 0 V	–	–	16	pF

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ELECTRICAL CHARACTERISTICS

1. DC Characteristics

V_{DD} = 5 V ±5%, V_{SS} = 0 V, T_A = +25°C

Parameter	Symbol	Conditions	Value			Unit
			Minimum	Typical	Maximum	
Supply current	I_{DDS}	Static $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	–	–	0.1	mA
	I_{DD}	Operating	–	–	(TBD)	mA
H-level input voltage	V_{IH}	–	2.2	–	V_{DD}	V
L-level input voltage	V_{IL}	–	V_{SS}	–	0.8	V
H-level output voltage	V_{OH}	I_{OH} = –2 mA	4.0	–	V_{DD}	V
L-level output voltage	V_{OL}	I_{OL} = 3.2 mA	V_{SS}	–	0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{DD}	–10	–	10	µA
Output leakage current	I_{LO}	V_I = 0 V to V_{DD}	–10	–	10	µA

2. AC Characteristics

1) Timing requirements

V_{DD} = 5 V ±5%, V_{SS} = 0 V, T_A = +25°C

Parameter	Symbol	Conditions	Value			Unit
			Minimum	Typical	Maximum	
Clock cycle	t_{CK}	–	50	–	–	ns
Clock pulse width	t_W	–	15	–	–	ns
Clock rise time	t_r	–	–	–	5	ns
Clock fall time	t_f	–	–	–	5	ns
Set-up time	t_{su}	Pins N0 to N9, D0 to D7	15	–	–	ns
Hold time	t_{h1}	Pins N0 to N9, D0 to D7	3	–	–	ns

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ELECTRICAL CHARACTERISTICS

2. AC Characteristics

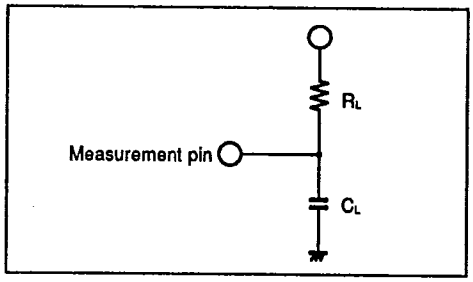
2) Switching characteristics

V_{DD} = 5 V ±5%, V_{SS} = 0 V, T_A = +25°C

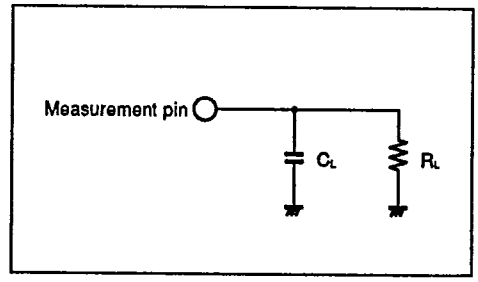
Parameter	Symbol	Conditions	Value			Unit
			Minimum	Typical	Maximum	
Valid status delay time	t_{dv1}	Time from CLK to Q0 to Q9, $\overline{ZDIV}$, and $\overline{OVFL}$	–	–	35	ns
	t_{dv2}	Time from $\overline{OE}$ to Q0 to Q9	–	–	30	ns
Float status delay time	t_{dz}	Time from $\overline{OE}$ to Q0 to Q9	–	–	30	ns

LOAD CIRCUIT

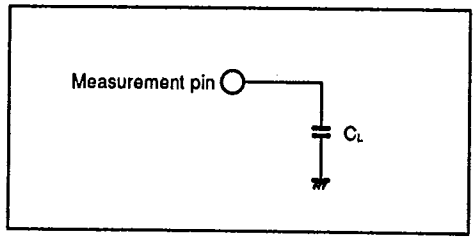
1. Low-level to high impedance transition delay
High Impedance to low-level transition delay



2. High-level to high impedance transition delay
High impedance to High-level transition delay



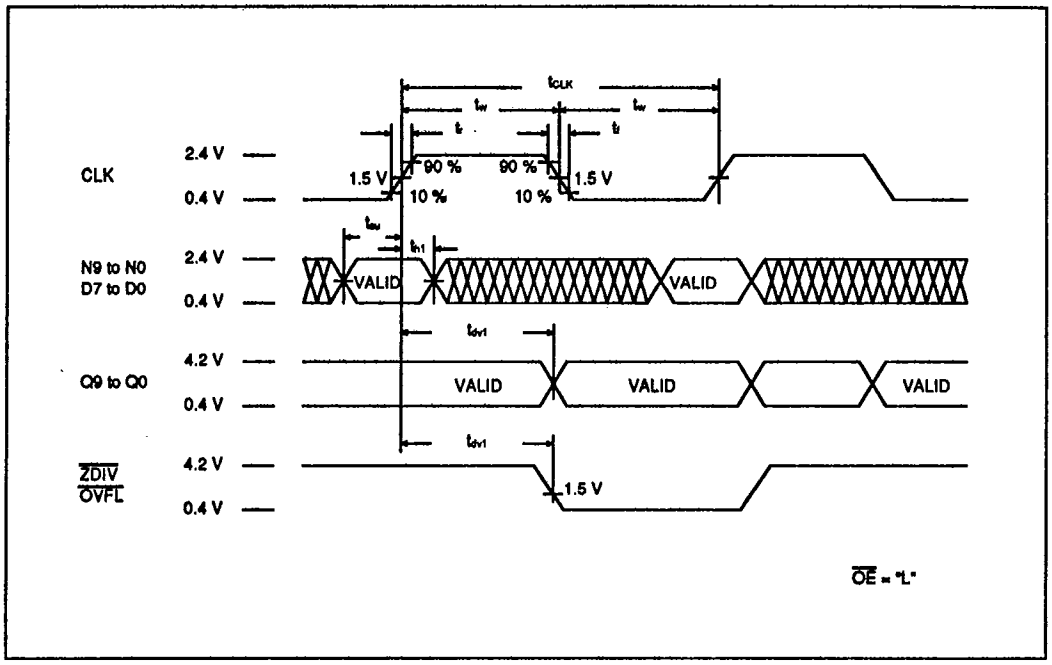
3. Low- to High-level transition delay
High- to Low-level transition delay



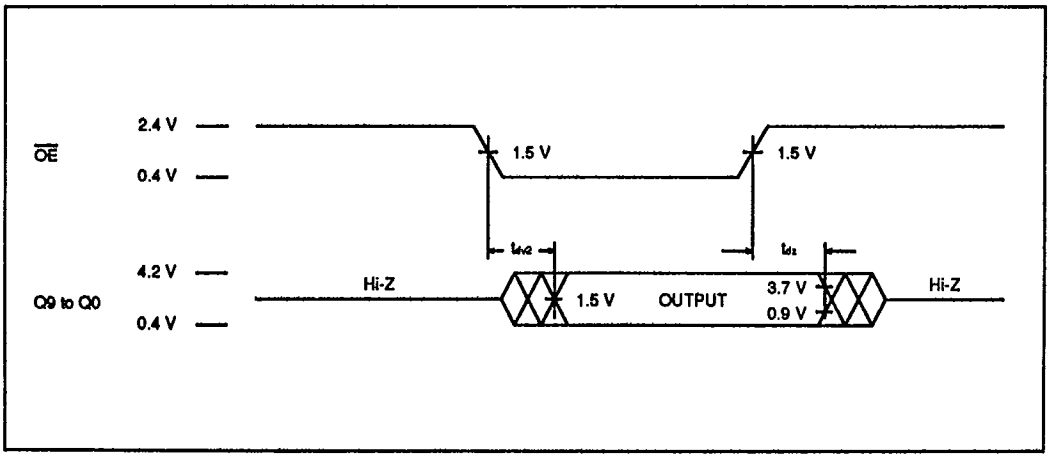
Load conditions:
R_L = 2 kΩ
C_L = 60 pF (Pins $\overline{ZDIV}$ and $\overline{OVFL}$)
65 pF (Pins Q0 to Q9)

TIMING CHART

1. AC characteristics (1)

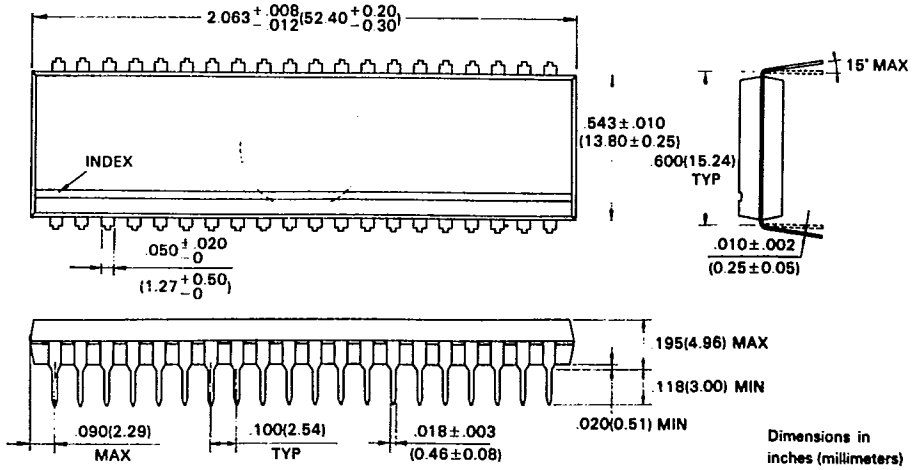


2. AC characteristics (2)



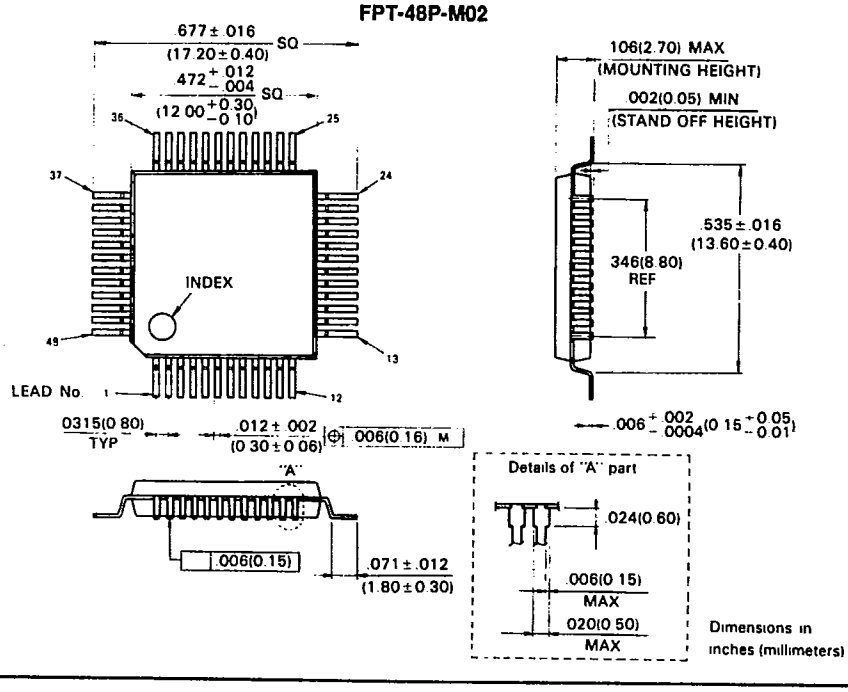
PACKAGE DIMENSIONS

DIP-40P-M01



Dimensions in inches (millimeters)

FPT-48P-M02



Dimensions in inches (millimeters)