

HD66773R

262,144-color, 132 x 176-dot Graphics Controller Driver
for TFT LCD panels

REJxxxxxxx-xxxxZ

Rev.1.20

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Description

The HD66773R is a controller driver LSI compliant to 132RGB x 176-dot graphics display on TFT LCD panel in 262,144 colors. The HD66773R's bit-operation functions, 18-bit high-speed bus interface, and high-speed RAM-write function enable efficient data transfer and high-speed update of graphics RAM data.

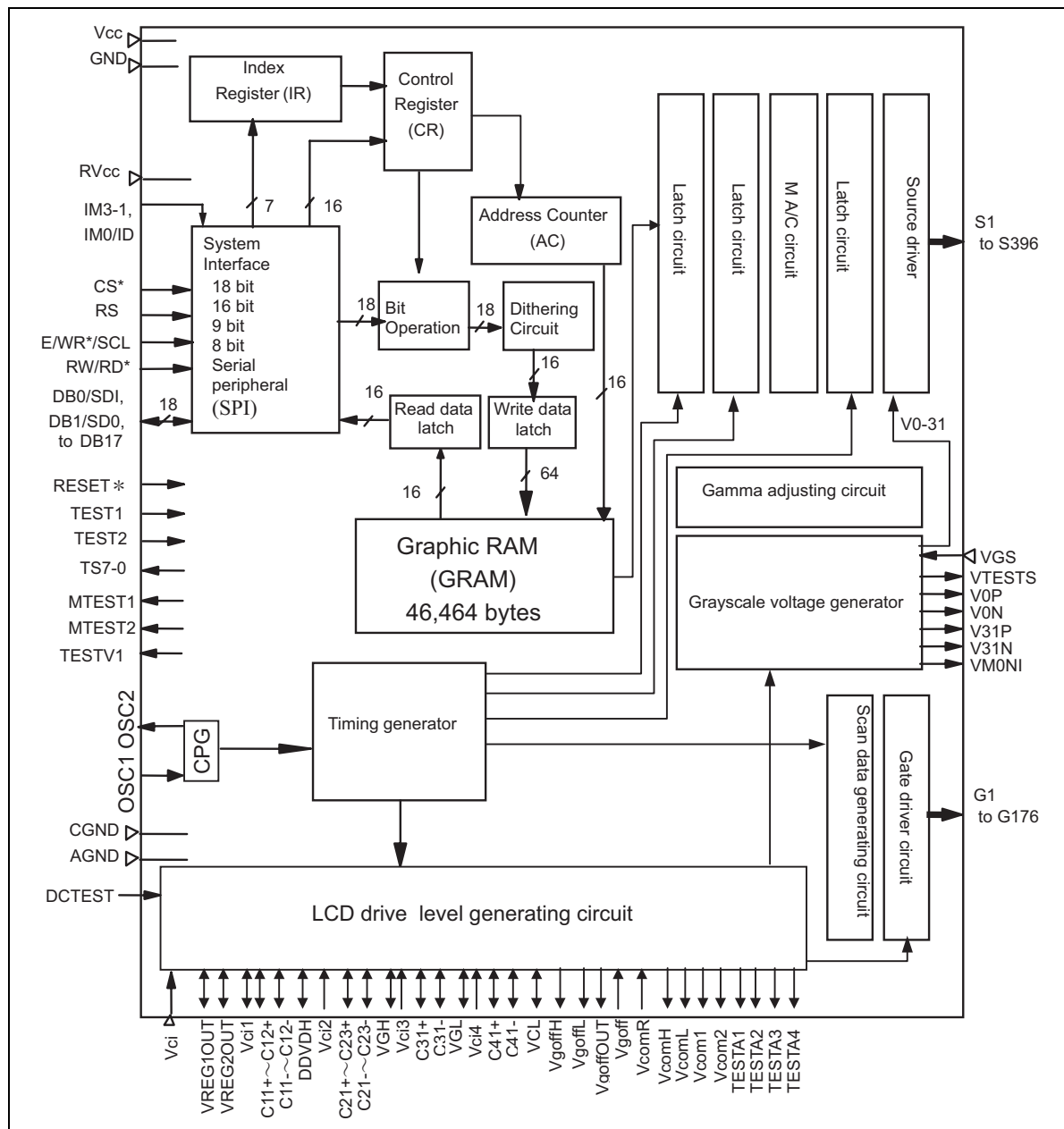
The HD66773R operates with low voltage up to 2.2V for power supply. The HD66773R incorporates TFT gate-drive and source-drive circuits, a step-up circuit to generate LCD drive voltage, and power supply circuits such as breeder resistor and voltage follower for LCD drive, which enable a configuration of LCD module only with external elements such as capacitors and resistors. The HD66773R supports 8-color-display and standby modes, which enable precise power control by software. These features make this LSI the best solution for medium or small sized portable products such as digital cellular phones, bi-directional pagers, or small PDA, which support WWW browser, where long life battery is major concern.

Features

- Single chip controller/driver for 262,144-color, 132RGB x 176-dot graphics display on TFT LCD
- 18-/16-/9-/8-bit high-speed bus interfaces and a Serial Peripheral Interface (SPI)
- High-speed burst-RAM write function
- Window address function enabling data write in a rectangular RAM-address area
- Internal bit-operation for graphics
 - Bit-unit write-data mask function
 - Pixel-unit logical operation / conditional rewrite function
- Abundant color-display control function:
 - 262,144-color display (max.) with gamma adjustment function
 - Line-unit vertical bi-directional scrolling display function
- Architecture with low power consumption
 - Low-voltage operation: $V_{CC} = 2.2 \sim 3.3 \text{ V}$
 - Internal reference voltage power supply: $V_{CI} = 2.5 \sim 3.3 \text{ V}$
 - Standby mode and other power-save functions:
 - Partial LCD drive: 2-screen display at arbitrary two positions
 - Internal power supply circuit
 - Internal equalizing function
- Compliant to Cst/Cadd structures
- Internal power supply circuits
 - Step-up circuit: 5 ~ 9-time scale, polarity inversion
 - Power supply for TFT common electrode: Compliant to Vcom n-raster-row AC drive
 - AC drive: Vgoff n-raster-row AC drive with Cadd structure
 - Vcom (Vgoff) amplitude adjustment: 22-scale internal electronic volume adjustment
 - Output power-supply voltage
 - Voltages for power supply for TFT common electrode:

Vcom amplitude = 6V (max.),
VcomH-GND = VREG1OUT (max.),
VcomL-GND = 1.0V ~ -Vci+0.5V (max.)
- Internal RAM capacity: 46,464 bytes
- LCD drive circuit with 396-output source signal and 176-output gate signal
- n-raster-row inversion drive: polarity inversion by arbitrary number of lines.
- Internal oscillation and hardware reset
- Changeable source and gate shift directions
- Compliant to COG with single chip, incorporating gates arranged on both sides.

Block Diagram



PAD Arrangement

-Chip size: 20.69mm×2.47mm
-Chip thickness: 400 μm (typ.)
-Pad Coordinate: Pad Center
-Coordinate Origin: Chip center

-Au bump size:
(1) 80 μm×80 μm
Corner dummy:
No.1, No.195, No.239, No.742

(2) 54 μm×100 μm
Input side
No.2 to No.194

(3) 36 μm×70 μm
Laced liquid crystal output side:
No.196 to No.238
No.240 to No.741
No.743 to No.786

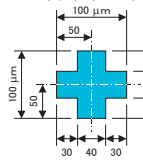
-Au bump pitch: Refer to Pad Coordinate
-Au bump height: 15 μm (typ.)

-Numbers in figure 2 refer to numbers
in Pad coordinate

-Alignment Mark

(1) Assignment: 2places

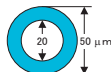
Coordinate (X, Y) = (±10135, 935)



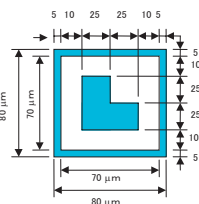
(2-a) Coordinate (X, Y) = (-10119, 1100)



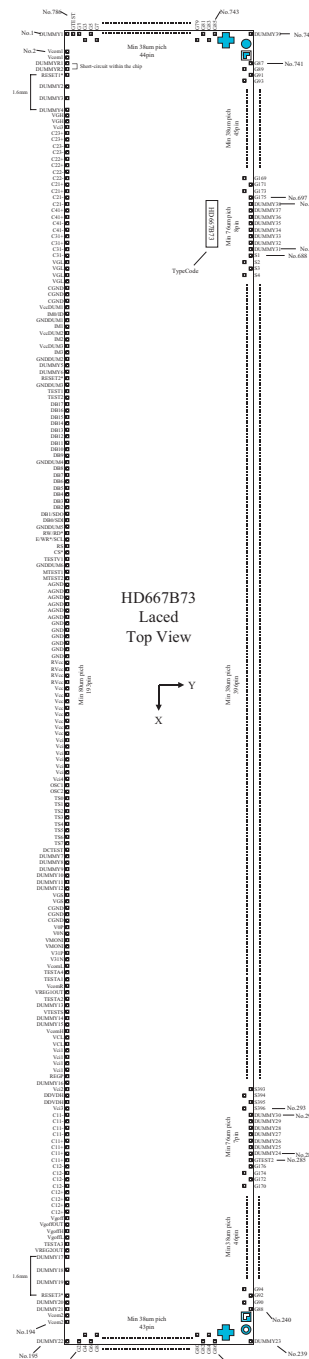
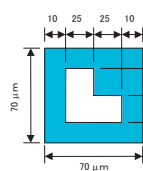
(2-b) Coordinate (X, Y) = (10119, 1100)



(3-a) Coordinate (X, Y) = (-10029, 1100)



(3-b) Coordinate (X, Y) = (10029, 1100)



PAD Coordinate

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-10209	-1099	101	Vcc	109	-1089	201	G12	10104	-4610	301	S388	72409	999
2	Vcom1	-10041	-1080	102	Vcc	189	-1089	202	G14	10214	-572	302	S387	72104	1104
3	Vcom1	-9961	-1080	103	Vcc	269	-1089	203	G16	10104	-534	303	S386	7172	999
4	DUMMYR1	-9859	-1080	104	Vcc	349	-1089	204	G18	10214	-496	304	S385	7134	1104
5	DUMMYR2	-9768	-1080	105	Vcc	430	-1089	205	G20	10104	-458	305	S384	7096	999
6	RESET1	-9650	-1080	106	Vcc	510	-1089	206	G22	10214	-420	306	S383	7058	1104
7	DUMMY2	-9116	-1080	107	Vci	590	-1089	207	G24	10104	-382	307	S382	7020	999
8	DUMMY3	-8582	-1080	108	Vci	670	-1089	208	G26	10214	-343	308	S381	6981	1104
9	DUMMY4	-8048	-1080	109	Vci	750	-1089	209	G28	10104	-305	309	S380	6943	999
10	VGH	-7947	-1080	110	Vci	830	-1089	210	G30	10214	-267	310	S379	6905	1104
11	VGH	-7867	-1080	111	Vci	911	-1089	211	G32	10104	-229	311	S378	6867	999
12	Vci3	-7765	-1080	112	Vci	991	-1089	212	G34	10214	-191	312	S377	6829	1104
13	C23+	-7685	-1080	113	Vci4	1120	-1089	213	G36	10104	-153	313	S376	6791	999
14	C23+	-7605	-1080	114	OSC1	1257	-1089	214	G38	10214	-114	314	S375	6753	1104
15	C23+	-7525	-1080	115	OSC2	1337	-1089	215	G40	10104	-76	315	S374	6714	999
16	C23+	-7445	-1080	116	T80	1418	-1089	216	G42	10214	-38	316	S373	6676	1104
17	C22+	-7365	-1080	117	T81	1498	-1089	217	G44	10104	0	317	S372	6638	999
18	C22+	-7284	-1080	118	T82	1578	-1089	218	G46	10214	38	318	S371	6600	1104
19	C22+	-7204	-1080	119	T83	1658	-1089	219	G48	10104	76	319	S370	6562	999
20	C22+	-7124	-1080	120	T84	1738	-1089	220	G50	10214	114	320	S369	6524	1104
21	C21+	-7044	-1080	121	T85	1818	-1089	221	G52	10104	153	321	S368	6486	999
22	C21+	-6964	-1080	122	S86	1898	-1089	222	G54	10214	191	322	S367	6447	1104
23	C21+	-6884	-1080	123	T87	1979	-1089	223	G56	10104	229	323	S366	6409	999
24	C21+	-6803	-1080	124	DCTEST	2059	-1089	224	G58	10214	267	324	S365	6371	1104
25	C41+	-6723	-1080	125	DUMMY7	2177	-1089	225	G60	10104	305	325	S364	6333	999
26	C41+	-6643	-1080	126	DUMMY8	2257	-1089	226	G62	10214	343	326	S363	6295	1104
27	C41+	-6563	-1080	127	DUMMY9	2337	-1089	227	G64	10104	382	327	S362	6257	999
28	C41+	-6483	-1080	128	DUMMY10	2418	-1089	228	G66	10214	420	328	S361	6218	1104
29	C31+	-6403	-1080	129	DUMMY11	2498	-1089	229	G68	10104	458	329	S360	6180	999
30	C31+	-6323	-1080	130	DUMMY12	2578	-1089	230	G70	10214	496	330	S359	6142	1104
31	C31+	-6242	-1080	131	VGS	2658	-1089	231	G72	10104	534	331	S358	6104	999
32	C31+	-6162	-1080	132	VGS	2765	-1089	232	G74	10214	572	332	S357	6066	1104
33	VGL	-6029	-1080	133	GNND	2872	-1089	233	G76	10104	610	333	S356	6028	999
34	VGL	-5949	-1080	134	GNND	2952	-1089	234	G78	10214	648	334	S355	5990	1104
35	VGL	-5869	-1080	135	GNND	3032	-1089	235	G80	10104	687	335	S354	5951	999
36	VGL	-5789	-1080	136	VOP	3139	-1089	236	G82	10214	725	336	S353	5913	1104
37	GNND	-5687	-1080	137	VON	3210	-1089	237	G84	10104	763	337	S352	5875	999
38	GNND	-5607	-1080	138	VMONI	3290	-1089	238	G86	10214	801	338	S351	5837	1104
39	GNND	-5527	-1080	139	VMONI	3380	-1089	239	DUMMY23	10209	1099	339	S350	5799	999
40	VcDUM1	-5447	-1080	140	V31P	3460	-1089	240	G88	9919	1104	340	S349	5761	1104
41	IMO1D	-5356	-1080	141	V31N	3540	-1089	241	G90	9981	999	341	S348	5723	999
42	GNDDUM1	-5337	-1080	142	VcomH	3620	-1089	242	G92	9943	1104	342	S347	5684	1104
43	IM1	-5146	-1080	143	TESTA4	3737	-1089	243	G94	9905	999	343	S346	5646	999
44	VcDUM2	-5028	-1080	144	TESTA1	3854	-1089	244	G96	9766	1104	344	S345	5608	1104
45	IM2	-4936	-1080	145	VcomR	3934	-1089	245	G98	9728	999	345	S344	5570	999
46	VcDUM3	-4818	-1080	146	REGOUT	4014	-1089	246	G100	9690	1104	346	S343	5532	999
47	IM3	-4727	-1080	147	TESTA2	4094	-1089	247	G102	9652	999	347	S342	5494	999
48	GNDDUM2	-4608	-1080	148	DUMMY13	4201	-1089	248	G104	9614	1104	348	S341	5455	1104
49	DUMMY5	-4528	-1080	149	TESTS	4308	-1089	249	G106	9576	999	349	S340	5417	999
50	DUMMY6	-4448	-1080	150	DUMMY14	4415	-1089	250	G108	9538	1104	350	S339	5379	999
51	RESET2	-4357	-1080	151	DUMMY15	4495	-1089	251	G110	9499	999	351	S338	5341	999
52	GNDDUM3	-4238	-1080	152	VcomH	4602	-1089	252	G112	9461	1104	352	S337	5303	1104
53	TEST1	-4147	-1080	153	VCL	4740	-1089	253	G114	9423	999	353	S336	5265	999
54	TEST2	-4067	-1080	154	VCL	4820	-1089	254	G116	9385	1104	354	S335	5227	1104
55	DB17	-3987	-1080	155	Vci1	4959	-1089	255	G118	9347	999	355	S334	5189	999
56	DB16	-3907	-1080	156	Vci1	5039	-1089	256	G120	9309	1104	356	S333	5150	1104
57	DB15	-3826	-1080	157	Vci1	5119	-1089	257	G122	9270	999	357	S332	5112	999
58	DB14	-3746	-1080	158	Vci1	5199	-1089	258	G124	9232	1104	358	S331	5074	1104
59	DB13	-3666	-1080	159	REGP	5343	-1089	259	G126	9194	999	359	S330	5036	999
60	DB12	-3586	-1080	160	DUMMY16	5450	-1089	260	G128	9156	1104	360	S329	4998	1104
61	DB11	-3506	-1080	161	Vci2	5557	-1089	261	G130	9118	999	361	S328	4960	999
62	DB10	-3426	-1080	162	DDVDH1	5695	-1089	262	G132	9080	1104	362	S327	4921	1104
63	DB9	-3346	-1080	163	DDVDH1	5776	-1089	263	G134	9042	999	363	S326	4883	999
64	GNDDUM4	-3227	-1080	164	Vci3	5909	-1089	264	G136	9003	1104	364	S325	4845	1104
65	DB8	-3136	-1080	165	C11+	6047	-1089	265	G138	8965	999	365	S324	4807	999
66	DB7	-3056	-1080	166	C11+	6127	-1089	266	G140	8927	1104	366	S323	4769	1104
67	DB6	-2976	-1080	167	C11+	6207	-1089	267	G142	8889	999	367	S322	4731	999
68	DB5	-2895	-1080	168	C11+	6287	-1089	268	G144	8851	1104	368	S321	4692	1104
69	DB4	-2815	-1080	169	C11+	6368	-1089	269	G146	8813	999	369	S320	4654	999
70	DB3	-2735	-1080	170	C11+	6448	-1089	270	G148	8775	1104	370	S319	4616	1104
71	DB2	-2655	-1080	171	C11+	6528	-1089	271	G150	8736	999	371	S318	4578	999
72	DB1/SDO	-2575	-1080	172	C11+	6608	-1089	272	G152	8698	1104	372	S317	4540	1104
73	DB0/SDI	-2495	-1080	173	C12+	6688	-1089	273	G154	8660	999	373	S316	4502	999
74	GNDDUM5	-2376	-1080	174	C12+	6768	-1089	274	G156	8622	1104	374	S315	4464	1104
75	EW/RD+	-2295	-1080	175	C12+	6848	-1089	275	G158	8584	999	375	S314	4425	999
76	EW/R+SC1	-2205	-1080	176	C12+	6929	-1089	276	G160	8546	1104	376	S313	4387	1104
77	RS	-2125	-1080	177	C12+	7009	-1089	277	G162	8507	999	377	S312	4349	999
78	TESTV1	-2045	-1080	178	C12+	7089	-1089	278	G164	8469	1104	378	S311	4311	1104
79	GNDDUM6	-1964	-1080	179	C12+	7169	-1089	279	G166	8431	999	379	S310	4273	999
80	GNDDUM6	-1884	-1080	180	C12+	7249	-1089	280	G168	8393	1104	380	S309	4235	1104
81	TEST1	-1755	-1080	181	Vgoff	7388	-1089	281	G170	8355	999	381	S308	4197	999
82	TEST2	-1675	-1080	182	VgoffOUT	7468	-1089	282	G172	8317	1104	382	S307	4158	1104
83	AGND	-1525	-1080	183	VgoffH	7601	-1089	283	G174	8279	999	383	S306	4120	999
84	AGND	-1445	-1080	184	VgoffH	7681	-1089	284	G176	8240	1104	384	S305	4082	1104
85	AGND	-1343	-1080	185	TESTA3	7814	-1089	285	GTEST2	8164	1104	385	S304	4044	999
86	AGND	-1263	-1080	186	REGOUT	7947	-1089	286	DUMMY24	8088	1104	386	S303	4006	1104
87	AGND	-1161	-1080	187	DUMMY17	8048	-1089	287	DUMMY25	8012	1104	387	S302	3968	999
88	AGND	-1081	-1080	188	DUMMY18	8582	-1089	288	DUMMY26	7935	1104	388	S301	3929	1104
89	GNND	-948	-1080	189	DUMMY19	9116	-1089	289	DUMMY27	7859	1104	389	S300	3891	999
90	GNND	-868	-1080	190	RESET3	9650	-1089								

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No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
401	S288	3434	994	501	S188	-420	1104	601	S88	-4235	1104	701	G167	-8393	1104
402	S287	3395	1104	502	S187	-458	994	602	S87	-4273	994	702	G165	-8431	994
403	S286	3357	994	503	S186	-496	1104	603	S86	-4311	1104	703	G163	-8469	1104
404	S285	3319	1104	504	S185	-534	994	604	S85	-4349	994	704	G161	-8507	994
405	S284	3281	994	505	S184	-572	1104	605	S84	-4387	1104	705	G159	-8546	1104
406	S283	3243	1104	506	S183	-610	994	606	S83	-4425	994	706	G157	-8584	994
407	S282	3205	994	507	S182	-649	1104	607	S82	-4464	1104	707	G155	-8622	1104
408	S281	3166	1104	508	S181	-687	994	608	S81	-4502	994	708	G153	-8660	994
409	S280	3128	994	509	S180	-725	1104	609	S80	-4540	1104	709	G151	-8698	1104
410	S279	3090	1104	510	S179	-763	994	610	S79	-4578	994	710	G149	-8736	994
411	S278	3052	994	511	S178	-801	1104	611	S78	-4616	1104	711	G147	-8775	1104
412	S277	3014	1104	512	S177	-839	994	612	S77	-4654	994	712	G145	-8813	994
413	S276	2976	994	513	S176	-877	1104	613	S76	-4692	1104	713	G143	-8851	1104
414	S275	2938	1104	514	S175	-916	994	614	S75	-4731	994	714	G141	-8889	994
415	S274	2899	994	515	S174	-954	1104	615	S74	-4769	1104	715	G139	-8927	1104
416	S273	2861	1104	516	S173	-992	994	616	S73	-4807	994	716	G137	-8965	994
417	S272	2823	994	517	S172	-1030	1104	617	S72	-4845	1104	717	G135	-9003	1104
418	S271	2785	1104	518	S171	-1068	994	618	S71	-4883	994	718	G133	-9042	994
419	S270	2747	994	519	S170	-1106	1104	619	S70	-4921	1104	719	G131	-9080	1104
420	S269	2709	1104	520	S169	-1145	994	620	S69	-4960	994	720	G129	-9118	994
421	S268	2671	994	521	S168	-1183	1104	621	S68	-4998	1104	721	G127	-9156	1104
422	S267	2632	1104	522	S167	-1221	994	622	S67	-5036	994	722	G125	-9194	994
423	S266	2594	994	523	S166	-1259	1104	623	S66	-5074	1104	723	G123	-9232	1104
424	S265	2556	1104	524	S165	-1297	994	624	S65	-5112	994	724	G121	-9270	994
425	S264	2518	994	525	S164	-1335	1104	625	S64	-5150	1104	725	G119	-9308	1104
426	S263	2480	1104	526	S163	-1373	994	626	S63	-5188	994	726	G117	-9347	994
427	S262	2442	994	527	S162	-1412	1104	627	S62	-5227	1104	727	G115	-9385	1104
428	S261	2403	1104	528	S161	-1450	994	628	S61	-5265	994	728	G113	-9423	994
429	S260	2365	994	529	S160	-1488	1104	629	S60	-5303	1104	729	G111	-9461	1104
430	S259	2327	1104	530	S159	-1526	994	630	S59	-5341	994	730	G109	-9499	994
431	S258	2289	994	531	S158	-1564	1104	631	S58	-5379	1104	731	G107	-9538	1104
432	S257	2251	1104	532	S157	-1602	994	632	S57	-5417	994	732	G105	-9576	994
433	S256	2213	994	533	S156	-1640	1104	633	S56	-5455	1104	733	G103	-9614	1104
434	S255	2175	1104	534	S155	-1679	994	634	S55	-5494	994	734	G101	-9652	994
435	S254	2136	994	535	S154	-1717	1104	635	S54	-5532	1104	735	G99	-9690	1104
436	S253	2098	1104	536	S153	-1755	994	636	S53	-5570	994	736	G97	-9728	994
437	S252	2060	994	537	S152	-1793	1104	637	S52	-5608	1104	737	G95	-9766	1104
438	S251	2022	1104	538	S151	-1831	994	638	S51	-5646	994	738	G93	-9805	994
439	S250	1984	994	539	S150	-1869	1104	639	S50	-5684	1104	739	G91	-9843	1104
440	S249	1946	1104	540	S149	-1908	994	640	S49	-5723	994	740	G89	-9881	994
441	S248	1908	994	541	S148	-1946	1104	641	S48	-5761	1104	741	G87	-9919	1104
442	S247	1869	1104	542	S147	-1984	994	642	S47	-5799	994	742	DUMMY39	-10209	1099
443	S246	1831	994	543	S146	-2022	1104	643	S46	-5837	1104	743	G85	-10214	801
444	S245	1793	1104	544	S145	-2060	994	644	S45	-5875	994	744	G83	-10104	763
445	S244	1755	994	545	S144	-2098	1104	645	S44	-5913	1104	745	G81	-10214	725
446	S243	1717	1104	546	S143	-2136	994	646	S43	-5951	994	746	G79	-10104	687
447	S242	1679	994	547	S142	-2175	1104	647	S42	-5990	1104	747	G77	-10214	649
448	S241	1640	1104	548	S141	-2213	994	648	S41	-6028	994	748	G75	-10104	610
449	S240	1602	994	549	S140	-2251	1104	649	S40	-6066	1104	749	G73	-10214	572
450	S239	1564	1104	550	S139	-2289	994	650	S39	-6104	994	750	G71	-10104	534
451	S238	1526	994	551	S138	-2327	1104	651	S38	-6142	1104	751	G69	-10214	496
452	S237	1488	1104	552	S137	-2365	994	652	S37	-6180	994	752	G67	-10104	458
453	S236	1450	994	553	S136	-2403	1104	653	S36	-6218	1104	753	G65	-10214	420
454	S235	1412	1104	554	S135	-2442	994	654	S35	-6257	994	754	G63	-10104	382
455	S234	1373	994	555	S134	-2480	1104	655	S34	-6295	1104	755	G61	-10214	343
456	S233	1335	1104	556	S133	-2518	994	656	S33	-6333	994	756	G59	-10104	305
457	S232	1297	994	557	S132	-2556	1104	657	S32	-6371	1104	757	G57	-10214	267
458	S231	1259	1104	558	S131	-2594	994	658	S31	-6409	994	758	G55	-10104	229
459	S230	1221	994	559	S130	-2632	1104	659	S30	-6447	1104	759	G53	-10214	191
460	S229	1183	1104	560	S129	-2671	994	660	S29	-6486	994	760	G51	-10104	153
461	S228	1145	994	561	S128	-2709	1104	661	S28	-6524	1104	761	G49	-10214	114
462	S227	1106	1104	562	S127	-2747	994	662	S27	-6562	994	762	G47	-10104	76
463	S226	1068	994	563	S126	-2785	1104	663	S26	-6600	1104	763	G45	-10214	38
464	S225	1030	1104	564	S125	-2823	994	664	S25	-6638	994	764	G43	-10104	0
465	S224	992	994	565	S124	-2861	1104	665	S24	-6676	1104	765	G41	-10214	-38
466	S223	954	1104	566	S123	-2899	994	666	S23	-6714	994	766	G39	-10104	-76
467	S222	916	994	567	S122	-2938	1104	667	S22	-6753	1104	767	G37	-10214	-114
468	S221	877	1104	568	S121	-2976	994	668	S21	-6791	994	768	G35	-10104	-153
469	S220	839	994	569	S120	-3014	1104	669	S20	-6829	1104	769	G33	-10214	-191
470	S219	801	1104	570	S119	-3052	994	670	S19	-6867	994	770	G31	-10104	-229
471	S218	763	994	571	S118	-3090	1104	671	S18	-6905	1104	771	G29	-10214	-267
472	S217	725	1104	572	S117	-3128	994	672	S17	-6943	994	772	G27	-10104	-305
473	S216	687	994	573	S116	-3166	1104	673	S16	-6981	1104	773	G25	-10214	-343
474	S215	649	1104	574	S115	-3205	994	674	S15	-7020	994	774	G23	-10104	-382
475	S214	610	994	575	S114	-3243	1104	675	S14	-7058	1104	775	G21	-10214	-420
476	S213	572	1104	576	S113	-3281	994	676	S13	-7096	994	776	G19	-10104	-458
477	S212	534	994	577	S112	-3319	1104	677	S12	-7134	1104	777	G17	-10214	-496
478	S211	496	1104	578	S111	-3357	994	678	S11	-7172	994	778	G15	-10104	-534
479	S210	458	994	579	S110	-3395	1104	679	S10	-7210	1104	779	G13	-10214	-572
480	S209	420	1104	580	S109	-3434	994	680	S9	-7249	994	780	G11	-10104	-610
481	S208	382	994	581	S108	-3472	1104	681	S8	-7287	1104	781	G9	-10214	-649
482	S207	343	1104	582	S107	-3510	994	682	S7	-7325	994	782	G7	-10104	-687
483	S206	305	994	583	S106	-3548	1104	683	S6	-7363	1104	783	G5	-10214	-725
484	S205	267	1104	584	S105	-3586	994	684	S5	-7401	994	784	G3	-10104	-763
485	S204	229	994	585	S104	-3624	1104	685	S4	-7439	1104	785	G1	-10214	-801
486	S203	191	1104	586	S103	-3662	994	686	S3	-7477	994	786	GTEST1	-10214	-877
487	S202	153	994	587	S102	-3701	1104	687	S2	-7516	1104				
488	S201	114	1104	588	S101	-3739	994	688	S1	-7554	994				
489	S200	76	994	589	S100	-3777	1104	689	DUMMY31	-7630	1104				
490	S199	38	1104	590	S99	-3815	994</								

Pin Function

Signals	Number of Pins	I/O	Connected to	Functions
IM3-1, IM0/ID	4	I	GND or V _{CC}	Select the mode interfacing with MPU.
				IM3IM2IM1IM0MPU interfacing modeDB pins
				GNDGNDGNDGND68-system 16-bit interfaceDB17-10,DB8-1
				GNDGNDGNDV _{CC} 68-system 8-bit interfaceDB17-10
				GNDGNDV _{CC} GND80-system 16-bit interfaceDB17-10,DB8-1
				GNDGNDV _{CC} V _{CC} 80-system 8-bit interfaceDB17-10
				GNDV _{CC} GNDIDSerial Peripheral InterfaceDB17-10,DB8-1
				GNDV _{CC} V _{CC} *Setting disabled
				V _{CC} GNDGNDGND68-system 18-bit interfaceDB17-0
				V _{CC} GNDGNDV _{CC} 68-system 9-bit interfaceDB17-9
				V _{CC} GNDV _{CC} GND80-system 18-bit interfaceDB17-0
				V _{CC} GNDV _{CC} V _{CC} 80-system 9-bit interfaceDB17-9
				V _{CC} V _{CC} **Setting disabled
				In Serial Peripheral Interface mode, IM0/ID pin is used for ID setting for the device code.
CS*	1	I	MPU	Chip selection signal. Low: Select HD66773R and accessible High: Not select HD66773R and inaccessible Must be fixed to GND when not used.
RS	1	I	MPU	Register selection signal. Low: Index/status High: Control Must be fixed to V _{CC} or GND in SPI mode.
E/WR*/SCL	1	I	MPU	ENABLE signal to activate data read/write operation in 68-system bus interface. Write strobe signal in 80-system bus interface, write data at low. Synchronizing clock signal in SPI mode.
RW/RD*	1	I	MPU	Read/write selection signal in 68-system bus interface. Low: Write, High: Read Read strobe signal in 80-system bus interface, read data at low. Must be fixed to V _{CC} or GND in SPI mode.
DB0/SDI	1	I/O	MPU	18-bit bi-directional data bus. 8-bit bus interface: DB17-10 9-bit bus interface: DB17-9 16-bit bus interface: DB17-10, 8-1 18-bit bus interface: DB17-0 The pins not used for data transfer must be fixed to V _{CC} or GND. Serial data input pin (SDI) to input on the rising edge of SCL signal in SPI mode.

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Signals	Number of Pins	I/O	Connected to	Functions
DB1/SDO	1	I/O	MPU	18-bit bi-directional data bus. 8-bit bus interface: DB17-10 9-bit bus interface: DB17-9 16-bit bus interface: DB17-10, 8-1 18-bit bus interface: DB17-0 The pins not used for data transfer must be fixed to Vcc or GND. Serial data output pin (SDO) to output on the falling edge of SCL signal in SPI mode.
DB2-DB17	16	I/O	MPU	18-bit bi-directional data bus. 8-bit bus interface: DB17-10 9-bit bus interface: DB17-9 16-bit bus interface: DB17-10, 8-1 18-bit bus interface: DB17-0 The pins not used for data transfer must be fixed to Vcc or GND.
OSC1, OSC2	2	I/O	Oscillation-resistor	Connect to an external resistor for R-C oscillation. When supplying clocks externally, supply with OSC1, and leave OSC2 open.
RESET1* RESET2* RESET3*	3	I	MPU or Reset generating circuit	Reset pin. Initialize the LSI at low. Power-on reset required when turning on the power supply. Supply with either one of RESET1,2,3, and leave the unused pins open.
TEST1	1	I	GND	Test pin. Must be fixed to GND level.
TEST2	1	I	GND	Test pin. Must be fixed to GND level.
Vcc, GND	2	-	Power supply	Logic Vcc: +2.2V ~ +3.3V Logic-side ground, GND: 0V
RVcc	1	-	Power supply	Vcc power supply for internal RAM. Supply same electric potential as Vcc.
AGND	1	-	Power supply	Analogue-side ground, AGND: 0 V
CGND	1	O	Opposing GND for external elements	Output GND level. Opposing GND for external elements (capacitors, diodes).
Vci	1	I	Vcc or power supply	Power supply for analogue circuits. Connect to an external power supply of 2.5V ~ 3.3V.
Vci1	1	I/O	Vcc or power supply	Output internal reference voltage with amplitude between Vci and GND. Reference voltage for step-up circuit1. Connect to an external power supply of 2.75V or lower, when internal reference voltage is not used.
DDVDH	1	I/O	Stabilizing Capacitor or open	Output Vci1 after stepped-up 2~3 times by step-up circuit 1. The step-up scale is determined with internal register setting. Connect to a stabilizing capacitor. When step-up circuit 1 is not used, leave open.
Vci2	1	I	DDVDH or power supply	Reference voltage for step-up circuit 2. Connect to DDVDH. Connect to an external power supply of 5.5V or lower, when DDVDH is not used.
VGH	1	I/O	Stabilizing Capacitor or power supply	Output voltage with amplitude between VGH and GND after stepped-up 2~4 times by step-up circuit 2. The step-up scale is determined with internal register setting. Connect to a stabilizing capacitor. When step-up circuit 2 is not used, connect to an external power supply of 16.5V or lower.

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Signals	Number of Pins	I/O	Connected to	Functions
Vci3	1	I	VGH or DDVDH or power supply	Reference voltage for step-up circuit 3. Connect to VGH or DDVDH. Connect to an external power supply of 16.5V or lower, when internal power supply is not used.
VGL	1	I/O	Stabilizing Capacitor or power supply	Output voltage with amplitude between VGH and GND after multiplied by -1 by step-up circuit 3. Connect to a stabilizing capacitor. When step-up circuit 3 is not used, connect to an external power supply of -16.5V or more.
Vci4	1	I	Vcc or Vci1 or power supply	Reference voltage for a step-up circuit 4. Connect to Vci or an external power supply between 2.5 ~ 3.3 V.
VCL	1	I/O	Stabilizing Capacitor or power supply	Output voltage with amplitude between Vci4 and GND after multiplied by -1 by step-up circuit 4. Connect to a stabilizing capacitor. Power supply for generating VcomL. When using an external power supply, connect to an external power supply of -3.3V or more if VcomL is negative voltage. When VcomL is GND or more, halt step-up circuit 4 and connect it to GND.
VREG1OUT	1	I/O	Stabilizing Capacitor or power supply	Generate from internally generated reference voltage with amplitude Vci-GND and output a reference voltage for VREG1 with amplitude DDVDH-GND. The step-up scale for output voltage is determined with internal register setting. Connect to a stabilizing capacitor. This is a reference voltage for generating Vcom. Connect to an external power supply of DDVDH or lower when step-up circuit 1 is not used.
VREG2OUT	1	I/O	Stabilizing Capacitor or power supply	Generate from internally generated reference voltage with amplitude Vci-GND and output a reference voltage for VREG2 with amplitude GND-VGL. The step-up scale for output voltage is determined with internal register setting. Connect to a stabilizing capacitor. This is a reference voltage for generating VgoffOUT. Connect to an external power supply of VGL or more when step-up circuit 2 is not used.
C11+ ~ C23+, C11 - ~ C23 -	10	—	Step-up capacitor	Connect to a step-up capacitor if necessary depending on step-up scale. When internal step-up circuit is not used, leave open.
C31+, C31-	2	—	Step-up capacitor	Connect to a step-up capacitor for generating the VGL level from the Vci3 and GND levels. When internal step-up circuit is not used, leave open.
C41+, C41-	2	—	Step-up capacitor	Connect to a step-up capacitor for generating the VCL level from the Vci4 and GND levels. When internal step-up circuit is not used, leave open.
Vcom1 Vcom2	2	O	TFT common electrode	Power supply for TFT common electrode. Output the same voltage level as VcomL during display off, and output the level with amplitude VcomH-VcomL during display on. The AC cycle is changeable with liquid crystal drive AC control register (R02). Connect to a TFT common electrode.
VcomR	1	I	Variable resistor or open	VcomH reference voltage. When VcomH is externally adjusted, halt the internal adjuster of VcomH with register setting and place a variable resistor between VREG1OUT and GND. When VcomH is not externally adjusted, leave it open and adjust VcomH with internal register setting.

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Signals	Number of Pins	I/O	Connected to	Functions
VcomH	1	O	Stabilizing Capacitor	Vcom high level generated during Vcom AC drive. Connect to a stabilizing capacitor.
VcomL	1	O	Stabilizing Capacitor or open	The Vcom level without Vcom AC drive, and Vcom low level with Vcom AC drive. The voltage can be adjusted with internal register setting. Connect to a stabilizing capacitor. VcomL output is halted when VCOMG bit is LOW, and in this case, stabilizing capacitor is not necessary.
VgoffOUT	1	O	Vgoff or Open	Output power supply for gate drive. Internal register setting enables AC drive in synchronization with Vcom. Make an appropriate setting for the structure of hold capacitor of TFT display. Output the amplitude VcomH-VcomL in reference to VgoffL with AC drive.
Vgoff	1	I	VgoffOUT or power supply	TFT gate off level. Negative voltage. Connect to VgoffOUT or otherwise, connect to external voltage power supply of VGL or more.
VgoffH	1	O	Stabilizing Capacitor or open	VgoffOUT high level with Vgoff AC drive. Connect to a stabilizing capacitor. The Vgoff output is halted when CAD bit is LOW. In this case, no stabilizing capacitor is necessary.
VgoffL	1	O	Stabilizing Capacitor	VgoffOUT without Vgoff AC drive, and VgoffOUT low level with Vgoff AC drive. The voltage can be adjusted with internal register setting. Connect to a stabilizing capacitor.
VOP V31P	2	I/O	Stabilizing Capacitor	Output from positive-polarity internal operational amplifier when the internal operational amplifier is turned on. Connect to a stabilizing capacitor.
VON V31N	2	I/O	Stabilizing Capacitor	Output from negative-polarity internal operational amplifier when the internal operational amplifier is turned on. Connect to a stabilizing capacitor.
VGS	1	I	GND or external resistor	Reference voltage for grayscale voltage generating circuit. Place a variable resistor externally when adjusting a level for each panel.
S1–S396	396	O	LCD	Source output signal. The shift direction of segment signal is changeable with SS bit: SS = 0, RAM address 0000 is output from S1. SS = 1, it is output from S396. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G1-176	176	O	LCD	Gate output signal. Output VGH level to select a gate line, and output Vgoff level not to select a gate line.
GTEST1-2	2	O	LCD or Open	Dummy gate output signal. Output the VGH level to select a gate line, and output the Vgoff level not to select a gate line when CAD bit is High. Output the Vgoff level not to select a gate line when CAD bit is Low. Leave open when not used.
TESTA1	1	I/O	Stabilizing Capacitor or Open	A test pin for the VcomH output. Leave it open or connect to a stabilizing capacitor if necessary depending on the quality of display.
TESTA2	1	I/O	Stabilizing Capacitor or Open	A test pin for the VcomL output. Leave it open or connect to a stabilizing capacitor if necessary depending on the quality of display.
TESTA3	1	I/O	Stabilizing Capacitor or Open	A test pin for the Vgoff output. Leave it open or connect to a stabilizing capacitor if necessary depending on the quality of display.

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Signals	Number of Pins	I/O	Connected to	Functions
TESTA4	1	I/O	Stabilizing Capacitor or Open	A test pin for the VcomL output. Leave it open or connect to a stabilizing capacitor if necessary depending on the quality of display.
DCTEST	1	I	GND	A test pin. Must be connected to GND.
MTEST1	2	O	Open	Test pins. Leave open.
MTEST2				
VTESTS	1	I/O	Open	A test pin. Leave open.
TS0-TS7	8	O	Open	A test pin. Leave open.
VMONI	1	O	Open	A test pin. Leave open.
TESTV1	1	I	GND	A test pin. Must be connected to GND.
REGP	1	I/O	Open	A test pin for VREG1OUT. Leave open.
DUMMY1, 22, 23, 39	4	O	Open	Test outputs. Leave open.
DUMMY2-21, DUMMY24-38	35	—	Dummy	Dummy pads. Connected to nowhere.

Block Function

1. System Interface

The HD66773R incorporates three kinds of high-speed system interfaces: 68-system and 80-system interfaces with 18-/16-/9-/8-bit bus, and Serial Peripheral Interface (SPI). The interfacing mode is selected with IM3-0 pins.

The HD66773R has three 16-bit registers: index register (IR), write data register (WDR), and read data register (RDR). The IR stores the information of each control register and the index information of GRAM. The WDR temporarily stores data before written to the control register or GRAM. The RDR temporarily stores the data, which is read from GRAM. Data written into GRAM from the MPU is first written into the WDR and then is automatically written into GRAM by internal operation. Since data are read through the RDR from GRAM, the data read out first are invalid and the ensuing data are read out normally.

The execution time for the instructions other than oscillation start is 0-clock cycle, which enables instructions to be written consecutively.

Register Selection (8/9/16/18 Parallel Interface)

80-system		68-system	RS	Operation
WR*	RD*	R/W		
0	1	0	0	Write index into IR
1	0	1	0	Read internal status
0	1	0	1	Write to control register and GRAM through WDR
1	0	1	1	Read from GRAM through RDR

Register Selection (Serial Peripheral Interface)

Start byte

R/W Bits	RS Bits	Operations
0	0	Write index into IR
1	0	Read internal status
0	1	Write to control register and GRAM through WDR
1	1	Read from GRAM through RDR

2. Bit Operation

The HD66773R supports write data mask function to write bit data selectively to GRAM and logical arithmetical operation to perform logical arithmetical operation and conditional rewrite on GRAM display data and then rewrite the data to GRAM. These functions significantly reduce the load on the graphics-processing software in the microcomputer, and enable high-speed overwrite of GRAM display data. For details, see "Graphics Operation Function".

3. Address Counter (AC)

The address counter (AC) assigns addresses to GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing data into GRAM, the AC is automatically updated plus or minus 1. The AC is not updated when the data are read from GRAM. Window address function enables data write only in the rectangular area of GRAM specified by window addresses.

4. Hardware-dither circuit

The hardware-dither circuit converts 18-bit one-pixel data to 16-bit data with hardware-dither conversion.

5. Graphics RAM (GRAM)

GRAM is graphics RAM that stores bit-pattern data of 132 x 176 bytes with 16 bits per pixel.

6. Gray scale power supply voltage generating circuit

The grayscale voltage generation circuit generates liquid crystal drive voltage according to the grayscale level set with the γ -adjustment register, enabling 262,144-color display with 18 bits per pixel. For details, see the “ γ -adjustment Register” section.

7. LCD drive power supply

The LCD drive power supply generates LCD drive voltage levels, VOP, VON, V31P, V31N, VGH, VGL, VgoffOUT, and Vcom.

8. Oscillation Circuit (OSC)

The HD66773R can provide R-C oscillation simply by placing an external oscillation-resistor between OSC1 and OSC2 pins. An appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can be supplied externally. Since R-C oscillation is halted during standby mode, current consumption will be reduced. For details, see “Oscillation Circuit”.

9. LCD Driver Circuit

The LCD driver circuit of HD66773R consists of a 396-output source driver (S1 ~ S396) and a 176-output gate driver (G1 ~ G176). Display pattern data are latched when 396-bit data arrive. The latched data controls source driver and generates drive waveforms. The gate driver, which operates display scan, selects either VGH or Vgoff level to output. The shift direction of outputting 396-bit data from source driver outputs is changeable with the SS bit. The shift direction of gate driver scan is changeable with the GS bit. The scan mode of gate driver is changeable with SM bit. Select an appropriate shift direction and scan mode for an assembly.

GRAM Address MAP

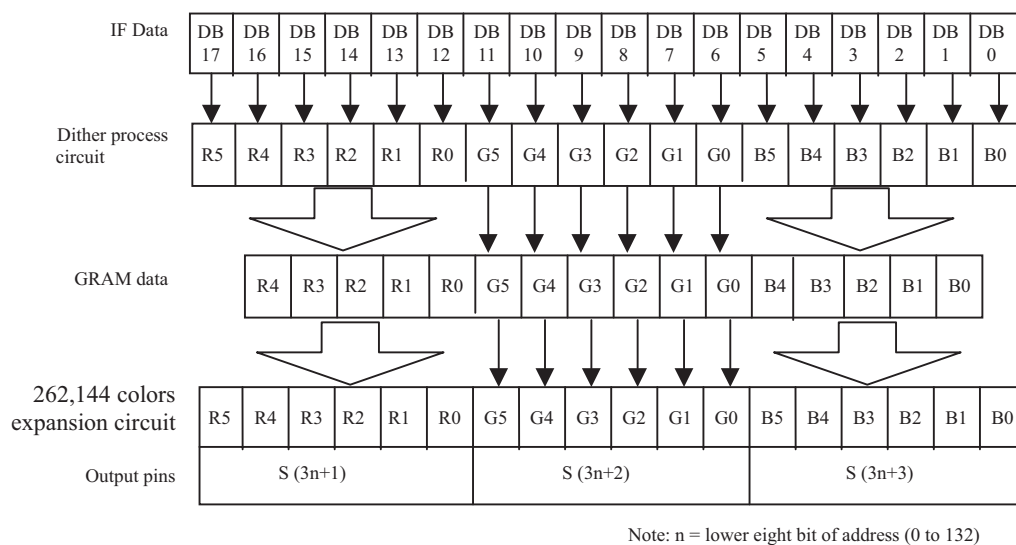
Gram Address and display position on the panel (SS = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0		DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0	DB... 17	DB 0
G1	G176	"0000"	H	"0001"	H	"0002"	H	"0003"	H						"0080"	H	"0081"	H	"0082"	H	"0083"	H				
G2	G175	"0100"	H	"0101"	H	"0102"	H	"0103"	H						"0180"	H	"0181"	H	"0182"	H	"0183"	H				
G3	G174	"0200"	H	"0201"	H	"0202"	H	"0203"	H						"0280"	H	"0281"	H	"0282"	H	"0283"	H				
G4	G173	"0300"	H	"0301"	H	"0302"	H	"0303"	H						"0380"	H	"0381"	H	"0382"	H	"0383"	H				
G5	G172	"0400"	H	"0401"	H	"0402"	H	"0403"	H						"0480"	H	"0481"	H	"0482"	H	"0483"	H				
G6	G171	"0500"	H	"0501"	H	"0502"	H	"0503"	H						"0580"	H	"0581"	H	"0582"	H	"0583"	H				
G7	G170	"0600"	H	"0601"	H	"0602"	H	"0603"	H						"0680"	H	"0681"	H	"0682"	H	"0683"	H				
G8	G169	"0700"	H	"0701"	H	"0702"	H	"0703"	H						"0780"	H	"0781"	H	"0782"	H	"0783"	H				
G9	G168	"0800"	H	"0801"	H	"0802"	H	"0803"	H						"0880"	H	"0881"	H	"0882"	H	"0883"	H				
G10	G167	"0900"	H	"0901"	H	"0902"	H	"0903"	H						"0980"	H	"0981"	H	"0982"	H	"0983"	H				
G11	G166	"0A00"	H	"0A01"	H	"0A02"	H	"0A03"	H						"0A80"	H	"0A81"	H	"0A82"	H	"0A83"	H				
G12	G165	"0B00"	H	"0B01"	H	"0B02"	H	"0B03"	H						"0B80"	H	"0B81"	H	"0B82"	H	"0B83"	H				
G13	G164	"0C00"	H	"0C01"	H	"0C02"	H	"0C03"	H						"0C80"	H	"0C81"	H	"0C82"	H	"0C83"	H				
G14	G163	"0D00"	H	"0D01"	H	"0D02"	H	"0D03"	H						"0D80"	H	"0D81"	H	"0D82"	H	"0D83"	H				
G15	G162	"0E00"	H	"0E01"	H	"0E02"	H	"0E03"	H						"0E80"	H	"0E81"	H	"0E82"	H	"0E83"	H				
G16	G161	"0F00"	H	"0F01"	H	"0F02"	H	"0F03"	H						"0F80"	H	"0F81"	H	"0F82"	H	"0F83"	H				
G17	G160	"1000"	H	"1001"	H	"1002"	H	"1003"	H						"1080"	H	"1081"	H	"1082"	H	"1083"	H				
G18	G159	"1100"	H	"1101"	H	"1102"	H	"1103"	H						"1180"	H	"1181"	H	"1182"	H	"1183"	H				
G19	G158	"1200"	H	"1201"	H	"1202"	H	"1203"	H						"1280"	H	"1281"	H	"1282"	H	"1283"	H				
G20	G157	"1300"	H	"1301"	H	"1302"	H	"1303"	H						"1380"	H	"1381"	H	"1382"	H	"1383"	H				
...	...	...		...		...		...		...		...			...		...		...		...		...		...	
G169	G8	"A800"	H	"A801"	H	"A802"	H	"A803"	H						"A880"	H	"A881"	H	"A882"	H	"A883"	H				
G170	G7	"A900"	H	"A901"	H	"A902"	H	"A903"	H						"A980"	H	"A981"	H	"A982"	H	"A983"	H				
G171	G6	"AA00"	H	"AA01"	H	"AA02"	H	"AA03"	H						"AA80"	H	"AA81"	H	"AA82"	H	"AA83"	H				
G172	G5	"AB00"	H	"AB01"	H	"AB02"	H	"AB03"	H						"AB80"	H	"AB81"	H	"AB82"	H	"AB83"	H				
G173	G4	"AC00"	H	"AC01"	H	"AC02"	H	"AC03"	H						"AC80"	H	"AC81"	H	"AC82"	H	"AC83"	H				
G174	G3	"AD00"	H	"AD01"	H	"AD02"	H	"AD03"	H						"AD80"	H	"AD81"	H	"AD82"	H	"AD83"	H				
G175	G2	"AE00"	H	"AE01"	H	"AE02"	H	"AE03"	H						"AE80"	H	"AE81"	H	"AE82"	H	"AE83"	H				
G176	G1	"AF00"	H	"AF01"	H	"AF02"	H	"AF03"	H						"AF80"	H	"AF81"	H	"AF82"	H	"AF83"	H				

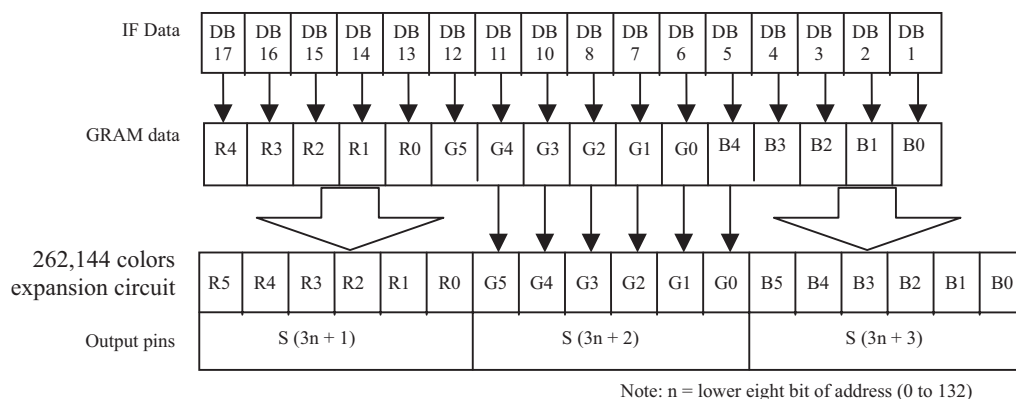
The relationship between GRAM data and display data (SS = "0")

The following figures illustrate the relationship between GRAM data and display data in each interface mode.

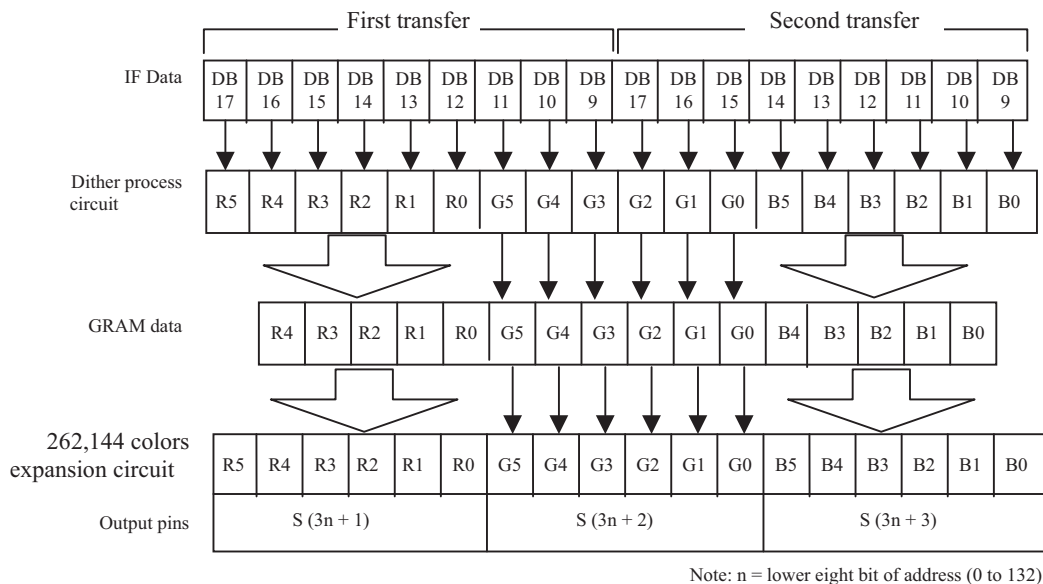
18-bit interface & hard dithering mode



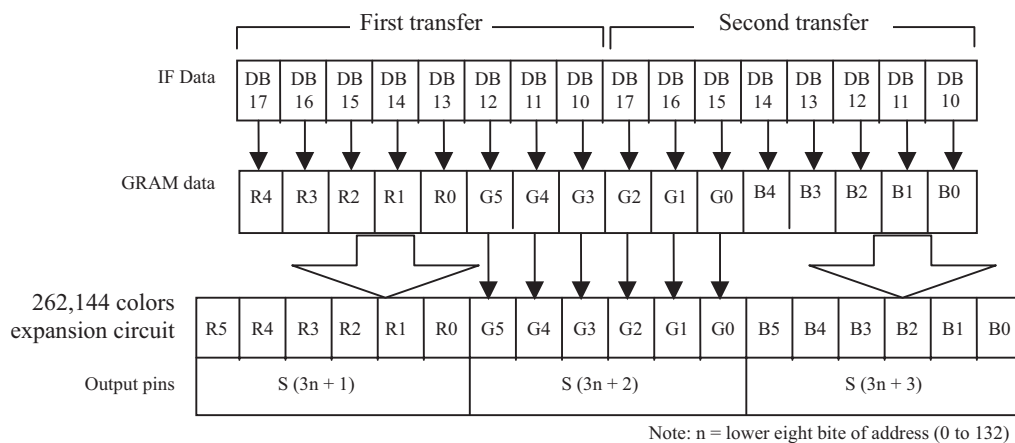
16-bit interface



9-bit interface & hard dither mode



8-bit interface / SPI



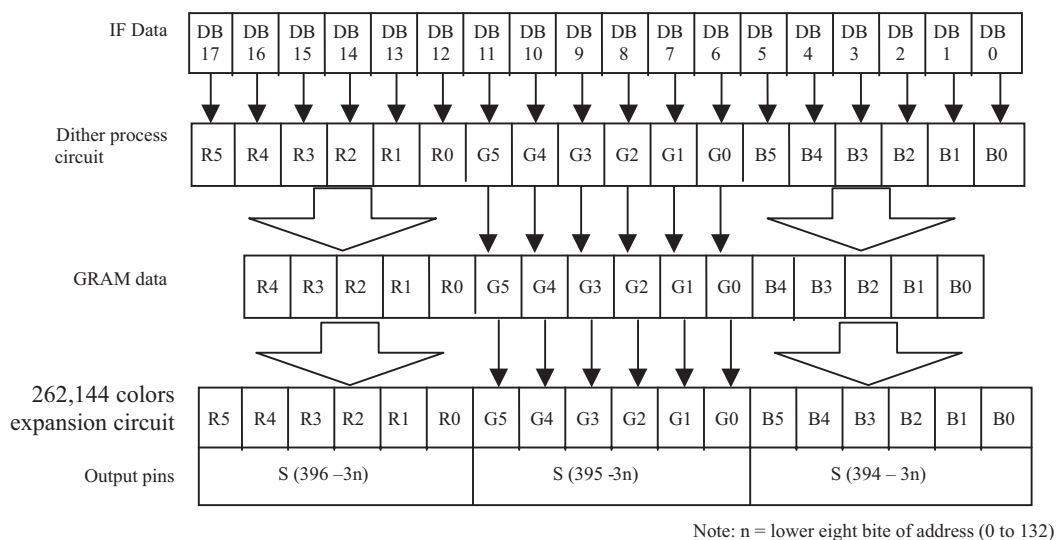
Gram Address and display position on the panel (SS = "1", BGR = "1")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17		DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	DB... 0 17	
G1	G176	"0083"H	"0082"H	"0081"H	"0080"H		"0003"H	"0002"H	"0001"H	"0000"H																
G2	G175	"0183"H	"0182"H	"0181"H	"0180"H		"0103"H	"0102"H	"0101"H	"0100"H																
G3	G174	"0283"H	"0282"H	"0281"H	"0280"H		"0203"H	"0202"H	"0201"H	"0200"H																
G4	G173	"0383"H	"0382"H	"0381"H	"0380"H		"0303"H	"0302"H	"0301"H	"0300"H																
G5	G172	"0483"H	"0482"H	"0481"H	"0480"H		"0403"H	"0402"H	"0401"H	"0400"H																
G6	G171	"0583"H	"0582"H	"0581 H	"0580"H		"0503"H	"0502"H	"0501 H	"0500"H																
G7	G170	"0683"H	"0682"H	"0681"H	"0680"H		"0603"H	"0602"H	"0601"H	"0600"H																
G8	G169	"0783"H	"0782"H	"0781"H	"0780"H		"0703"H	"0702"H	"0701"H	"0700"H																
G9	G168	"0883"H	"0882"H	"0881"H	"0880"H		"0803"H	"0802"H	"0801"H	"0800"H																
G10	G167	"0983"H	"0982"H	"0981"H	"0980"H		"0903"H	"0902"H	"0901"H	"0900"H																
G11	G166	"0A83"H	"0A82"H	"0A81"H	"0A80"H		"0A03"H	"0A02"H	"0A01"H	"0A00"H																
G12	G165	"0B83"H	"0B82"H	"0B81"H	"0B80"H		"0B03"H	"0B02"H	"0B01"H	"0B00"H																
G13	G164	"0C83"H	"0C82"H	"0C81"H	"0C80"H		"0C03"H	"0C02"H	"0C01"H	"0C00"H																
G14	G163	"0D83"H	"0D82"H	"0D81"H	"0D80"H		"0D03"H	"0D02"H	"0D01"H	"0D00"H																
G15	G162	"0E83"H	"0E82"H	"0E81"H	"0E80"H		"0E03"H	"0E02"H	"0E01"H	"0E00"H																
G16	G161	"0F83"H	"0F82"H	"0F81"H	"0F80"H		"0F03"H	"0F02"H	"0F01"H	"0F00"H																
G17	G160	"1083"H	"1082"H	"1081"H	"1080"H		"1003"H	"1002"H	"1001"H	"1000"H																
G18	G159	"1183"H	"1182"H	"1181"H	"1180"H		"1103"H	"1102"H	"1101"H	"1100"H																
G19	G158	"1283"H	"1282"H	"1281"H	"1280"H		"1203"H	"1202"H	"1201"H	"1200"H																
G20	G157	"1383"H	"1382"H	"1381"H	"1380"H		"1303"H	"1302"H	"1301"H	"1300"H																
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
G169	G8	"A883"H	"A882"H	"A881"H	"A880"H		"A803"H	"A802"H	"A801"H	"A800"H																
G170	G7	"A983"H	"A982"H	"A981"H	"A980"H		"A903"H	"A902"H	"A901"H	"A900"H																
G171	G6	"AA83"H	"AA82"H	"AA81"H	"AA80"H		"AA03"H	"AA02"H	"AA01"H	"AA00"H																
G172	G5	"AB83"H	"AB82"H	"AB81"H	"AB80"H		"AB03"H	"AB02"H	"AB01"H	"AB00"H																
G173	G4	"AC83"H	"AC82"H	"AC81"H	"AC80"H		"AC03"H	"AC02"H	"AC01"H	"AC00"H																
G174	G3	"AD83"H	"AD82"H	"AD81"H	"AD80"H		"AD03"H	"AD02"H	"AD01"H	"AD00"H																
G175	G2	"AE83"H	"AE82"H	"AE81"H	"AE80"H		"AE03"H	"AE02"H	"AE01"H	"AE00"H																
G176	G1	"AF83"H	"AF82"H	"AF81"H	"AF80"H		"AF03"H	"AF02"H	"AF01"H	"AF00"H																

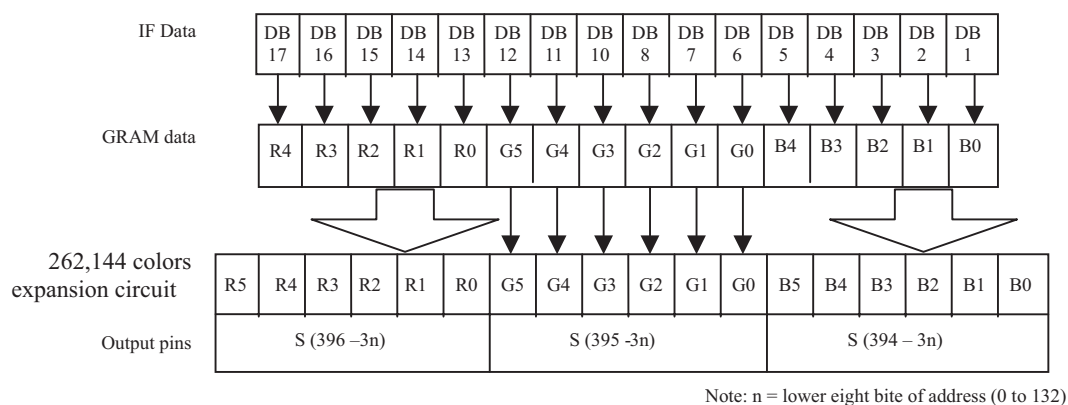
The relationship between GRAM data and display data (SS = "1")

The following figures illustrate the relationship between GRAM data and display data in each interface mode.

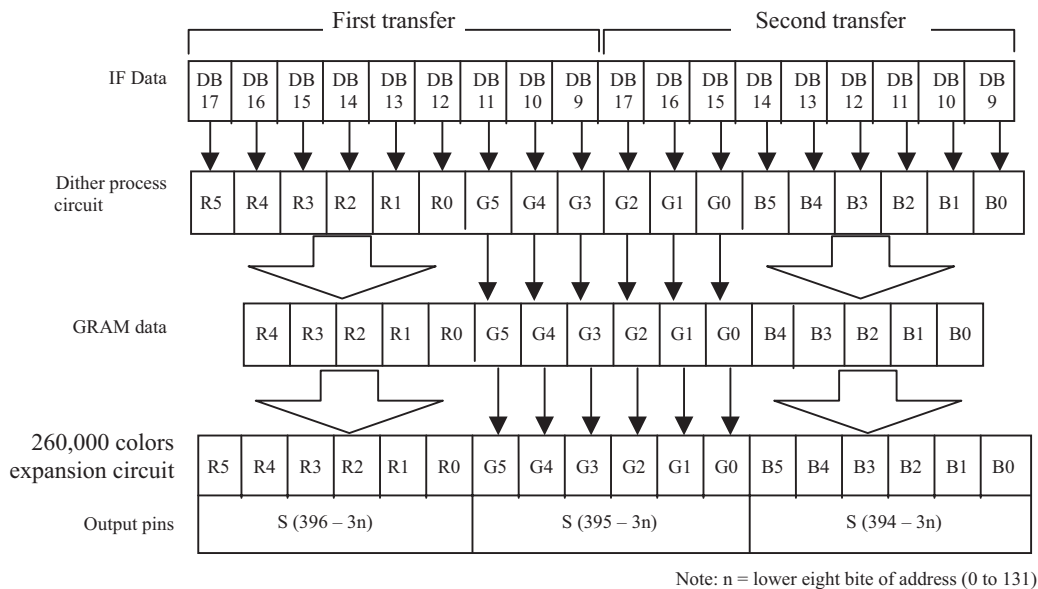
18-bit interface & hard dither mode



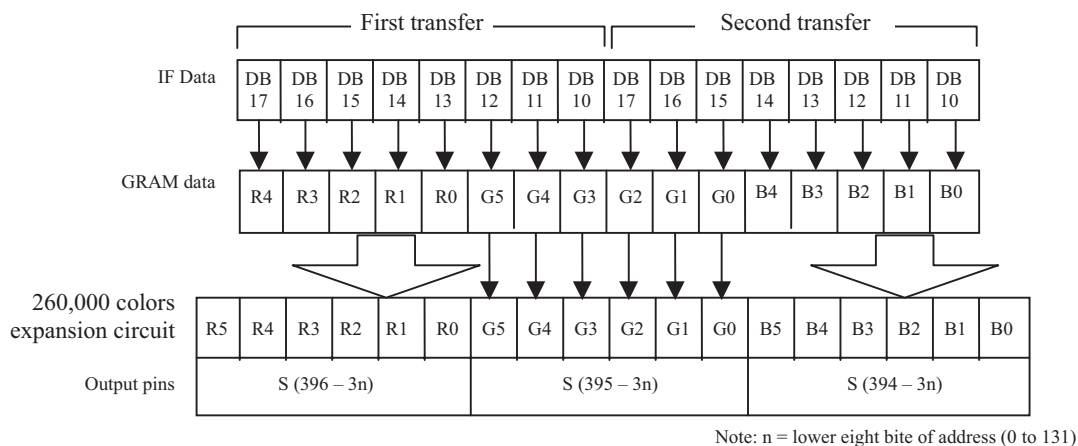
16-bit interface



9-bit interface & hardware dither mode



8-bit interface / SPI



Instructions

Outline

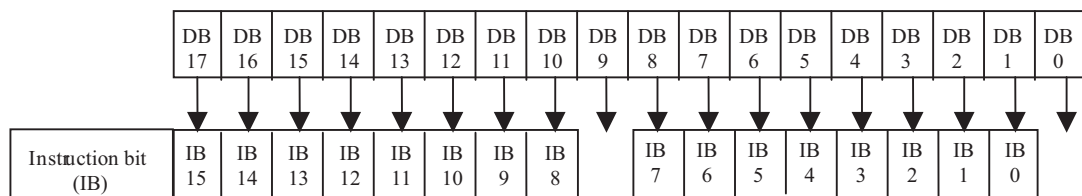
The HD66773R adapts 18-bit bus architecture that enables high-speed interfacing with a high-performance microcomputer. Data sent from external (18/16/9/8 bits) are stored temporarily in the instruction register (IR) and the data register (DR) to store control information before internal operation starts. Since internal operation is decided according to the signal sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signal (DB15 to DB0) are called instruction. GRAM is accessed through internal 18-bit data bus. There are eight categories of instructions:

1. Specify index
2. Read status
3. Control display
4. Control power management
5. Process graphics data
6. Set internal GRAM addresses
7. Transfer data to and from internal GRAM
8. Set grayscale level for internal grayscale γ -adjustment

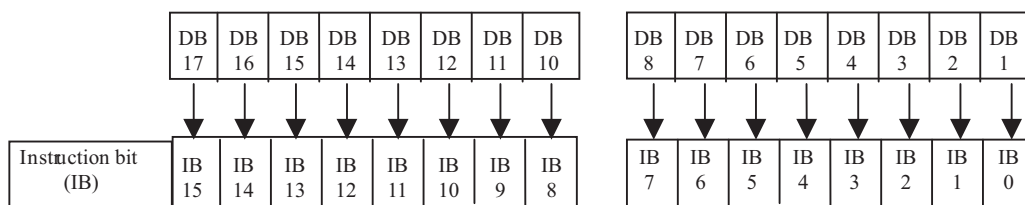
Normally, the 7th instruction to write data to be displayed is executed the most frequently. The address of internal GRAM is updated automatically after data are written to internal GRAM. With window address function, this reduces the amount of data transmission to minimum and thereby lightens the load on the program in the microcomputer. Since instructions are executed in 0 cycle, it is possible to write instructions consecutively.

As the following figure shows, the assignment to the 16 instruction bits (IB15-0) varies according to the interface to be used. An instruction must adopt the data format for each interface.

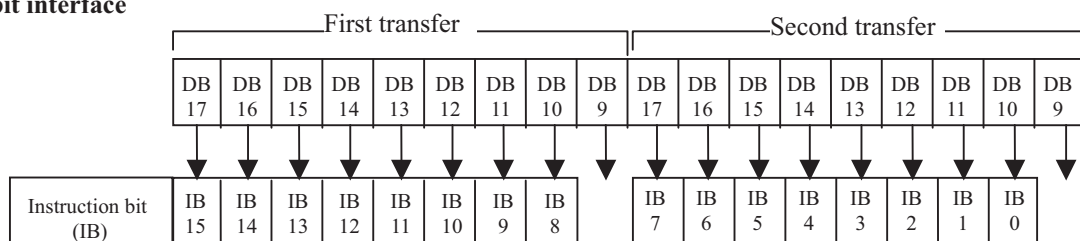
18-bit interface



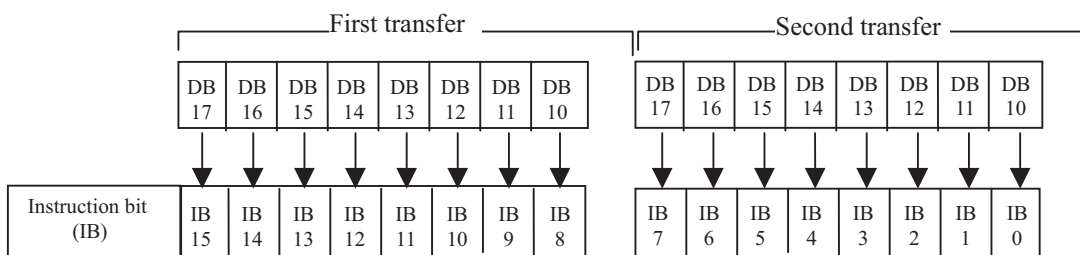
16-bit interface



9-bit interface



8-bit interface/SPI



Instruction bit assignment

HD66773R

Instructions

The following are detail explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index

The index instruction specifies a index (R00h to R3Bh) of control registers and RAM control, that is accessed. It sets the register number from 0000000 to 11111111 in binary form. Do not try to access to the register to which instruction is not assigned.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Status Read

The status read instruction reads the internal status of the HD66773R.

L7–0: Indicate the position of raster-row driving liquid crystal.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator in a halt state during standby mode. After executing this instruction, wait at least 10 ms for stabilizing oscillation before issuing a next instruction. For details, see the “Standby Mode” section.

“0773”H is read out, if this register is forced to read out.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	1	1

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

GS: Select the shift direction of outputs from the gate driver. The scan order by the gate driver is changeable in accordance to the scan mode of gate driver. Select an optimum shift direction for the assembly.

SM: Set the scan order by the gate driver. Select an optimum scan order for the assembly. For details, see “Scan Mode Setting”.

SS: Select the shift direction of outputs from the source driver. When SS = 0, the shift direction of outputs is from S1 to S396. When SS = 1, the shift direction of outputs is from S396 to S1. In addition to the shift direction, setting for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins. To assign R, G, B dots to the source driver pins interchangeably from S1, set SS = 0, BGR = 0. To assign R, G, B dots to the source driver pins interchangeably from S396, set SS = 1, BGR = 1.

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NL4-0: Specify the number of LCD drive raster-rows. The number of drive raster-rows is adjusted by 8 multiple raster-rows. The mapping of addresses to GRAM is independent of this setting. Select the number of raster-rows so that the display size covers the size of a panel.

NL bits

NL4	NL3	NL2	NL1	NL0	Display Size	Number of LCD Driver Lines	Gate Driver Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	396 x 16 dots	16	G1 to G16
0	0	0	1	0	396 x 24 dots	24	G1 to G24
0	0	0	1	1	396 x 32 dots	32	G1 to G32
0	0	1	0	0	396 x 40 dots	40	G1 to G40
0	0	1	0	1	396 x 48 dots	48	G1 to G48
0	0	1	1	0	396 x 56 dots	56	G1 to G56
0	0	1	1	1	396 x 64 dots	64	G1 to G64
0	1	0	0	0	396 x 72 dots	72	G1 to G72
0	1	0	0	1	396 x 80 dots	80	G1 to G80
0	1	0	1	0	396 x 88 dots	88	G1 to G88
0	1	0	1	1	396 x 96 dots	96	G1 to G96
0	1	1	0	0	396 x 104 dots	104	G1 to G104
0	1	1	0	1	396 x 112 dots	112	G1 to G112
0	1	1	1	0	396 x 120 dots	120	G1 to G120
0	1	1	1	1	396 x 128 dots	128	G1 to G128
1	0	0	0	0	396 x 136 dots	136	G1 to G136
1	0	0	0	1	396 x 144 dots	144	G1 to G144
1	0	0	1	0	396 x 152 dots	152	G1 to G152
1	0	0	1	1	396 x 160 dots	160	G1 to G160
1	0	1	0	0	396 x 168 dots	168	G1 to G168
1	0	1	0	1	396 x 176 dots	176	G1 to G176

Note 1) A blanking period which lasts 8H, where all gate lines output Vgoff level, will be inserted after driving all gate lines.

LCD Driving Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

FLD1-0: Specify the number of fields during n-field interlaced drive. For details, see “Interlaced Drive”.

FLD Bits

FLD1	FLD0	Number of Fields
0	0	Setting disabled
0	1	1 field
1	0	Setting disabled
1	1	3 fields

B/C: When B/C =0, a field AC waveform is generated. Alternation occurs every frame to drive liquid crystal. When B/C=1, alternation occurs every n raster-rows according to the settings in EOR and NW5-0 bits of the LCD driving waveform control register. For details, see “n-raster-row Inversion AC Drive”.

EOR: When EOR = 1 and a C-pattern waveform is generated (B/C =1), an odd/even frame select signal and an n-raster-row inversion signal are AC-driven. This instruction is available when liquid crystal AC drive is not made depending on the combination of numbers of LCD drive raster-rows and the value of “n” of n-raster-row inversion AC drive. For details, see “n-raster-row inversion AC drive”.

NW5-0: Specify n, the number of raster-rows from 1 to 64 to alternate every n+1 raster-rows when C-pattern waveform is generated (B/C = 1).

Power Control 1 (R03h)**Power Control 2 (R04h)**

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
W	1	CAD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BT2–0: Change the step-up scale of the step-up circuit. Adjust the scale according to the voltage. Smaller scale consumes lesser current.

BT2	BT1	BT0	DDVDH Output	VGH Output	Note*	Capacitor connect pin
0	0	0	2 x Vci1	3 x Vci2	$VGH = Vci1 \times 6$	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C31±, C41±
0	0	1	2 x Vci1	4 x Vci2	$VGH = Vci1 \times 8$	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C23±, C31±, C41±
0	1	0	3 x Vci1	3 x Vci2	$VGH = Vci1 \times 9$	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±, C31±, C41±
0	1	1	3 x Vci1	2 x Vci2	$VGH = Vci1 \times 6$	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±, C31±, C41±
1	0	0	2 x Vci1	$Vci1 + 2 \times Vci2$	$VGH = Vci1 \times 5$	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C31±, C41±
1	0	1	2 x Vci1	$Vci1 + 3 \times Vci2$	$VGH = Vci1 \times 7$	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C23±, C31±, C41±
1	1	0	Step-up disabled	3 x Vci2	$VGH = Vci2 \times 3$	DDVDH, VGH, VGL, VCL, C21±, C22±, C31±, C41±
1	1	1	Setting disabled	Setting disabled	Setting disabled	—

Note*) The VGH is stepped-up from Vci1, which is the voltage level when DDVDH and Vci2 is short-circuited. The VGH must be set to satisfy $VDDVDH \leq 5.5 \text{ V}$ and $VGH \leq 16.5 \text{ V}$.

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DC2–0: Select the operating frequency for the step-up circuit. The higher step-up frequency enhances the drive capacity of step-up circuit as well as the display quality, while the current consumption will increase. Adjust the frequency taking both the display quality and the current consumption into consideration.

DC2	DC1	DC0	Step-up Cycle of Step-up Circuit 1	Step-up Cycle in Step-up Circuits 2/3/4
0	0	0	DCCLK / 16	DCCLK / 64
0	0	1	DCCLK / 32	DCCLK / 64
0	1	0	DCCLK / 64	DCCLK / 64
0	1	1	DCCLK / 32	DCCLK / 256
1	0	0	DCCLK / 16	DCCLK / 128
1	0	1	DCCLK / 32	DCCLK / 128
1	1	0	DCCLK / 64	DCCLK / 128
1	1	1	DCCLK / 64	DCCLK / 256

AP2–0: Adjust the amount of fixed current from the fixed current source in the operational amplifier circuit in the liquid crystal drive power supply. When the amount of fixed current is set large, the liquid crystal drive capacity is enhanced and the display quality will improve, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. During non-display operation, set AP2-0 = “000” to halt the operation of operational amplifier and step-up circuit to further reduce current consumption.

AP2	AP1	AP0	Amount of Current in Operational Amplifier
0	0	0	Halt operational amplifier and step-up circuit
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting disabled
1	1	1	Setting disabled

SLP: When SLP = 1, the HD66773R enters into the sleep mode. In the sleep mode, internal display operation is halted except the R-C oscillator to reduce current consumption. No change is made to the GRAM data or instructions during the sleep mode, but it is retained.

STB: When STB = 1, the HD66773R enters into the standby mode. In the standby mode, display operation is completely halted, and all internal operation including the internal R-C oscillator and reception of external clock pulse, is halted. For details, see “Standby Mode”. Only instructions to access R03h including the standby bit and to start oscillation are accepted during the standby mode.

CAD: Make an appropriate setting for the structure of TFT panel holding capacitor.

Set CAD = “0” for Cst structure.

Set CAD = “1” for Cadd structure.

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Power Control 3 (R0Ch)

Power Control 4 (R0Dh)

Power Control 5 (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
W	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
W	1	0	0	VCO MG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

VC2-0: Adjust reference voltage for VREG1OUT, VREG2OUT, and Vci1 to the level of Vci multiples. When VC2-0 = “111”, internal reference voltage generation is halted and an arbitrary level of voltage can be applied through Vci1.

VC2	VC1	VC0	VREG1OUT (reference, Vci1 output , REGP output voltage)
0	0	0	Vci
0	0	1	0.92 x Vci
0	1	0	0.87 x Vci
0	1	1	0.83 x Vci
1	0	0	0.76 x Vci
1	0	1	0.73 x Vci
1	1	0	0.68 x Vci
1	1	1	Vci1: Hi-Z REGP: GND

Note) Leave REGP open so that the voltage as specified above is output.

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VRL3-0: Set the amplifying scale of VREG2OUT voltage (the reference voltage for V_{goff}). The output from V_{ci} voltage adjustment circuit can be amplified by $-1.5 \sim -6.5$ times.

VRL3	VRL2	VRL1	VRL0	VREG2OUT Voltage
0	0	0	0	$V_{ci} \times -1.5$
0	0	0	1	$V_{ci} \times -2.0$
0	0	1	0	$V_{ci} \times -2.5$
0	0	1	1	$V_{ci} \times -3.0$
0	1	0	0	$V_{ci} \times -3.5$
0	1	0	1	$V_{ci} \times -4.0$
0	1	1	0	$V_{ci} \times -4.5$
0	1	1	1	Halt
1	0	0	0	$V_{ci} \times -5.0$
1	0	0	1	$V_{ci} \times -5.5$
1	0	1	0	$V_{ci} \times -6.0$
1	0	1	1	$V_{ci} \times -6.5$
1	1	0	0	Setting inhibited
1	1	0	1	Setting inhibited
1	1	1	0	Setting inhibited
1	1	1	1	Halt

Note) Adjust V_{ci} and VRL3-0 so that the VREG2OUT voltage is -16.0 V or more.

PON: Start operation of step-up circuit 3. To halt operation, set $PON = 0$. To start operation, set $PON = 1$.

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VRH3-0: Set the amplifying scale of VLOUT1 voltage (the reference voltage for VCOM and grayscale voltage). The output from Vciout output amplifier can be amplified by 1.33 ~ 2.775 times.

VRH3	VRH2	VRH1	VRH0	VREG1OUT Voltage
0	0	0	0	REGP x 1.33
0	0	0	1	REGP x 1.45
0	0	1	0	REGP x 1.55
0	0	1	1	REGP x 1.65
0	1	0	0	REGP x 1.75
0	1	0	1	REGP x 1.80
0	1	1	0	REGP x 1.85
0	1	1	1	Halt
1	0	0	0	REGP x 1.900
1	0	0	1	REGP x 2.175
1	0	1	0	REGP x 2.325
1	0	1	1	REGP x 2.475
1	1	0	0	REGP x 2.625
1	1	0	1	REGP x 2.700
1	1	1	0	REGP x 2.775
1	1	1	1	Halt

Note) Adjust VC2-0 and VRH3-0 so that the VREG1OUT voltage is 5.0 V or less.

VCOMG: When VCOMG = 1, VcomL outputs a negative voltage up to -5V. When VCOMG = 0, the VcomL voltage is GND and negative-polarity amplifier is halted to reduce power consumption. When VCOMG = "0", the setting in VDV4-0 is made invalid. In this case, make adjustment for the AC amplitudes of Vcom and Vgoff with VCM4-0, VcomH settings.

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VDV4-0: Set the AC amplitude of Vcom and Vgoff during Vcom AC drive. The amplitude can be specified within the range of VREG1OUT x 0.6 ~ 1.23. When VCOMG = 0, this setting is invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VREG1OUT x 0.60
0	0	0	0	1	VREG1OUT x 0.63
0	0	0	1	0	VREG1OUT x 0.66
:	:	:	:	:	
0	1	1	0	0	VREG1OUT x 0.96
0	1	1	0	1	VREG1OUT x 0.99
0	1	1	1	0	VREG1OUT x 1.02
0	1	1	1	1	Setting disabled
1	0	0	0	0	VREG1OUT x 1.05
1	0	0	0	1	VREG1OUT x 1.08
1	0	0	1	0	VREG1OUT x 1.11
1	0	0	1	1	VREG1OUT x 1.14
1	0	1	0	0	VREG1OUT x 1.17
1	0	1	0	1	VREG1OUT x 1.20
1	0	1	1	0	VREG1OUT x 1.23
1	0	1	1	1	Setting disabled
1	1	*	*	*	Setting disabled

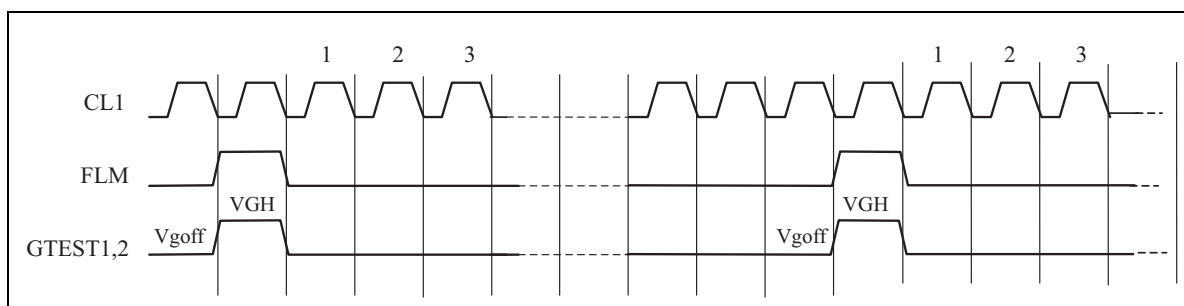
Note) Adjust VREG1OUT and VDV4-0 so that the Vcom and Vgoff amplitudes are 6.0 V or less.

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VC4-0: Set the VcomH voltage (The higher voltage during Vcom AC drive). The amplitude can be specified within the range of VREG1OUT x 0.4 ~ 0.98. When VC4-0 = “1111”, the internal volume adjustment operation is halted, and the VcomH voltage can be adjust by placing an external resistor at VcomR.

VC4	VC3	VC2	VC1	VC0	VcomH Voltage
0	0	0	0	0	VREG1OUT x 0.40
0	0	0	0	1	VREG1OUT x 0.42
0	0	0	1	0	VREG1OUT x 0.44
:	:	:	:	:	
0	1	1	0	0	VREG1OUT x 0.64
0	1	1	0	1	VREG1OUT x 0.66
0	1	1	1	0	VREG1OUT x 0.68
0	1	1	1	1	Halt internal volume. Adjust by an external variable resistor VcomR.
1	0	0	0	0	VREG1OUT x 0.70
1	0	0	0	1	VREG1OUT x 0.72
1	0	0	1	0	VREG1OUT x 0.74
:	:	:	:	:	
1	1	1	0	0	VREG1OUT x 0.94
1	1	1	0	1	VREG1OUT x 0.96
1	1	1	1	0	VREG1OUT x 0.98
1	1	1	1	1	Halt internal volume. Adjust by an external variable resistor VcomR.

Note) Adjust VREG1OUT and VC4-0 so that the VcomH voltage is the VDH level or less.



GTEST1, 2 Output Timing Chart

Entry Mode (R05h)

Compare Register (R06h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DIT	0	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

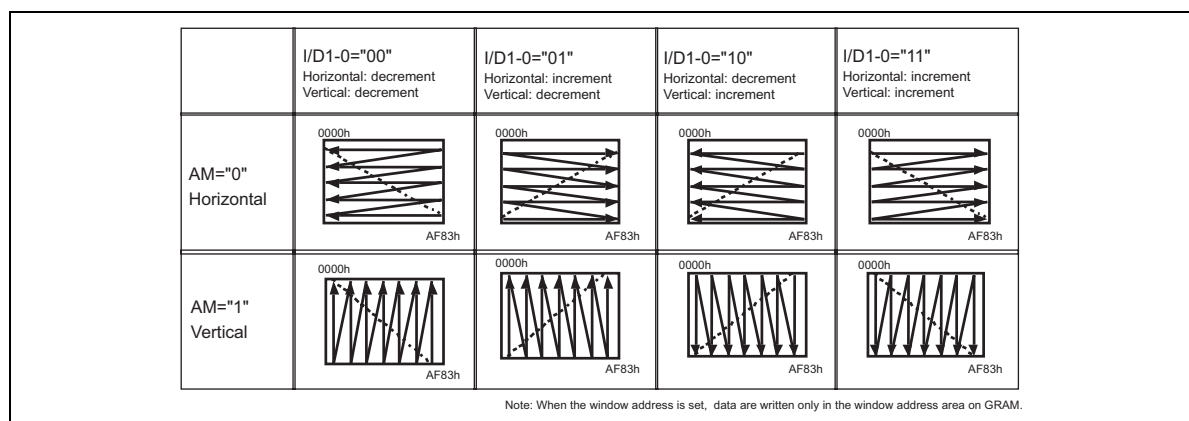
The HD66773R modifies write data sent from the microcomputer before writing to GRAM. This enables high-speed GRAM data update, and reduces the load on the microcomputer software. For details, see “Graphics Operation Function”.

HWM: When HWM=1, data are written to GRAM in high speed. In high-speed write mode, 4 words are written to GRAM in a single operation after executing 4 RAM write operations. If RAM write is terminated before it is executed 4 times, the last data will not be written. Make sure that RAM write is executed 4 times. For this reason, the lower 2 bits must be set to “0” when setting the RAM address. For details, “High-Speed RAM Write Mode”.

I/D1-0: The address counter is automatically incremented by 1, after data are written to GRAM when I/D1-0 = “1”. The address counter is automatically decremented by 1, after data are written to GRAM when I/D1-0 = “0”. The setting for the increment or decrement of the address counter can be made independently for each upper and lower bits of the address. The transition direction of the address when data are written to GRAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to GRAM. When AM = “0”, the address counter is updated in the horizontal direction. When AM = “1”, the address counter is updated in the vertical direction. When window addresses are specified, data are written to the GRAM area specified by the window address in the manner specified with I/D1-0, AM bits.

DIT: Hardware-dither mode when DIT = “1”. Use hardware-dither mode with 18/9-bit interface modes.

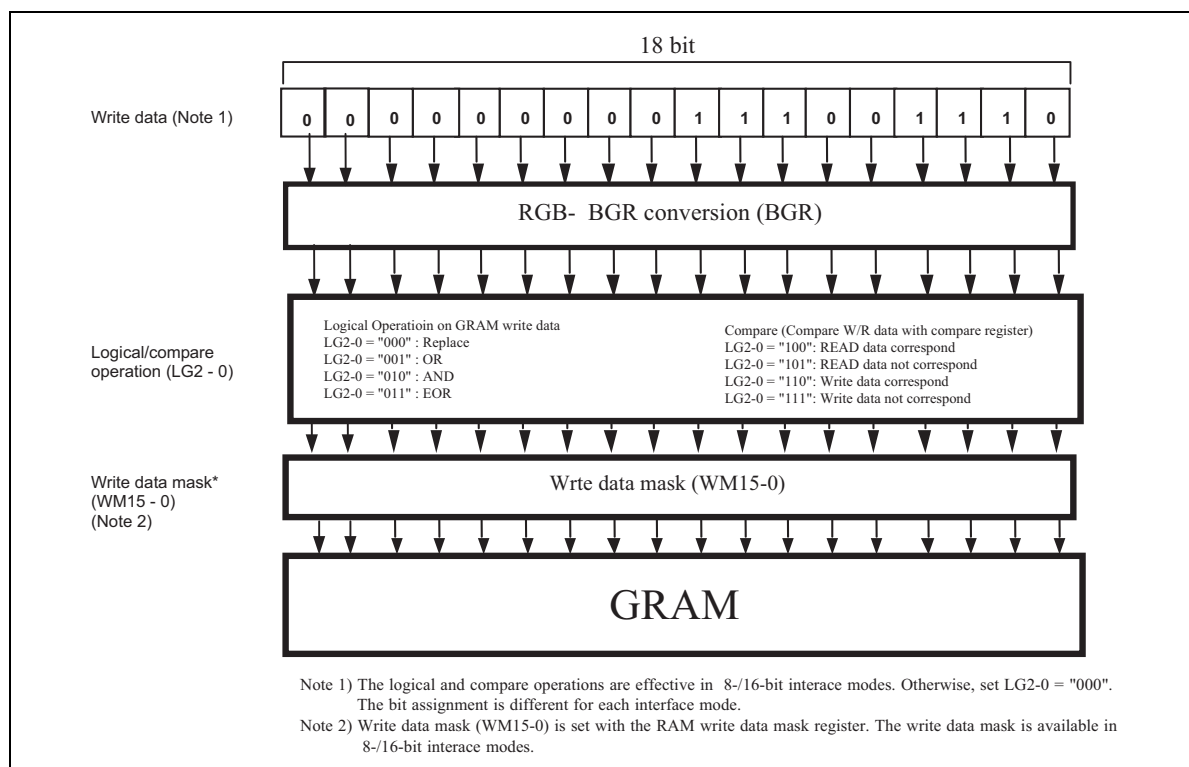


Address transition direction

LG2-0: Rewrite data to GRAM after comparing the data that are written by the microcomputer to GRAM with the values in the compare registers (CP17-0) and performing a logical operation. For details, see “Graphics Operation function”.

CP15-0: Set the value for the compare register, with which the data read out from GRAM or data written to GRAM by the microcomputer are compared. This function is not available with 18/19-bit interface modes. In 18/19-bit interface modes, make sure LG2-0 = “000”.

BGR: Reverse the order from R, G, B to B, G, R for GRAM data. When setting BGR = 1, CP15-0 and WM15-0 bits will be automatically changed to the same effect.



Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

PT1-0: Specify the kind of source output when non-display area is driven in the partial display mode. For details, see “Screen-split drive function”.

VLE2-1: When VLE1 = 1, the first screen is scrolled in the vertical direction. When VLE2 = 1, the second screen is scrolled in the vertical direction. The first and second screens cannot be scrolled simultaneously. This function is not available with external display interface mode.

VLE Bits

VLE2	VLE1	Image on 2nd Screen	Image on 1st Screen
0	0	Stationary	Stationary
0	1	Stationary	Scrolled
1	0	Scrolled	Stationary
1	1	Setting disabled	Setting disabled

CL: When CL = 1, 8-color display mode is selected. For details, see “8-Color Display Mode”.

CL Bit

CL	Colors
0	65,536
1	8

SPT: When SPT = 1, liquid crystal is driven with 2 split screens. For details, see “Screen Split Drive Function”.

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REV: When REV = 1, a reverse display is shown. Inverting the grayscale levels allows the display of same data on both normally white and normally black panels. The source output level is as follows.

Combination with partial display

REV	GRAM data	Source output level							
		Display area		non-display area					
				PT1-0 = (0.*)		PT1-0 = (1.0)		PT1-0 = (1.1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	16'h0000	V31	V0	V31	V0	GND	GND	Hi-z	Hi-z
	16'hFFFF	V0	V31						
1	16'h0000	V0	V31	V31	V0	GND	GND	Hi-z	Hi-z
	16'hFFFF	V31	V0						

Combination with D1-0 bits

REV	GRAM data	Source output level							
		D1-0 = (1.1)		D1-0 = (1.0)		D1-0 = (0.1)		D1-0 = (0.0)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	16'h0000	V31	V0	V31	V0	GND	GND	GND	GND
	16'hFFFF	V0	V31						
1	16'h0000	V0	V31	V31	V0	GND	GND	GND	GND
	16'hFFFF	V31	V0						

GON: When GON = 0, the gate-off level is VGH.

D1-0: The graphics display is on when D1 = 1, and off when D1 = 0. When setting D1 = 0, the data are retained in GRAM. This means the graphics is instantly redisplayed when setting D1 to 1. When D1 is 0 (i.e., the display is off) all the source outputs are set to the GND level. This reduces the charged/discharged current during liquid crystal AC drive.

When D1-0 = 01, the HD66773R continues internal display operation, even while the external display is off. When D1-0 = 00, both internal and external display operation are halted.

In combination with GON and DTE bits, D1-0 bits control ON/OFF of display. For details, see "Instruction Setting Flow".

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GON	DTE	D1	D0	HD66773R Internal Display Operation	Source output	Gate output
0	0	0	0	Halt	GND	VGH
0	0	0	1	Operate	GND	VGH
1	0	0	1	Operate	GND	VGOFF
1	0	1	1	Operate	Grayscale level output	VGOFF
1	1	1	1	Operate	Grayscale level output	Gate selective line: VGH, Gate non-selective line: VGOFF

Note 1) GRAM write operation from the microcomputer is irrelevant to the setting in D1–0.

Note 2) In the standby mode, D1–0 = “00”. The setting in the register D1–0 is retained.

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN3-0: Set the 1H (1 raster-row) period.

RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Clock Cycles per Raster-row
0	0	0	0	16 clocks
0	0	0	1	17 clocks
0	0	1	0	18 clocks
		:	:	
1	1	1	0	30 clocks
1	1	1	1	31 clocks

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DIV1-0: Set the division ratio of clocks for internal operations (DIV1-0). Internal operations are in synchronization with the clock, the frequency of which is divided according to the DIV1-0 setting. When changing the number of drive raster-rows, adjust the frame frequency too. For details, see “Frame Frequency Adjustment Function”.

DIV1	DIV0	Division Ratio	Internal Operating Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc = R-C oscillation frequency

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times (\text{Line} + 8)} \quad [\text{Hz}]$$

fosc: R-C oscillation frequency

Line: number of drive raster-rows (NL bit)

Division ratio: DIV bit

Clock cycles per raster-row: RTN bit

EQ1-0: Set the period for equalization, where Vcom output becomes Hi-z.

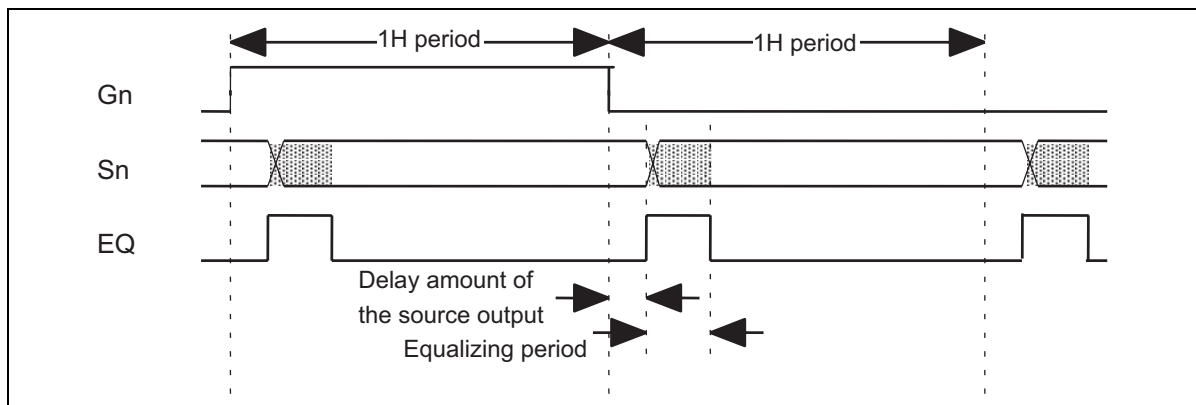
EQ1	EQ0	Equalizing period
0	0	Not equalized
0	1	1 clock
1	0	2 clocks
1	1	3 clocks

Note) Equalizing is valid while VcomL is 0V or more. Otherwise, set EQ = “00”

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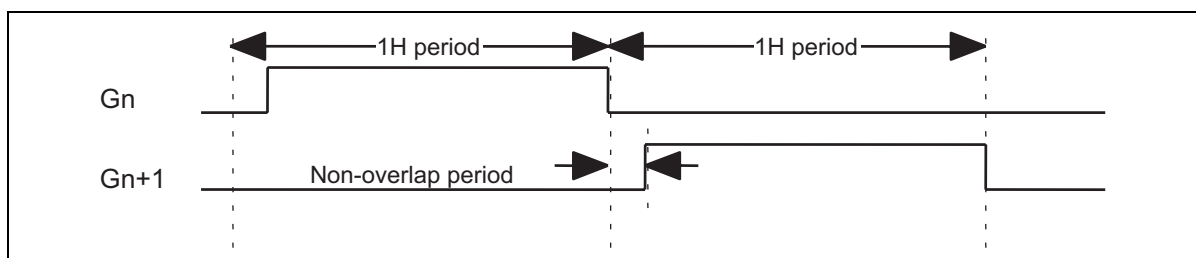
SDT1-0: Determine the amount of delay for the source output from the falling edge of the gate output.

SDT1	SDT0	Delay Time for Source Signal
0	0	1 clock
0	1	2 clocks
1	0	3 clocks
1	1	4 clocks



NO1-0: Specify the amount of non-overlap time for the gate output.

NO1	NO0	Non-overlap time
0	0	0 clock
0	1	4 clocks
1	0	6 clocks
1	1	8 clocks

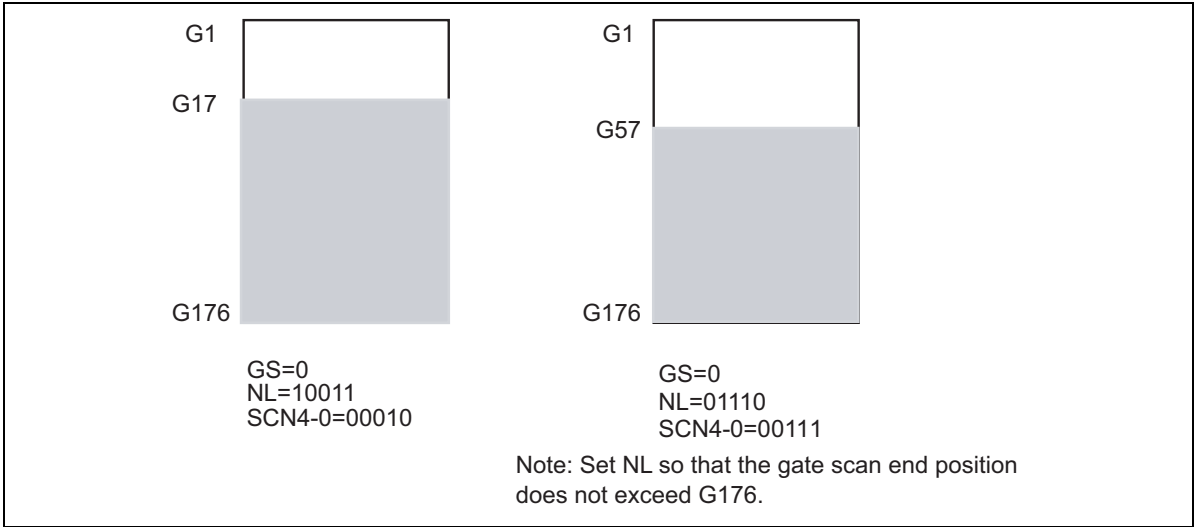


Gate Scan Position (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

SCN4-0: Specify the position where the gate scan starts.

SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position	
					GS = 0	GS = 1
0	0	0	0	0	G1	G176
0	0	0	0	1	G9	G168
0	0	0	1	0	G17	G160
.	.	.	.	.	.	.
1	0	1	0	0	G161	G17
1	0	1	0	1	G169	G9



Vertical Scroll Control (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL7–0: Specify the number of raster-rows to be scrolled and control smooth scrolling in the vertical direction. The number of raster-rows is specified between 0 to 176, the raster-rows of the specified number are scrolled during display. When the 176th raster-row is displayed, the scrolling display starts afresh from the 1st raster-row. The number of raster-rows to be scrolled (VL7–0) can be specified when the first screen vertical scroll enable bit VLE1 = 1 or the second screen vertical scroll enable bit VLE2 = 1. The number of raster-rows is fixed (not changeable) when VLE2-1 = 00.

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Amount of Scrolling (Number of raster-row)
0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	1	0	2 raster-rows
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	0	1	1	1	0	174 raster-rows
1	1	1	0	1	1	1	1	175 raster-rows

Note: When setting the number of raster-rows for scrolling, it must be 175 ("AF" h) or less.

1st-Screen Drive Position (R14h)**2nd-Screen Drive Position (R15h)**

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS17–10: Specify the start position for driving the first screen by line. The liquid crystal is driven by from the gate driver of "the set value + 1".

SE17–10: Specify the end position for driving the first screen by line. The liquid crystal is driven by to the gate driver of "the set value + 1". For instance, when SS17–10 = "07" H and SE17–10 = "10" H, the liquid crystal is driven from G8 to G17, and black display is driven from G1 to G7, and G18 thereafter. Make sure that $SS17-10 \leq SE17-10 \leq "AF" H$. For details, see "Screen-split Drive Function".

SS27–20: Specify the start position for driving the second screen by line. The liquid crystal is driven by from the gate driver of "the set value + 1". The second screen is driven when SPT = 1.

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SE27-20: Specify the end position for driving the second screen by line. The liquid crystal is driven by to the gate driver of “the set value + 1”. For instance, when SPT = 1, and SS27-20 = “20”H, SE27-20 = “4F”H, the liquid crystal is driven from 33 to G80. Make sure that SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ “AEF”H. For details, see “Screen-split Drive Function”.

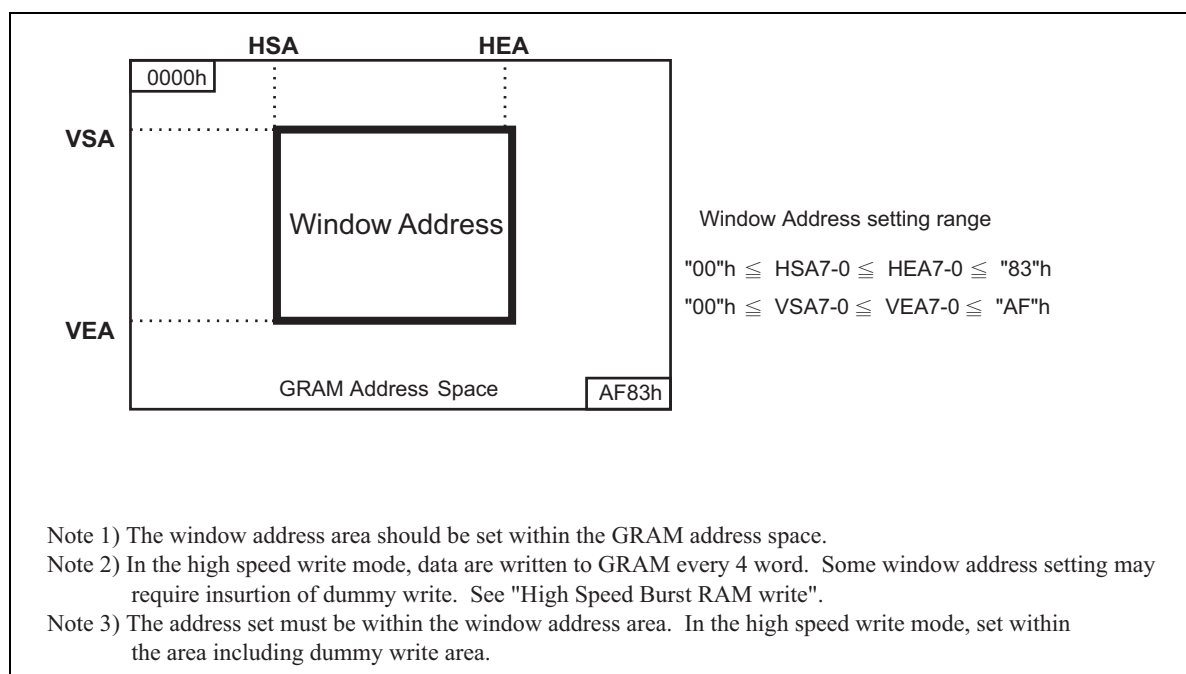
Horizontal RAM Address Position (R16h)

Vertical RAM Address Position (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA7-0/HEA7-0: Specify the start/end positions of the window-address range by address in the horizontal direction. Data are written to GRAM within the area determined by the addresses specified by HEA7-0 and HSA7-0. These addresses must be set before RAM write. In setting these bits, make sure that “00”h ≤ HSA7-0 ≤ HEA7-0 ≤ “83”h.

VSA7-0/VEA7-0: Specify the start/end positions of the window-address range by address in the vertical direction. Data are written to GRAM within the area determined by the addresses specified by VEA7-0 and VSA7-0. These addresses must be set before RAM write. In setting these bits, make sure that “00”h ≤ VSA7-0 ≤ VEA7-0 ≤ “AF”h.



RAM Write Data Mask (R20h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

WM15–0: Write-mask the data when written to GRAM by bit. The write-mask function is available with 8/16-bit interface modes. For example, if WM15 = 1, the data in WD15 bit is write-masked so that it is not written to GRAM. The rest of WM14-0 bits also write-mask the data in the corresponding WD bits when these bits are set to “1”. For details, see “Graphics Operation Function”.

RAM Address Set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0

AD15–0: Make a GRAM address initial setting in the address counter (AC). After GRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and the setting for a new GRAM address is not required in the address counter. Therefore, data are written consecutively without resetting the address. The address counter is not automatically updated when data are read out from GRAM.

GRAM address setting can not be made during the standby mode. An address set should be made within the area specified with the window address.

GRAM Address Range

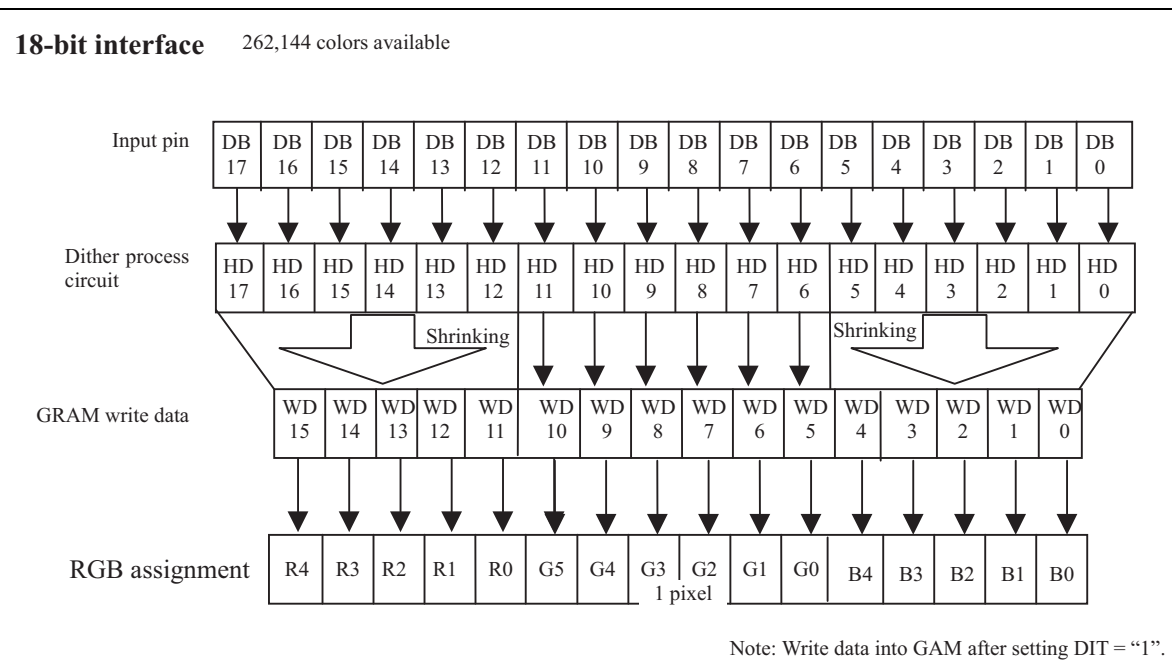
AD15–AD0	GRAM Setting
“0000”H – “0083”H	Bitmap data for G1
“0100”H – “0183”H	Bitmap data for G2
“0200”H – “0283”H	Bitmap data for G3
“0300”H – “0383”H	Bitmap data for G4
:	:
“AC00”H – “AC83”H	Bitmap data for G173
“AD00”H – “AD83”H	Bitmap data for G174
“AE00”H – “AE83”H	Bitmap data for G175
“AF00”H – “AF83”H	Bitmap data for G176

Write Data to GRAM (R22h)

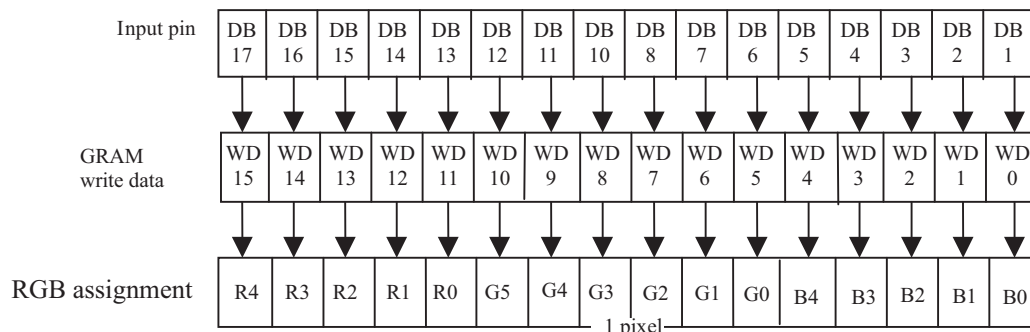
R/W	RS																		
W	1				RAM write data (WD17-0) The pin assignment for DB17-0 varies for each interface (see below).														
When RGB-I/F	PD17 PD16 PD15 PD14 PD13 PD12 PD11 PD10 PD9 PD8 PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0																		
	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0	

WD17–0: All data are expanded into 18 bits internally before being written to GRAM. Each interface has its own way of expanding data to 18 bits.

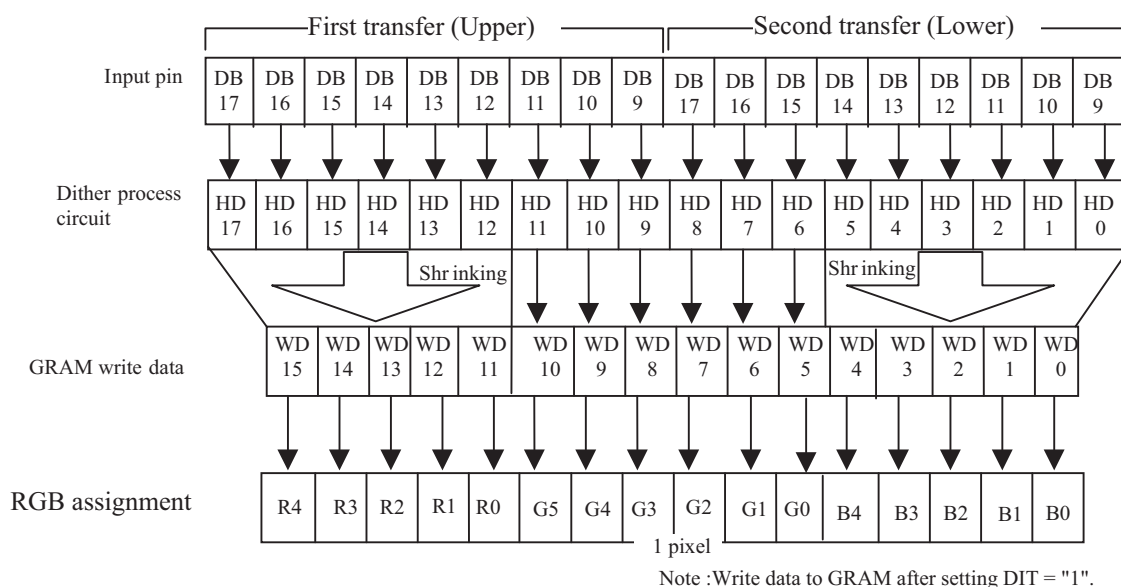
The grayscale level is selected according to GRAM data. The address is automatically updated according to the setting with the AM and I/D bits after data are written to GRAM. During the standby mode, no access is allowed to GRAM. When the 9 or 18 bit interface mode is selected, set DIT = “1” to activate the internal hardware-dither circuit before writing to GRAM.



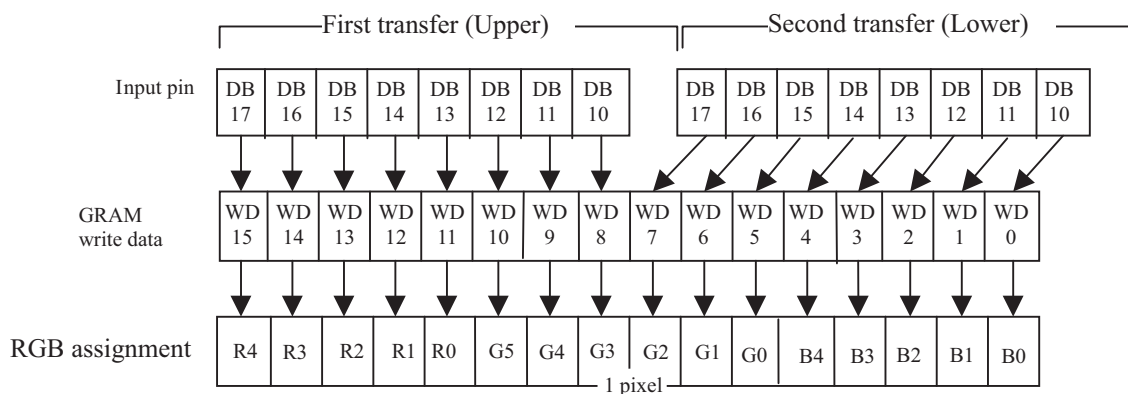
16-bit interface 65,536 Colors available



9-bit Interface 262,144 Colors available



8-bit Interface 65,536 Colors available



GRAM data and liquid crystal output level

GRAM Data Setting		Selected grayscale		GRAM Data Setting		Selected grayscale	
G	R/B	Negative	Positive	G	R/B	Negative	Positive
000000	00000	V0	V31	010000	01000	V8	V23
000001	-	V0 – V1	V31 – V30	010001	-	V8 – V9	V23 – V22
000010	00001	V1	V30	010010	01001	V9	V22
000011	-	V1 – V2	V30 – V29	010011	-	V9 – V10	V22 – V21
000100	00010	V2	V29	010100	01010	V10	V21
000101	-	V2 – V3	V29 – V28	010101	-	V10 – V11	V21 – V20
000110	00011	V3	V28	010110	01011	V11	V20
000111	-	V3 – V4	V28 – V27	010111	-	V11 – V12	V20 – V19
001000	00100	V4	V27	011000	01100	V12	V19
001001	-	V4 – V5	V27 – V26	011001	-	V12 – V13	V19 – V18
001010	00101	V5	V26	011010	01101	V13	V18
001011	-	V5 – V6	V26 – V25	011011	-	V13 – V14	V18 – V17
001100	00110	V6	V25	011100	01110	V14	V17
001101	-	V6 – V7	V25 – V24	011101	-	V14 – V15	V17 – V16
001110	00111	V7	V24	011110	01111	V15	V16
001111	-	V7 – V8	V24 – V23	011111	-	V15 – V16	V16 – V15

GRAM Data Setting		Selected grayscale		GRAM Data Setting		Selected grayscale	
G	R/B	Negative	Positive	G	R/B	Negative	Positive
100000	10000	V16	V15	110000	11000	V24	V7
100001	-	V16 – V17	V15 – V14	110001	-	V24 – V25	V7 – V6
100010	10001	V17	V14	110010	11001	V25	V6
100011	-	V17 – V18	V14 – V13	110011	-	V25 – V26	V6 – V5
100100	10010	V18	V13	110100	11010	V26	V5
100101	-	V18 – V19	V13 – V12	110101	-	V26 – V27	V5 – V4
100110	10011	V19	V12	110110	11011	V27	V4
100111	-	V19 – V20	V12 – V11	110111	-	V27 – V28	V4 – V3
101000	10100	V20	V11	111000	11100	V28	V3
101001	-	V20 – V21	V11 – V10	111001	-	V28 – V29	V3 – V2
101010	10101	V21	V10	111010	11101	V29	V2
101011	-	V21 – V22	V10 – V9	111011	-	V29 – V30	V2 – V1
101100	10110	V22	V9	111100	11110	V30	V1
101101	-	V22 – V23	V9 – V8	111101	-	V30 – V31	V1 – V0
101110	10111	V23	V8	111110	11111	V31	V0
101111	-	V23 – V24	V8 – V7	111111	-	V31	V0

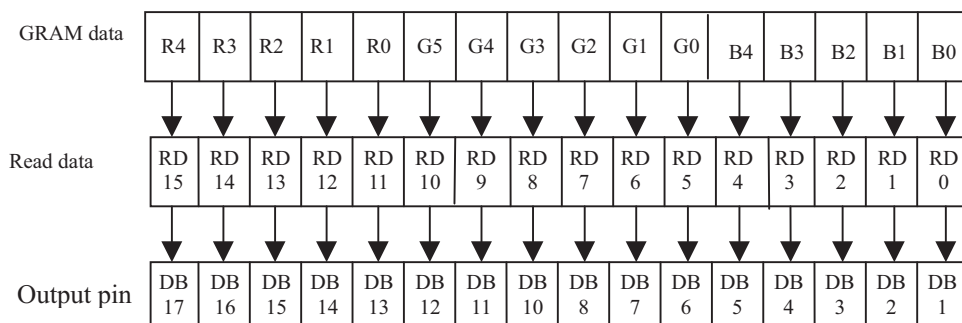
Read Data from GRAM (R22h)

R/W	RS	RAM Read data (RD17-0) The pin assignment for DB17-0 varies for each interface (see below).															
R	1																

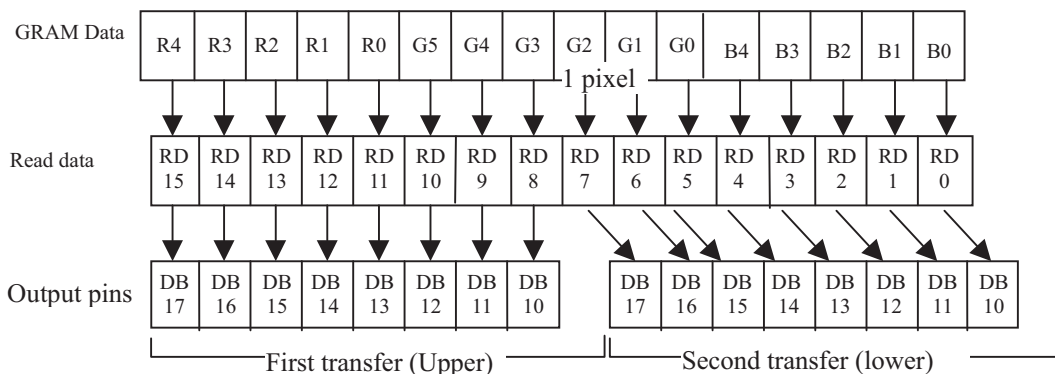
RD15-0: Read 16-bit data from GRAM. The bit assignment for the data to be read out from GRAM is different according to the interface.

When data are read out from GRAM to the microcomputer, the first word read immediately after GRAM address set are latched in the internal read-data latch, and the data in the data bus (DB17-0) are nullified. The second word is read as a valid data. When the HD66773R performs an internal bit processing, such as logical operation, it uses the data latched in the read-data latch, and completes it by single read out operation. The data are expanded internally into 18 bits before going through the logical operation. GRAM data read and logical operation are available with 8-/16-bit interface mode. If 9-/18-bit interface modes are selected, this function is not available.

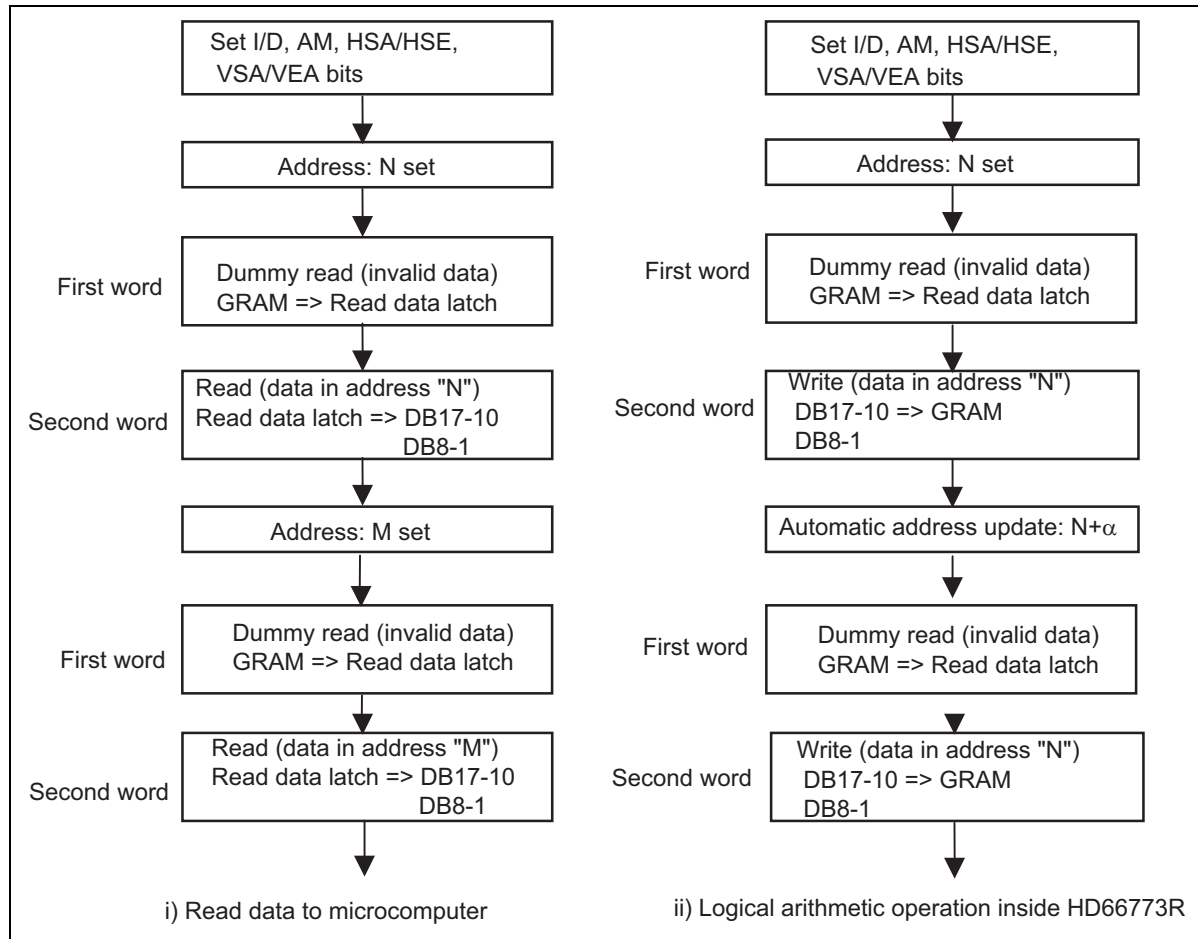
16-bit interface



8-bit interface / Interface SPI



GRAM read sequence



Gamma Control (R30h to R3Bh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31	W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32	W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33	W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34	W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35	W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36	W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37	W	1	0	0	0	0	0	PRN 42	PRN 41	PRN 40	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3A	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3B	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

PKP52-00: Gamma fine adjustment register for the positive polarity output

PRP12-00: Gradient adjustment register for the positive polarity output

VRP14-00: Amplitude adjustment register for the positive polarity output

PKN52-00: Gamma fine adjustment register for the negative polarity output

PRN12-00: Gradient adjustment register for the negative polarity output

VRN14-00: Amplitude adjustment register for the negative polarity output.

For details, see “Gamma Adjustment Function”.

Note1) "*" is "Don'tcare".
Note2) High-speed write mode is available only with RAM write.

Reset Function

The HD66773R makes internal initial settings with RESET input. During the RESET, the HD66773R is in a busy state, and no instructions from the MPU and access to GRAM are accepted. The time required for the RESET input is at least 1ms. In case of power-on reset, wait at least 10ms after the power is turned on until the R-C oscillation frequency becomes stabilized. While waiting, do not make initial settings for the instruction set, nor access to GRAM.

Initial State of Instructions

- a. Start oscillation
- b. Driver output control (NL4-0 = "10101", SS = "0", CS = "0")
- c. Liquid crystal AC drive control (FLD1-0 = "01", B/C = "0", EOR = "0", NW5-0 = "00000")
- d. Power control 1 (BT2-0 = "000", DC2-0 = "000", AP2-0 = "000": liquid crystal power supply off, SLP = "0", STB = "0" : Standby mode off)
- e. Power control 2 (CAD = "0")
- f. Entry mode set (DIT = "0", BGR = "0", HWM = "0", I/D1-0 = "11": Increment by 1, AM = "0": Horizontal direction, LG2-0 = "000": Replace mode)
- g. Compare register (CP15-0 : "0000 0000 0000 0000")
- h. Display control (PT1-0 = "00", VLE2-1 = "00": No vertical scroll, SPT = "0", GON = "0", DTE = "0", CL = "0": 262,144 colors, REV = "0", D1-0 = "00": Display OFF)
- i. Power control 3 (VC2-0 = "000")
- j. Power control 4 (VRL3-0 = "0000", PON = "0", VRH3-0 = "0000")
- k. Power control 5 (VDV4-0 = "00000", VCOMG = "0", VCM4-0 = "00000")
- l. Frame cycle control (NO1-0 = "00", SDT1-0 = "00", EQ1-0 = "00" : No equalization, DIV1-0 = "00": clock/1, RTN3-0 = "0000" : 16 clocks in 1H period)
- m. Gate scan starting position (SCN4-0 = "00000")
- n. Vertical scroll (VL7-0 = "00000000")
- o. 1st split-screen (SE17-10 = "11111111", SS17-10 = "00000000")
- p. 2nd split-screen (SE27-20 = "11111111", SS27-20 = "00000000")
- q. Horizontal RAM address position (HEA7-0 = "10000011", HSA7-0 = "00000000")
- r. Vertical RAM address position (VEA7-0 = "10101111", VSA7-0 = "00000000")
- s. RAM write data mask (WM15-0 = "0000"H: No mask)
- t. RAM address set (AD15-0 = "0000"H)
- u. γ control
(PKP02-00 = "000", PKP12-10 = "000", PKP22-20 = "000", PKP32-30 = "000",
PKP42-40 = "000", PKP52-50 = "000", PRP02-00 = "000", PRP12-10 = "000")
(PKN02-00 = "000", PKN12-10 = "000", PKN22-20 = "000", PKN32-30 = "000",
PKN42-40 = "000", PKN52-50 = "000", PRN02-00 = "000", PRN12-10 = "000")
(VRP14-10 = "00000", VRP03-00 = "0000", VRN14-10 = "00000", VRN12-10 = "000")

GRAM Data Initialization

The data in GRAM are not initialized with the RESET input. Initialize through software during the display OFF (D1-0 = "00").

Initial state of output pin

- a. Liquid crystal driver output pins (source outputs): Output GND level
Liquid crystal driver output pins (gate outputs): Output VGH level
- b. Oscillator output pin (OSC2): Output oscillation signal

System Interface

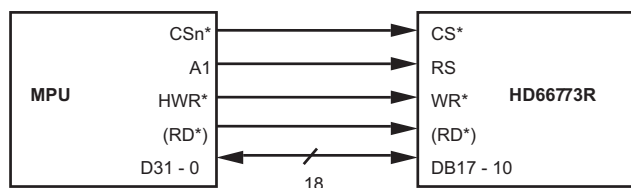
A system interface is selected among the following interfaces with the IM3-0 pin setting. The system interface enables instruction setting and RAM access.

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin
0	0	0	0	68-system 16-bit interface	DB17 to 10, 8-to-1
0	0	0	1	68-system 8-bit interface	DB17 to 10
0	0	1	0	80-system 16-bit interface	DB17 to 10, 8-to-1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*	Serial Peripheral Interface (SPI)	DB1 to 0
0	1	1	*	Setting inhibited	—
1	0	0	0	68-system 18-bit interface	DB17-0
1	0	0	1	68-system 9-bit interface	DB17-9
1	0	1	0	80-system 18-bit interface	DB17-0
1	0	1	1	80-system 9-bit interface	DB17-9
1	1	*	*	Setting inhibited	—

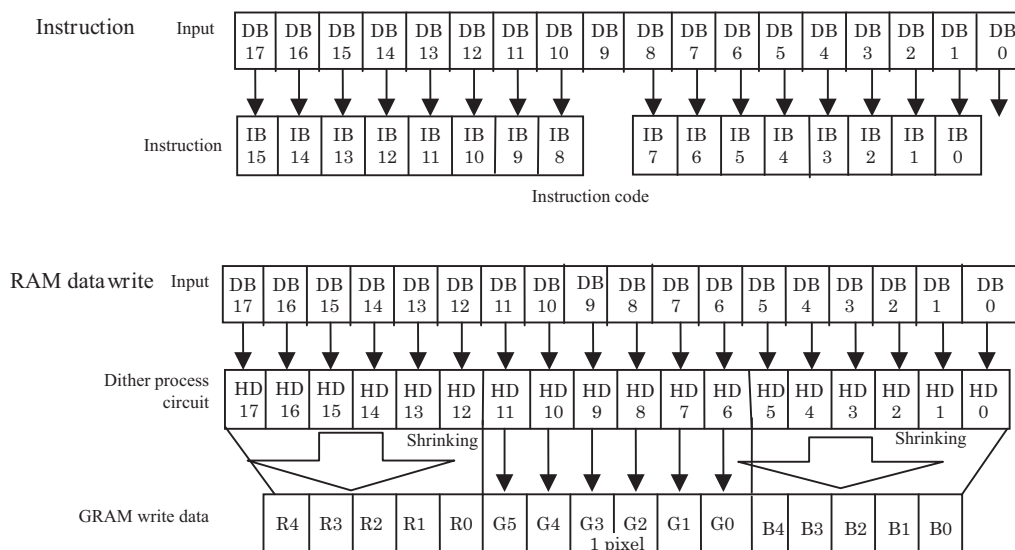
18-bit interface

68-system 18-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to Vcc/GND/GND/GND levels respectively. 80-system 18-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to Vcc/GND/Vcc/GND levels respectively. The data transfer through 18-bit mode is effective only for write mode, and not effective for read operation.

18-bit bus interface



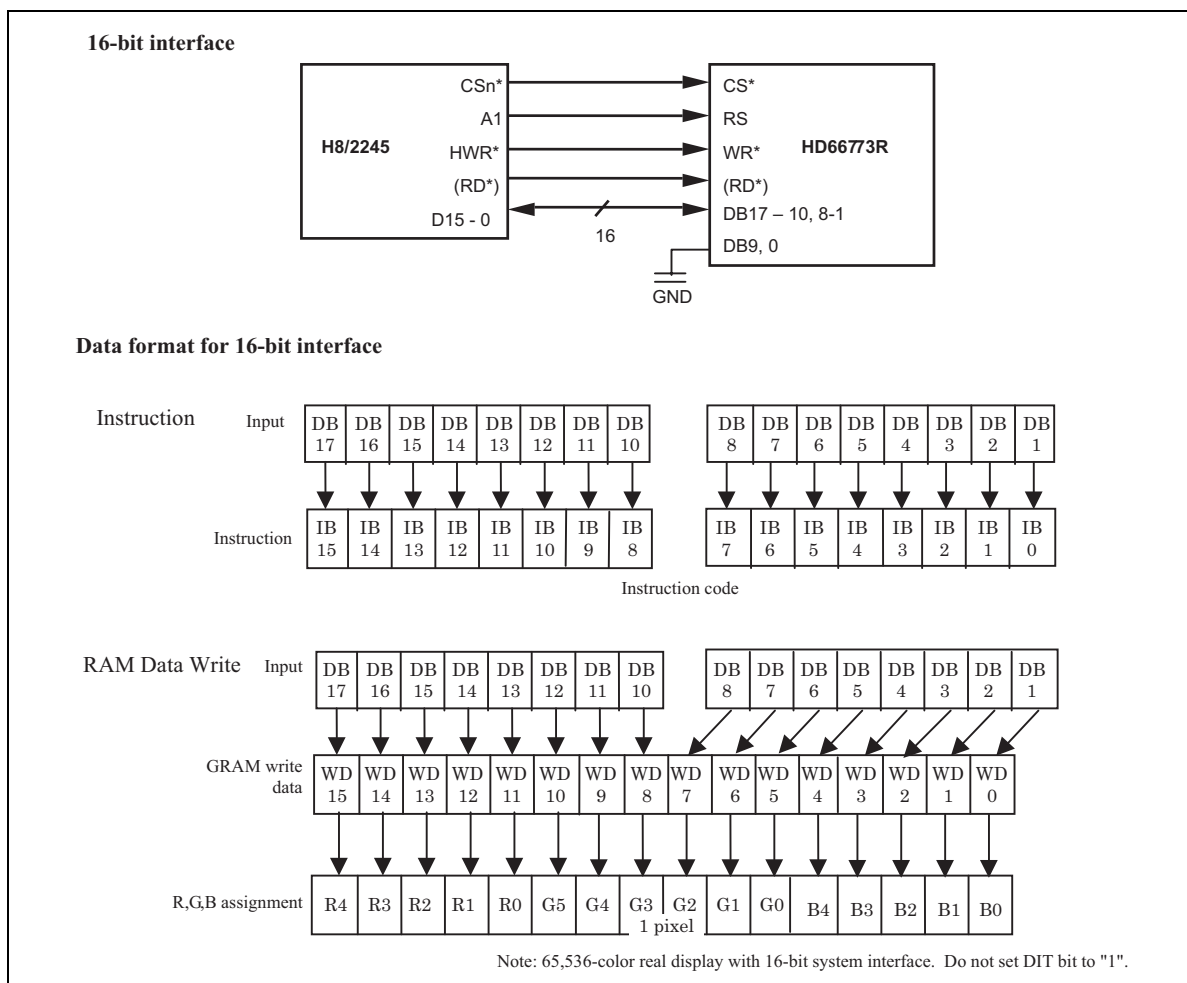
Data format for 18-bit bus interface



Note: 262,144 colocs available with 18-bit system interface by setting DIT bit to "1".

16-bit interface

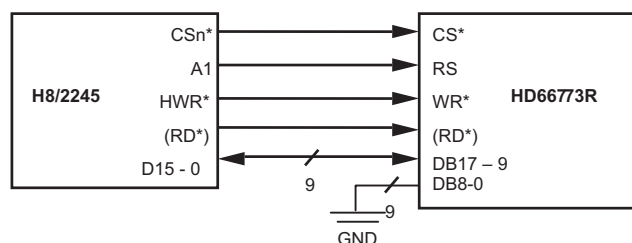
68-system 16-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to GND/GND/GND/GND levels respectively. 80-system 16-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to GND/GND/Vcc/GND levels respectively.



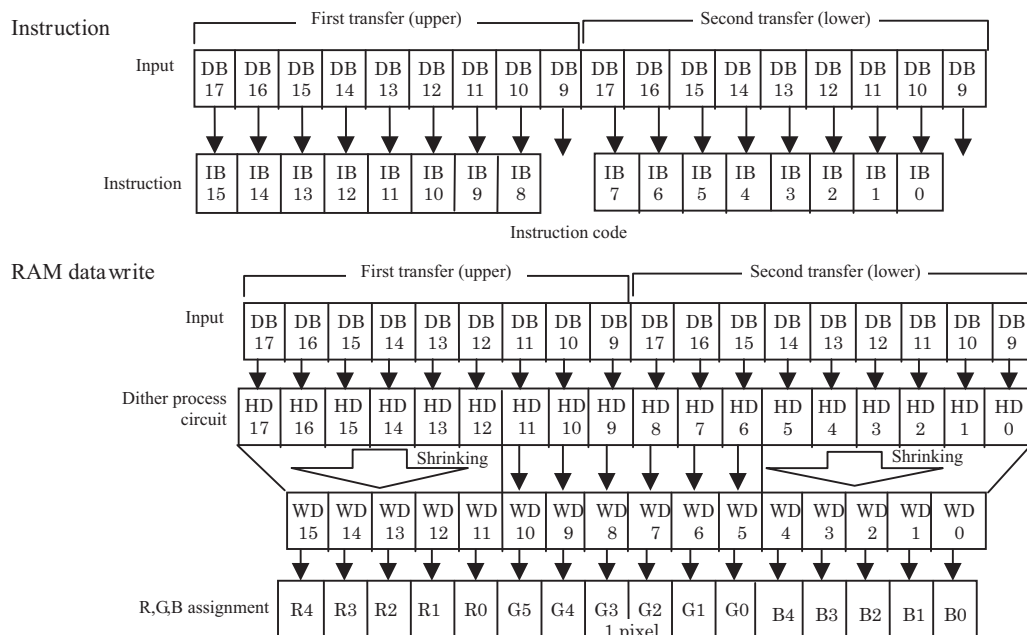
9-bit interface

68-system 9-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to Vcc/GND/GND/Vcc levels respectively through DB17-9 pins. 80-system 9-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to Vcc/GND/Vcc/Vcc levels respectively through DB17-9 pins. The 16-bit instruction is divided into 2 8-bit data and upper 8-bit data is transferred first. The LSB is not used for each upper/lower-bit data transfer. The 18-bit RAM data is also divided into 2 9-bit data and upper 9-bit data is transferred first. The unused pins DB8-0 must be fixed to either "Vcc" or "GND". The upper-byte write is also required when writing index registers. The data transfer through 9-bit mode is effective only for write mode, and not effective for read operation.

9-bit bus interface



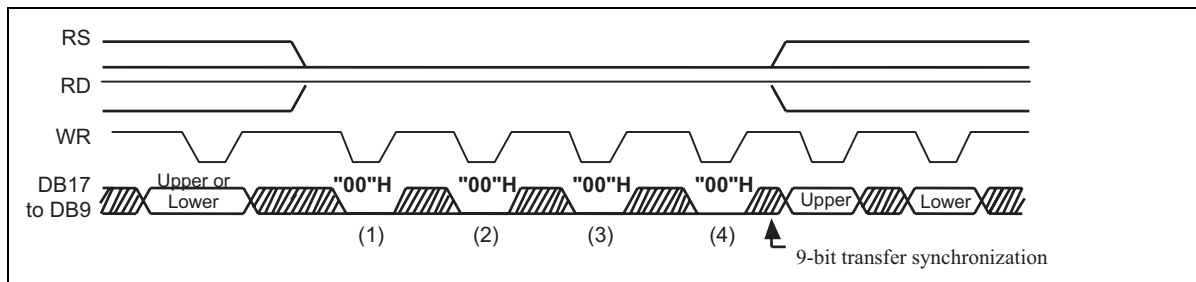
Data format for 9-bit bus interface



Note: 262,144 colocs available with 9-bit system interface by setting DIT bit to "1".

Data transmission synchronization in 9-bit bus interface mode

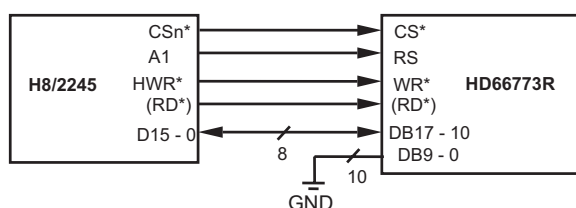
The HD66773R supports the data transmission synchronizing function, which resets the upper/lower counter that counts the number of transmission of upper/lower 9-bit data in the 9-bit bus interface mode. When a discrepancy occurs in the transmission of upper/lower 9-bit data due to effects from noise and so on, the "00" H instruction is written 4 times consecutively to forcibly reset the upper/lower counter so that data transmission restarts with an upper 9-bit transmission. Periodical execution of the synchronization allows the system recovery from the excursion.



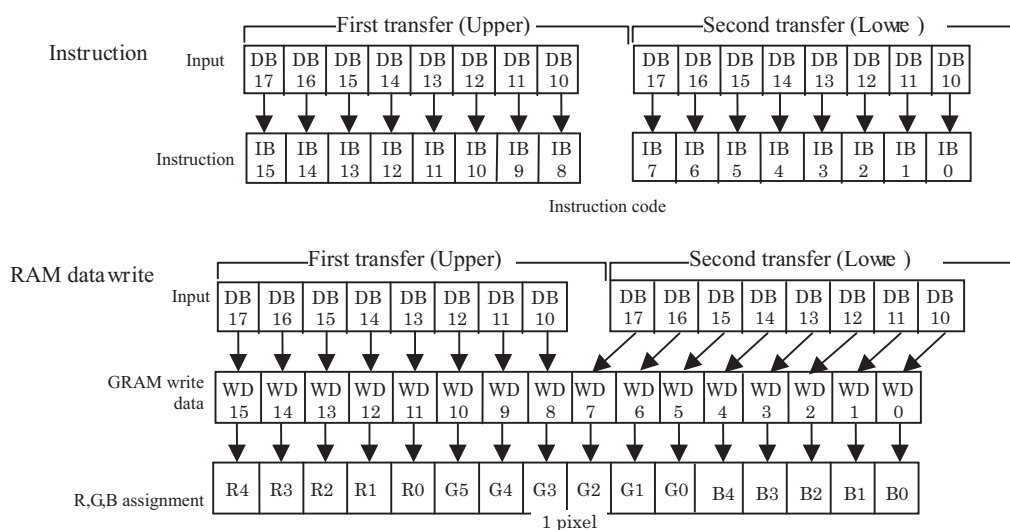
8-bit interface

68-system 8-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to GND/GND/GND/Vcc levels respectively through DB17-10 pins. 80-system 8-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to GND/GND/Vcc/Vcc levels respectively through DB17-10 pins. The 16-bit instruction is divided into 2 8-bit data and upper 8-bit data is transferred first. The LSB is not used for each upper/lower-bit data transfer. The 16-bit RAM data is also divided into 2 8-bit data and upper 9-bit data is transferred first. The unused pins DB9-0 must be fixed to either "Vcc" or "GND". The upper-byte write is also required when writing index registers.

8-bit bus interface



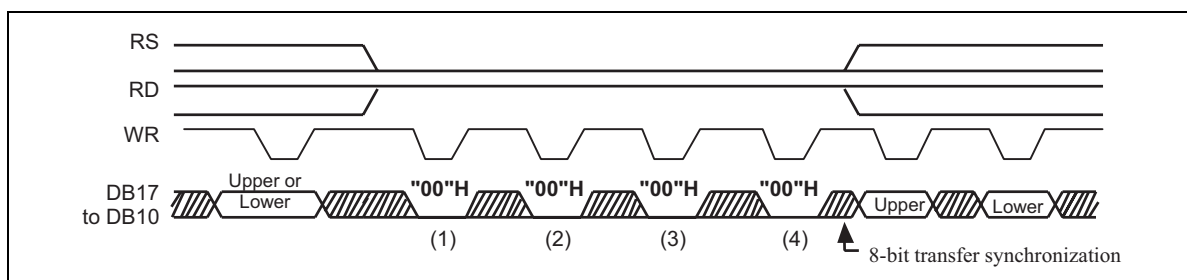
Data format for 8-bit bus interface



Note: 65,536-color real display with 8-bit system interface. Do not set DIT bit to "1".

Data transmission synchronization in 8-bit bus interface mode

The HD66773R supports the data transmission synchronizing function, which resets the upper/lower counter that counts the number of transmission of upper/lower 8-bit data in the 8-bit bus interface mode. When a discrepancy occurs in the transmission of upper/lower 8-bit data due to effects from noise and so on, the "00" H instruction is written 4 times consecutively to forcibly reset the upper/lower counter so that data transmission restarts with an upper 8-bit transmission. Periodical execution of the synchronization allows the system recovery from the excursion.



Serial Peripheral interface (SPI)

The Serial Peripheral Interface (SPI) becomes operable by setting IM3/2/1 pins to GND/Vcc/GND levels respectively. The SPI is available through the chip select line (CS*), serial transfer clock line (SCL), serial data input (SDI), and serial data output (SDO). In the SPI mode, the IM0/ID pin functions as ID pin. In the SPI mode, the unused DB15-2 pins must be fixed at either Vcc or GND level.

The HD66773R recognizes the start of data transfer at the falling edge of CS* input to initiate the transfer of a start byte. It recognizes the end of data transfer at the rising edge of CS* input. The HD66773R is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the HD66773R are compared and the both 6-bit data correspond. When selected, the HD66773R starts taking in the subsequent data string. The setting for the least significant bit of the identification code is made with the ID pin. The five upper bits of the identification code must be 01110. Two different chip addresses must be assigned to the HD66789 because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When RS = 1, instruction write or RAM read/write is executed. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

In the SPI mode, the data are written to GRAM after the two-byte data transmission. The data are expanded into 18 bits by adding one bit (the same data as the MSB of RB) next to the LSB of RB data.

After receiving the start byte, the HD66773R starts data transmission/reception by byte. The data transmission adopts the format which the MSB is first transmitted. All HD66773R instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (DB15 to 0). The data to be written to RAM are expanded into 18-bit data. After the start byte is received, the upper eight bits of the instruction are always fetched as the first byte, and the lower eight bits of the instruction are always fetched as the second byte. The 4-byte data that are read from RAM right after the start byte are made invalid. The HD66773R reads as valid data from the 5th-byte data.

Start Byte Format

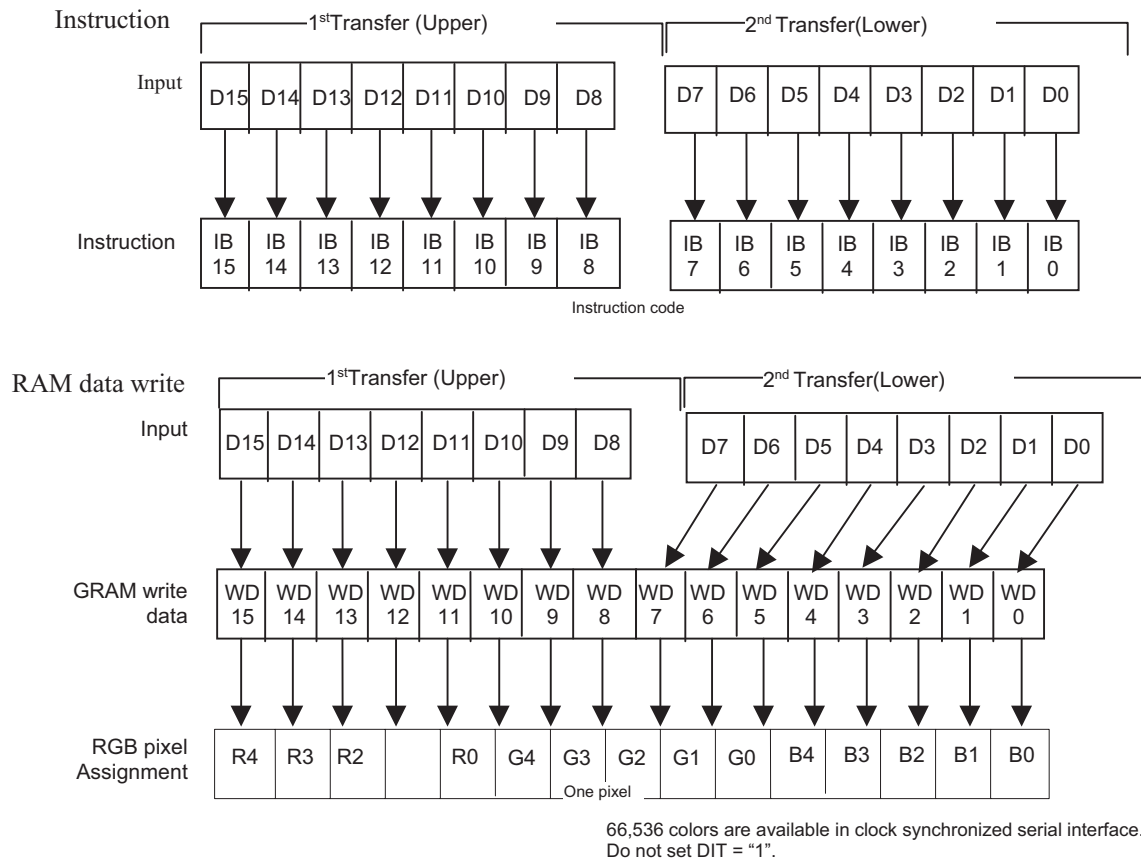
Transmitted bits	S	1	2	3	4	5	6	7	8
Start byte format	Transmission start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected with the IM0/ID pin.

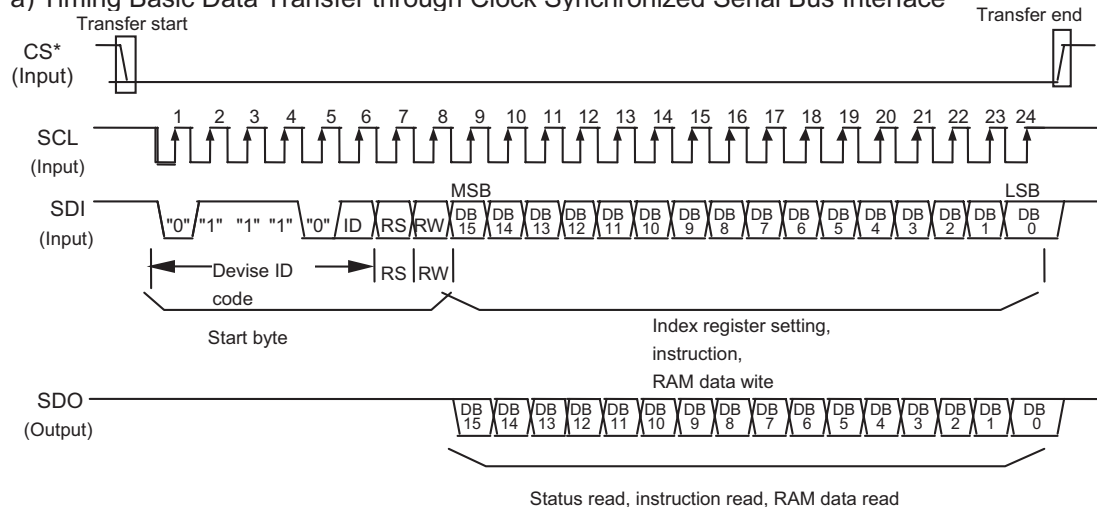
RS and R/W Bit Function

RS	R/W	Function
0	0	Set index register
0	1	Read status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

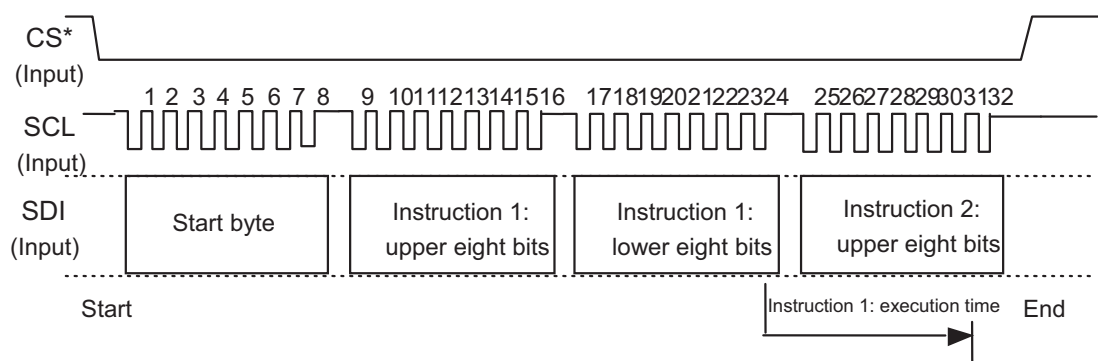
Data format for Serial Peripheral Interface



a) Timing Basic Data Transfer through Clock Synchronized Serial Bus Interface

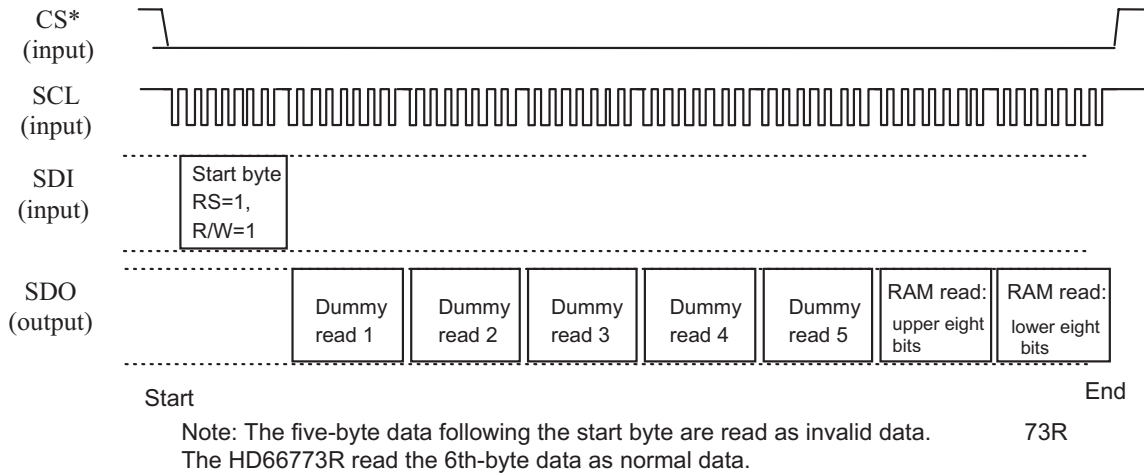


b) Timing of Consecutive Data-Transfer through Clock-synchronized serial Bus Interface

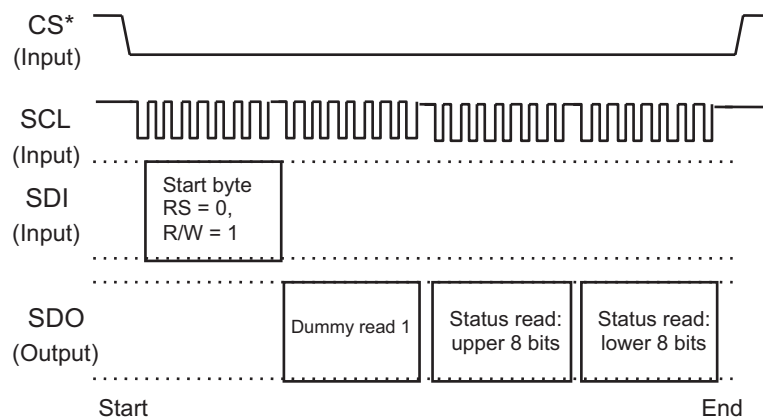


Note: The first byte after the start byte is always the upper eight bits.

c) RAM-Data Read-Transfer Timing



d) Status Read / Instruction Read



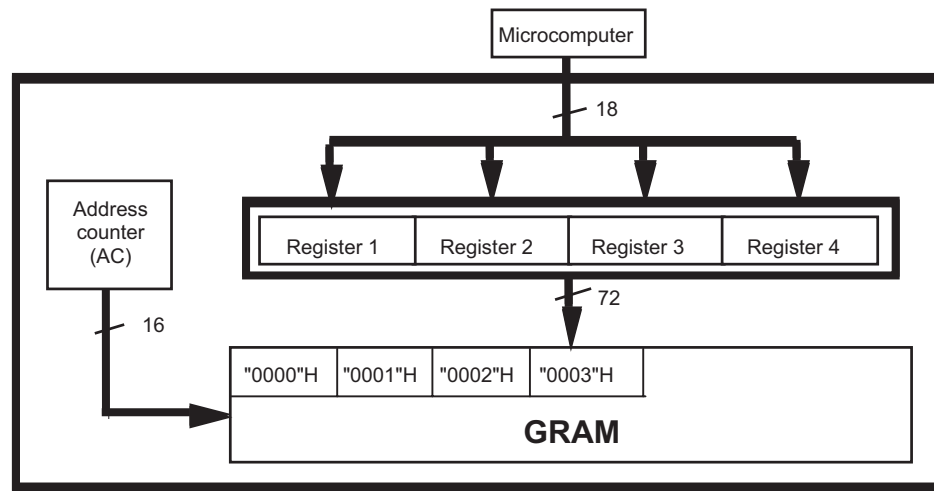
Note: The one-byte data read after the start byte is invalid.
The HD6677R starts to read the second-byte data as normal data.

High-Speed Burst RAM Write Function

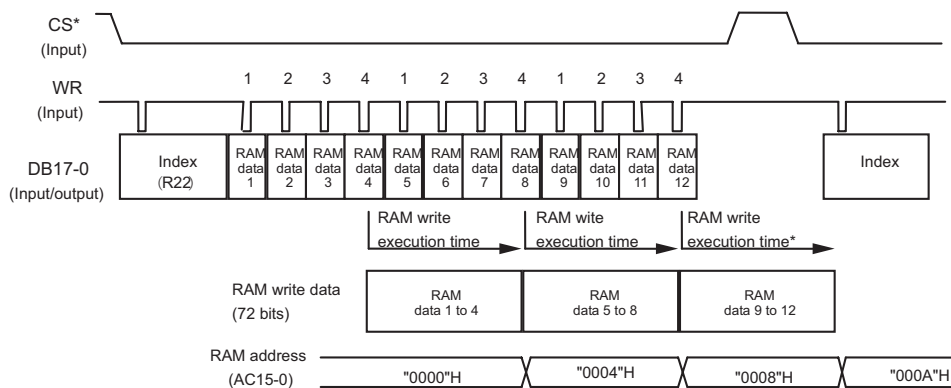
The HD66773R incorporates the high-speed burst RAM-write function, which writes data to RAM in one-fourth the access time required for the standard RAM-write operation. This function is especially useful for applications which require the high-speed rewrite of the display data such as display of colored moving picture and so on.

In high-speed RAM write mode (HWM), data to be written to RAM is temporarily stored to the internal register of HD66773R. The data storage in the register is executed by word. When the data storage operation is executed 4 times, all the data stored in the register is written to RAM at once. While the data is being written from the register to RAM, another set of data is being written to the register. This function enables high-speed and consecutive RAM write, which is required in displaying moving pictures and so on.

a) Operational flow of high-speed consecutive RAM write



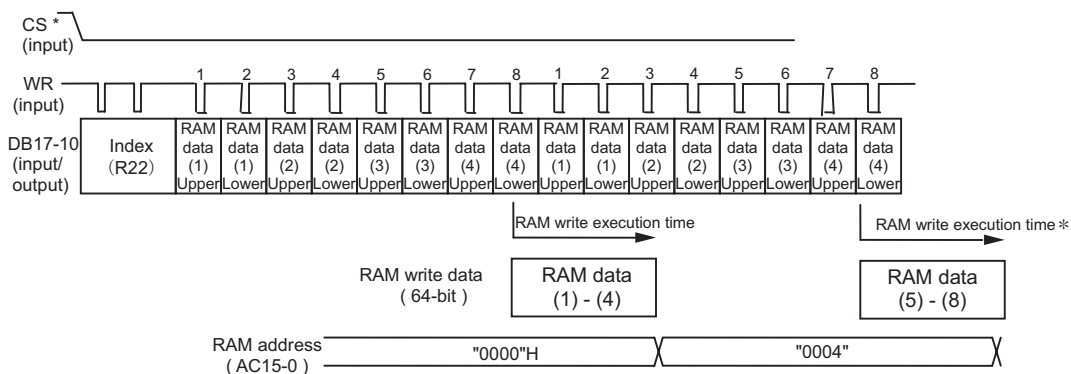
b) Example of high-speed consecutive RAM write



* Set the lower two bits of the address as follows in the high-speed write mode.
When ID0 = "0", the lower two bits of the address must be set to "11".
When ID1 = "0", the lower two bits of the address must be set to "00".

Note: When terminating high-speed RAM write, wait until RAM write execution is completed (tCYC: bus cycle time) for normal RAM write before executing a next instruction.

c) Example of high-speed consecutive RAM write



* Set the lower two bits of the address as follows in the high-speed write mode.
When ID0 = "0", the lower two bits of the address must be set to "11".
When ID1 = "0", the lower two bits of the address must be set to "00".

Note: The high-speed burst RAM write function writes data to RAM every 4 words. This means in the 8-bit interface mode, RAM write is executed every 8 write operations to the internal register.

Conditions on using high-speed RAM write mode

1. The logical/compare operations are not available.
2. RAM write operation is executed every four words. Set the lower 2 bits of the addresses as follows when setting addresses.

 *When ID0=0, the lower two bits in the address must be set to 11 before RAM write.
 *When ID0=1, the lower two bits in the address must be set to 00 before RAM write.
3. RAM write operation is executed every four words. If RAM write operation is terminated before all four-word data is written to RAM, the last data will not be written to RAM.
4. When the index register is set to R22H (RAM data write), the first RAM write operation is always executed. In this case, the RAM data read is not operable simultaneously. During RAM read, set the HWM to 0.
5. The high-speed RAM write mode is not compatible with the normal RAM write mode. When the mode must be switched to the other, make a new address setting before starting RAM write.
6. When writing data in high speed RAM write mode within the range specified with the window address, some window-address range may require dummy write operation. See "High-Speed RAM Write with Window Address Function".

Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	High-Speed RAM Write (HWM=1)
Logical operation	Available in 8-/16-bit interface	Not available
Compare operation	Available in 8-/16-bit interface	Not available
BGR function	Available	Available
Write mask function	Available in 8-/16-bit interface	Available
RAM address set	Specified by one word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Read by one word	Not available
RAM write	Write by one word	Some window-address range may require insertion of dummy write
Window address	Set by one word	Horizontal range(HSA/HSE): 4 word or more Number of horizontal writing : 4N (N>=2)
AM Setting	AM = 1/0	AM = 0

High-Speed RAM Write with Window Address

To rewrite the data in an arbitrary rectangular area of RAM consecutively in high speed, the number of RAM access should be made 4 multiple times. Accordingly some window-address range may require dummy write operation to make the RAM access 4 multiple times.

The horizontal window-address range specifying bits (HSA1-0, HEA1-0) specify the number of dummy write operations executed at the start and end of the data to be written to RAM. The total RAM access must be 4 multiple times per line.

Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2 times
1	1	3 times

Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

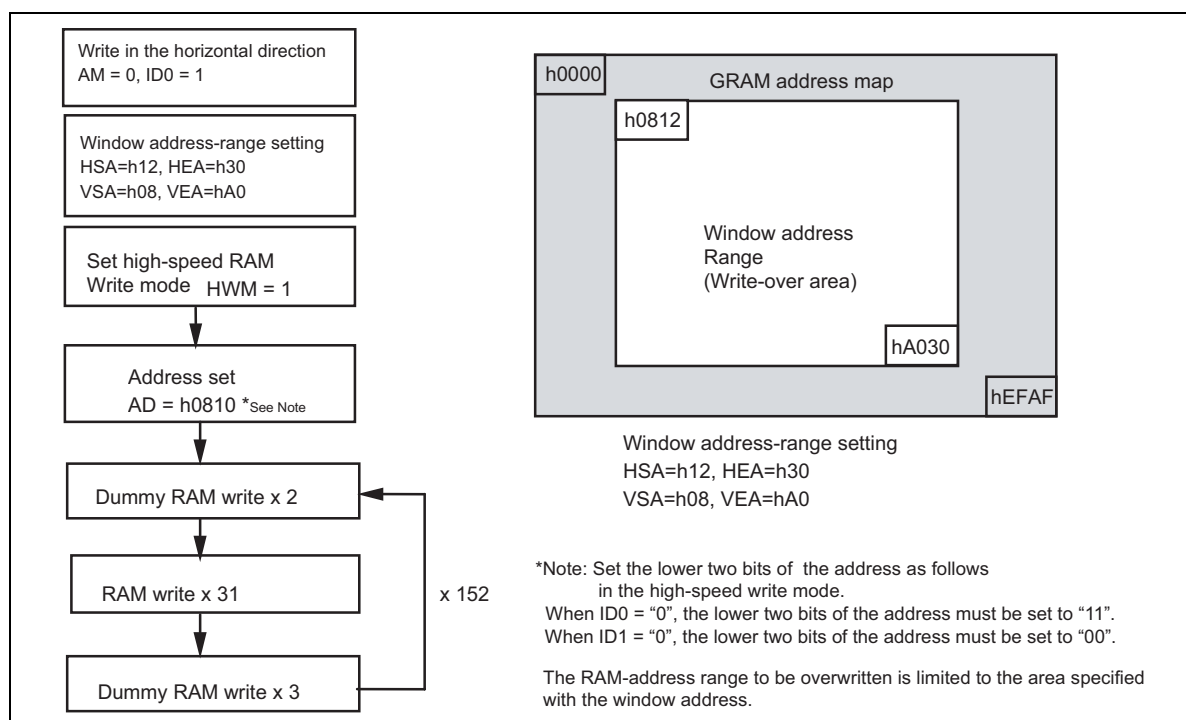
HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3 times
0	1	2 times
1	0	1 time
1	1	0

The number of RAM access when writing data in the horizontal direction must be made $4 \times N$ times by including the dummy writes.

Horizontal RAM write = start dummy write + write data + end dummy write = $4 \times N$ (times)

An example of RAM write in high speed RAM write mode with the window address is as follows.

The RAM data in the specified window-address range is written over consecutively in high speed by inserting two dummy writes at the start of the line and three dummy writes at the end of the line.



Window Address Function

The window address function enables consecutive data write within the rectangular window-address area on the on-chip GRAM, which is specified with horizontal address registers (start: HSA7-0, end: HEA 7-0) and vertical address registers (start: VSA7-0, end: VEA7-0).

The address transition direction is determined with AM bits (either increment or decrement). Accordingly, the data, including picture data, are written consecutively without taking the data wrap position into consideration.

The window-address range must be specified within the GRAM address area. An address set must be set within the window-address range.

[The condition of setting window-address range]

(Horizontal direction) "00"H ≤ HSA7-0 ≤ HSE7-0 ≤ "83"H

(Vertical direction) "00"H ≤ VSA7-0 ≤ VEA7-0 ≤ "AF"H

[The condition of making an address set within the window-address range]

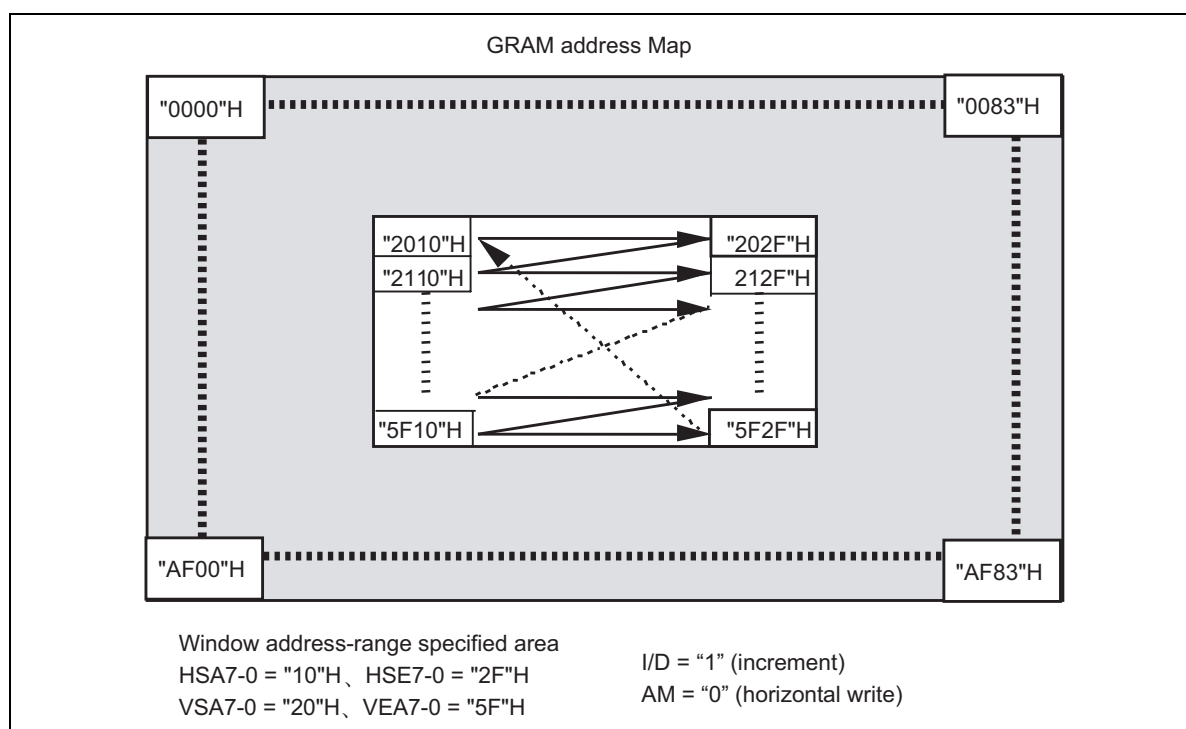
(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0

VSA7-0 ≤ AD15-8 ≤ VEA7-0

Note: In high-speed RAM write mode, the lower two bits of the address must be set as follows.

ID0=0: The lower two bits of the address must be set to 11.

ID0=1: The lower two bits of the address must be set to 00.



Graphics Operation Function

The HD66773R significantly reduces the load on the graphics-processing software in the microcomputer. The graphics operation includes:

1. The write data mask function that selectively rewrites some of the 16-bit write data.
2. Logical rewrite function to rewrite data after performing logical operation on the data from the microcomputer and graphics RAM base data.
3. The conditional rewrite function that compares the write data and the compare bit data and writes the data sent from the microcomputer only when the conditions are satisfied.

The graphics bit operation is controlled by the setting of bits in the entry mode register and RAM-write-data mask register, and the write operation from the microcomputer.

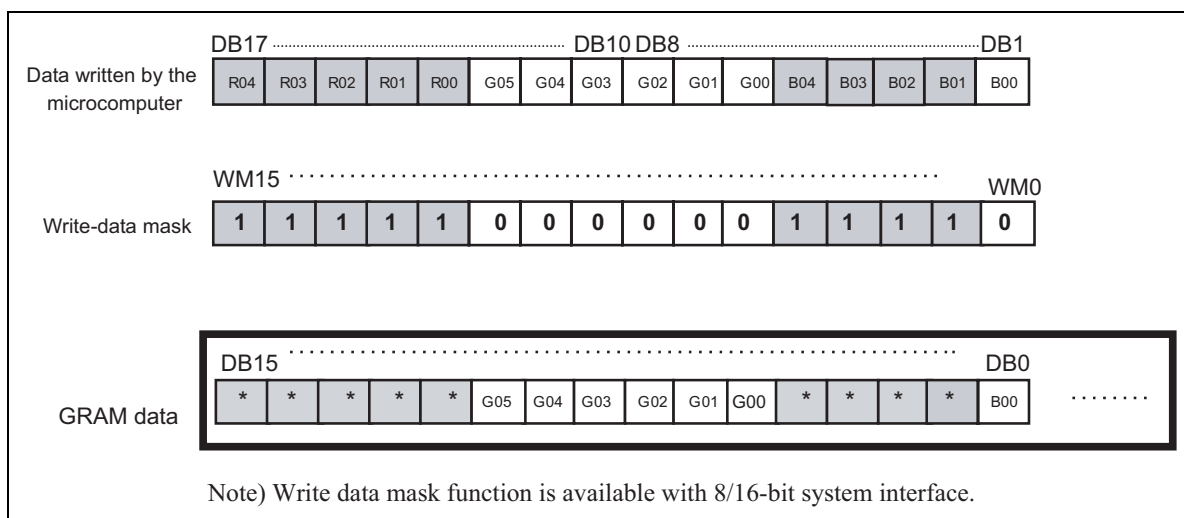
Graphics Operation

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG2-0	
Write mode 1	0/1	0	000	Horizontal data replacement, Draw a horizontal line
Write mode 2	0/1	1	000	Vertical data replacement, Draw a vertical line
Write mode 3	0/1	0	110 111	Horizontal conditional data replacement, Draw a horizontal line
Write mode 4	0/1	1	110 111	Vertical conditional data replacement Draw a vertical line
Read/Write mode 1	0/1	0	001 010 011	Horizontal logical write, Draw a horizontal line
Read/Write mode 2	0/1	1	001 010 011	Vertical logical write, Draw a vertical line
Read/Write mode 3	0/1	0	100 101	Horizontal conditional data replacement, Draw a horizontal line
Read/Write mode 4	0/1	1	100 101	Vertical conditional data replacement Draw a vertical line

Note) In 18-/9-bit interface modes, only write modes 1, 2 are effective. All operations are effective in 16-/8-bit interface modes.

Write-data Mask Function

The HD66773R supports write data mask function, which controls GRAM data write by bit when 16-bit data from the microcomputer is being written to GRAM. The write data mask function write data in the bits whose corresponding bits in the write data mask register (WM15–0) are assigned with “0”. It does not write data in the bits whose corresponding bits in the write data mask register (WM15–0) are assigned with “1”, and the corresponding data in GRAM are not overwritten but retained. This function is useful when only one-pixel data are rewritten or a particular color in the display is selectively changed.



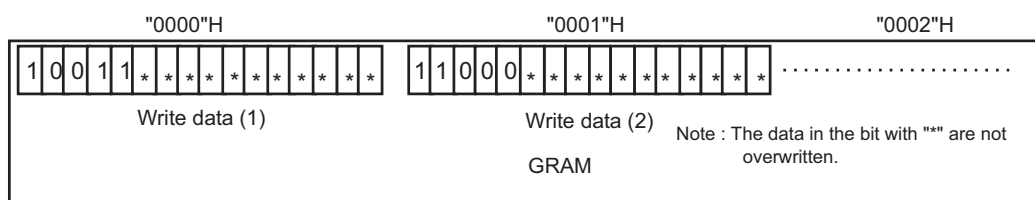
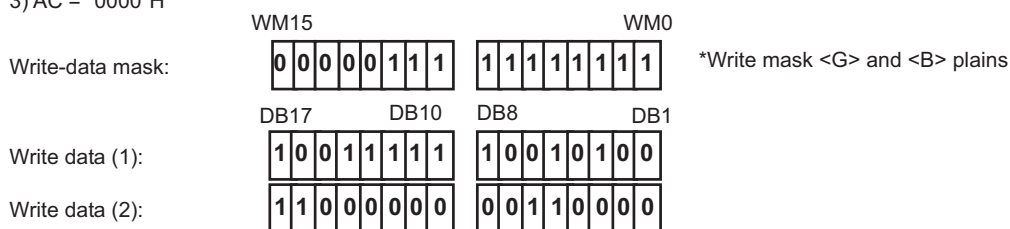
Graphics Operation Processing

1. Write mode 1: AM = 0, LG2-0 = 000

This mode is used when data are horizontally written in high-speed mode. It is also used to initialize the graphics RAM (GRAM) or to draw a line horizontally. The write-data mask function (WM15-0) is also available in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the counter at the opposing edge of the next one-raster-row below after when the counter reaches either left or right edge of GRAM.

Operation Examples:

- 1) I/D = "1", AM = "0", LG2-0 = "000"
- 2) WM15-0 = "07FF"H
- 3) AC = "0000"H



2. Write mode 2: AM = 1, LG2-0 = 000

This mode is used when data are vertically written in high-speed mode. It is also used to initialize the graphics RAM (GRAM), develop font patterns or draw a line vertically. The write-data mask function (WM15-0) is also available in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the counter either at the top of the next right row (ID = 1) or the next left row (I/D = 0) according to the setting in the I/D bit, when the address reaches the bottom of GRAM.

- 1) I/D = "1", AM = "1", LG2-0 = "000"
- 2) WM15-0 = "07FF"H
- 3) AC = "0000"H

Write-data mask:	WM15								WM0							
	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
Write data (1):	DB17								DB10							
	1	0	0	1	1	1	1	1	1	1	0	1	0	1	0	0
Write data (2):	DB17								DB10							
	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0
Write data (3):	DB17								DB10							
	0	1	1	1	1	1	1	0	0	0	1	0	0	0	0	1

"0000"H	1	0	0	1	1	*	*	*	*	*	*	*	*	*	*	*	Write data (1)
"0100"H	1	1	0	0	0	*	*	*	*	*	*	*	*	*	*	*	Write data (2)
"0200"H	0	1	1	1	1	*	*	*	*	*	*	*	*	*	*	*	Write data (3)

GRAM

Note 1) The data in the bit with "*" are not overwritten.

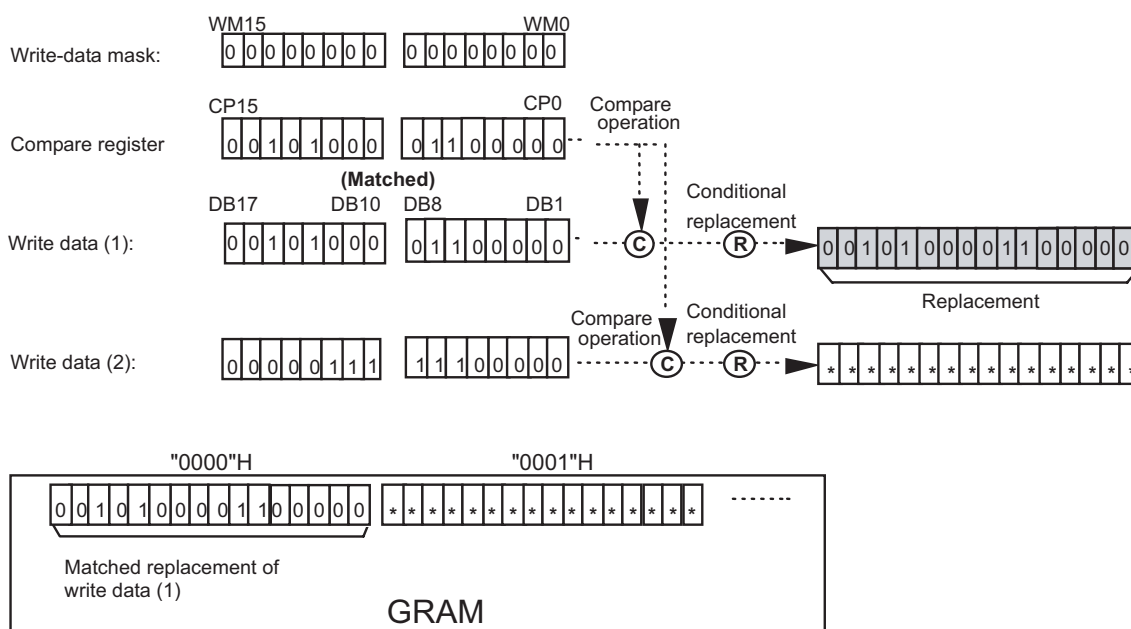
Note 2) When data are written to the address "AF00"H, the Address Counter (AC) jumps to "0001"H.

3. Write mode 3: AM = 0, LG2-0 = 110/111

This mode is used when data are horizontally written with comparing the write data and the value set in the compare register (CP15-0). When the result of the comparison satisfies a condition, the write data sent from the microcomputer are written to GRAM. In this operation, the write-data mask function (WM15-0) is available. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the counter at the opposing edge of the next one-raster-row below after when the counter reaches either left or right edge of GRAM.

Operation Examples:

- 1) I / D = "1", AM = "0", LG2-0 = "110" (matched write)
- 2) CP15-0 = "2860"H
- 2) WM15-0 = "0000"H
- 3) AC = "0000"H

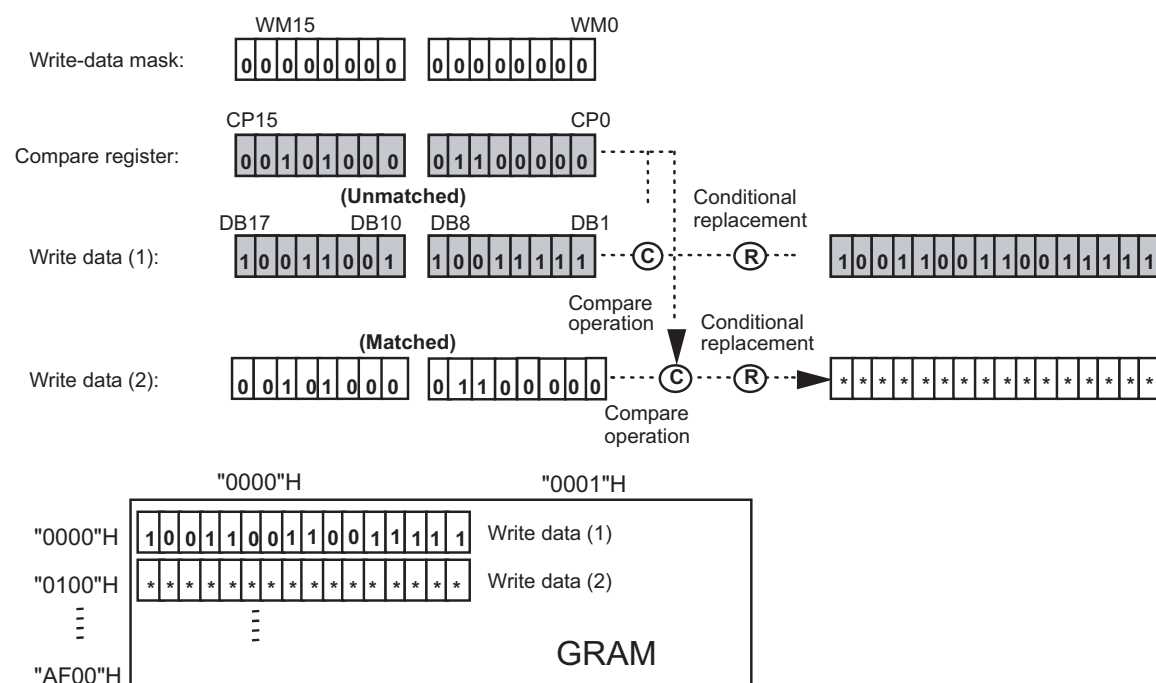


4. Write mode 4: AM = 1, LG2-0 = 110/111

This mode is used when data are horizontally written with comparing the write data and the value set in the compare register (CP15-0). When the result of the comparison satisfies a condition, the write data sent from the microcomputer are written to GRAM. In this operation, the write-data mask function (WM15-0) is available. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the counter either at the top of the next right row (ID = 1) or the next left row (I/D = 0) according to the setting in the I/D bit, when the address reaches the bottom of GRAM.

Operation Examples:

- 1) I/D = "1", AM = "1", LG2-0 = "111" (unmatched write)
- 2) CP15-0 = "2860"H
- 2) WM15-0 = "0000"H
- 3) AC = "0000"H



- Note 1) The data in the bit with "*" are not overwritten.
 Note 2) When data are written to the address "AF00"H, the Address Counter (AC) jumps to "0001"H.

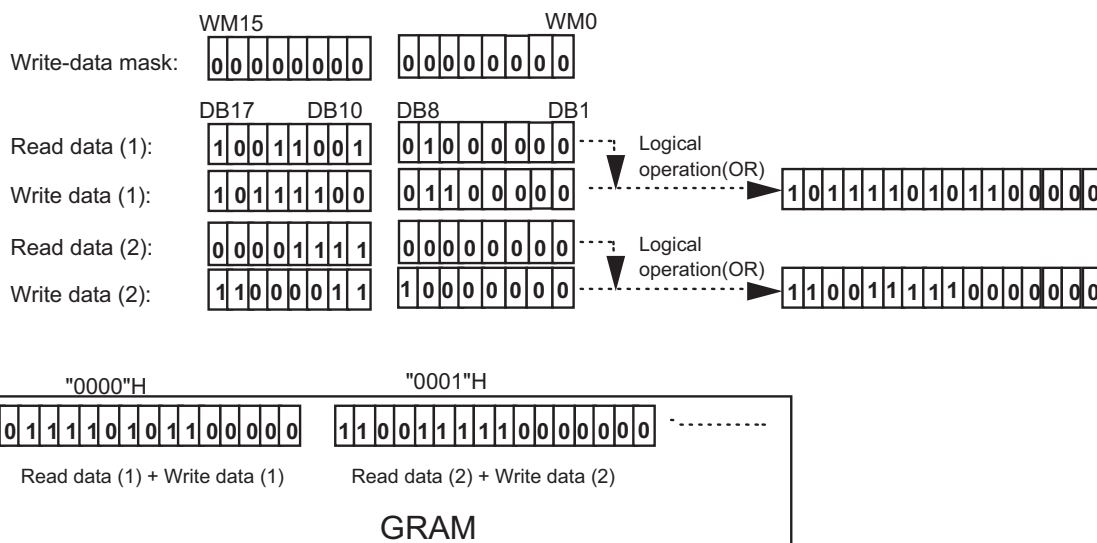
HD66773R

5. Read/Write mode 1: AM = 0, LG2-0 = 001/010/011

This mode is used when data are horizontally written in high-speed with performing logical operation on the GRAM data (base data) and data from the microcomputer. The logical operation is performed on the GRAM read-out data and the data sent from the microcomputer, and the result of the logical operation is written to GRAM. In the read operation, the GRAM data is not read out to the microcomputer but retained temporarily in the read-data latch of the HD66773R. Accordingly, the read operation can be performed using the same pulse width with the write-access pulse (68-system: ENABLE "High" level width, 80-system: ENABLE "Low" level width), but requires the same bus cycle time as the normal read operation. In this operation, the write-data mask function (WM15-0) is available. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the counter at the opposing edge of the next one-raster-row below after when the counter reaches either left or right edge of GRAM.

Operation Examples:

- 1) I/D = "1", AM = "0", LG2-0 = "001"(OR)
- 2) WM15-0 = "0000"H
- 3) AC = "0000"H



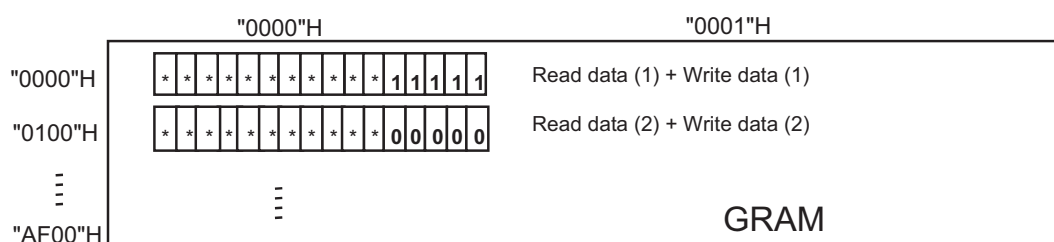
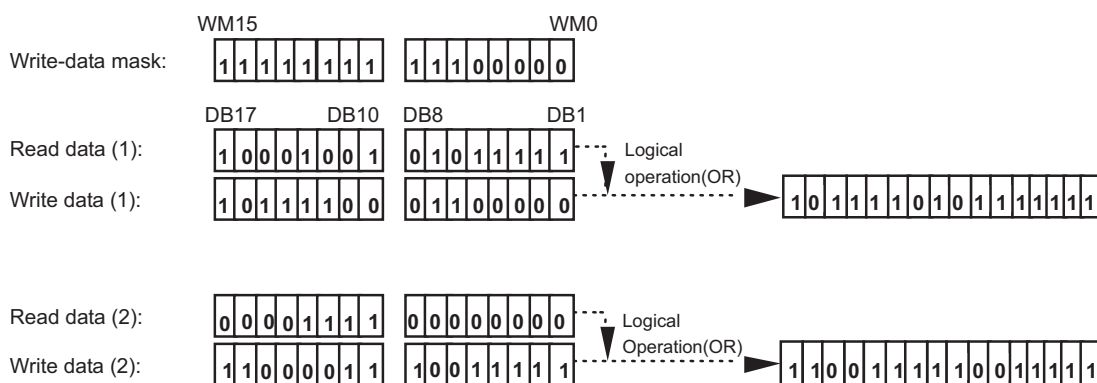
HD66773R

6. Read/Write mode 2: AM = 1, LG2-0 = 110/111

This mode is used when data are vertically written in high-speed with performing logical operation on the GRAM data (base data) and data from the microcomputer. The logical operation is performed on the GRAM read-out data and the data sent from the microcomputer, and the result of the logical operation is written to GRAM. In the read operation, the GRAM data is not read out to the microcomputer but retained temporarily in the read-data latch of the HD66773R. Accordingly, the read operation can be performed using the same pulse width with the write-access pulse (68-system: ENABLE "High" level width, 80-system: ENABLE "Low" level width), but requires the same bus cycle time as the normal read operation. In this operation, the write-data mask function (WM15-0) is available. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the counter either at the top of the next right row (ID = 1) or the next left row (I/D = 0) according to the setting in the I/D bit, when the address reaches the bottom of GRAM.

Operation Examples:

- 1) I / D = "1", AM = "1", LG2-0 = "001"(OR)
- 2) WM15-0 = "FFE0"H
- 3) AC = "0000"H



Note 1) The data in the bit with "*" are not overwritten.

Note 2) When data are written to the address "AF00"H, the Address Counter (AC) jumps to "0001"H.

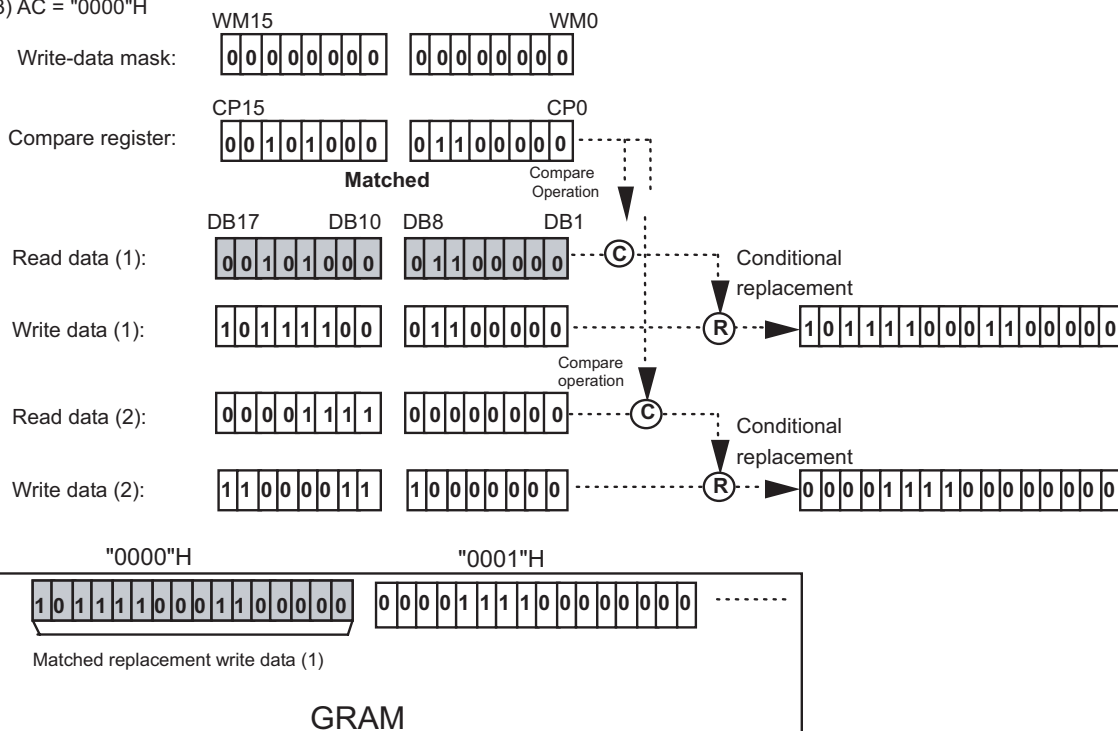
HD66773R

7. Read/Write mode 3: AM = 0, LG2-0 = 100/101

This mode is used when data are horizontally written in high-speed with performing compare operation on the GRAM data (base data) and the value set in the compare register (CP15-0). The compare operation is performed on the GRAM read-out data and the value set in the compare register by word. When the result of the comparison satisfies a condition, the data sent from the microcomputer are written to GRAM. In the read operation, the GRAM data is not read out to the microcomputer but retained temporarily in the read-data latch of the HD66773R. Accordingly, the read operation can be performed using the same pulse width with the write-access pulse (68-system: ENABLE "High" level width, 80-system: ENABLE "Low" level width), but requires the same bus cycle time as the normal read operation. In this operation, the write-data mask function (WM15-0) is available. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the counter at the opposing edge of the next one-raster-row below after when the counter reaches either left or right edge of GRAM.

Operation Examples:

- 1) I/D = "1", AM = "0", LG2-0 = "100" (matched write)
- 2) CP15-0 = "2860"H
- 2) WM15-0 = "0000"H
- 3) AC = "0000"H

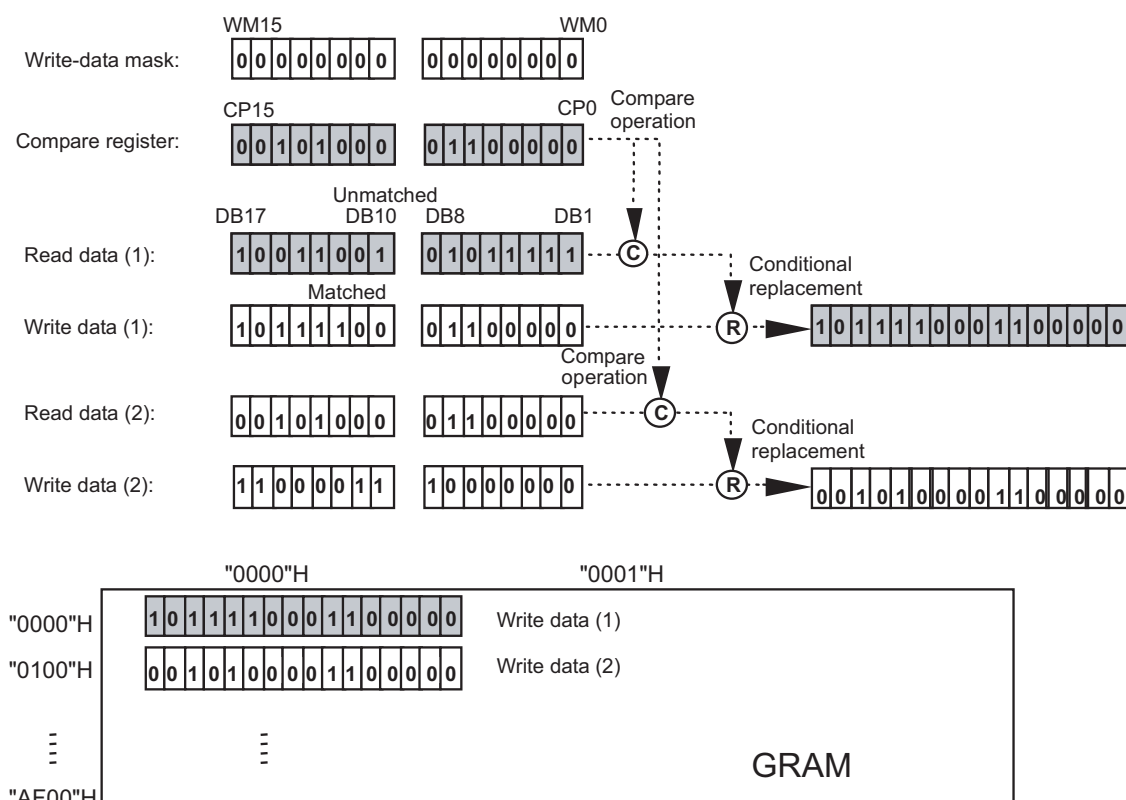


8. Read/Write mode 4: AM = 1, LG2-0 = 100/101

This mode is used when data are vertically written in high-speed with performing compare operation on the GRAM data (base data) and the value set in the compare register (CP15-0). The compare operation is performed on the GRAM read-out data and the value set in the compare register by word. When the result of the comparison satisfies a condition, the data sent from the microcomputer are written to GRAM. In the read operation, the GRAM data is not read out to the microcomputer but retained temporarily in the read-data latch of the HD66773R. Accordingly, the read operation can be performed using the same pulse width with the write-access pulse (68-system: ENABLE "High" level width, 80-system: ENABLE "Low" level width), but requires the same bus cycle time as the normal read operation. In this operation, the write-data mask function (WM15-0) is available. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the counter either at the top of the next right row (ID = 1) or the next left row (I/D = 0) according to the setting in the I/D bit, when the address reaches the bottom of GRAM.

Operation Examples:

- 1) I / D = "1", AM = "1", LG2-0 = "101" (unmatched write)
- 2) CP15-0 = "2860"H
- 2) WM15-0 = "0000"H
- 3) AC = "0000"H

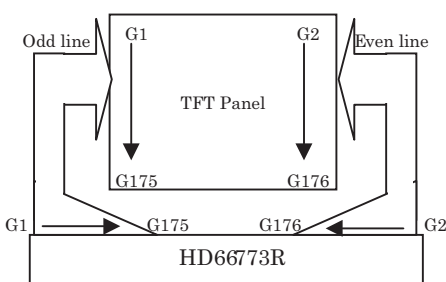
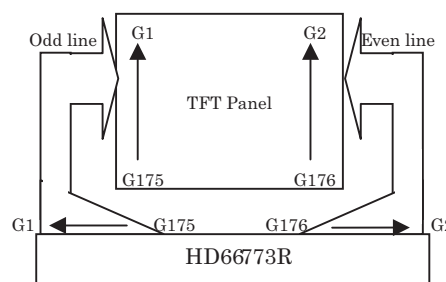
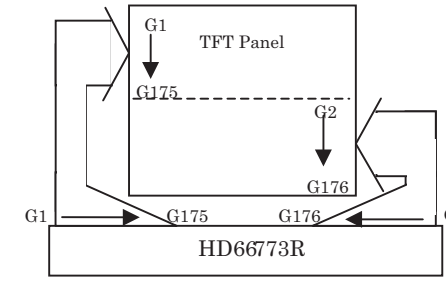
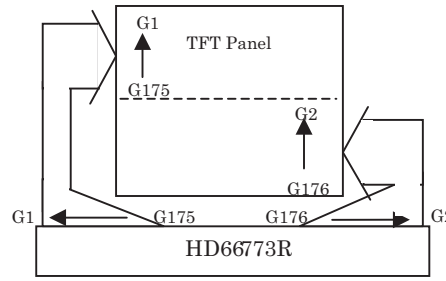


Note 1) The data in the bit with "*" are not overwritten.

Note 2) When data are written to the address "AF00"H, the Address Counter (AC) jumps to "0001"H.

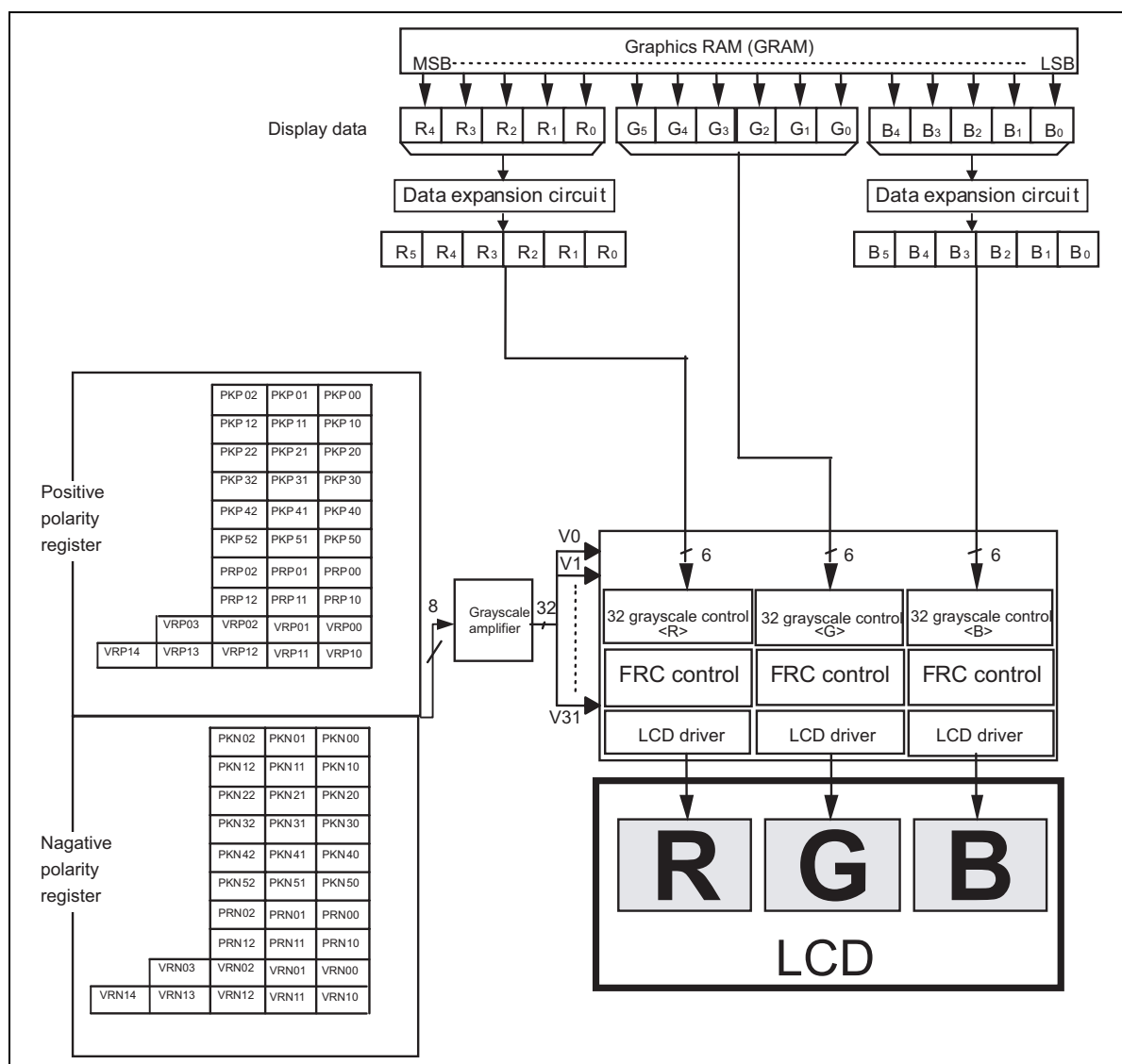
Scan Mode Setting

The shift direction of gate signal is changeable by the combination of SM and GS bit settings. This allows various ways of connecting a liquid crystal panel and the HD66773R.

SM	GS	Scan direction	
0	0		G1→G2→G3 G4→...→G173 G174→G175→G176
0	1		G176→G175→G174 173→...→G4 G3→G2→G1
1	0		G1→G3 G5→...→G173→G175 G2→G4 G6→...→G174→G176
1	1		G176→G174 G172→...→G4→G2 G175→G173 G171→...→G3→G1

γ -Correction Function

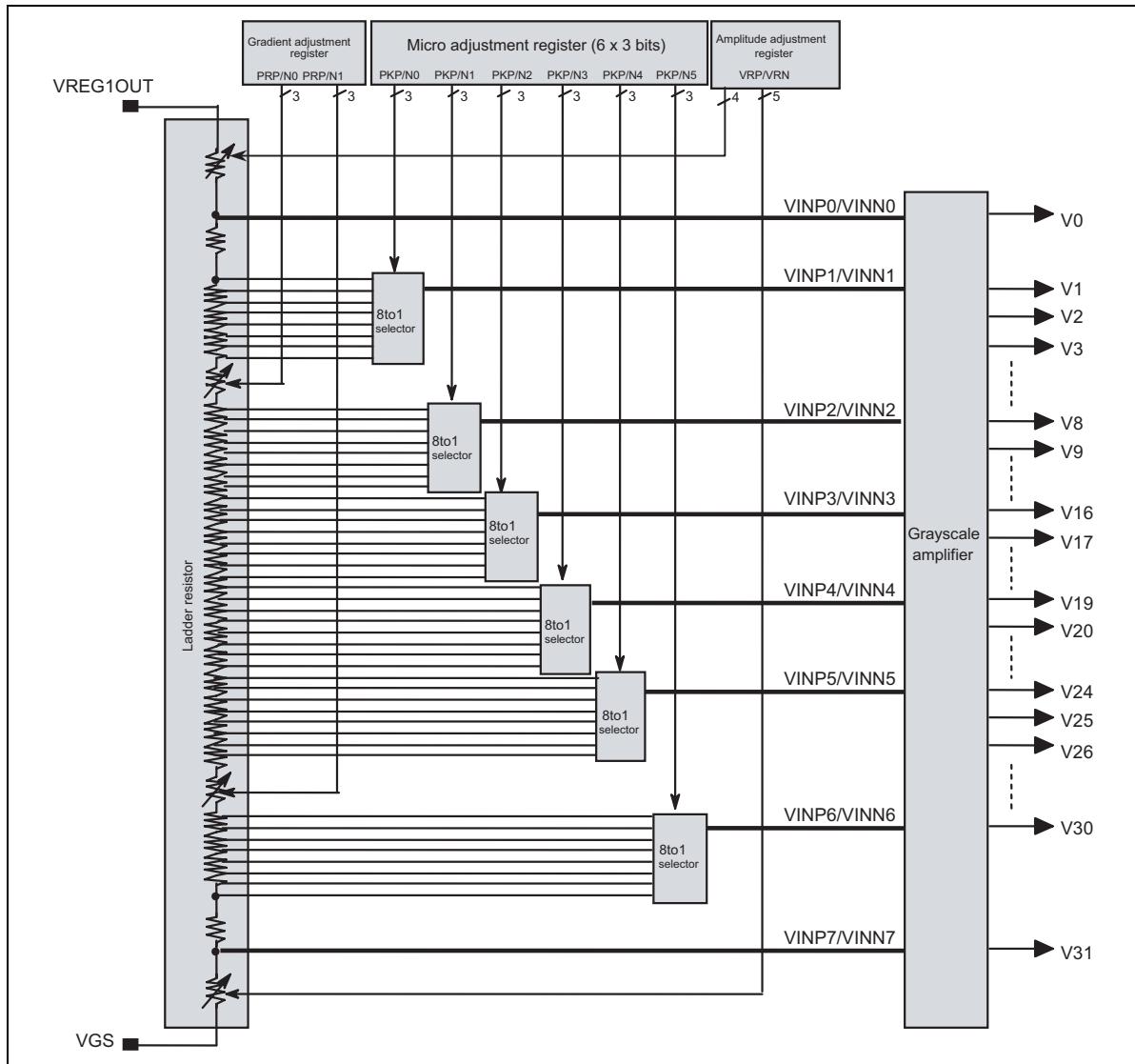
The HD66773R incorporates γ -correction function to simultaneously display 262,144 colors, by which 8-level grayscale is determined by the gradient-adjustment and fine-adjustment registers. Select either positive or negative polarity of the registers according to the characteristics of a liquid crystal panel.

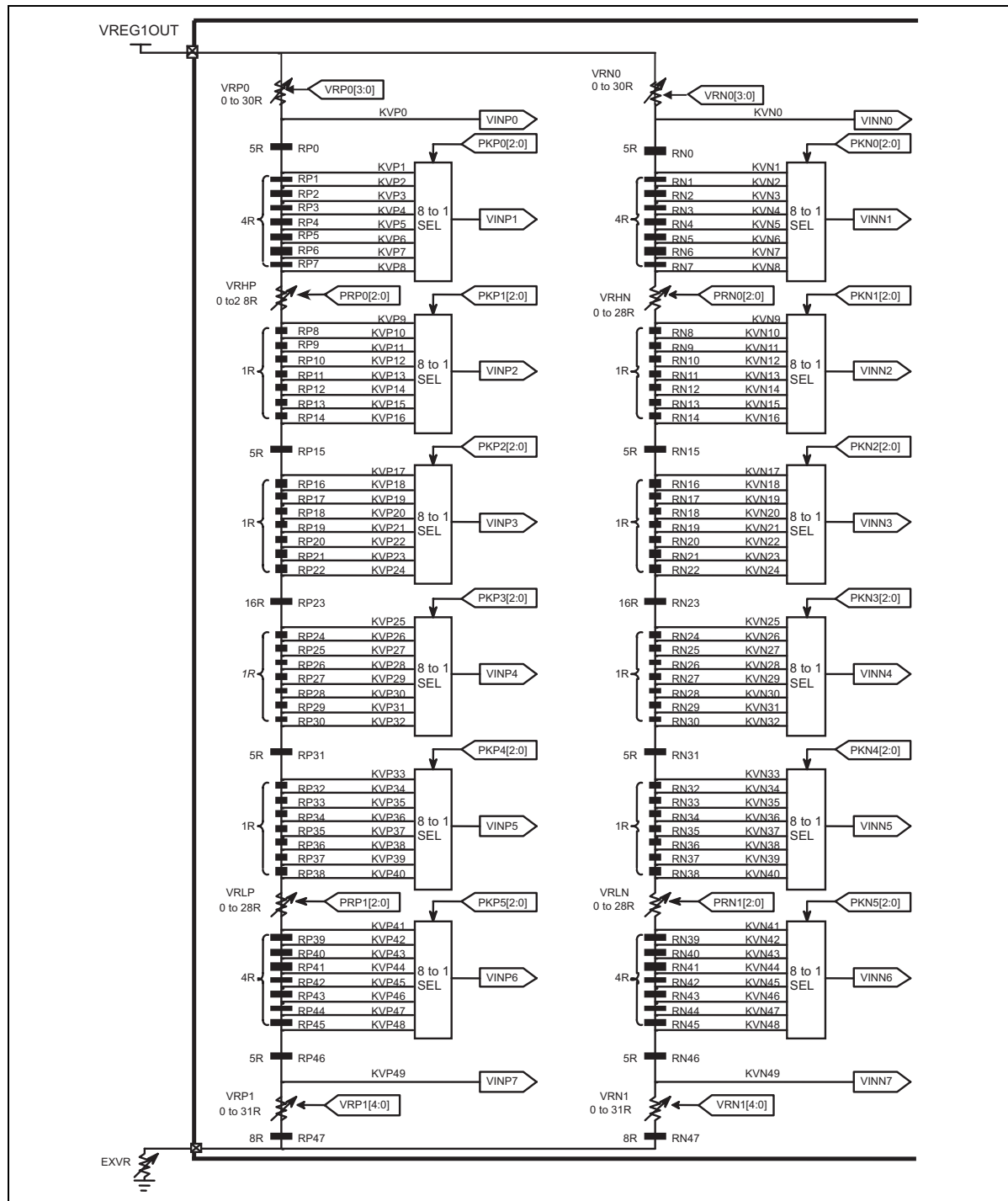


Note 1) 16-bit RAM data is expanded into 18-bit data through data expansion circuit.

Configuration of Grayscale Amplifier

The gradient adjustment and fine adjustment registers determine the eight levels (VIN0-7) of grayscale. The 8 levels are then divided into 32 levels (V0-31) by the ladder resistors placed between each level.

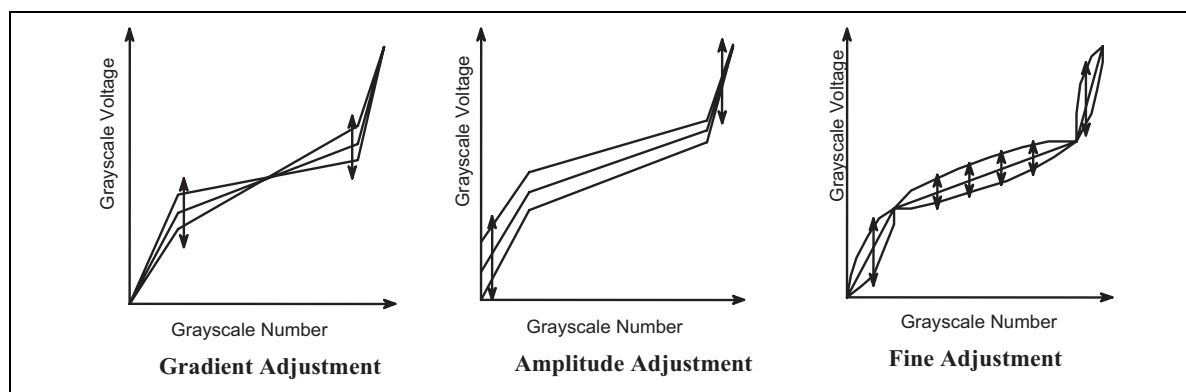




Ladder Resistors and 8-to-1 Selectors

γ -Correction Register

The γ -adjustment register is a group of registers to set an appropriate grayscale voltage for the γ -characteristics of a liquid crystal panel. The register group is categorized into the ones adjusting gradient, amplitude, and fine-tuning in relation to grayscale number and voltage characteristics. Each register can make an independent setting for the positive/negative polarity. The reference value and RGB are common for all registers.



γ -Correction Register

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient around the middle of the grayscale number and voltage characteristics without changing the dynamic range. To adjust a gradient, the values of the variable resistors (VRHP (N)/VRL (N)) in the middle of the ladder resistor block for grayscale voltage generation are controlled. The registers incorporate separate registers for positive and negative polarities to be compatible with asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. To adjust the amplitude, the values of the variable resistor (VRP(N)1/0) located at the lower side of the ladder resistor block for grayscale voltage generation are adjusted. The variable resistor located at the upper side of the ladder resistor block is adjusted by the input VDH level or reference resistor. Same with the gradient registers, the registers also incorporate separate registers for positive and negative polarities.

3. Fine adjustment registers

The fine adjustment register is to fine-adjust the grayscale voltage level. To fine-adjust the grayscale voltage level, each level of 8-level reference voltages generated from the ladder registers is controlled by 8-to-1 selector. Same with the other registers, the registers also incorporate separate registers for positive and negative polarities.

γ -Correction Registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 2 to 0	PRN0 2 to 0	Variable resistor VRHP (N)
	PRP1 2 to 0	PRN1 2 to 0	Variable resistor VRLP (N)
Amplitude adjustment	VRP0 3 to 0	VRN0 3 to 0	Variable resistor VRP (N)0
	VRP1 4 to 0	VRN1 4 to 0	Variable resistor VRP (N)1
Fine adjustment	PKP0 2 to 0	PKN0 2 to 0	8-to-1 selector (voltage level of grayscale 1)
	PKP1 2 to 0	PKN1 2 to 0	8-to-1 selector (voltage level of grayscale 8)
	PKP2 2 to 0	PKN2 2 to 0	8-to-1 selector (voltage level of grayscale 20)
	PKP3 2 to 0	PKN3 2 to 0	8-to-1 selector (voltage level of grayscale 43)
	PKP4 2 to 0	PKN4 2 to 0	8-to-1 selector (voltage level of grayscale 55)
	PKP5 2 to 0	PKN5 2 to 0	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector
Block configuration

The block diagram of page **86** consists of two ladder resistors including variable resistors, and 8-to-1 selectors which select the voltage generated by the ladder resistors to output a reference voltage for the grayscale voltage. The variable resistors and the 8-to-1 selectors are controlled by the γ correction register. Pins to be connected to a variable resistor are provided to compensate the variation among the panels.

Variable resistor

There are two kinds of variable resistors for the gradient adjustment (VRHP(N)/VRLP(N)) and the amplitude adjustment (VRP(N)0/ VRP(N)1). The resistance is determined by the gradient adjustment and amplitude adjustment registers as is shown below.

Gradient adjustment (1)		Gradient adjustment (2)	
Register value PRP(N)0[2:0]	Resistance VRHP(N)	Register value PRP(N)1[2:0]	Resistance VRLP(N)
000	0R	000	0R
001	4R	001	4R
010	8R	010	8R
011	12R	011	12R
100	16R	100	16R
101	20R	101	20R
110	24R	110	24R
111	28R	111	28R

HD66773R

Amplitude adjustment (1) Amplitude adjustment (2)

Register value VRP(N)0[3:0]	Resistance VRP(N)0	Register value VRP(N)1[4:0]	Resistance VRP(N)1
0000	0R	00000	0R
0001	2R	00001	1R
0010	4R	00010	2R
⋮	⋮	⋮	⋮
1101	26R	11101	29R
1111	28R	11110	30R
1111	30R	11111	31R

8-to-1 selector

The 8-to-1 selectors select a voltage level generated by the ladder resistors according to the fine adjustment registers, and output six kinds of reference voltage, VIN1 to VIN 6. The relationship between the fine adjustment register and the selected voltage is as follows.

Fine adjustment registers and selected voltage

The value of Register PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

HD66773R

The grayscale levels (V0-V31) are calculated according to the following formulas.

Formulas for calculating voltage (Positive polarity) (1)

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	$VREG1OUT - \Delta V \cdot VRP0 / SUMRP$	-	VINP0
KVP1	$VREG1OUT - \Delta V \cdot (VRP0 + 5R) / SUMRP$	PKP02-00 = "000"	VINP1
KVP2	$VREG1OUT - \Delta V \cdot (VRP0 + 9R) / SUMRP$	PKP02-00 = "001"	
KVP3	$VREG1OUT - \Delta V \cdot (VRP0 + 13R) / SUMRP$	PKP02-00 = "010"	
KVP4	$VREG1OUT - \Delta V \cdot (VRP0 + 17R) / SUMRP$	PKP02-00 = "011"	
KVP5	$VREG1OUT - \Delta V \cdot (VRP0 + 21R) / SUMRP$	PKP02-00 = "100"	
KVP6	$VREG1OUT - \Delta V \cdot (VRP0 + 25R) / SUMRP$	PKP02-00 = "101"	
KVP7	$VREG1OUT - \Delta V \cdot (VRP0 + 29R) / SUMRP$	PKP02-00 = "110"	
KVP8	$VREG1OUT - \Delta V \cdot (VRP0 + 33R) / SUMRP$	PKP02-00 = "111"	
KVP9	$VREG1OUT - \Delta V \cdot (VRP0 + 33R + VRHP) / SUMRP$	PKP12-10 = "000"	VINP2
KVP10	$VREG1OUT - \Delta V \cdot (VRP0 + 34R + VRHP) / SUMRP$	PKP12-10 = "001"	
KVP11	$VREG1OUT - \Delta V \cdot (VRP0 + 35R + VRHP) / SUMRP$	PKP12-10 = "010"	
KVP12	$VREG1OUT - \Delta V \cdot (VRP0 + 36R + VRHP) / SUMRP$	PKP12-10 = "011"	
KVP13	$VREG1OUT - \Delta V \cdot (VRP0 + 37R + VRHP) / SUMRP$	PKP12-10 = "100"	
KVP14	$VREG1OUT - \Delta V \cdot (VRP0 + 38R + VRHP) / SUMRP$	PKP12-10 = "101"	
KVP15	$VREG1OUT - \Delta V \cdot (VRP0 + 39R + VRHP) / SUMRP$	PKP12-10 = "110"	
KVP16	$VREG1OUT - \Delta V \cdot (VRP0 + 40R + VRHP) / SUMRP$	PKP12-10 = "111"	
KVP17	$VREG1OUT - \Delta V \cdot (VRP0 + 45R + VRHP) / SUMRP$	PKP22-20 = "000"	VINP3
KVP18	$VREG1OUT - \Delta V \cdot (VRP0 + 46R + VRHP) / SUMRP$	PKP22-20 = "001"	
KVP19	$VREG1OUT - \Delta V \cdot (VRP0 + 47R + VRHP) / SUMRP$	PKP22-20 = "010"	
KVP20	$VREG1OUT - \Delta V \cdot (VRP0 + 48R + VRHP) / SUMRP$	PKP22-20 = "011"	
KVP21	$VREG1OUT - \Delta V \cdot (VRP0 + 49R + VRHP) / SUMRP$	PKP22-20 = "100"	
KVP22	$VREG1OUT - \Delta V \cdot (VRP0 + 50R + VRHP) / SUMRP$	PKP22-20 = "101"	
KVP23	$VREG1OUT - \Delta V \cdot (VRP0 + 51R + VRHP) / SUMRP$	PKP22-20 = "110"	
KVP24	$VREG1OUT - \Delta V \cdot (VRP0 + 52R + VRHP) / SUMRP$	PKP22-20 = "111"	
KVP25	$VREG1OUT - \Delta V \cdot (VRP0 + 68R + VRHP) / SUMRP$	PKP32-30 = "000"	VINP4
KVP26	$VREG1OUT - \Delta V \cdot (VRP0 + 69R + VRHP) / SUMRP$	PKP32-30 = "001"	
KVP27	$VREG1OUT - \Delta V \cdot (VRP0 + 70R + VRHP) / SUMRP$	PKP32-30 = "010"	
KVP28	$VREG1OUT - \Delta V \cdot (VRP0 + 71R + VRHP) / SUMRP$	PKP32-30 = "011"	
KVP29	$VREG1OUT - \Delta V \cdot (VRP0 + 72R + VRHP) / SUMRP$	PKP32-30 = "100"	
KVP30	$VREG1OUT - \Delta V \cdot (VRP0 + 73R + VRHP) / SUMRP$	PKP32-30 = "101"	
KVP31	$VREG1OUT - \Delta V \cdot (VRP0 + 74R + VRHP) / SUMRP$	PKP32-30 = "110"	
KVP32	$VREG1OUT - \Delta V \cdot (VRP0 + 75R + VRHP) / SUMRP$	PKP32-30 = "111"	
KVP33	$VREG1OUT - \Delta V \cdot (VRP0 + 80R + VRHP) / SUMRP$	PKP42-00 = "000"	VINP5
KVP34	$VREG1OUT - \Delta V \cdot (VRP0 + 81R + VRHP) / SUMRP$	PKP42-40 = "001"	
KVP35	$VREG1OUT - \Delta V \cdot (VRP0 + 82R + VRHP) / SUMRP$	PKP42-40 = "010"	
KVP36	$VREG1OUT - \Delta V \cdot (VRP0 + 83R + VRHP) / SUMRP$	PKP42-40 = "011"	
KVP37	$VREG1OUT - \Delta V \cdot (VRP0 + 84R + VRHP) / SUMRP$	PKP42-40 = "100"	
KVP38	$VREG1OUT - \Delta V \cdot (VRP0 + 85R + VRHP) / SUMRP$	PKP42-40 = "101"	
KVP39	$VREG1OUT - \Delta V \cdot (VRP0 + 86R + VRHP) / SUMRP$	PKP42-40 = "110"	
KVP40	$VREG1OUT - \Delta V \cdot (VRP0 + 87R + VRHP) / SUMRP$	PKP42-40 = "111"	
KVP41	$VREG1OUT - \Delta V \cdot (VRP0 + 87R + VRHP + VRLP) / SUMRP$	PKP52-50 = "000"	VINP6
KVP42	$VREG1OUT - \Delta V \cdot (VRP0 + 91R + VRHP + VRLP) / SUMRP$	PKP52-50 = "001"	
KVP43	$VREG1OUT - \Delta V \cdot (VRP0 + 95R + VRHP + VRLP) / SUMRP$	PKP52-50 = "010"	
KVP44	$VREG1OUT - \Delta V \cdot (VRP0 + 99R + VRHP + VRLP) / SUMRP$	PKP52-50 = "011"	
KVP45	$VREG1OUT - \Delta V \cdot (VRP0 + 103R + VRHP + VRLP) / SUMRP$	PKP52-50 = "100"	
KVP46	$VREG1OUT - \Delta V \cdot (VRP0 + 107R + VRHP + VRLP) / SUMRP$	PKP52-50 = "101"	
KVP47	$VREG1OUT - \Delta V \cdot (VRP0 + 111R + VRHP + VRLP) / SUMRP$	PKP52-50 = "110"	
KVP48	$VREG1OUT - \Delta V \cdot (VRP0 + 115R + VRHP + VRLP) / SUMRP$	PKP52-50 = "111"	
KVP49	$VREG1OUT - \Delta V \cdot (VRP0 + 120R + VRHP + VRLP) / SUMRP$	-	VINP7

SUMRP: Total of the positive-polarity ladder resistors = 128 R + VRHP + VRLP + VRP0 + VRP1
SUMRN: Total of the negative-polarity ladder resistors= 128 R + VRHN + VRLN + VRN0 + VRN1
Δ V: Voltage difference between VREG1OUT - VGS

Formulas for calculating voltage (Positive polarity) (2)

grayscale voltage	Formula
V0	VINP0
V1	$V3D + (VINP1 - V3D) * (8/24)$
V2	$V4 + (V3D - V4) * (16/24)$
V3	$V4 + (V3D - V4) * (8/24)$
V4	VINP2
V5	$V10 + (V4 - V10) * (20/24)$
V6	$V10 + (V4 - V10) * (16/24)$
V7	$V10 + (V4 - V10) * (12/24)$
V8	$V10 + (V4 - V10) * (8/24)$
V9	$V10 + (V4 - V10) * (4/24)$
V10	VINP3
V11	$V21 + (V10 - V21) * (21/24)$
V12	$V21 + (V10 - V21) * (19/24)$
V13	$V21 + (V10 - V21) * (17/24)$
V14	$V21 + (V10 - V21) * (15/24)$
V15	$V21 + (V10 - V21) * (13/24)$
V16	$V21 + (V10 - V21) * (11/24)$
V17	$V21 + (V10 - V21) * (9/24)$
V18	$V21 + (V10 - V21) * (7/24)$
V19	$V21 + (V10 - V21) * (5/24)$
V20	$V21 + (V10 - V21) * (3/24)$
V21	VINP4
V22	$V27 + (V21 - V27) * (20/24)$
V23	$V27 + (V21 - V27) * (16/24)$
V24	$V27 + (V21 - V27) * (12/24)$
V25	$V27 + (V21 - V27) * (8/24)$
V26	$V27 + (V21 - V27) * (4/24)$
V27	VINP5
V28	$VINP6 + (V27 - VINP6) * (780/960)$
V29	$VINP6 + (V27 - VINP6) * (600/960)$
V30	$VINP6 + (V27 - VINP6) * (280/960)$
V31	VINP7

$$V3D: V3D = V4 + (VINP1 - V4) * (540/960)$$

Formulas for calculating voltage (Negative polarity) (1)

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	$VREG1OUT - \Delta V \cdot VRN0 / SUMRN$	-	VINN0
KVN1	$VREG1OUT - \Delta V \cdot (VRN0 + 5R) / SUMRN$	PKN02-00 = "000"	VINN1
KVN2	$VREG1OUT - \Delta V \cdot (VRN0 + 9R) / SUMRN$	PKN02-00 = "001"	
KVN3	$VREG1OUT - \Delta V \cdot (VRN0 + 13R) / SUMRN$	PKN02-00 = "010"	
KVN4	$VREG1OUT - \Delta V \cdot (VRN0 + 17R) / SUMRN$	PKN02-00 = "011"	
KVN5	$VREG1OUT - \Delta V \cdot (VRN0 + 21R) / SUMRN$	PKN02-00 = "100"	
KVN6	$VREG1OUT - \Delta V \cdot (VRN0 + 25R) / SUMRN$	PKN02-00 = "101"	
KVN7	$VREG1OUT - \Delta V \cdot (VRN0 + 29R) / SUMRN$	PKN02-00 = "110"	
KVN8	$VREG1OUT - \Delta V \cdot (VRN0 + 33R) / SUMRN$	PKN02-00 = "111"	VINN2
KVN9	$VREG1OUT - \Delta V \cdot (VRN0 + 33R + VRHN) / SUMRN$	PKN12-10 = "000"	
KVN10	$VREG1OUT - \Delta V \cdot (VRN0 + 34R + VRHN) / SUMRN$	PKN12-10 = "001"	
KVN11	$VREG1OUT - \Delta V \cdot (VRN0 + 35R + VRHN) / SUMRN$	PKN12-10 = "010"	
KVN12	$VREG1OUT - \Delta V \cdot (VRN0 + 36R + VRHN) / SUMRN$	PKN12-10 = "011"	
KVN13	$VREG1OUT - \Delta V \cdot (VRN0 + 37R + VRHN) / SUMRN$	PKN12-10 = "100"	
KVN14	$VREG1OUT - \Delta V \cdot (VRN0 + 38R + VRHN) / SUMRN$	PKN12-10 = "101"	
KVN15	$VREG1OUT - \Delta V \cdot (VRN0 + 39R + VRHN) / SUMRN$	PKN12-10 = "110"	VINN3
KVN16	$VREG1OUT - \Delta V \cdot (VRN0 + 40R + VRHN) / SUMRN$	PKN12-10 = "111"	
KVN17	$VREG1OUT - \Delta V \cdot (VRN0 + 45R + VRHN) / SUMRN$	PKN22-20 = "000"	
KVN18	$VREG1OUT - \Delta V \cdot (VRN0 + 46R + VRHN) / SUMRN$	PKN22-20 = "001"	
KVN19	$VREG1OUT - \Delta V \cdot (VRN0 + 47R + VRHN) / SUMRN$	PKN22-20 = "010"	
KVN20	$VREG1OUT - \Delta V \cdot (VRN0 + 48R + VRHN) / SUMRN$	PKN22-20 = "011"	
KVN21	$VREG1OUT - \Delta V \cdot (VRN0 + 49R + VRHN) / SUMRN$	PKN22-20 = "100"	
KVN22	$VREG1OUT - \Delta V \cdot (VRN0 + 50R + VRHN) / SUMRN$	PKN22-20 = "101"	VINN4
KVN23	$VREG1OUT - \Delta V \cdot (VRN0 + 51R + VRHN) / SUMRN$	PKN22-20 = "110"	
KVN24	$VREG1OUT - \Delta V \cdot (VRN0 + 52R + VRHN) / SUMRN$	PKN22-20 = "111"	
KVN25	$VREG1OUT - \Delta V \cdot (VRN0 + 68R + VRHN) / SUMRN$	PKN32-30 = "000"	
KVN26	$VREG1OUT - \Delta V \cdot (VRN0 + 69R + VRHN) / SUMRN$	PKN32-30 = "001"	
KVN27	$VREG1OUT - \Delta V \cdot (VRN0 + 70R + VRHN) / SUMRN$	PKN32-30 = "010"	
KVN28	$VREG1OUT - \Delta V \cdot (VRN0 + 71R + VRHN) / SUMRN$	PKN32-30 = "011"	
KVN29	$VREG1OUT - \Delta V \cdot (VRN0 + 72R + VRHN) / SUMRN$	PKN32-30 = "100"	VINN5
KVN30	$VREG1OUT - \Delta V \cdot (VRN0 + 73R + VRHN) / SUMRN$	PKN32-30 = "101"	
KVN31	$VREG1OUT - \Delta V \cdot (VRN0 + 74R + VRHN) / SUMRN$	PKN32-30 = "110"	
KVN32	$VREG1OUT - \Delta V \cdot (VRN0 + 75R + VRHN) / SUMRN$	PKN32-30 = "111"	
KVN33	$VREG1OUT - \Delta V \cdot (VRN0 + 80R + VRHN) / SUMRN$	PKN42-00 = "000"	
KVN34	$VREG1OUT - \Delta V \cdot (VRN0 + 81R + VRHN) / SUMRN$	PKN42-00 = "001"	
KVN35	$VREG1OUT - \Delta V \cdot (VRN0 + 82R + VRHN) / SUMRN$	PKN42-00 = "010"	VINN6
KVN36	$VREG1OUT - \Delta V \cdot (VRN0 + 83R + VRHN) / SUMRN$	PKN42-00 = "011"	
KVN37	$VREG1OUT - \Delta V \cdot (VRN0 + 84R + VRHN) / SUMRN$	PKN42-00 = "100"	
KVN38	$VREG1OUT - \Delta V \cdot (VRN0 + 85R + VRHN) / SUMRN$	PKN42-00 = "101"	
KVN39	$VREG1OUT - \Delta V \cdot (VRN0 + 86R + VRHN) / SUMRN$	PKN42-00 = "110"	
KVN40	$VREG1OUT - \Delta V \cdot (VRN0 + 87R + VRHN) / SUMRN$	PKN42-00 = "111"	
KVN41	$VREG1OUT - \Delta V \cdot (VRN0 + 87R + VRHN + VRLN) / SUMRN$	PKN52-50 = "000"	VINN7
KVN42	$VREG1OUT - \Delta V \cdot (VRN0 + 91R + VRHN + VRLN) / SUMRN$	PKN52-50 = "001"	
KVN43	$VREG1OUT - \Delta V \cdot (VRN0 + 95R + VRHN + VRLN) / SUMRN$	PKN52-50 = "010"	
KVN44	$VREG1OUT - \Delta V \cdot (VRN0 + 99R + VRHN + VRLN) / SUMRN$	PKN52-50 = "011"	
KVN45	$VREG1OUT - \Delta V \cdot (VRN0 + 103R + VRHN + VRLN) / SUMRN$	PKN52-50 = "100"	
KVN46	$VREG1OUT - \Delta V \cdot (VRN0 + 107R + VRHN + VRLN) / SUMRN$	PKN52-50 = "101"	
KVN47	$VREG1OUT - \Delta V \cdot (VRN0 + 111R + VRHN + VRLN) / SUMRN$	PKN52-50 = "110"	
KVN48	$VREG1OUT - \Delta V \cdot (VRN0 + 115R + VRHN + VRLN) / SUMRN$	PKN52-50 = "111"	
KVN49	$VREG1OUT - \Delta V \cdot (VRN0 + 120R + VRHN + VRLN) / SUMRN$	-	VINN7

SUMRP: Total of the positive-polarity ladder resistors = 128 R + VRHP + VRLP + VRP0 + VRP1

SUMRN: Total of the negative-polarity ladder resistors = 128 R + VRHN + VRLN + VRN0 + VRN1

 ΔV : Voltage difference between VREG1OUT - VGS

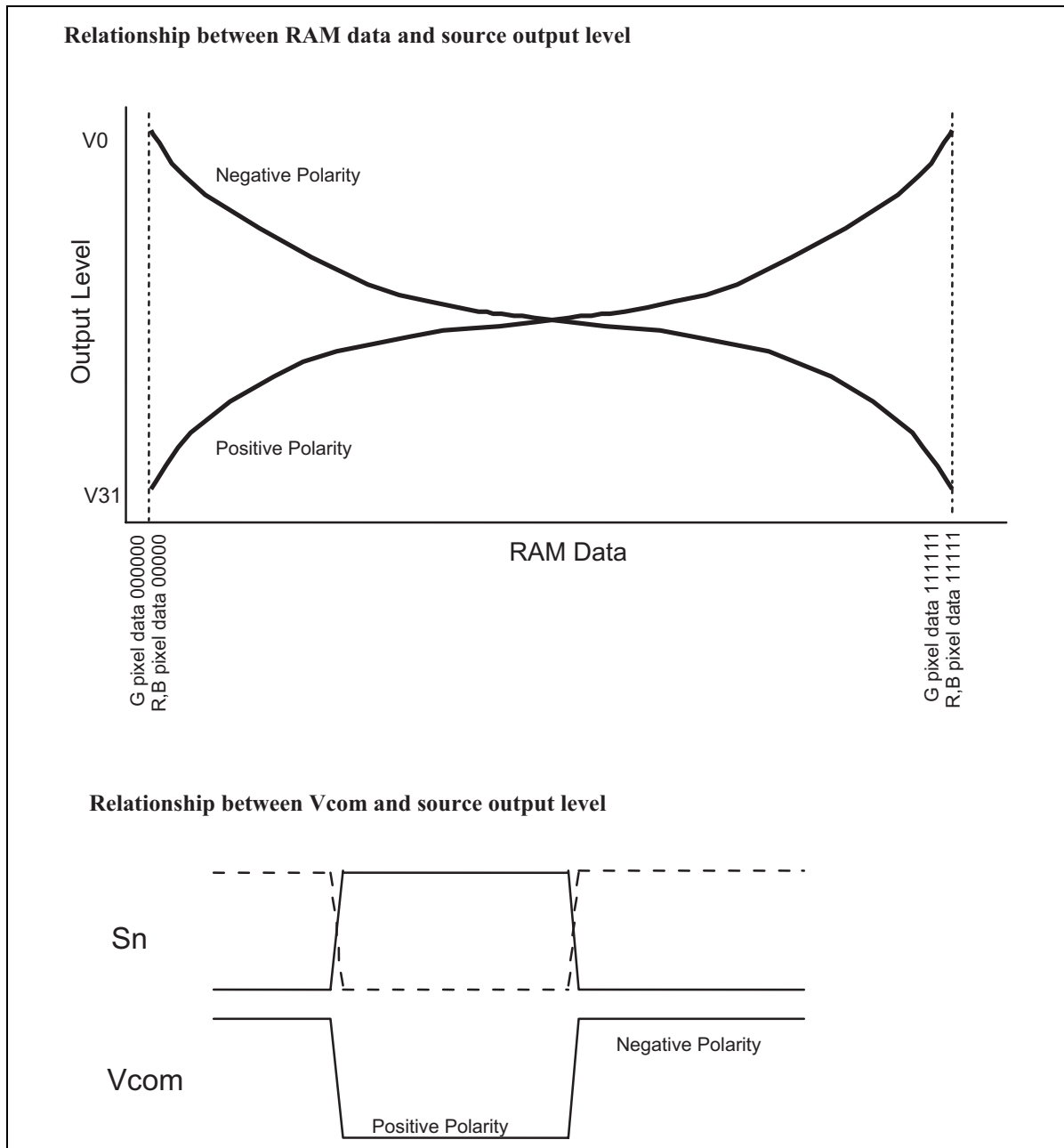
Formulas for calculating voltage (Negative polarity) (2)

grayscale voltage	Formula
V0	VINN0
V1	$V3D + (VINN1 - V3D) * (8/24)$
V2	$V4 + (V3D - V4) * (16/24)$
V3	$V4 + (V3D - V4) * (8/24)$
V4	VINN2
V5	$V10 + (V4 - V10) * (20/24)$
V6	$V10 + (V4 - V10) * (16/24)$
V7	$V10 + (V4 - V10) * (12/24)$
V8	$V10 + (V4 - V10) * (8/24)$
V9	$V10 + (V4 - V10) * (4/24)$
V10	VINN3
V11	$V21 + (V10 - V21) * (21/24)$
V12	$V21 + (V10 - V21) * (19/24)$
V13	$V21 + (V10 - V21) * (17/24)$
V14	$V21 + (V10 - V21) * (15/24)$
V15	$V21 + (V10 - V21) * (13/24)$
V16	$V21 + (V10 - V21) * (11/24)$
V17	$V21 + (V10 - V21) * (9/24)$
V18	$V21 + (V10 - V21) * (7/24)$
V19	$V21 + (V10 - V21) * (5/24)$
V20	$V21 + (V10 - V21) * (3/24)$
V21	VINN4
V22	$V27 + (V21 - V27) * (20/24)$
V23	$V27 + (V21 - V27) * (16/24)$
V24	$V27 + (V21 - V27) * (12/24)$
V25	$V27 + (V21 - V27) * (8/24)$
V26	$V27 + (V21 - V27) * (4/24)$
V27	VINN5
V28	$VINN6 + (V27 - VINN6) * (780/960)$
V29	$VINN6 + (V27 - VINN6) * (600/960)$
V30	$VINN6 + (V27 - VINN6) * (280/960)$
V31	VINN7

V3D: $V3D = V4 + (VINN1 - V4) * (540/960)$

Relationship between RAM data and output level

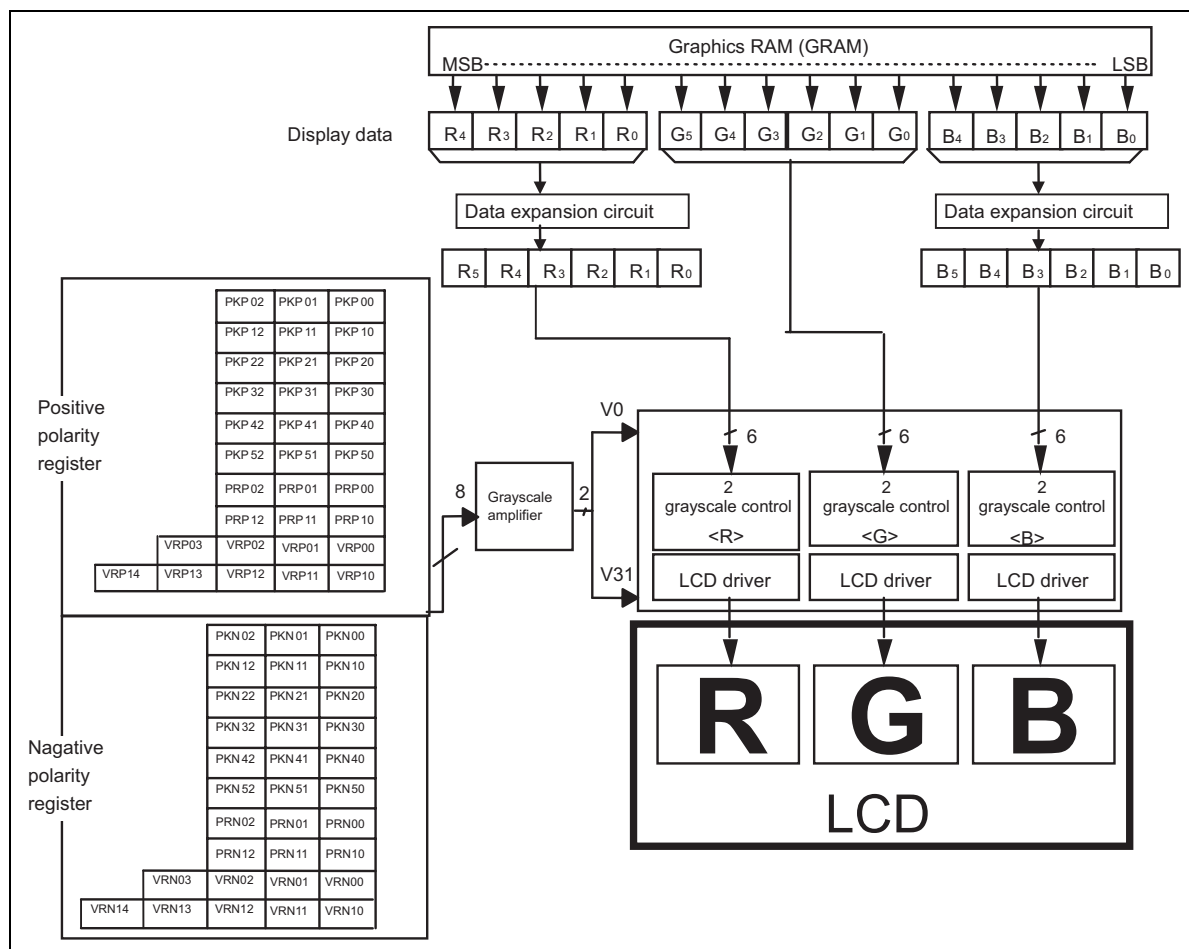
The relationship between the RAM data and the source output level is as follows.



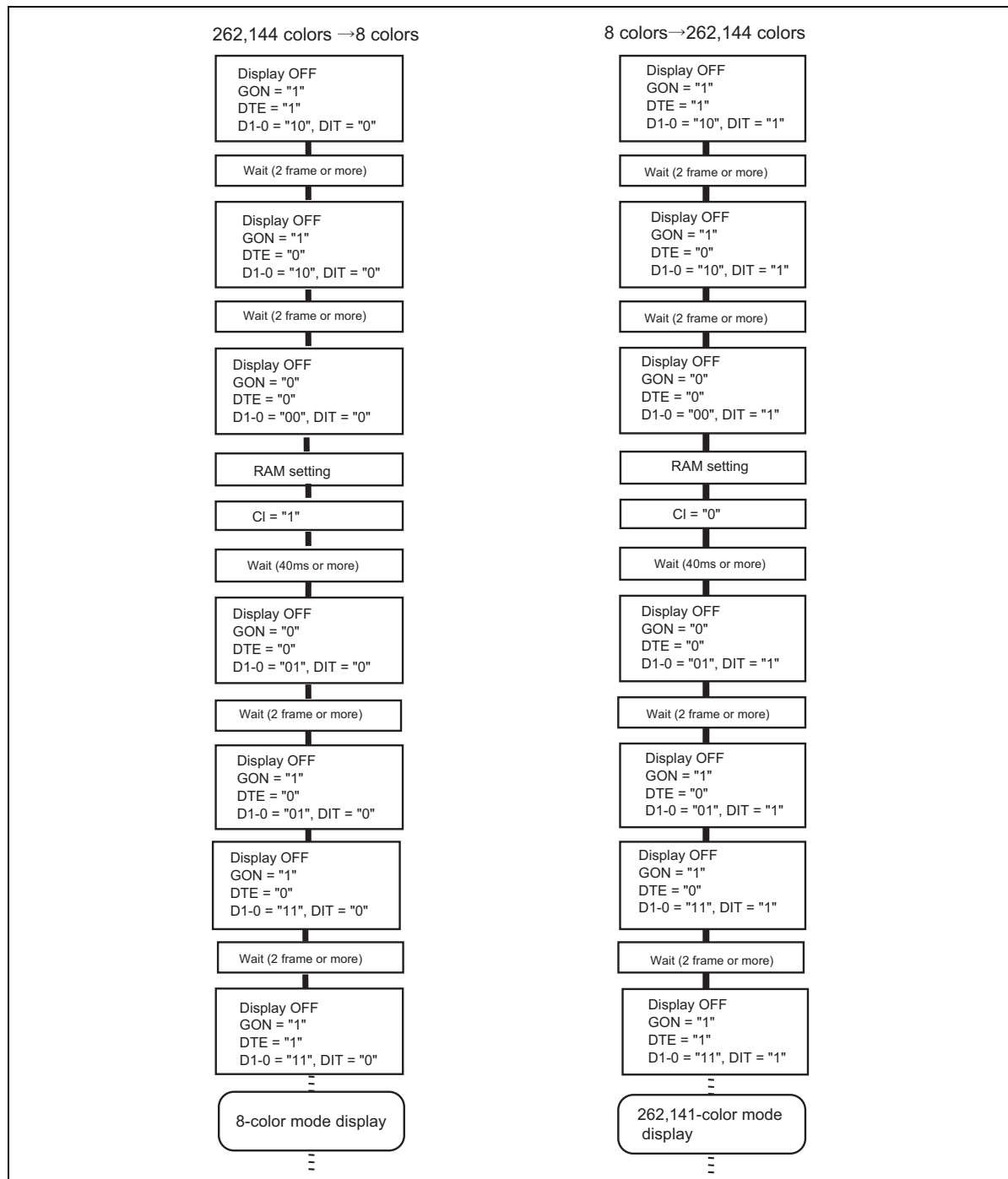
8-color Display Mode

The HD66773R incorporates 8-color display mode. The available grayscale levels are V0 and V31, and the voltages for the other levels (V1-V30) are halted to reduce power consumption.

The γ -fine-adjustment registers, PKP0-PKP5 and PKN0-PKN5 are not available in the 8-color display mode. Since the power supply for the levels V1-V30 are halted, R and B data in GRAM should be set to either "00000" or "11111" and G data in GRAM to either "000000" or "111111" before setting this mode so that V0 or V31 is selected.



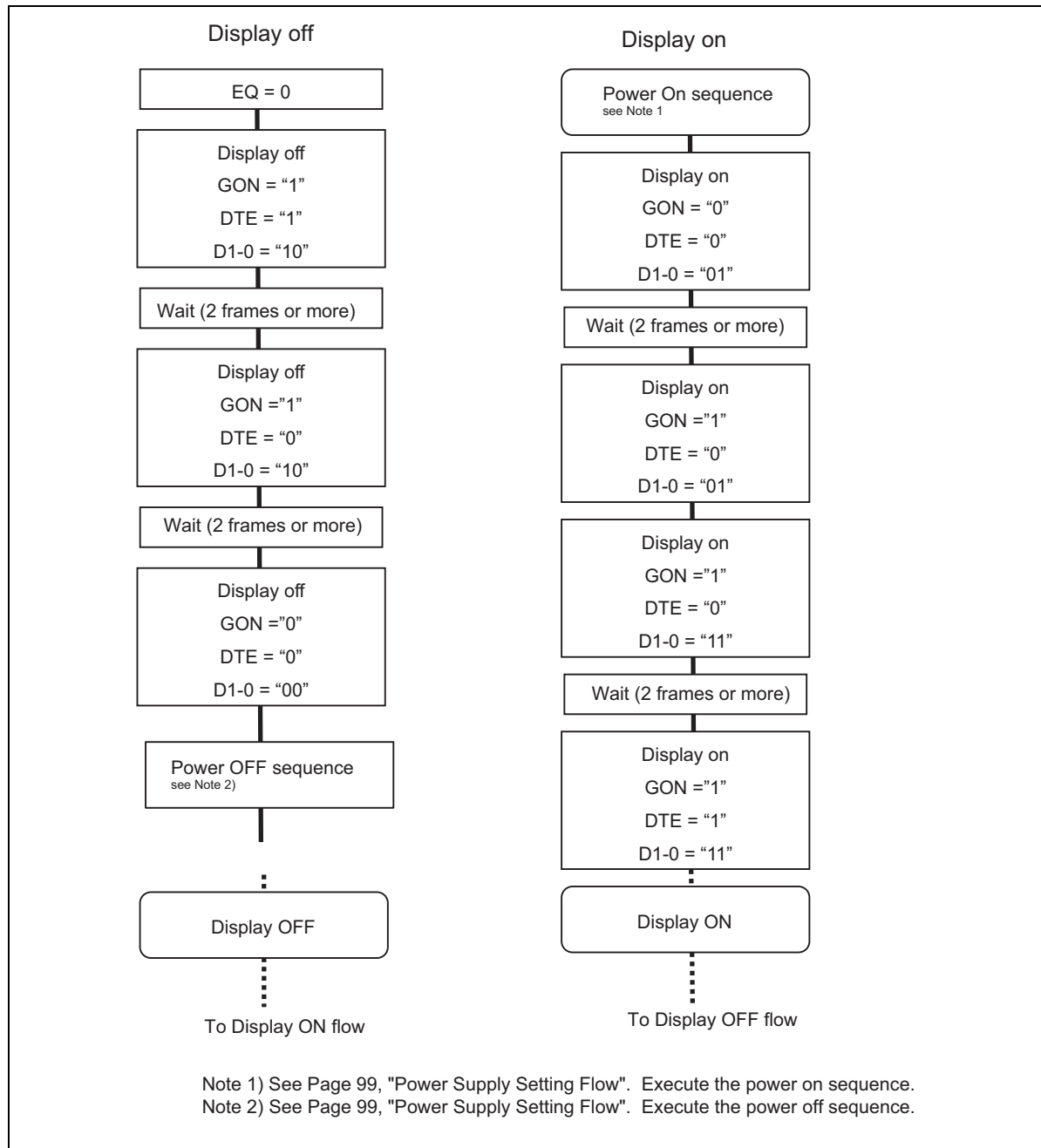
To switch between the 262, 144-color mode and the 8-color mode, make settings according to the following sequences.



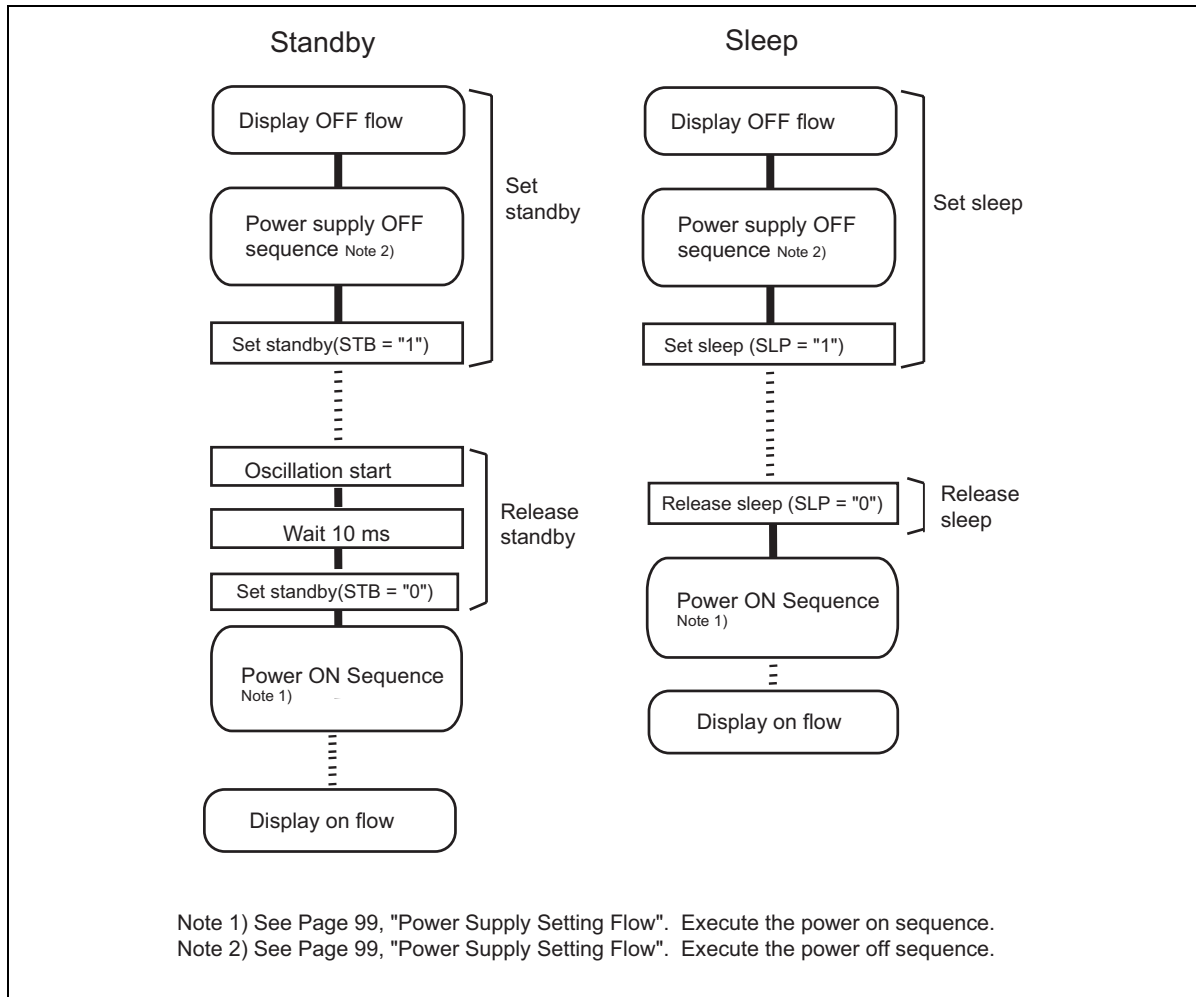
Instruction Setting Flow

Make the setting for each instruction according to the following sequence.

Display ON/OFF



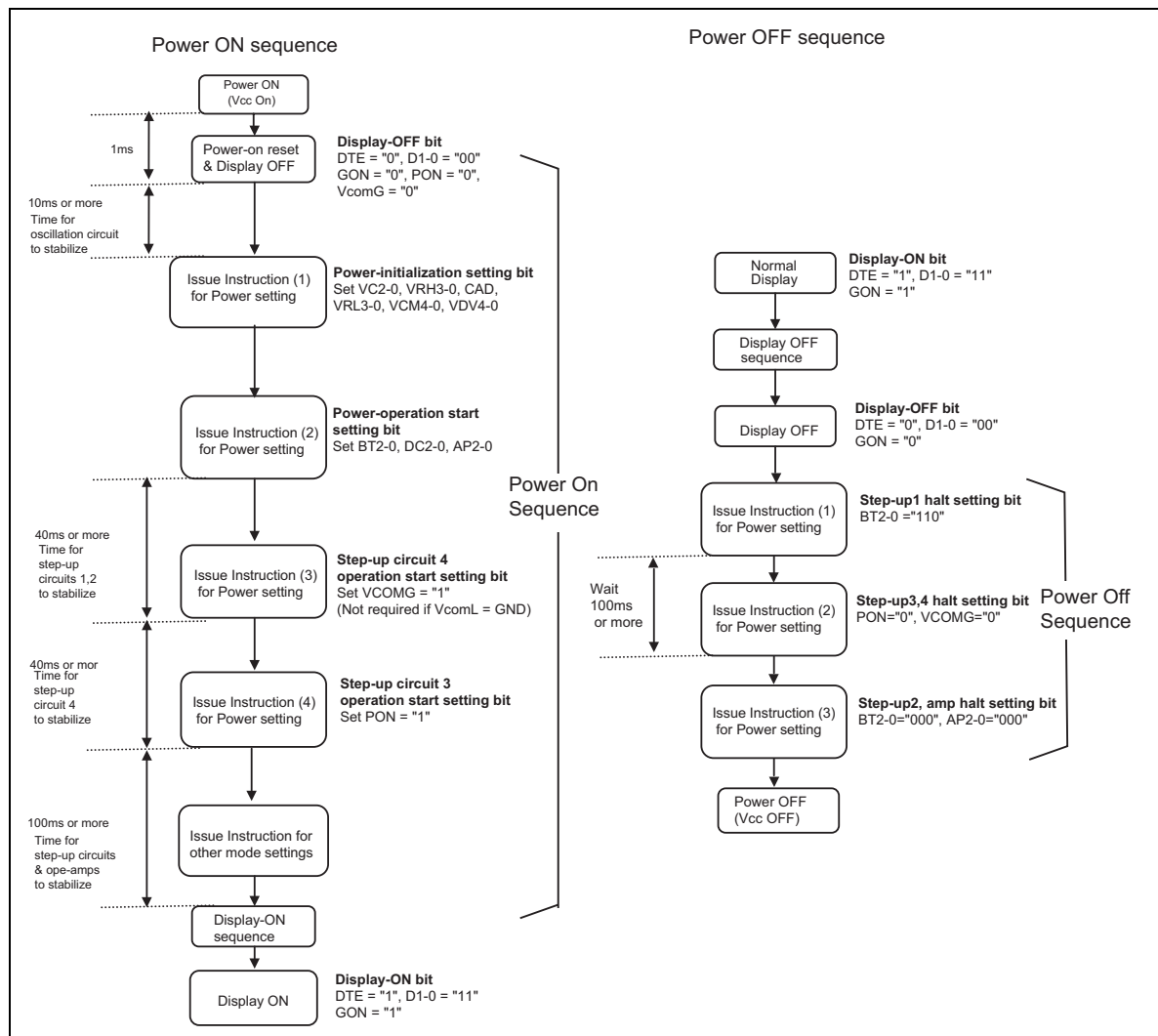
Standby and Sleep



Power Supply Setting Flow

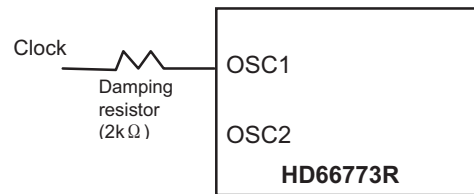
When turning on the power supply, follow the sequence below.

The stabilization time for the oscillation circuits, step-up circuits, and operation amplifiers may vary depending on the external resistors and capacitors.

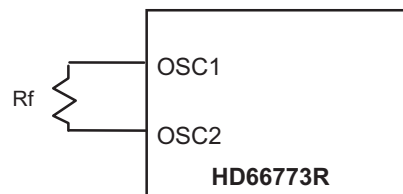


Oscillation Circuit

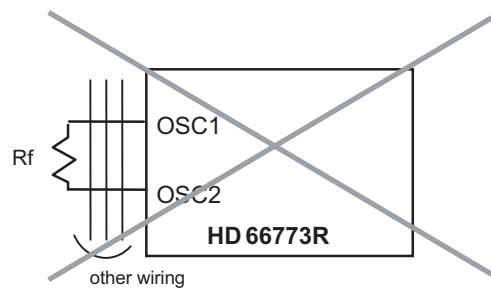
1) External clock mode



2) External resistor oscillation mode



Place the R_f resistor as close as possible to the OSC1, OSC2 pins

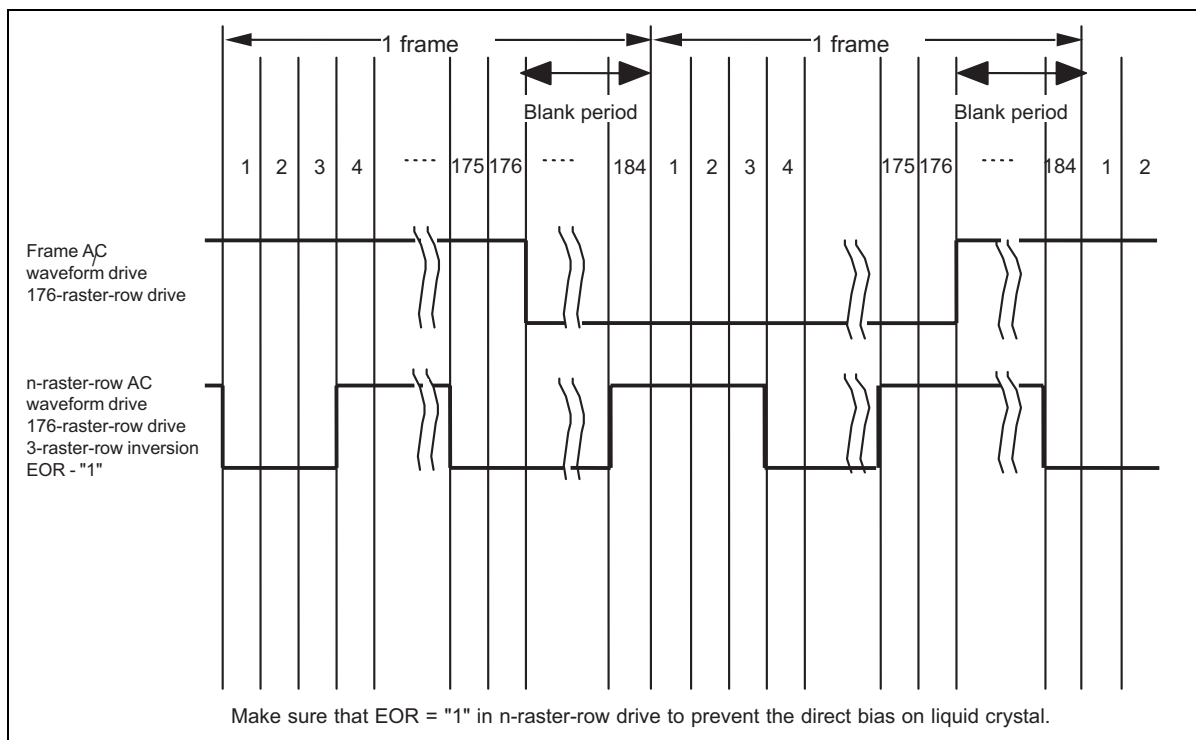


Place the R_f oscillation resistor as close as possible to the OSC1, OSC2 pins.
Do not arrange other wiring beneath OSC1-OSC2 wiring to avoid effects from coupling.

n-raster-row Inversion AC Drive

The HD66773R, in addition to LCD inversion AC drive by frame, supports n-raster-row inversion AC drive where alternation occurs by n raster-rows, where n takes a number between 1 to 64. The n-raster-row inversion AC drive allows overcoming the problems related to display quality.

In determining n (the value set in the NW bit +1), the number of raster-rows by which alternation occurs, check the display quality on the actual liquid crystal panel. Setting a small number of raster-rows will raise the AC frequency of the liquid crystal and increase the charge/discharge current on the liquid crystal cells.



Interlaced Drive

The HD66773R supports interlaced drive, which divide one frame into n fields and then drive to prevent flickers.

To determine the number of fields (n: value set in the FLD bits), check the display quality on the actual liquid crystal panel. The following table shows the gate selection for each number of fields, 1 to 3. The figure illustrates the output waveforms of the 3-field interlaced drive.

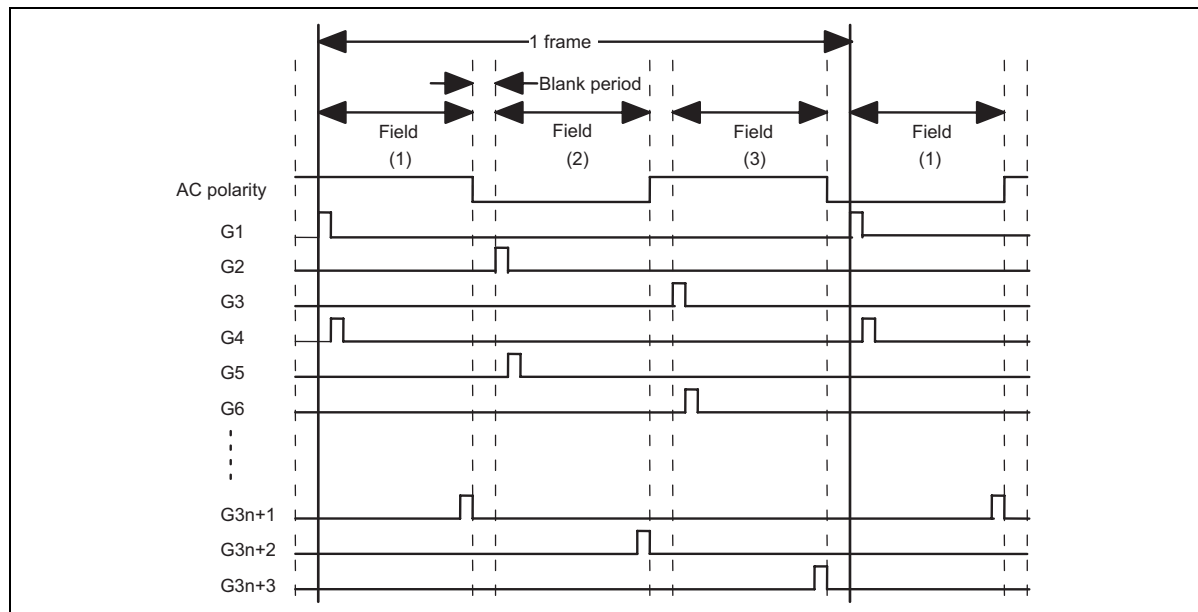
Gate selection

GS = 0

FLD1-0	01	11
Field	-	1 2 3
Gate		
G1	O	O
G2	O	O
G3	O	O
G4	O	O
G5	O	O
G6	O	O
G7	O	O
G8	O	O
G9	O	O
•	•	•
•	•	•
•	•	•
G173	O	O
G174	O	O
G175	O	O
G176	O	O

GS = 1

FLD1-0	01	11
Field	-	1 2 3
Gate		
G176	O	O
G175	O	O
G174	O	O
G173	O	O
G172	O	O
G171	O	O
G170	O	O
G169	O	O
G168	O	O
•	•	•
•	•	•
•	•	•
G4	O	O
G3	O	O
G2	O	O
G1	O	O

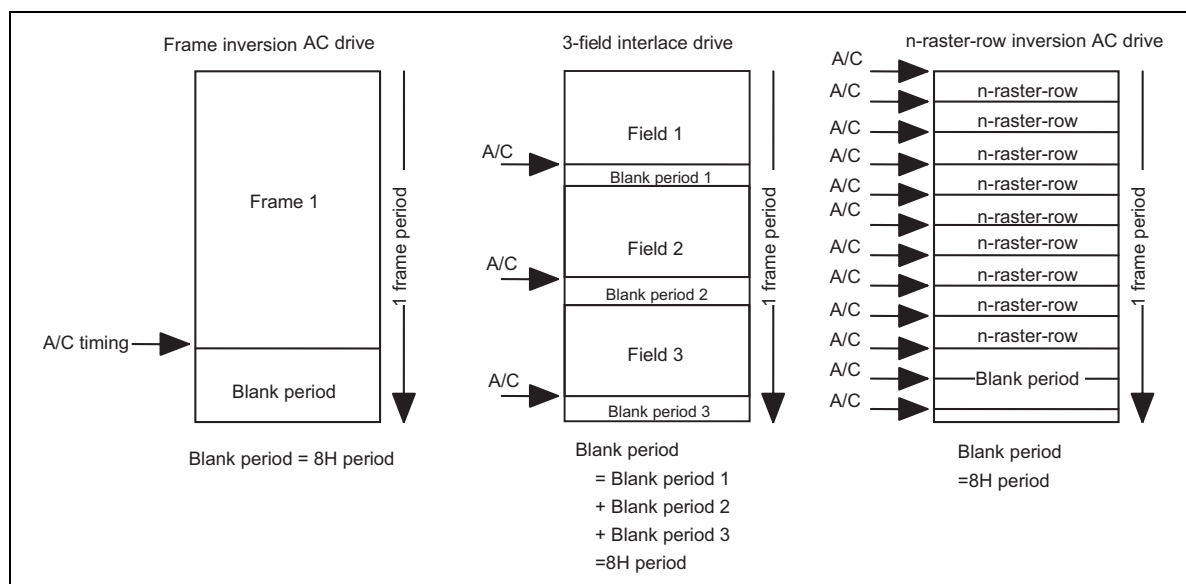


Gate output timing during 3-field interlaced drive

AC Timing

The AC timings of frame inversion AC drive, 3-field interlaced drive, and n-raster-row inversion drive are illustrated as follows. In case of frame inversion AC drive, alternation occurs at the completion of drawing one frame, followed by a blank, which lasts for 16H periods. AC Timing

The AC timings of frame inversion AC drive, 3-field interlaced drive, and n-raster-row inversion drive are illustrated as follows. In case of frame inversion AC drive, alternation occurs at the completion of drawing one frame, followed by a blank, which lasts for 8H periods. In this case, all the outputs from the gate are Vgoff outputs. In case of interlaced drive, alternation occurs at the completion of drawing one field, followed by a blank. The total period of the blanks in one frame amounts to 8 period. In case of n-raster-row, a blank lasting 8H period is inserted after drawing a full screen.



Frame-Frequency Adjustment Function

The HD66773R incorporates frame frequency adjustment function. The frame frequency during the liquid crystal drive is adjusted by the instruction setting (DIV, RTN) while keeping the oscillation frequency fixed.

Setting the oscillation frequency high in advance allows switching the frame frequency in accordance to the kind of picture to be displayed (i.e. moving/still picture). When displaying a still picture, set the frame frequency low to save power consumption, while setting the frame frequency high for displaying a moving picture which requires high-speed switching of screens.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated by the following formula. The frame frequency is adjusted through instruction setting with the 1-H period adjustment bit (RTN bit) and the operation clock division bit (DIV bit).

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{f_{\text{osc}}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times (\text{Line} + 8)} \quad [\text{Hz}]$$

f_{osc} : R-C oscillation frequency
 Line: number of drive raster-rows (NL bit)
 Clock cycles per raster-row: RTN bit
 Division ratio: DIV bit

Calculation Example The maximum frame frequency = 60 Hz

Number of drive raster-rows: 176

1-H period: 16 clock cycles (RTN3-0 = 0000)

Operation clock division ratio: 1 division

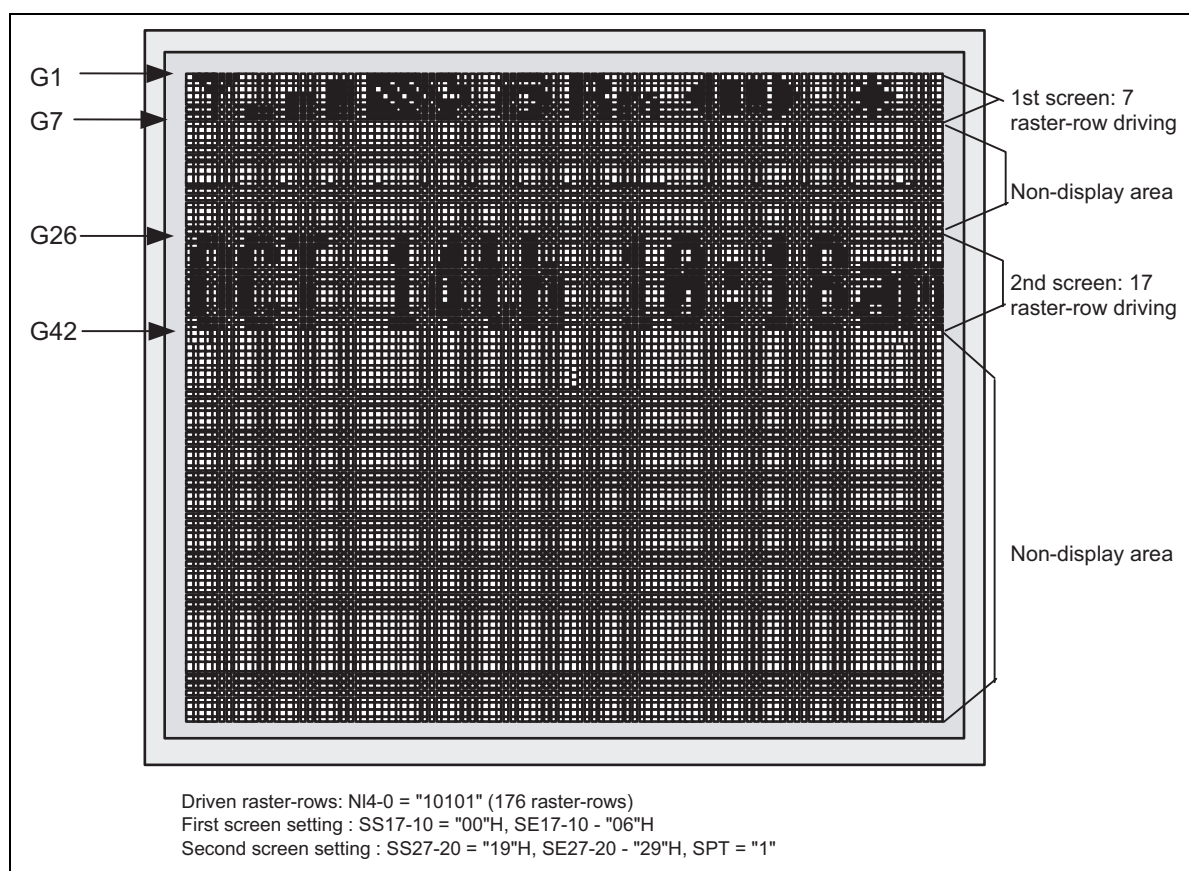
$$f_{\text{osc}} = 60 \text{ Hz} \times (0 + 16) \text{ clock} \times 1 \text{ division} \times (176 + 8) \text{ lines} = 177 \text{ (kHz)}$$

In this case, the R-C oscillation frequency becomes 177 kHz. Adjust the resistance of external resistor for the R-C oscillator to 177 kHz.

Screen -split Drive Function

The HD66773R allows selectively driving two screens at arbitrary positions with the screen-drive position registers (R42 and R43). Only the raster-rows required to display two screens at arbitrary positions are selectively driven to reduce power consumption.

The first screen drive position register (R42) specifies the start line (SS17-10) and the end line (SE17-10) for displaying the first screen. The second screen drive position register (R43) specifies the start line (SS27-20) and the end line (SE27-20) for displaying the second screen. The second screen control is effective when the SPT bit is set to 1. The total number of raster-rows driven for displaying the first and second screens must be less than the number of liquid crystal drive raster-rows.



Conditions on Setting the 1st/2nd Screen Drive Position Register

When making settings for the start line (SS17-10) and end line (SE17-10) of the first screen drive position register (R42), and the start line (SS27-20) and end line (SE27-20) of the second screen drive position register (R43) with the HD66773R, it is necessary to satisfy the following conditions to display screens correctly.

One-screen Drive (SPT = 0)

Register Settings	Display Operation
$(SE17-10) - (SS17-10) = NL$	Full screen display The area of $(SE17-10) - (SS17-10)$ is normally displayed.
$(SE17-10) - (SS17-10) < NL$	Partial screen display The area of $(SE17-10) - (SS17-10)$ is normally displayed. The rest of the area is white display irrespective of data in RAM.
$(SE17-10) - (SS17-10) > NL$	Setting disabled

Note 1) $SS17-10 \leq SE17-0 \leq "AF"H$
 Note 2) Setting disabled for SS27-20 and SE27-20.

Two-screen Drive (SPT = 1)

Register Settings	Display Operation
$((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) = NL$	Full screen display The area of $(SE27-20) - (SS17-10)$ is normally displayed.
$((SE17-10) - (SS17-10)) + ((SE27-20) - (S27-20)) < NL$	Partial screen display The area of $(SE27-10) - (SS17-10)$ is normally displayed. The rest of the area is white display irrespective of data in RAM.
$((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) > NL$	Setting disabled

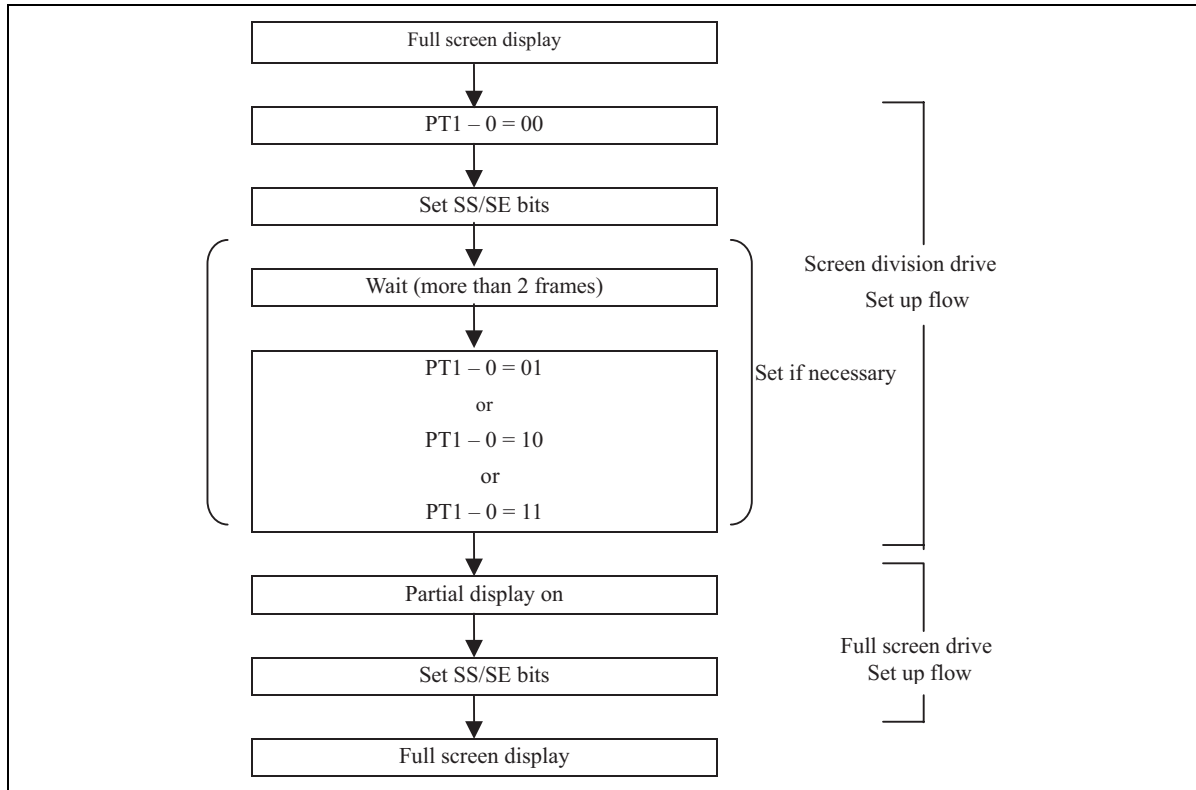
Note 1) Make sure that $SS17-10 \leq SE17-10 < SS27-20 \leq SE27-20 \leq "AF"H$.
 Note 2) Make sure that $((SE27-20) - (SS17-10)) \leq NL$.

The setting for the driver output in the non-display area during the partial display is changeable according to the characteristics of the display panel.

Source outputs in non-display area

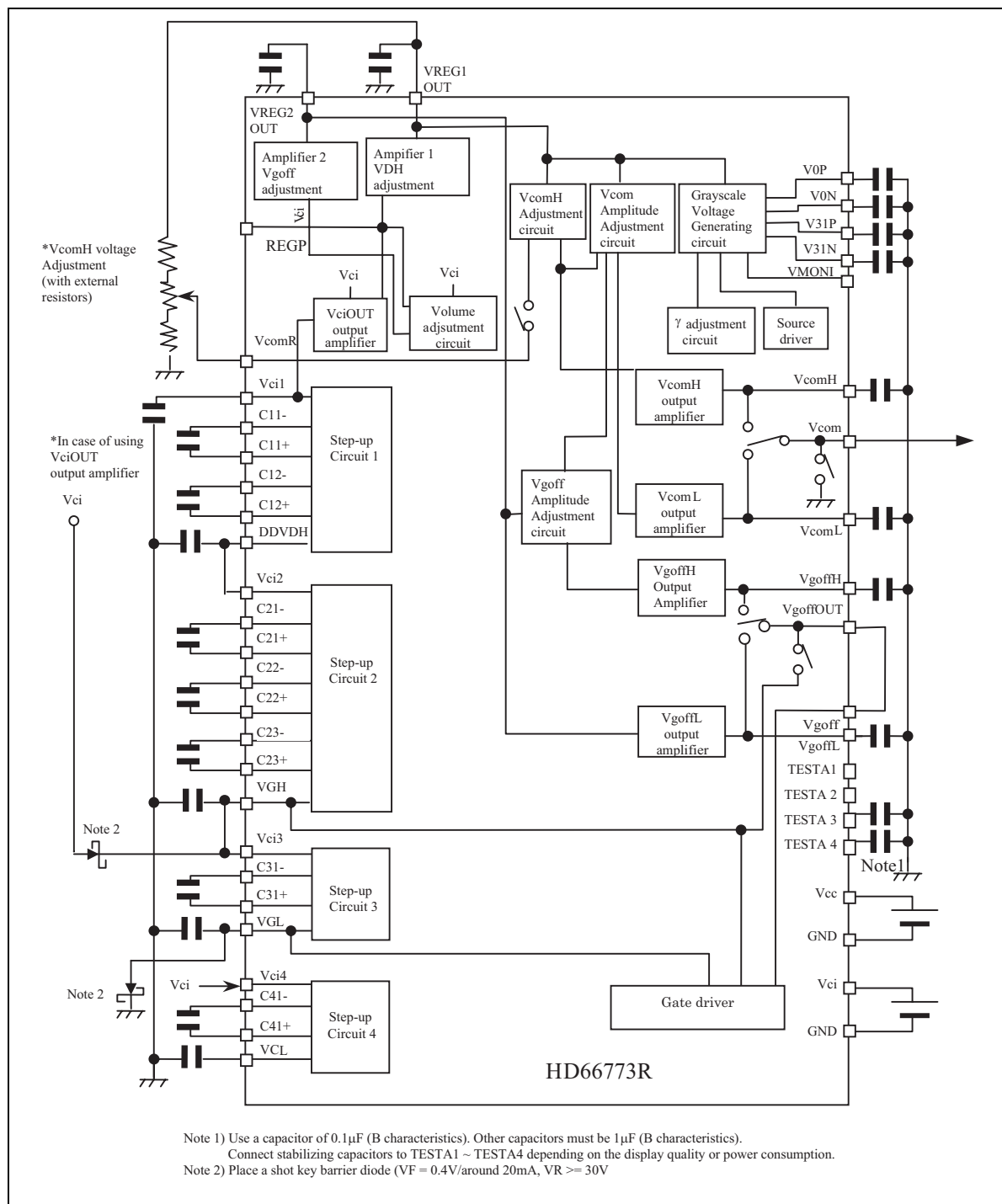
PT1	PT0	Source Output for Non-display Area		Source Output for Non-display Area
		Positive Polarity	Negative Polarity	
0	0	V31	V0	Normal drive
0	1	V31	V0	Vgoff
1	0	GND	GND	Vgoff
1	1	High-Z	High-Z	Vgoff

To make a setting for the partial display, follow the sequence below.



Internal Configuration of Power Generation Circuit

The internal configuration of power generation circuit of HD66773R is as follows. The step-up circuit is comprised of the step-up circuit 1 which boost 2 to 3 times the voltage supplied with V_{ci1} , the step-up circuit 2 which further boost 2 to 4 times the voltage boosted by the step-up circuit 1, the step-up circuit 3 which invert the VGH-level voltage with the GND level as the axis and output the VGL-level voltage, and the step-up circuit 4 which invert the V_{ci} -level voltage with the GND level as the axis and output the VCL-level voltage. The step-up circuit generates the voltage to drive a TFT LCD. Reference voltage V_{DH} , V_{com} and V_{goff} for the grayscale voltage are generated either by being adjusted in the internal voltage adjustment circuit or from the voltage at REGP, which is amplified in the amplifiers 1, 2. The V_{com} , V_{goff} voltages can alternate at an arbitrary voltage level. V_{com} must be connected to the panel.



Internal configuration of power supply circuit

Specification of External Elements Connected to HD66773R

The following table shows specifications of external elements connected to HD66773R power supply.

Capacitor

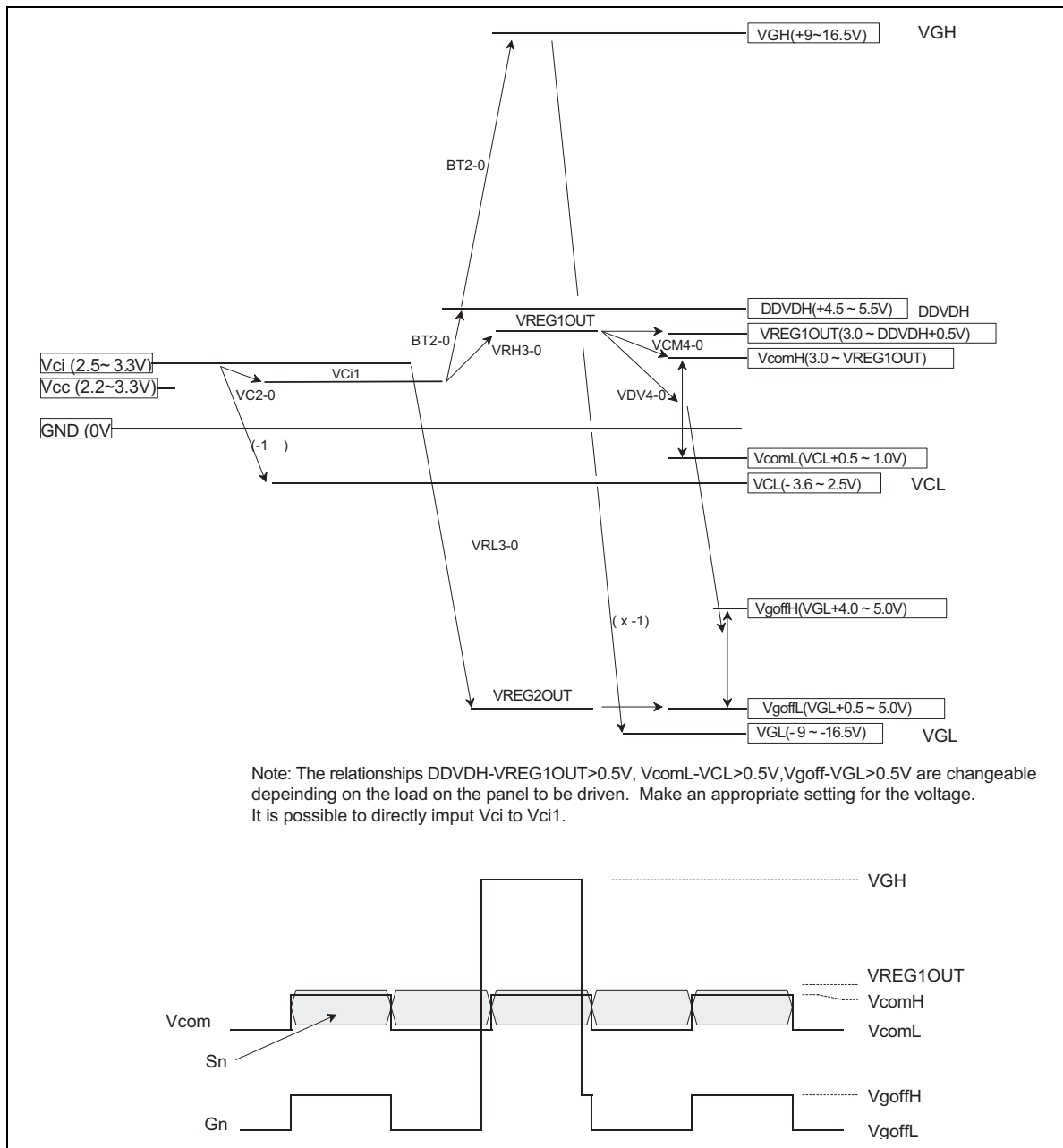
Capacity	Recommended voltage	Connect pins
1 μ F (B characteristic)	6V	VREG1OUT, Vci1, C41-/+ ^{Note 1)} , VCL ^{Note 1)} , VcomH, VcomL ^{Note 1)}
	10V	DDVDH, C11+/-, C12+/-, C21+/-, C22+/-, C23+/-
	25V	VREG2OUT, VGH, VGL, C31-/+ , VgoffH ^{Note 1)} , VgoffL
0.1 μ F (B characteristic)	25V	(TESTA3) ^{Note 2)}
0.1 μ F (B characteristic)	6V	V0P, V0N, V31P, V31N, (TESTA4) ^{Note 2)}

Note 1) These pins may not be required for some mode setting.

Note 2) Connect to a stabilizing capacitor depending on the display quality or power consumption.

Pattern Diagram for Voltage Setting

The following figures are the pattern diagram of voltage setting for the HD66733R and the voltage waveforms.



Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	Vcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci - GND	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (3)	DDVDH - GND	V	-0.3 ~ + 6.0	1, 2
Power supply voltage (4)	GND -VCL	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (5)	DDVDH - VCL	V	-0.3 ~ + 9.0	1
Power supply voltage (6)	VGH - GND	V	-0.3 ~ + 18.5	1, 2
Power supply voltage (7)	GND - VGL	V	-0.3 ~ + 18.5	1, 2
Input voltage	Vt	V	-0.3 ~ Vcc + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 3
Storage temperature	Tstg	°C	-55 ~ + 110	1

Note 1) The LSI may be permanently damaged if it is used under the condition exceeding the above absolute maximum ratings. It is also recommended to use the LSI within the limit of its electric characteristics during normal operation. Exceeding the conditions may lead to malfunction of LSI and affect its credibility.

Note 2) The voltage from GND.

Note 3) The DC and AC characteristics of chip and wafer products are guaranteed at 85 °C.

Electric Characteristics

DC Characteristics

($V_{CC} = 1.8$ to 3.7 V, $T_a = -40 \sim +85^\circ\text{C}$ ^{Note 1})

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	$V_{CC} = 2.2$ to 3.3 V	$0.7 V_{CC}$	—	V_{CC}	2, 3
Input low voltage (1) (OSC1 pin)	V_{IL1}	V	$V_{CC} = 2.2$ to 3.3 V	-0.3	—	$0.15V_{CC}$	2, 3
Input low voltage (2) (Except OSC1 pin)	V_{IL2}	V	$V_{CC} = 2.2$ to 2.4 V	-0.3	—	$0.15V_{CC}$	2, 3
			$V_{CC} = 2.4$ to 3.3 V	-0.3	—	$0.2 V_{CC}$	2, 3
Output high voltage (1) (DB0-17 pins)	V_{OH1}	V	$I_{OH} = -0.1\text{mA}$	$-0.75V_{CC}$	—	—	2
Output low voltage (1) (DB0-17 pins)	V_{OL1}	V	$V_{CC} = 2.2\text{V}$ to 2.4V , $I_{OL} = 0.1\text{mA}$	—	—	$0.2V_{CC}$	2
			$V_{CC} = 2.4\text{V}$ to 3.3V , $I_{OL} = 0.1\text{mA}$	—	—	$0.15V_{CC}$	2
I/O leakage current	I_{LI}	μA	$V_{in} = 0$ to V_{CC}	-1	—	1	4
Current consumption during normal operation ($V_{CC} - \text{GND}$)	I_{OP}	μA	$T_a = 25^\circ\text{C}$, 260,000 colors display, $V_{CC} = 3\text{V}$, CR oscillation; $f_{osc} = 176\text{kHz}$ (176 line drive), RAM data: 0000h, AP=001, CAD=1, VCOMG=1 $V_{CI1} = 0.92 \times V_{CI}$ ($V_{C2-0} =$ 001), $DDVDH = 2 \times V_{CI1}$, V_{GH} $= 3 \times V_{CI2}$ ($BT2-0 = 000$), Step up circuit 1 = 60 divided cycle, Step up circuit 2, 3, and 4 = 240 divided cycle ($DC2-0 =$ 000), $V_{REG1OUT} = \text{REGP} \times$ 1.65 = 4.55V, ($VRH = 0011$) $V_{COMH} = V_{REG1OUT} \times 0.76$ $= 3.46\text{V}$, ($V_{CM} = 10011$), $V_{COML} = 3.46 - (V_{REG1OUT}$ $\times 1.23) = -2.13\text{V}$, ($VDV =$ 10110), $V_{REG2OUT} = V_{CI} \times -$ 5.5 = -16.5V, ($V_{RL} = 1001$), $V_{goffL} = -16.5\text{V}$, $V_{goffH} = -$ 16.5V + 5.59V = -10.9V	—	90	200	5
Current consumption during Normal operation ($V_{ci} - \text{GND}$)	I_{ci}	mA	$V_{goffL} = -16.5\text{V}$, $V_{goffH} = -$ 16.5V + 5.59V = -10.9V	—	1.25	1.5	5
Current consumption during Standby mode ($V_{CC} - \text{GND}$)	I_{ST}	μA	$V_{CC} = 3\text{V}$, $T_a \leq 50^\circ\text{C}$	—	0.1	5	5
			$V_{CC} = 3\text{V}$, $T_a > 50^\circ\text{C}$	—	—	20	
Output voltage difference	ΔV_o	mV	—	—	5	—	6
Average output voltage fluctuation	ΔV	mV	—	—	—	35	7

HD66773R

AC Characteristics

($V_{CC} = 2.2$ to 3.3 V, $T_a = -40$ to $+85^{\circ}\text{C}^{*1}$)

Clock Characteristics ($V_{CC} = 2.2$ to 3.3 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock frequency	Fcp	kHz	$V_{CC} = 2.2$ to 3.3 V	100	176	600	8
External clock duty ratio	Duty	%	$V_{CC} = 2.2$ to 3.3 V	45	50	55	8
External clock rise time	Trcp	μs	$V_{CC} = 2.2$ to 3.3 V	—	—	0.2	8
External clock fall time	Tfcp	μs	$V_{CC} = 2.2$ to 3.3 V	—	—	0.2	8
R-C oscillation clock	f _{osc}	kHz	Rf = 240k Ω , $V_{CC} = 3$ V	184	229	274	9

68system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0) (V_{CC} = 2.2 to 2.4 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	600	—	—
	Read		ns	Figure 1	800	—	—
Enable "High" level pulse width	Write	PW_{EH}	ns	Figure 1	90	—	—
	Read				350	—	—
Enable "Low" level pulse width	Write	PW_{EL}	ns	Figure 1	300	—	—
	Read				400	—	—
Inable rising and falling time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W, to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—
Address hold time		t_{AHE}	ns	Figure 1	5	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t_{HE}	ns	Figure 1	15	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—

High-Speed Write Mode (HWM=1) (V_{CC} = 2.2 to 2.4 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	200	—	—
	Read		ns	Figure 1	800	—	—
Enable "High" level pulse width	Write	PW_{EH}	ns	Figure 1	90	—	—
	Read				350	—	—
Enable "Low" level pulse width	Write	PW_{EL}	ns	Figure 1	90	—	—
	Read				400	—	—
Inable rising and falling time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W, to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—
Address hold time		t_{AHE}	ns	Figure 1	5	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t_{HE}	ns	Figure 1	15	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—

HD66773R**Normal Write Mode (HWM=0) (Vcc = 2.4 to 3.3 V)**

Item		Symbol	Unit	Timing diagram	Min	Typ	Max	Note
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	200	—	—	—
	Read		ns	Figure 1	300	—	—	—
Enable "High" level pulse width	Write	PW_{EH}	ns	Figure 1	40	—	—	—
	Read				150	—	—	—
Enable "Low" level pulse width	Write	PW_{EL}	ns	Figure 1	100	—	—	—
	Read				100	—	—	—
Inable rising and falling time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25	
Set up time (RS, R/W, to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—	with status read
					0	—	—	without status read
Address hold time		t_{AHE}	ns	Figure 1	2	—	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—	—
Write data hold time		t_{HE}	ns	Figure 1	2	—	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	100	—
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—	—

High-Speed Write Mode (HWM=1) (Vcc = 2.4 to 3.3 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max	Note
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	100	—	—	
	Read		ns	Figure 1	300	—	—	
Enable "High" level pulse width	Write	PW_{EH}	ns	Figure 1	40	—	—	
	Read			Figure 1	150	—	—	
Enable "Low" level pulse width	Write	PW_{EL}	ns	Figure 1	40	—	—	
	Read			Figure 1	100	—	—	
Inable rising and falling time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25	
Set up time (RS, R/W, to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—	with status read
					0			without status read
Address hold time		t_{AHE}	ns	Figure 1	2	—	—	
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—	
Write data hold time		t_{HE}	ns	Figure 1	2	—	—	
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	100	
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—	

80-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0) (Vcc = 2.2 to 2.4 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	600	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	300	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRf, WRf}$	ns	Figure 2	—	—	25
Setup time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_{HWR}	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

High-Speed Write Mode (HWM=1) (Vcc = 2.2 to 2.4 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	200	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	90	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRf, WRf}$	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_{HWR}	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

HD66773R**Normal Write Mode (HWM=0) (Vcc = 2.4 to 3.3 V)**

Item		Symbol	Unit	Timing diagram	Min	Typ	Max	Notes
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	200	—	—	
	Read	t_{CYCR}	ns	Figure 2	300	—	—	
Write low-level pulse width		PW_{LW}	ns	Figure 2	40	—	—	
Read low-level pulse width		PW_{LR}	ns	Figure 2	150	—	—	
Write high-level pulse width		PW_{HW}	ns	Figure 2	100	—	—	
Read high-level pulse width		PW_{HR}	ns	Figure 2	100	—	—	
Write/Read rise/fall time		$t_{WRf, WRr}$	ns	Figure 2	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—	with status read
				Figure 2	0	—	—	without status read
Address hold time		t_{AH}	ns	Figure 2	2	—	—	
Write data setup time		t_{DSW}	ns	Figure 2	60	—	—	
Write data hold time		t_{HWR}	ns	Figure 2	2	—	—	
Read data delay time		t_{DDR}	ns	Figure 2	—	—	100	
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—	

High-Speed Write Mode (HWM=1) (Vcc = 2.4 to 3.3 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max	Notes
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	100	—	—	
	Read	t_{CYCR}	ns	Figure 2	300	—	—	
Write low-level pulse width		PW_{LW}	ns	Figure 2	40	—	—	
Read low-level pulse width		PW_{LR}	ns	Figure 2	150	—	—	
Write high -level pulse width		PW_{HW}	ns	Figure 2	40	—	—	
Read high -level pulse width		PW_{HR}	ns	Figure 2	100	—	—	
Write/Read rise/fall time		$t_{WRf, WRr}$	ns	Figure 2	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—	with status read
				Figure 2	0	—	—	without status read
Address hold time		t_{AH}	ns	Figure 2	2	—	—	
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—	
Write data hold time		t_{HWR}	ns	Figure 2	2	—	—	
Read data delay time		t_{DDR}	ns	Figure 2	—	—	100	
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—	

HD66773R

Serial Peripheral Interface timing characteristics

(V_{CC} = 2.2V to 2.4V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Serial clock cycle time	Write (received)	t _{SCYC}	us	Figure 3	0.1	—	20
	Read (transmitted)	t _{SCYC}	us	Figure 3	0.25	—	20
Serial clock hith-level pulse width	Write (received)	t _{SCH}	ns	Figure 3	40	—	—
	Read (transmitted)	t _{SCH}	ns	Figure 3	120	—	—
Serial clock low-level pulse width	Write (received)	t _{SCL}	ns	Figure 3	40	—	—
	Read (transmitted)	t _{SCL}	ns	Figure 3	120	—	—
Serial clock rise/fall time		t _{scr} , t _{scf}	ns	Figure 3	—	—	20
Chip select set up time		t _{CSU}	ns	Figure 3	20	—	—
Chip select hold time		t _{CH}	ns	Figure 3	60	—	—
Serial input data set up time		t _{SISU}	ns	Figure 3	30	—	—
Serial input data hold time		t _{SIH}	ns	Figure 3	30	—	—
Serial output data delay time		t _{SOD}	ns	Figure 3	—	—	130
Serial output data hold time		t _{SOH}	ns	Figure 3	5	—	—

(V_{CC} = 2.4V to 3.3V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Serial clock cycle time	Write (received)	t _{SCYC}	us	Figure 3	0.076	—	20
	Read (transmitted)	t _{SCYC}	us	Figure 3	0.15	—	20
Serial clock hith-level pulse width	Write (received)	t _{SCH}	ns	Figure 3	40	—	—
	Read (transmitted)	t _{SCH}	ns	Figure 3	70	—	—
Serial clock low-level pulse width	Write (received)	t _{SCL}	ns	Figure 3	35	—	—
	Read (transmitted)	t _{SCL}	ns	Figure 3	70	—	—
Serial clock rise/fall time		t _{scr} , t _{scf}	ns	Figure 3	—	—	20
Chip select set up time		t _{CSU}	ns	Figure 3	20	—	—
Chip select hold time		t _{CH}	ns	Figure 3	60	—	—
Serial input data set up time		t _{SISU}	ns	Figure 3	30	—	—
Serial input data hold time		t _{SIH}	ns	Figure 3	30	—	—
Serial output data delay time		t _{SOD}	ns	Figure 3	—	—	130
Serial output data hold time		t _{SOH}	ns	Figure 3	5	—	—

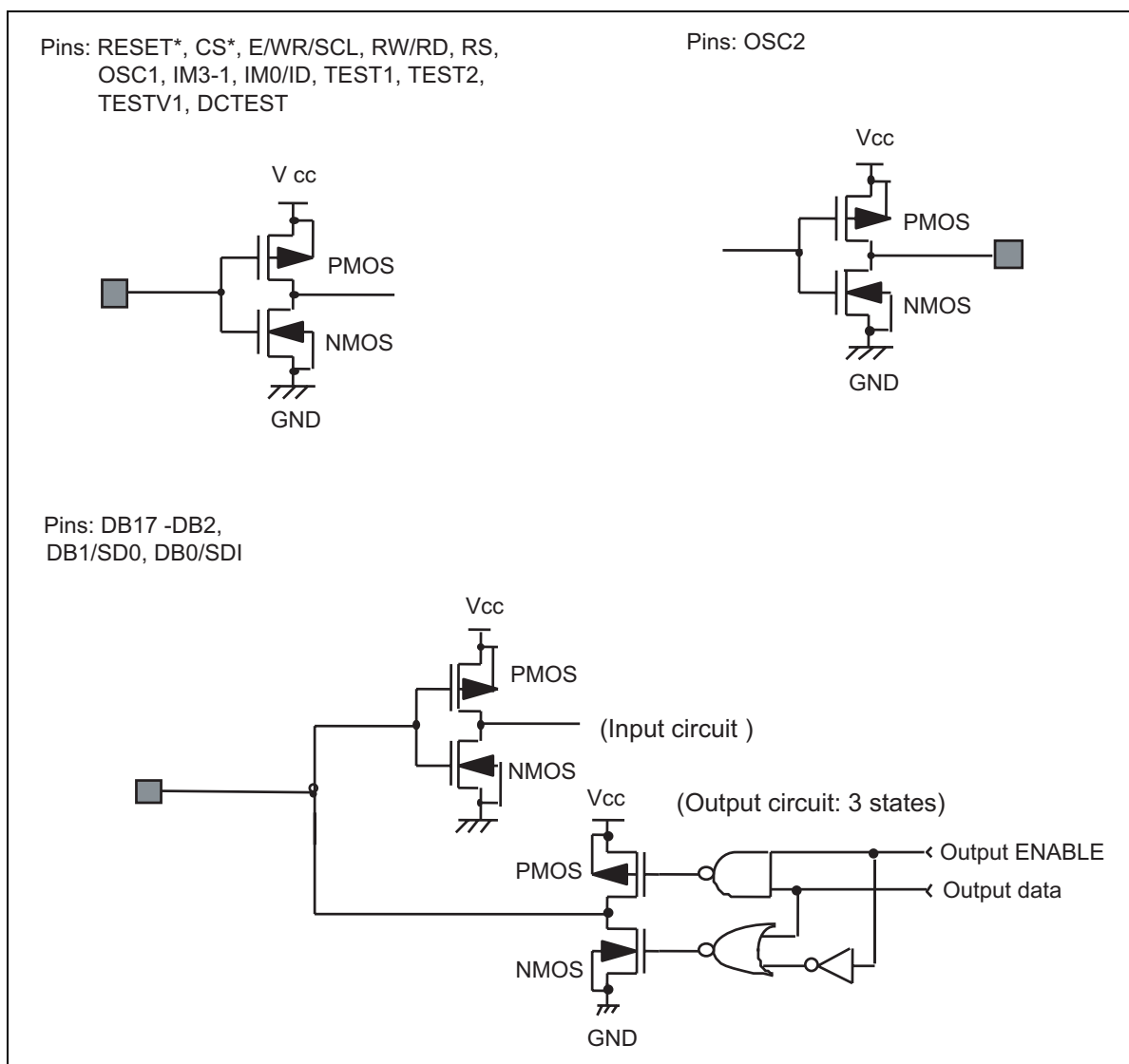
Reset Timing Characteristics

(V_{CC} = 2.2 to 3.3 V)

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset low-level width	t _{RES}	ms	Figure 4	1	—	—
Reset rise time	t _{rRES}	μs	Figure 4	—	—	10

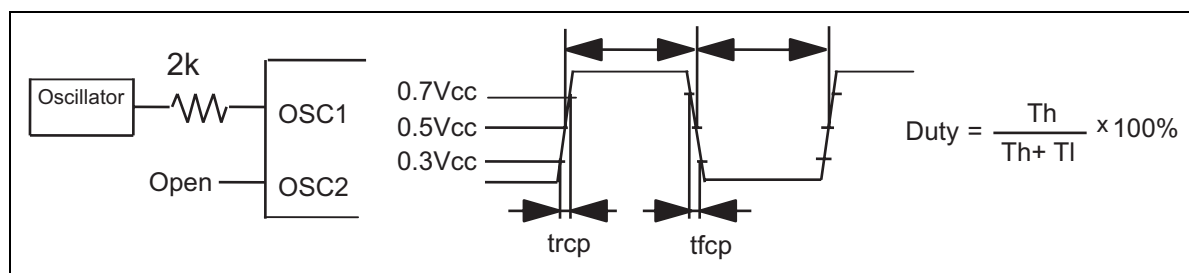
Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following figures illustrate the configurations of I pin, I/O pin, and O pin.

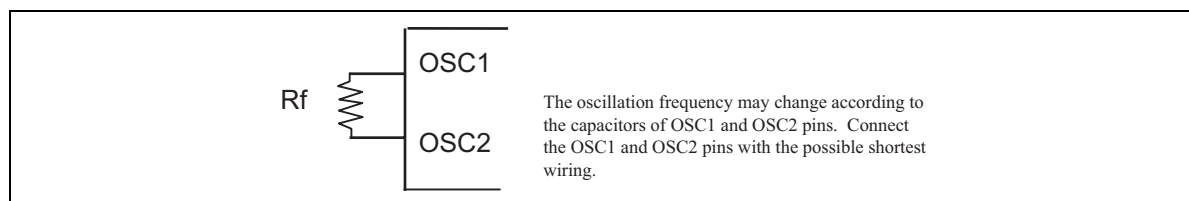


HD66773R

3. TEST, IM1, IM0/ID pins must be grounded or connected to Vcc.
4. This excludes the current through output drive MOS.
5. This excludes the current through the input/output units. The input level must be fixed to a certain level because penetrating current increases in the input circuit when CMOS input level takes a middle level. The current consumption is unchanged irrespective of “High” or “Low” of CS*pin while the HD66773R is not accessed through interface pins.
6. The output voltage difference is the difference in the voltages of neighboring source outputs for a same display (within a chip). This value is just for a referential purpose.
7. The average output voltage fluctuation is the difference in the average source output voltages among different chips. The average output voltage is an average source voltage within a chip for a same display.
8. This applies to the case when clocks are supplied externally.



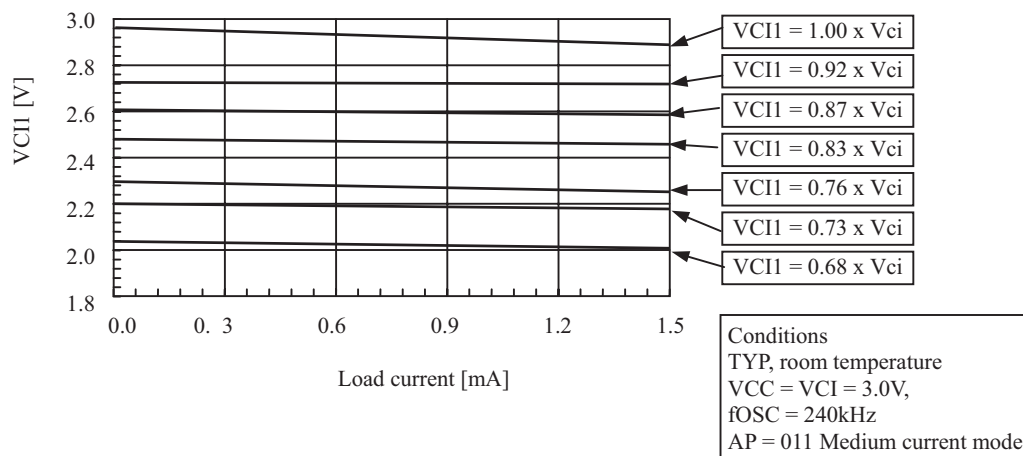
9. This applies to the internal oscillator when external oscillation resistor Rf is used.



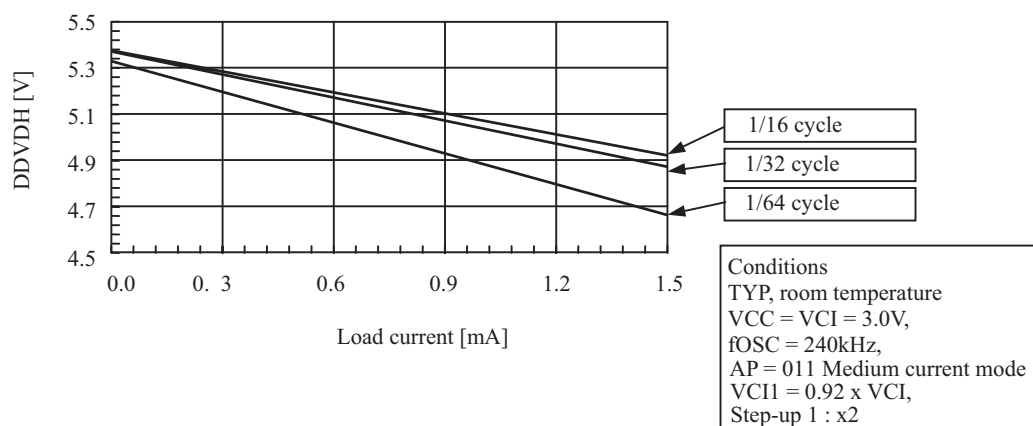
Referential data

Oscillation Resistance (kΩ)	Vcc = 1.8 V	Vcc = 2.0 V	Vcc = 2.4 V	Vcc = 3.0V	Vcc = 3.3V
110k Ω	329.6	362.6	399.4	438.5	447.6
150k Ω	260.7	285.4	313.3	337.4	343.4
180k Ω	230.9	252.2	274.0	294.9	302.1
200 k Ω	213.0	230.4	251.5	268.7	274.8
240 k Ω	187.7	201.3	216.8	229.4	234.8
270 k Ω	168.6	181.3	195.1	206.9	210.2
300 k Ω	154.5	166.1	178.2	187.5	191.1
390 k Ω	125.4	133.7	142.3	148.9	151.6
430 k Ω	115.9	121.6	129.0	135.2	137.3

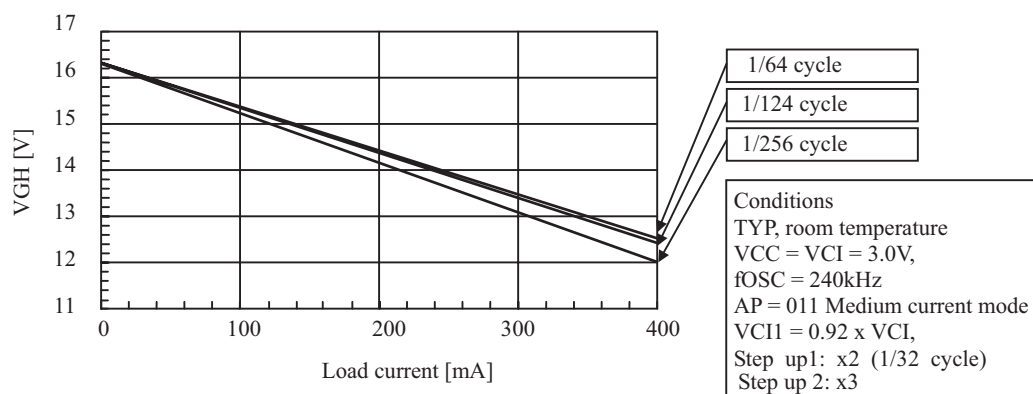
VCI adjustment circuit – Load characteristics



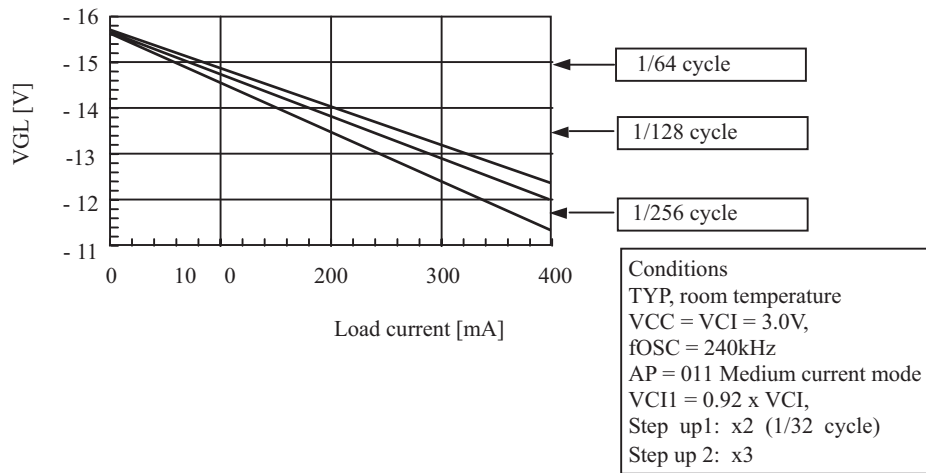
Step- up1 – Load characteristics



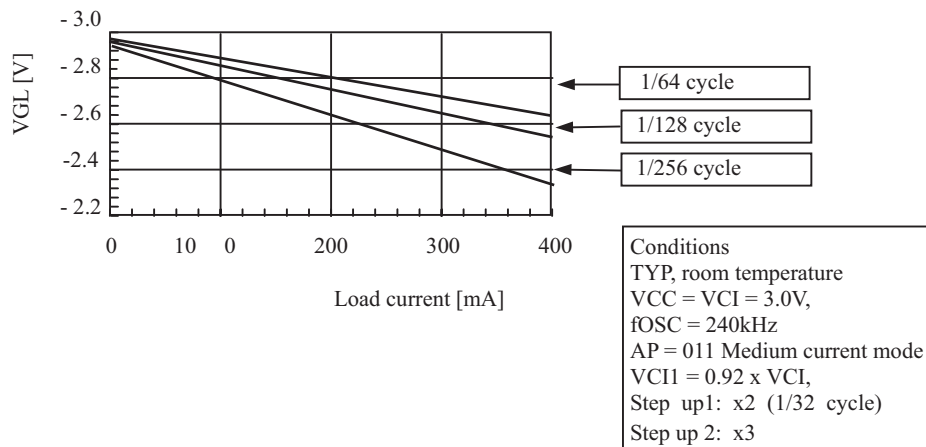
Step- up2 – Load characteristics



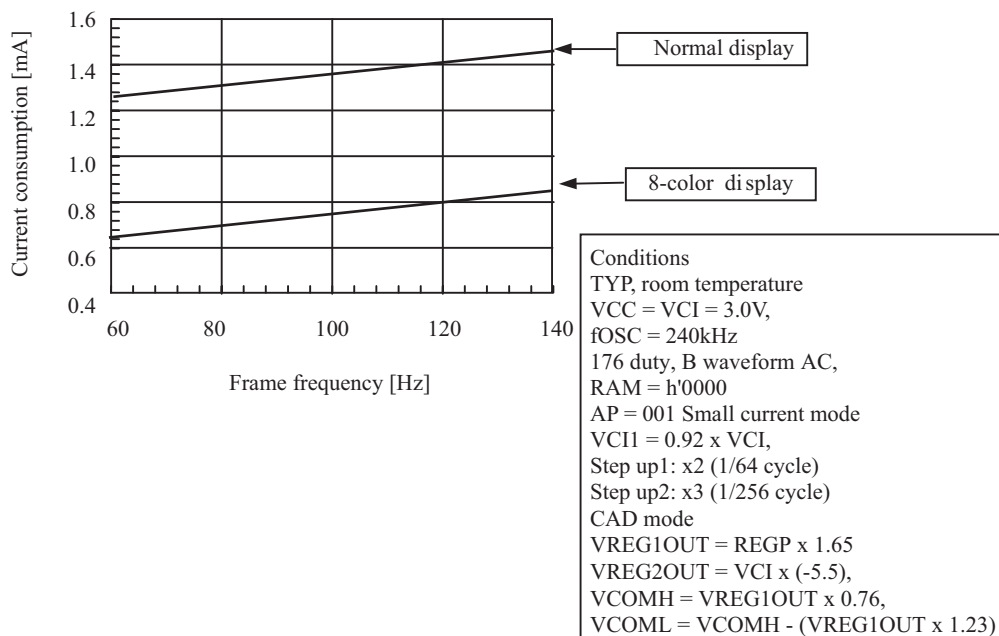
Step-up3 – Load characteristics



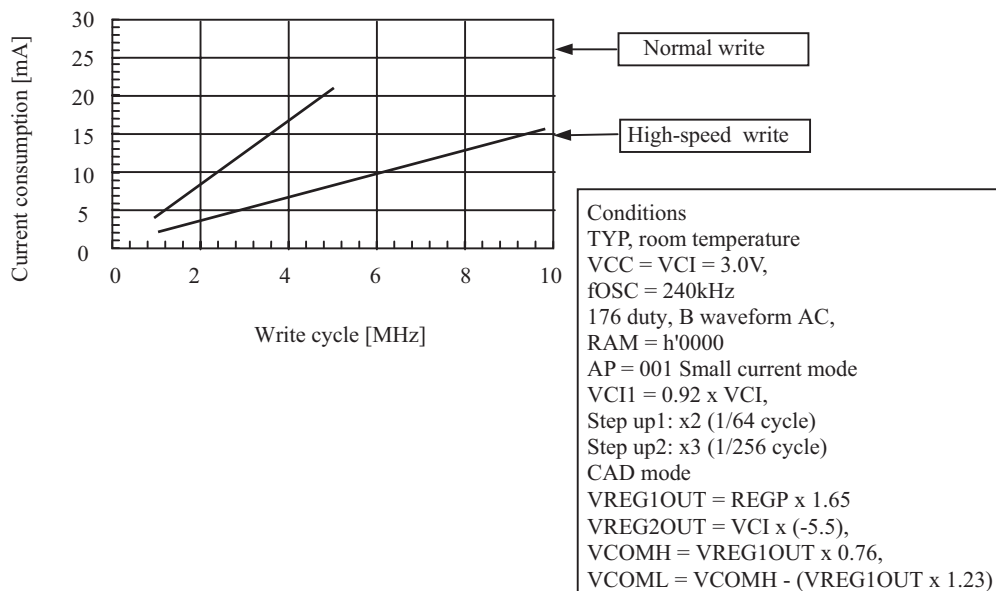
Step-up 4 – Load characteristics

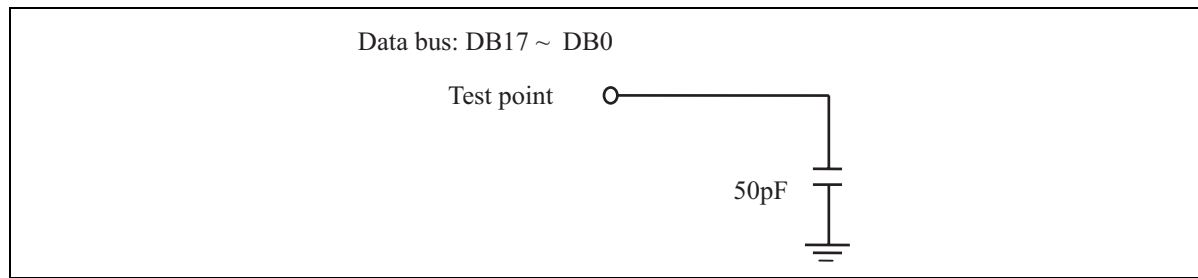


Current consumption - Frame frequency dependence



Current consumption – Write cycle dependency





Load circuit for AC characteristics test

Timing characteristics diagram

68-system bus interface operation

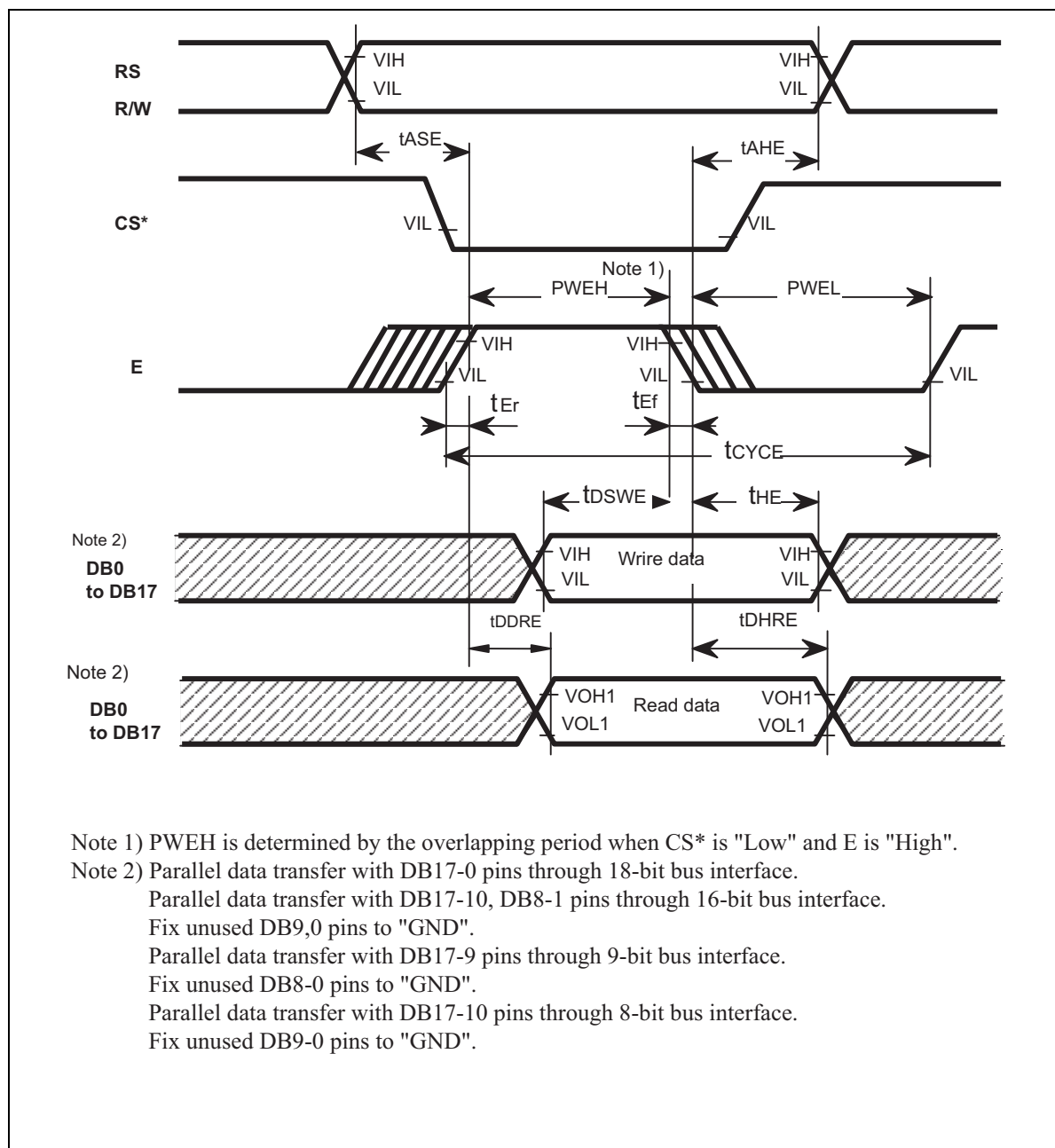


Figure 1

80-system bus interface operation

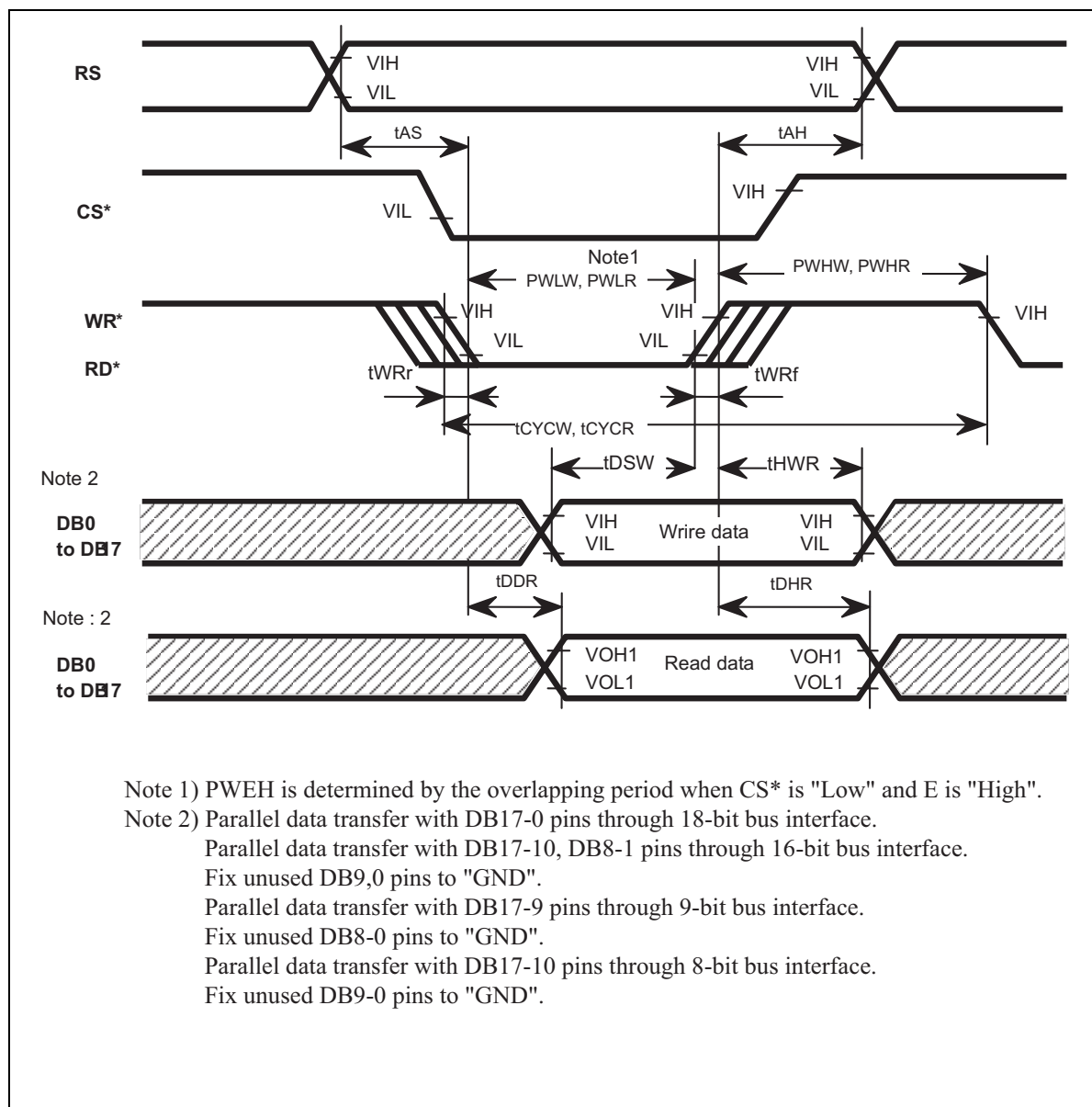


Figure 2

Serial Peripheral Interface Operation

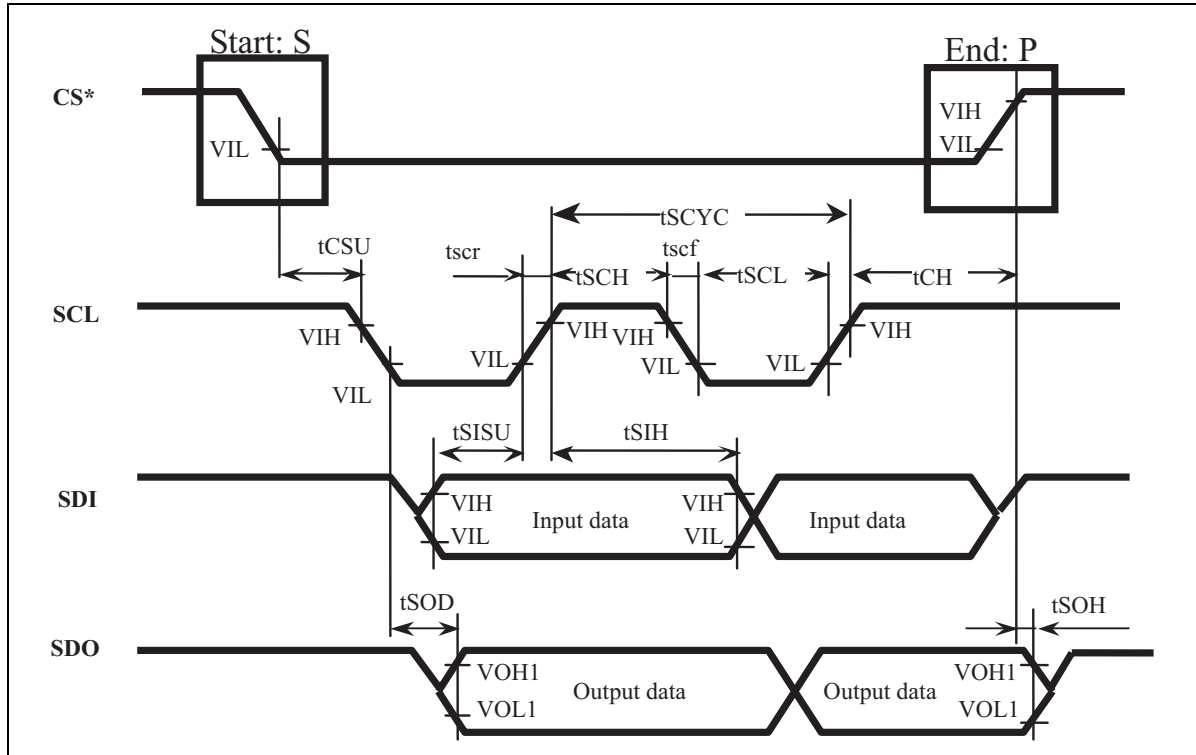


Figure 3

Reset operation

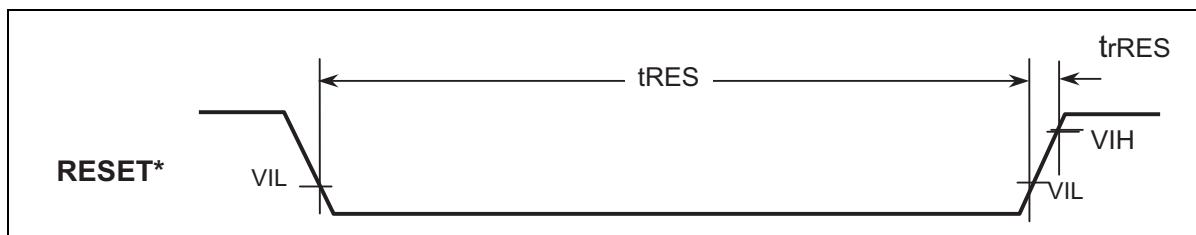


Figure 4

Insert Wiring example

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.01	2003.Jan.	Page 112. Delete "DB1SD0" and "DB0/SD1" in the figure.		
		Page 113. Change Note 6.		
		Change "R1" to "%RF" in the figure.		
1.2	2003.Jun.	Page 7. Add "or DDVDH".		
		Page 8. Error corrections.		
		Page 9. Error corrections. Add descriptions to "DUMMY1, 21, 23, 39" and "DUMMY 2-21, 24-38".		
		Page 21. Specify the instruction accessible during the standby mode: R03h		
		Page 73. Error correction.		
		Page 77. Add the power off sequence.		
		Page 78. Add the power off sequence.		
		Page 79. Correction to the Figure: Power Off Sequence.		
		Page 89. Change the recommended voltage for TEST4.		
		Page 90. Error correction.		
		Page 95, 96. Error corrections. Change Figure 1 to Figure 2, "t _H " to "T _{HWR} "		
		Page 97. Error correction.		
		Page 99. Specify the application of notes 6, 7.		
