DATA SHEET

OM6206
65 × 102 pixels matrix LCD driver

Product specification
File under Integrated Circuits, IC17

2001 Nov 14

Philips
Semiconductors

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CONTENTS

1 FEATURES

- Single-chip LCD controller and driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Configurable 5 (4, 3 and 2) × voltage multiplier generating V_{LCD} (external V_{LCD} also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- External reset input pin $\overline{RES}$
- Serial interface maximum 4.0 Mbits/s
- CMOS compatible inputs
- Multiplex rate of 1 : 65
- Logic supply voltage range from 2.5 to 5.5 V (V_{DD1} to V_{SS})
- High-voltage generator supply voltage range from 2.5 to 4.5 V (V_{DD2} and V_{DD3} to V_{SS})
- Display supply voltage range from 4.5 to 9.0 V (V_{LCD} to V_{SS})
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Temperature range from –40 to +85 °C
- Slim chip layout, suited for Chip-On-Glass (COG) applications.

2 APPLICATIONS

- Telecom equipment.

3 GENERAL DESCRIPTION

The OM6206 is a low-power CMOS LCD controller and driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption.

The OM6206 interfaces to microcontrollers via a serial bus interface.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM6206U/Z	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

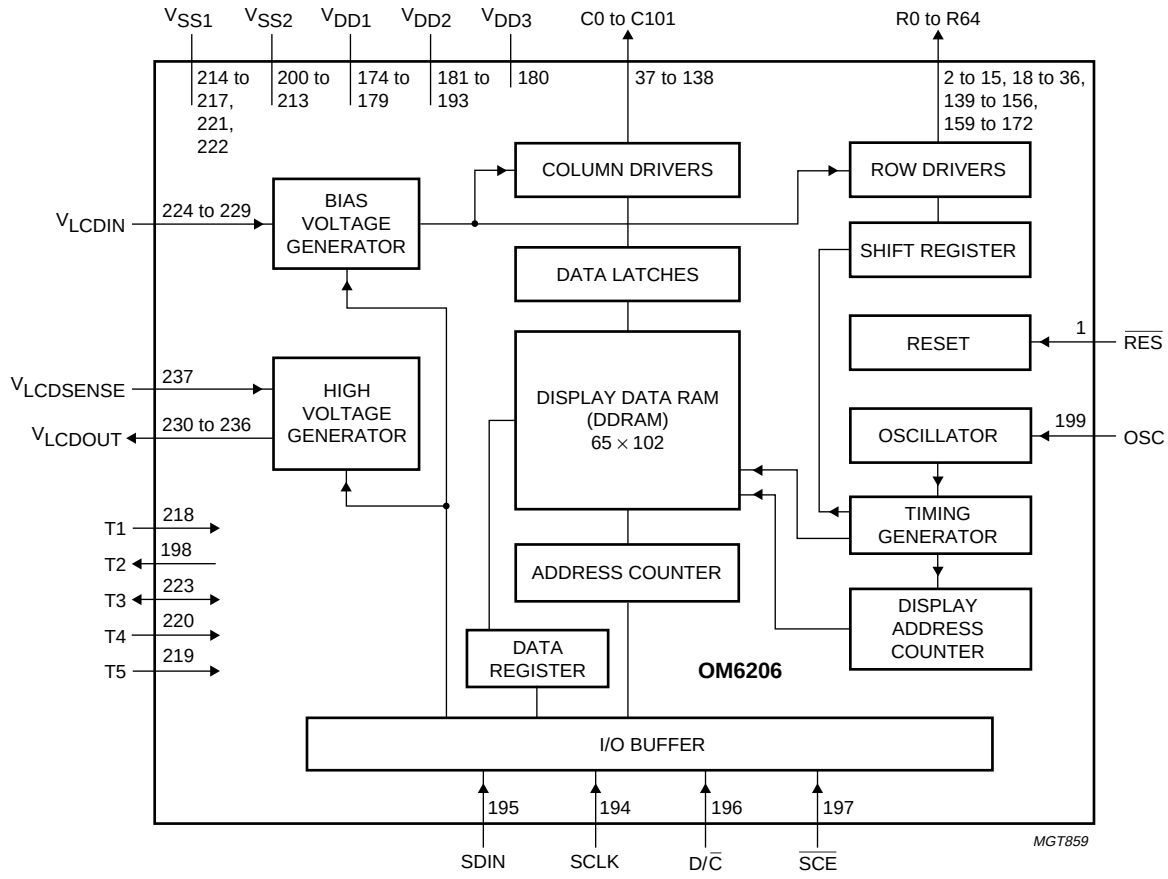


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	DESCRIPTION
R0 to R18	18 to 36	LCD row driver outputs
R19 to R32	2 to 15	LCD row driver outputs
R33 to R50	156 to 139	LCD row driver outputs
R51 to R64	159 to 172	LCD row driver outputs
C0 to C101	37 to 138	LCD column driver outputs
V_{SS1}	214 to 217, 221 and 222	ground supply 1
V_{SS2}	200 to 213	ground supply 2
V_{DD1}	174 to 179	supply voltage 1
V_{DD2}	181 to 193	supply voltage 2
V_{DD3}	180	supply voltage 3
V_{LCDIN}	224 to 229	LCD supply voltage (V_{LCD})
V_{LCDOUT}	230 to 236	voltage multiplier output (V_{LCD})
$V_{LCDSENSE}$	237	voltage multiplier regulation input (V_{LCD})
T1	218	test 1 input
T2	198	test 2 output
T3	223	test 3 input/output
T4	220	test 4 input
T5	219	test 5 input
SCLK	194	serial clock input
SDIN	195	serial data input
D/$\overline{C}$	196	data or command selection input
$\overline{SCE}$	197	chip enable (active LOW)
OSC	199	oscillator signal input
$\overline{RES}$	1	external reset input (active LOW)

6.1 Pin functions

6.1.1 R0 TO R64: ROW DRIVER OUTPUTS

These pins output the row signals.

6.1.2 C0 TO C101: COLUMN DRIVER OUTPUTS

These pins output the column signals.

6.1.3 V_{SS1} AND V_{SS2}: GROUND SUPPLY RAILS

The supply rails V_{SS1} and V_{SS2} must be connected together.

6.1.4 V_{DD1}, V_{DD2} AND V_{DD3}: SUPPLY VOLTAGE RAILS

V_{DD2} and V_{DD3} are the supply voltage for the internal voltage generator. Both have the same voltage and should be connected together outside the chip. V_{DD1} is used as supply voltage for the rest of the chip. V_{DD1} can be connected together with V_{DD2} and V_{DD3} but in this case care must be taken to respect the supply voltage range (see Chapter 11).

If the internal voltage generator is not used the pins V_{DD2} and V_{DD3} must be connected to pin V_{DD1} or connected to the supply voltage.

6.1.5 V_{LCDIN}: LCD SUPPLY VOLTAGE

Positive supply voltage for the liquid crystal display. An external LCD supply voltage can be supplied using pin V_{LCDIN}. In this case, V_{LCDOUT} has to be left open and the internal voltage generator has to be programmed to zero. If the OM6206 is in Power-down mode, the external LCD supply voltage has to be switched off.

6.1.6 V_{LCDOUT}: VOLTAGE MULTIPLIER OUTPUT

Positive supply voltage for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCDIN} and V_{LCDOUT} must be connected together. If an external supply is used this pin must be left open.

6.1.7 $V_{LCDSENSE}$: VOLTAGE MULTIPLIER REGULATION INPUT

$V_{LCDSENSE}$ is the input of the internal voltage multiplier regulation.

If the internal voltage generator is used then $V_{LCDSENSE}$ must be connected to V_{LCDOUT}. If an external supply voltage is used then $V_{LCDSENSE}$ can be left open or connected to ground.

6.1.8 T1 TO T5: TEST PINS

T1, T3, T4 and T5 must be connected to V_{SS}, T2 must be left open. Not accessible to user.

6.1.9 SDIN: SERIAL DATA LINE

Input for the data line.

6.1.10 SCLK: SERIAL CLOCK LINE

Input for the clock signal: up to 4.0 Mbits/s.

6.1.11 D/$\overline{C}$: MODE SELECT

Input to select either command or address data input.

6.1.12 $\overline{SCE}$: CHIP ENABLE

The enable pin allows data to be clocked in. Signal is active LOW.

6.1.13 OSC: OSCILLATOR

When the on-chip oscillator is used this input must be connected to V_{DD}. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting pin OSC to V_{SS}, the display is not clocked and may be left in a DC state. To avoid this the chip should always be put into Power-down mode before stopping the clock.

6.1.14 $\overline{RES}$: RESET

This signal will reset the device and must be applied to properly initialize the chip. Signal is active LOW.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD}. An external clock signal, if used, is connected to this input.

7.2 Address counter

The address counter assigns addresses to the display data RAM for writing. The X-address X_6 to X_0 and the Y-address Y_3 to Y_0 are set separately. After a write operation, the address counter is automatically incremented by 1 according to bit V (see Section 7.7).

7.3 Display Data RAM (DDRAM)

The OM6206 contains a 65 × 102 bits static RAM which stores the display data. The RAM is divided into eight banks of 102 bytes (8 × 8 × 102 bits) and one bank of 102 bits (1 × 102 bits). During RAM access, data is transferred to the RAM via the serial interface. There is a direct correspondence between X-address and column output number.

7.4 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

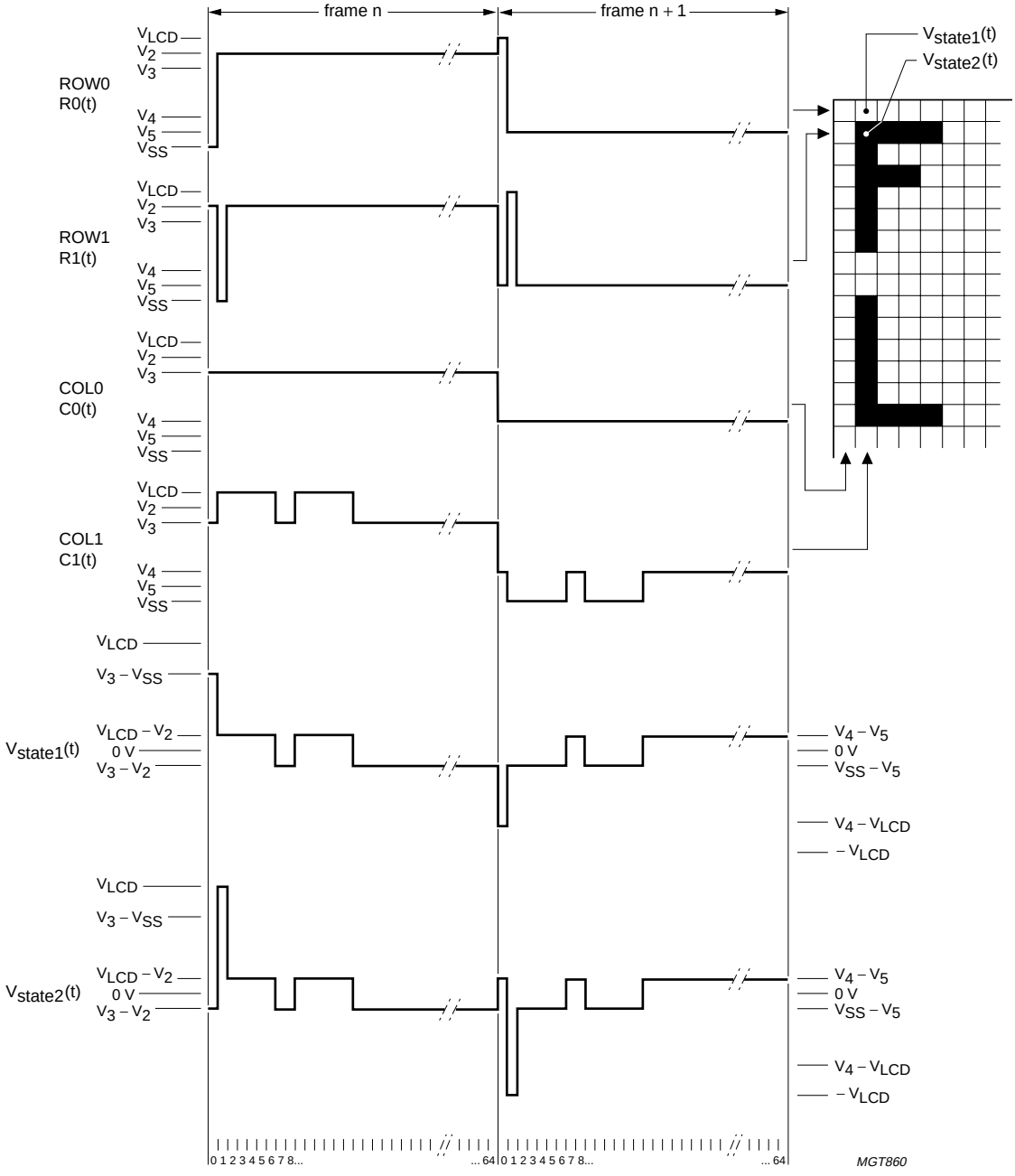
7.5 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs.

The display status (all dots on/off and normal/inverse video) is set by bits E and D in the command ‘Display control’ (see Table 2).

7.6 LCD row and column drivers

The OM6206 contains 65 rows and 102 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.



$V_{state1}(t)$ = C1(t) to R0(t).
$V_{state2}(t)$ = C1(t) to R1(t).

Fig.2 Typical LCD driver waveforms.

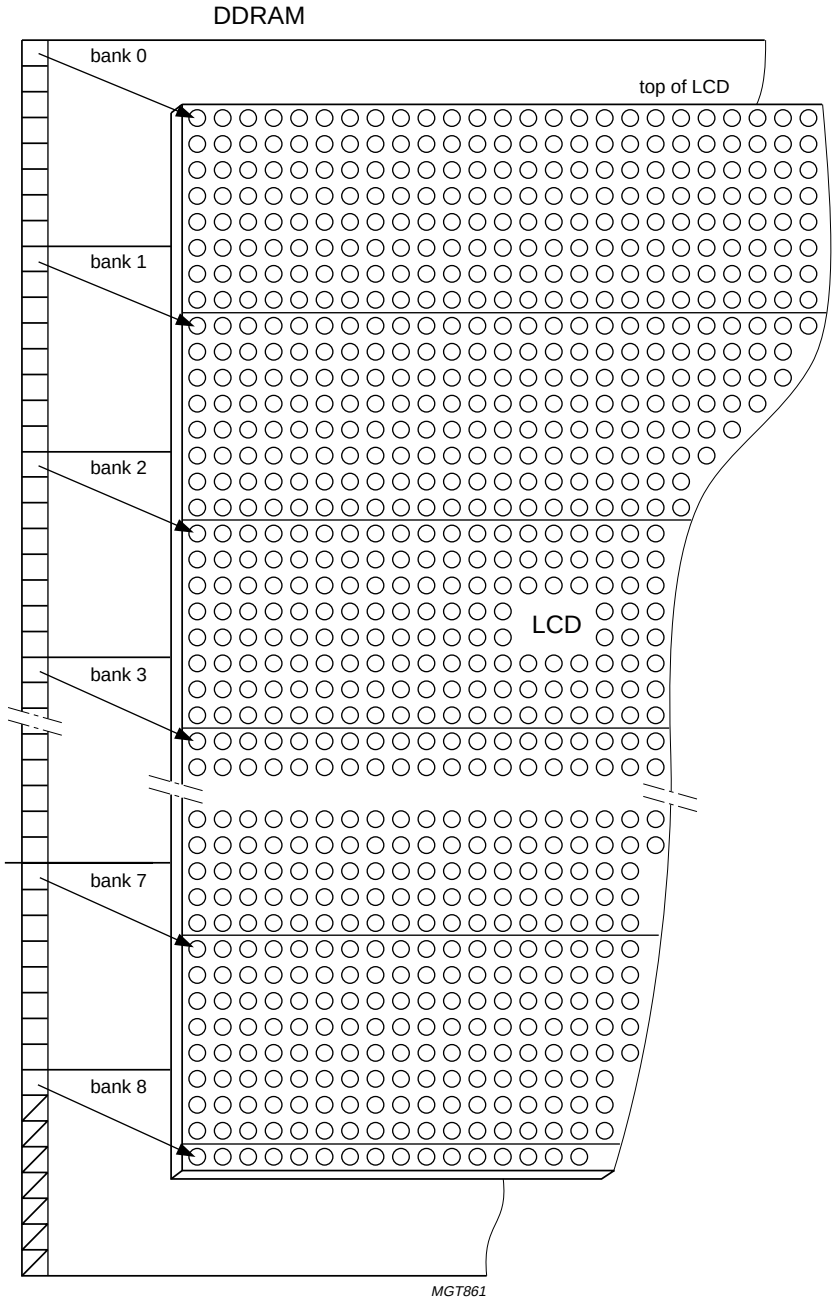


Fig.3 DDRAM to display mapping.

7.7 Addressing

Data is downloaded in bytes into the RAM matrix of OM6206 as indicated in Figs.3, 4, 5 and 6.

The display RAM has a matrix of 65 × 102 bits. The columns are addressed by the address pointer. The address ranges are: X from 0 to 101 (1100101) and Y from 0 to 8 (1000). Addresses outside these ranges are not allowed.

In vertical addressing mode (bit V = 1) the Y-address increments after each byte (see Fig.6).

After the last Y-address (Y = 8) Y wraps around to 0 and X increments to address the next column.

In horizontal addressing mode (bit V = 0) the X-address increments after each byte (see Fig.5). After the last X-address (X = 101) X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 101, Y = 8) the address pointers wrap around to address X = 0, Y = 0.

7.7.1 DATA STRUCTURE

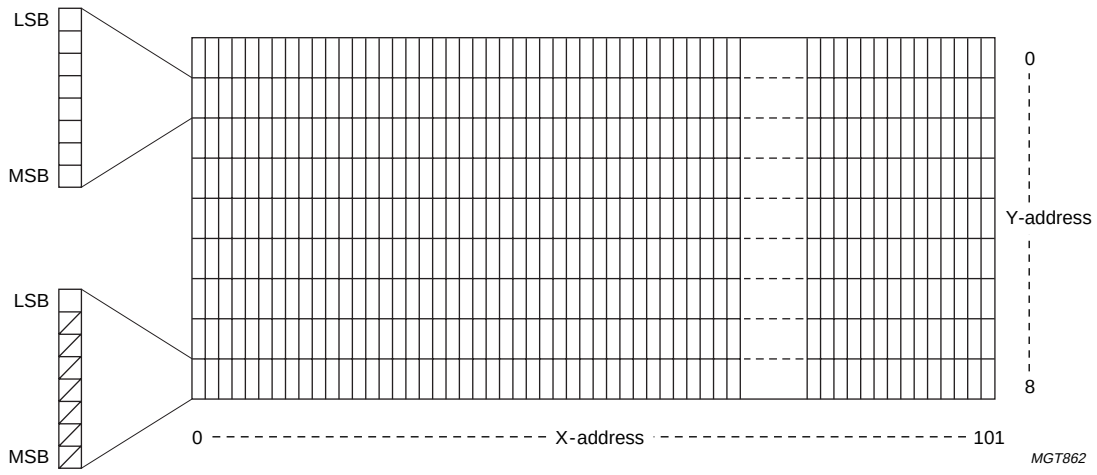


Fig.4 RAM format, addressing.

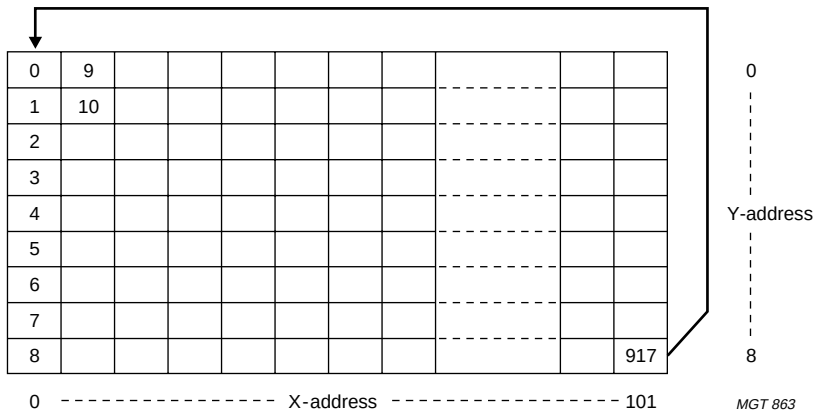


Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

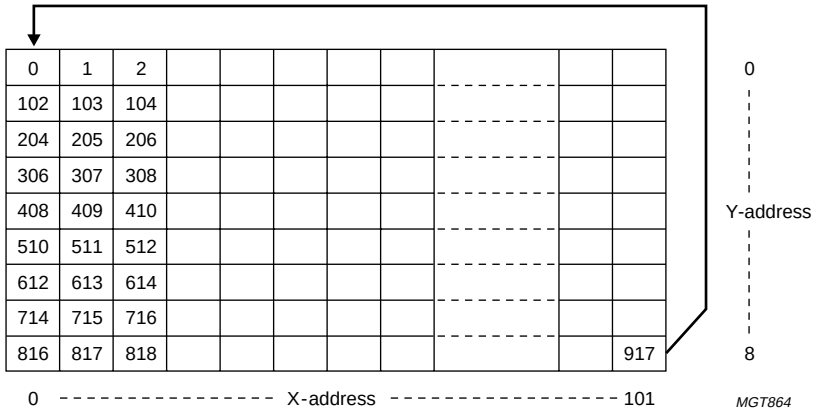


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

8 INSTRUCTIONS

The instruction format is divided into two modes:

- If D/$\overline{C}$ (mode select) is set LOW, the current byte is interpreted as command byte (see Table 1).
- If D/$\overline{C}$ is set HIGH, the following bytes are stored in the display data RAM. After every data byte the address counter is incremented automatically.

The level of the D/$\overline{C}$ signal is read during the last bit of data byte.

Every instruction can be sent in any order to the OM6206. The MSB of a byte is transmitted first (see Fig.7). Figure 8 shows one possible command stream, used to set up the LCD driver.

The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state SCLK clock pulses have no effect and no power is consumed by the serial interface. A negative edge on $\overline{SCE}$ enables the serial interface and indicates the start of a data transmission.

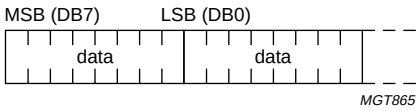


Fig.7 General format of data stream.

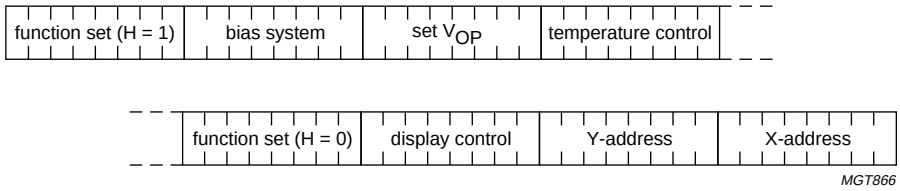


Fig.8 Serial data stream, example.

Figures 9 and 10 show the serial bus protocol:

- When $\overline{SCE}$ is HIGH, SCLK clock signals are ignored. During the HIGH time of $\overline{SCE}$, the serial interface is initialized (see Fig.11)
- SDIN is sampled at the positive edge of SCLK
- D/$\overline{C}$ indicates, whether the byte is a command (D/$\overline{C}$ = LOW) or RAM data (D/$\overline{C}$ = HIGH); it is read with the eighth SCLK pulse
- If $\overline{SCE}$ stays LOW after the last bit of a command/data byte, the serial interface expects bit 7 of the next byte at the next positive edge of SCLK (see Fig.11)
- A reset pulse with $\overline{RES}$ interrupts the transmission. No data are written into the RAM. The registers are cleared. If $\overline{SCE}$ is LOW after the positive edge of $\overline{RES}$, the serial interface is ready to receive bit 7 of a command/data byte (see Fig.11).

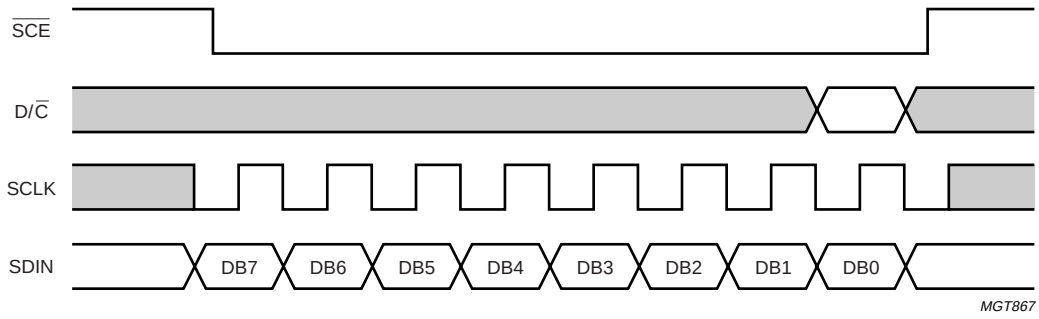


Fig.9 Serial bus protocol for transmission of one byte.

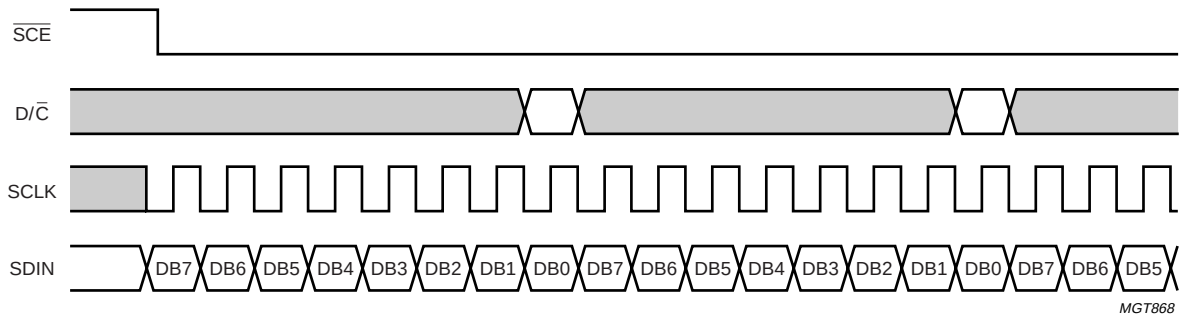


Fig.10 Serial bus protocol for transmission of several bytes.

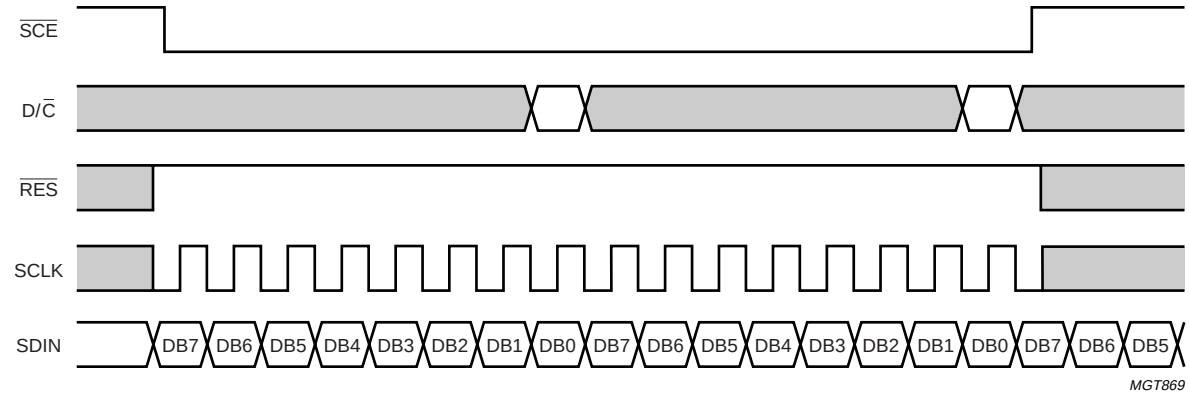


Fig.11 Serial bus reset function ($\overline{SCE}$).

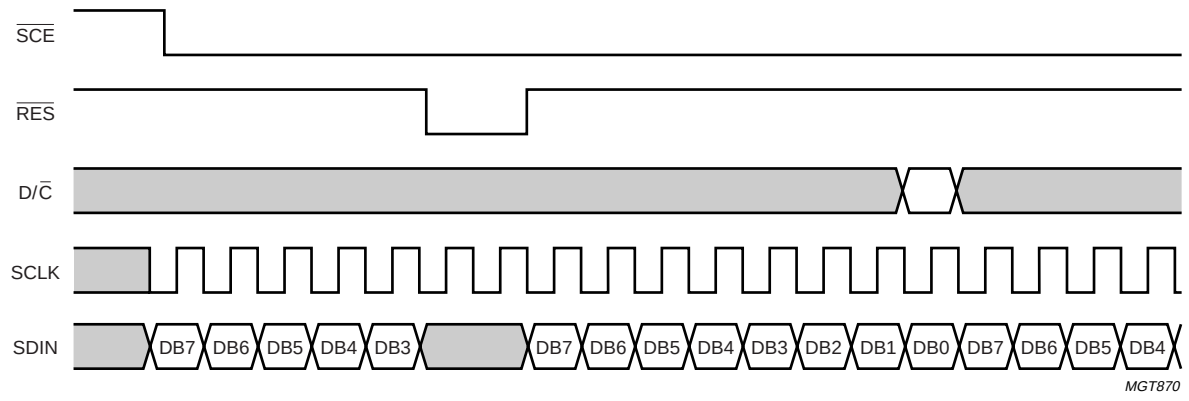


Fig.12 Serial bus interrupt function ($\overline{RES}$).

Table 1 Instruction set

INSTRUCTION	DESCRIPTION	PIN	COMMAND BYTE							
		D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
(H = 0 or 1)										
NOP	no operation	LOW	0	0	0	0	0	0	0	0
Function set	power down control; entry mode; extended instruction set control (H)	LOW	0	0	1	0	0	PD	V	H
Write data	writes data to display RAM	HIGH	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
(H = 0)										
Reserved	do not use	LOW	0	0	0	0	0	1	X	X
Display control	sets display configuration	LOW	0	0	0	0	1	D	0	E
Set HIGH or LOW program range V_{OP}	V_{LCD} programming range select	LOW	0	0	0	1	0	0	0	PRS
Set Y-address of RAM	sets Y-address of RAM; $0 \leq Y \leq 8$	LOW	0	1	0	0	Y_3	Y_2	Y_1	Y_0
Set X-address of RAM	sets X-address of RAM; $0 \leq X \leq 101$	LOW	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0
(H = 1)										
Reserved	do not use	LOW	0	0	0	0	0	0	0	1
	do not use	LOW	0	0	0	0	0	0	1	X
Temperature control	set Temperature Coefficient (TC_x)	LOW	0	0	0	0	0	1	TC_1	TC_0
HVgen stages	multiplication of high-voltage generator voltage (S_x)	LOW	0	0	0	0	1	0	S_1	S_0
Bias system	set Bias System (BS_x)	LOW	0	0	0	1	0	BS_2	BS_1	BS_0
Reserved	do not use (reserved for test)	LOW	0	1	X	X	X	X	X	X
Set V_{OP}	write V_{OPx} to register	LOW	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}

Table 2 Explanations for symbols in Table 1

BIT	BIT VALUE	DESCRIPTION	RESET STATE
PD	0	chip is active	1
	1	chip is in Power-down mode	
V	0	horizontal addressing	0
	1	vertical addressing	
H	0	use basic instruction set	0
	1	use extended instruction set	
D and E	00	display blank	00
	10	normal mode	
	01	all display segments on	
	11	inverse video mode	
PRS	0	V_{LCD} programming range LOW	0
	1	V_{LCD} programming range HIGH	

BIT	BIT VALUE	DESCRIPTION	RESET STATE
TC_1 and TC_0	00	V_{LCD} temperature coefficient 0	00
	01	V_{LCD} temperature coefficient 1	
	10	V_{LCD} temperature coefficient 2	
	11	V_{LCD} temperature coefficient 3	
S_1 and S_0	00	2 × voltage multiplier	00
	01	3 × voltage multiplier	
	10	4 × voltage multiplier	
	11	5 × voltage multiplier	
BS_2 to BS_0	–	bias system	000
V_{OP6} to V_{OP0}	–	V_{LCD} programming	0000000

8.1 Initialization

Immediately following power-on, all internal registers as well as the RAM content are undefined. A $\overline{RES}$ pulse must be applied.

Reset is accomplished by applying an external reset pulse (active LOW) at pin $\overline{RES}$. When reset occurs within the specified time, all internal registers are reset however the RAM is still undefined. The state after reset is described in Section 8.2.

$\overline{RES}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches $V_{DD(min)}$ (or higher) within a maximal time t_{VHRL} after V_{DD} going HIGH (see Fig.16).

8.2 Reset function

After reset the LCD driver has the following state:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Display blank (E and D = 0)
- Address counter X_6 to X_0 = 0, Y_3 to Y_0 = 0
- Temperature control (TC_1 and TC_0 = 0)
- Bias system (BS_2 to BS_0 = 0)
- V_{LCD} is equal to 0 V and the high-voltage generator is switched off (V_{OP6} to V_{OP0} = 0 and PRS = 0)
- After power-on, RAM data are undefined, the reset signal does not change the content of the RAM
- All LCD outputs at V_{SS} (display off).

8.3 Function set

8.3.1 PD

When PD = 1 the chip is in Power-down mode:

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off; V_{LCD} can be disconnected
- Oscillator off (external clock possible)
- Serial bus: command, function etc.
- RAM contents not cleared; RAM data can be written
- V_{LCD} discharged to V_{SS} in Power-down mode.

8.3.2 V

When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig.6.
When V = 1, the vertical addressing is selected. The data is written into the DDRAM as shown in Fig.5.

8.3.3 H

When H = 0 the commands ‘display control’, ‘set Y-address’, ‘set X-address’ and ‘set the PRS bit’ (LOW or HIGH range of the high-voltage generator) can be performed; when H = 1 the others can be executed. The commands ‘write data’ and ‘function set’ can be executed in both cases.

8.4 Display control

8.4.1 D AND E

The bits D and E select the display mode (see Table 2).

8.5 Set Y-address of RAM

Y_3 to Y_0 define the Y-address vector address of the display RAM.

Table 3 X/Y-address range

Y_3	Y_2	Y_1	Y_0	BANK(1)	ALLOWED X-RANGE
0	0	0	0	0	0 to 101
0	0	0	1	1	0 to 101
0	0	1	0	2	0 to 101
0	0	1	1	3	0 to 101
0	1	0	0	4	0 to 101
0	1	0	1	5	0 to 101
0	1	1	0	6	0 to 101
0	1	1	1	7	0 to 101
1	0	0	0	8; note 2	0 to 101

Notes

1. Display RAM.
2. Only the MSB is accessed.

8.6 Set X-address of RAM

The X-address points to the columns. The range of X is 0 to 101 (65H).

8.7 Set high-voltage generator stages

The OM6206 incorporates a software configurable voltage multiplier. After reset ($\overline{RES}$) the voltage multiplier is set to $2 \times V_{DD2}$. Other voltage multiplier factors are set via the command ‘HVgen stages’ (see Tables 1 and 2).

8.8 Bias system

The bias voltage levels are set in the ratio of R - R - nR - R - R giving a $\frac{1}{n+4}$ bias system. Different multiplex rates require different factors n (see Table 4). This is programmed by BS_2 to BS_0. For multiplex rate 1 : 65 the optimum bias value n is given by:

$$n = \sqrt{65} - 3 = 5.062 = 5 \quad (1)$$

resulting in a $^1/_9$ bias system.

Table 4 Programming the required bias system

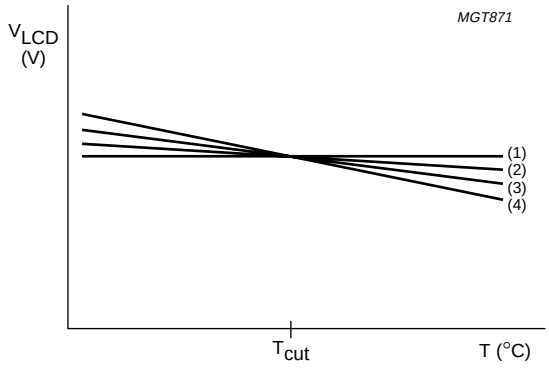
BS_2	BS_1	BS_0	n	RECOMMENDED MULTIPLEX RATE
0	0	0	7	1 : 100
0	0	1	6	1 : 80
0	1	0	5	1 : 65 or 1 : 65
0	1	1	4	1 : 48
1	0	0	3	1 : 40 or 1 : 34
1	0	1	2	1 : 24
1	1	0	1	1 : 18 or 1 : 16
1	1	1	0	1 : 10 or 1 : 9 or 1 : 8

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES	BIAS VOLTAGE FOR 1⁄9 BIAS
V1	V_{LCD}	V_{LCD}
V2	$\frac{n+3}{n+4}$	$^{8}/_{9} \times V_{LCD}$
V3	$\frac{n+2}{n+4}$	$^{7}/_{9} \times V_{LCD}$
V4	$\frac{2}{n+4}$	$^{2}/_{9} \times V_{LCD}$
V5	$\frac{1}{n+4}$	$^{1}/_{9} \times V_{LCD}$
V6	V_{SS}	V_{SS}

8.9 Temperature control

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimal contrast. There are four temperature coefficients available in the OM6206 (see Fig.13). The coefficients are selected by the two bits TC_1 and TC_0. Table 6 shows the typical values of the temperature coefficients. The coefficients are proportional to the programmed V_{LCD} at reference temperature.



(1) TC0.
(2) TC1.
(3) TC2.
(4) TC3.

Fig.13 Temperature coefficients behaviour.

8.10 Set V_{OP} value

The operation voltage V_{LCD} can be set by software. The generated voltage is dependent on the programmed voltage at reference temperature (T_{cut}), the programmed Temperature Coefficient (TC) and the operating temperature (T).

The voltage at reference temperature can be calculated as:

$$V_{LCD(Tcut)} = a + b \times V_{OP} \quad (2)$$

The voltage at operating temperature can be calculated as:

$$V_{LCD(T)} = V_{LCD(Tcut)} + (T - T_{cut}) \times TC \quad (3)$$

The parameters are explained in Table 6.

The maximum voltage that can be generated is depending on the V_{DD2} voltage and the display load current.

Two overlapping V_{LCD} ranges are selectable via the command 'set HIGH or LOW program range V_{OP}'.

For the LOW range (bit PRS = 0) component a = a_1 and for the HIGH range (bit PRS = 1) component a = a_2. The steps in both ranges are equal to b.

It should be noted that the charge pump is turned off if bits V_{OP6} to V_{OP0} and bit PRS are all set to zero (see Fig.14).

For multiplexer rate 1 : 65 the optimum operation voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{65}}\right)}} \times V_{th} = 6.85 \times V_{th} \quad (4)$$

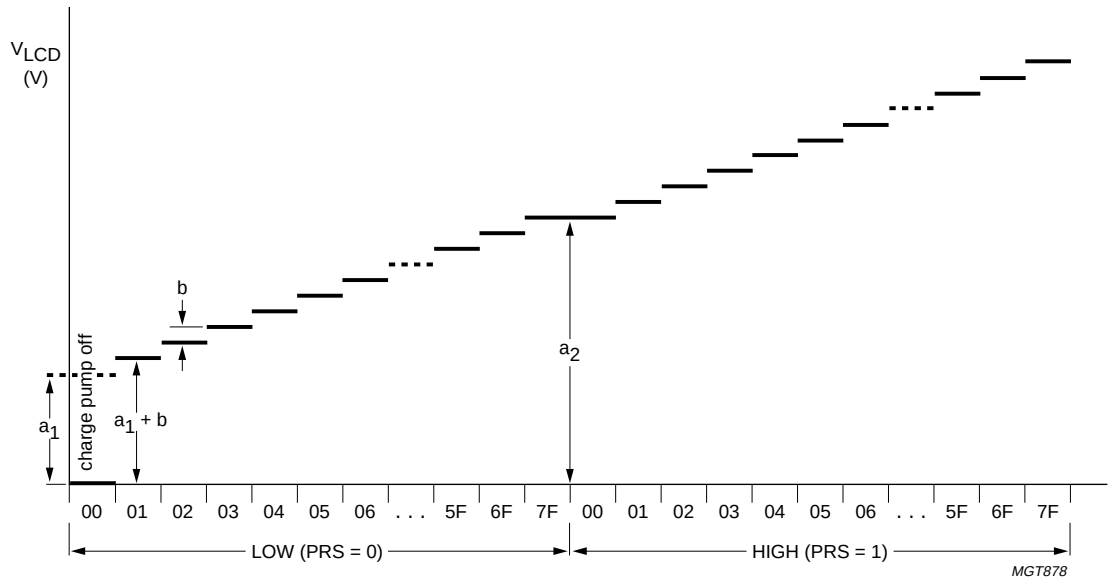
where V_{th} is the threshold voltage of the liquid crystal material used.

Table 6 Typical values for parameters for the high-voltage generator programming

SYMBOL	VALUE	UNIT
a_1	2.94 (PRS = 0)	V
a_2	6.75 (PRS = 1)	V
b	0.03	V
T_{cut}	27	°C

Table 7 Temperature coefficients

NAME	BIT		VALUE	UNIT
	TC_1	TC_0		
TC0	0	0	$-0.00 \times 10^{-3} \times V_{LCD(Tcut)}$	V/°C
TC1	0	1	$-0.76 \times 10^{-3} \times V_{LCD(Tcut)}$	V/°C
TC2	1	0	$-1.05 \times 10^{-3} \times V_{LCD(Tcut)}$	V/°C
TC3	1	1	$-2.10 \times 10^{-3} \times V_{LCD(Tcut)}$	V/°C



V_{OP6} to V_{OP0} to be programmed (00H to 7FH), programming ranges LOW and HIGH.

Fig.14 V_{OP} programming at T = T_{cut}.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9.0 V) the user has to ensure while setting the V_{OP} value and selecting the Temperature Coefficient (TC), that under all conditions and including all tolerances the V_{LCD} remains below 9.0 V.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	supply voltage 1	–0.5	+6.5	V
$V_{DD2,}$, V_{DD3}	supply voltages 2 and 3	–0.5	+4.5	V
V_{LCD}	supply voltage LCD	–0.5	+9.0	V
V_i	all input voltages	–0.5	V_{DD} + 0.5	V
I_{SS}	ground supply current	–50	+50	mA
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	300	mW
P/out	power dissipation per output	–	30	mW
T_{stg}	storage temperature	–65	+150	°C

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise specified.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

11 DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage 1		2.5	–	5.5	V
V_{DD2}, V_{DD3}	supply voltages 2 and 3	LCD voltage internally generated (voltage generator enabled)	2.5	–	4.5	V
V_{LCDIN}	input supply voltage LCD	LCD voltage externally supplied (voltage generator disabled)	4.5	–	9.0	V
V_{LCDOUT}	output supply voltage LCD	LCD voltage internally generated (voltage generator enabled); note 1	4.5	–	9.0	V
$I_{DD(tot)}$	total supply current	normal mode; V_{DD} = 2.8 V; V_{LCD} = 7.6 V; no serial clock; T_{amb} = 25 °C; no display load; 4 × charge pump; note 2	–	200	300	µA
		Power-down mode; with internal or external V_{LCD}; note 3	–	1.5	–	µA
I_{LCDIN}	supply current from external V_{LCD}	V_{DD} = 2.8 V; V_{LCD} = 7.6 V; no serial clock; T_{amb} = 25 °C; no display load; notes 2 and 4	–	30	–	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_L	leakage current	V_I = V_{DD} or V_{SS}	–1	–	+1	µA
Column and row outputs						
R_{col}	output resistance of columns C0 to C101	V_{LCD} = 7.6 V	–	12	20	kΩ
R_{row}	output resistance of rows R0 to R64	V_{LCD} = 7.6 V	–	12	20	kΩ
V_{col}	bias tolerance voltage of columns C0 to C101		–100	0	+100	mV
V_{row}	bias tolerance voltage of rows R0 to R64		–100	0	+100	mV
LCD supply voltage generator						
ΔV_{LCD}	tolerance of internally generated V_{LCD}	V_{DD} = 2.8 V; V_{LCD} = 7.6 V; no serial clock; T_{amb} = 25 °C; display load is 10 µA; notes 5 and 6	–300	0	+300	mV
TC0	V_{LCD} temperature coefficient 0	note 7	–	$0 \times 10^{-3} V_{LCD}$	–	V/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TC1	V_{LCD} temperature coefficient 1	note 7	–	$-0.76 \times 10^{-3} V_{LCD}$	–	V/°C
TC2	V_{LCD} temperature coefficient 2	note 7	–	$-1.05 \times 10^{-3} V_{LCD}$	–	V/°C
TC3	V_{LCD} temperature coefficient 3	note 7	–	$-2.10 \times 10^{-3} V_{LCD}$	–	V/°C

Notes

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. During Power-down mode, all static currents are switched off.
4. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
5. Tolerance depends on the temperature; typical null at T_{amb} = 27 °C; maximum tolerance values are measured at the temperate range limit; maximum tolerance is proportional to V_{LCD}.
6. For TC1 to TC3.
7. V_{DD} = 2.8 V; no serial clock; T_{amb} = –20 to +70 °C; display load = 10 μA.

12 AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{osc}	oscillator frequency	V_{DD} = 2.8 V; T_{amb} = –20 to +70 °C	22	38	67	kHz
f_{ext}	external clock frequency		20	38	67	kHz
f_{frame}	frame frequency	f_{osc} or f_{ext} = 38 kHz; note 1	–	73	–	Hz
t_{VHRL}	V_{DD} HIGH to $\overline{RES}$ LOW time	see Fig.16	0 (2)	–	1	μs
t_{RW}	$\overline{RES}$ LOW pulse width	see Fig.16	100	–	–	ns
Serial bus timing characteristics; see Fig.15						
f_{SCLK}	clock frequency	V_{DD} = 3.0 V ±10%; note 3	0	–	4	MHz
t_{CYC}	SCLK clock cycle time		250	–	–	ns
t_{PWH1}	SCLK pulse width HIGH		100	–	–	ns
t_{PWL1}	SCLK pulse width LOW		100	–	–	ns
t_{S2}	$\overline{SCE}$ setup time		60	–	–	ns
t_{H2}	$\overline{SCE}$ hold time		100	–	–	ns
t_{PWH2}	$\overline{SCE}$ HIGH time		100	–	–	ns
t_{H5}	$\overline{SCE}$ start hold time	note 4	100	–	–	ns
t_{S3}	D/$\overline{C}$ setup time		100	–	–	ns
t_{H3}	D/$\overline{C}$ hold time		100	–	–	ns
t_{S4}	SDIN setup time		100	–	–	ns
t_{H4}	SDIN hold time		100	–	–	ns

Notes

1. $f_{frame} = \frac{f_{ext}}{520}$

2. $\overline{RES}$ may be LOW before V_{DD} goes HIGH.
3. All signal timing is based on 20% to 80% of V_{DD} and a maximum rise and fall time of 10 ns.
4. t_{H5} is the time from the previous SCLK positive edge (irrespective of the state of $\overline{SCE}$) to the negative edge of $\overline{SCE}$.

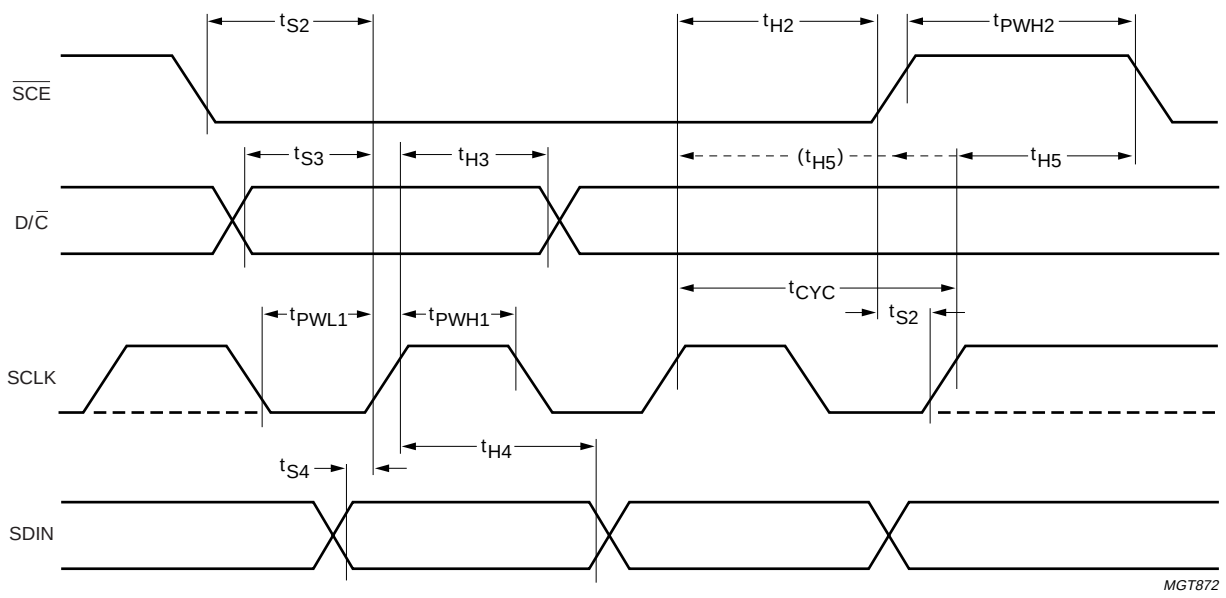


Fig.15 Serial interface timing.

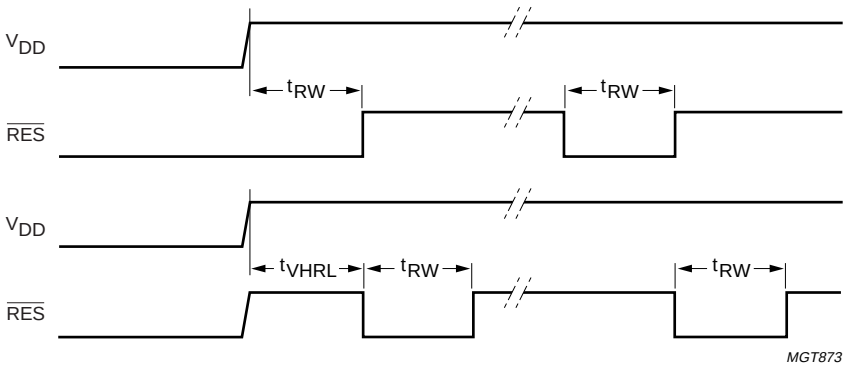
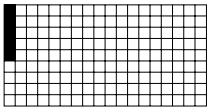
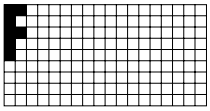
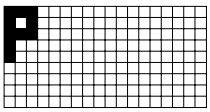
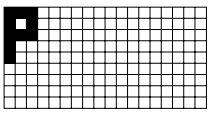
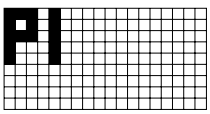
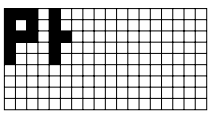


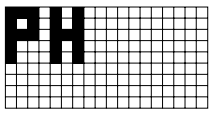
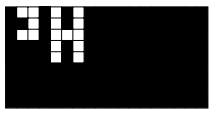
Fig.16 Reset timing.

13 APPLICATION INFORMATION

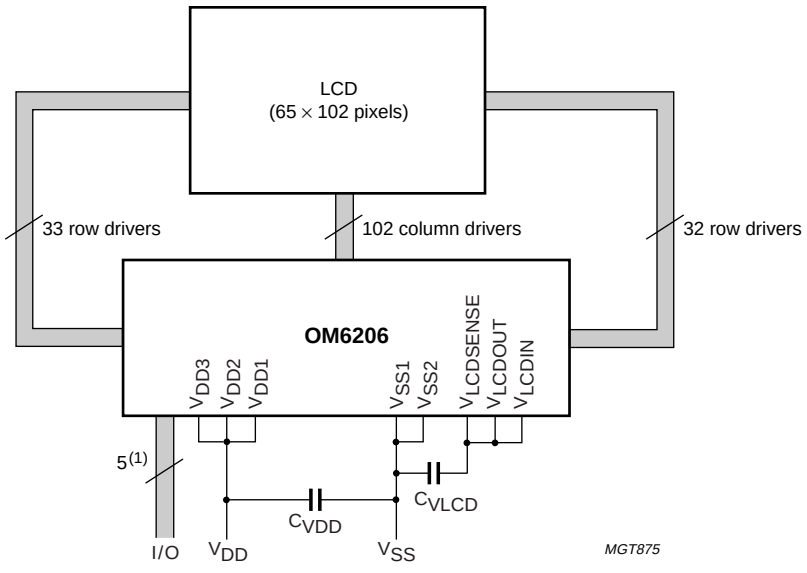
13.1 Programming example for the OM6206

Table 8 Programming example

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	start										$\overline{SCE}$ is going LOW
2	0	0	0	1	0	0	0	0	1		function set: PD = 0 and V = 0; select extended instruction set (H = 1)
3	0	1	0	0	1	0	0	0	0		set V_{OP}: V_{OP} is set to a +16 × b [V]
4	0	0	0	1	0	0	0	0	0		function set: PD = 0 and V = 0; select normal instruction set (H = 0)
5	0	0	0	0	0	1	1	0	0		display control: set normal mode (D = 1 and E = 0)
6	1	0	0	0	1	1	1	1	1	 MGT144	data write: Y and X are initialized to 0 by default, so they are not set here
7	1	0	0	0	0	0	1	0	1	 MGT145	data write
8	1	0	0	0	0	0	1	1	1	 MGT146	data write
9	1	0	0	0	0	0	0	0	0	 MGT146	data write
10	1	0	0	0	1	1	1	1	1	 MGT148	data write
11	1	0	0	0	0	0	1	0	0	 MGT149	data write

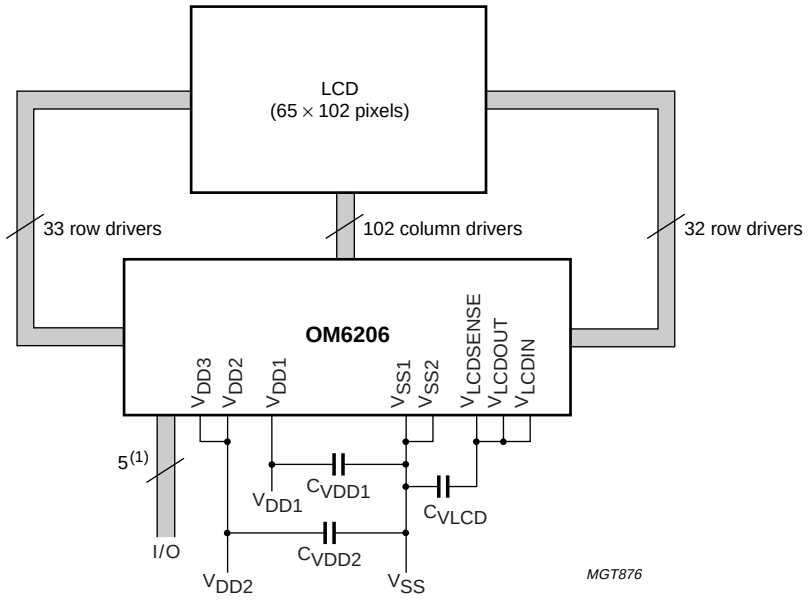
STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
12	1	0	0	0	1	1	1	1	1	 MGT151	data write
13	0	0	0	0	0	1	1	0	1	 MGT152	display control: set inverse video mode (D = 1 and E = 1)
14	0	1	0	0	0	0	0	0	0	 MGT152	set X-address of RAM: set address to ‘0000000’
15	1	0	0	0	0	0	0	0	0	 MGT874	data write

13.2 Application diagrams



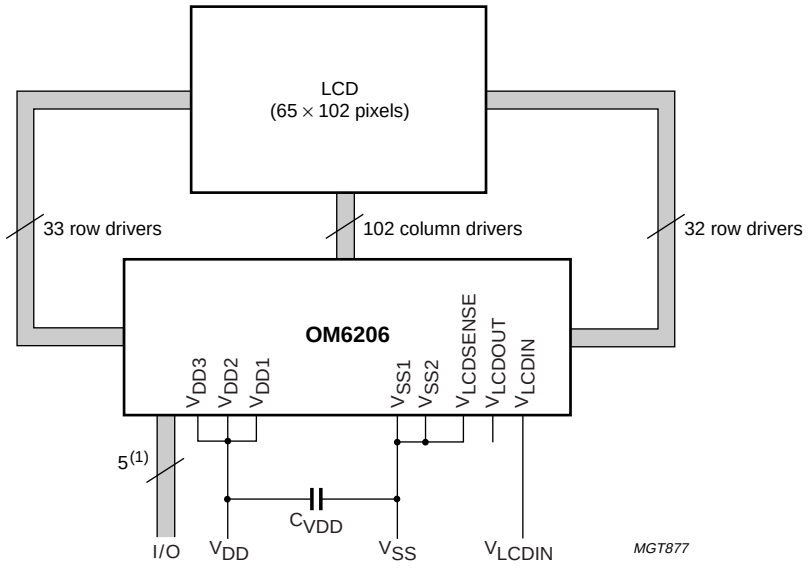
(1) 6 if external oscillator is used.

Fig.17 Application diagram: internal charge pump is used and a single supply V_{DD}.



(1) 6 if external oscillator is used.

Fig.18 Application diagram: internal charge pump is used and two separate supplies V_{DD1} and V_{DD2}.



(1) 6 if external oscillator is used.

Fig.19 Application diagram: external supply V_{LCDIN} is used.

The required minimum value for the external capacitors in an application with the OM6206 are:

- C_{VLCD} > 100 μF
- C_{VDD}, C_{VDD1} and C_{VDD2} > 1 μF

Higher capacitor values are recommended for ripple reduction.

13.3 Application for COG

The pinning of the OM6206 is optimized for single plane wiring e.g. for Chip-On-Glass (COG) display modules with display size of 65 × 102 pixels.

To reduce the sensitivity of a reset to ESD/EMC disturbances for a chip-on-glass application, it is strongly recommended to implement on the glass (indium track resistance) a series input resistance in the reset line (recommended minimum value of 8 kΩ).

13.4 Chip information

The OM6206 is manufactured in n-well CMOS technology. The substrate is on V_{SS} potential.

14 BONDING PAD INFORMATION

SYMBOL	PAD	COORDINATES(1)	
		x	y
$\overline{RES}$_B	1	–3870	+935
row32	2	–4270	+935
row31	3	–4340	+935
row30	4	–4410	+935
row29	5	–4480	+935
row28	6	–4550	+935
row27	7	–4620	+935
row26	8	–4690	+935
row25	9	–4760	+935
row24	10	–4830	+935
row23	11	–4900	+935
row22	12	–4970	+935
row21	13	–5040	+935
row20	14	–5110	+935
row19	15	–5180	+935
dummy pad	16	–5320	+935
dummy pad	17	–5355	–935
row0	18	–5005	–935
row1	19	–4935	–935
row2	20	–4865	–935
row3	21	–4795	–935
row4	22	–4725	–935
row5	23	–4655	–935
row6	24	–4585	–935
row7	25	–4515	–935
row8	26	–4445	–935
row9	27	–4375	–935
row10	28	–4305	–935
row11	29	–4235	–935
row12	30	–4165	–935
row13	31	–4095	–935
row14	32	–4025	–935
row15	33	–3955	–935
row16	34	–3885	–935
row17	35	–3815	–935
row18	36	–3745	–935
col0	37	–3605	–935
col1	38	–3535	–935
col2	39	–3465	–935
col3	40	–3395	–935
col4	41	–3325	–935
col5	42	–3255	–935
col6	43	–3185	–935
col7	44	–3115	–935
col8	45	–3045	–935
col9	46	–2975	–935
col10	47	–2905	–935
col11	48	–2835	–935
col12	49	–2765	–935
col13	50	–2695	–935
col14	51	–2625	–935
col15	52	–2555	–935
col16	53	–2485	–935
col17	54	–2415	–935
col18	55	–2345	–935

SYMBOL	PAD	COORDINATES(1)	
		x	y
col19	56	–2275	–935
col20	57	–2205	–935
col21	58	–2135	–935
col22	59	–2065	–935
col23	60	–1995	–935
col24	61	–1925	–935
col25	62	–1785	–935
col26	63	–1715	–935
col27	64	–1645	–935
col28	65	–1575	–935
col29	66	–1505	–935
col30	67	–1435	–935
col31	68	–1365	–935
col32	69	–1295	–935
col33	70	–1225	–935
col34	71	–1155	–935
col35	72	–1085	–935
col36	73	–1015	–935
col37	74	–945	–935
col38	75	–875	–935
col39	76	–805	–935
col40	77	–735	–935
col41	78	–665	–935
col42	79	–595	–935
col43	80	–525	–935
col44	81	–455	–935
col45	82	–385	–935
col46	83	–315	–935
col47	84	–245	–935
col48	85	–175	–935
col49	86	–105	–935
col50	87	+35	–935
col51	88	+105	–935
col52	89	+175	–935
col53	90	+245	–935
col54	91	+315	–935
col55	92	+385	–935
col56	93	+455	–935
col57	94	+525	–935

SYMBOL	PAD	COORDINATES(1)	
		x	y
col58	95	+595	–935
col59	96	+665	–935
col60	97	+735	–935
col61	98	+805	–935
col62	99	+875	–935
col63	100	+945	–935
col64	101	+1015	–935
col65	102	+1085	–935
col66	103	+1155	–935
col67	104	+1225	–935
col68	105	+1295	–935
col69	106	+1365	–935
col70	107	+1435	–935
col71	108	+1505	–935
col72	109	+1575	–935
col73	110	+1645	–935
col74	111	+1715	–935
col75	112	+1785	–935
col76	113	+1925	–935
col77	114	+1995	–935
col78	115	+2065	–935
col79	116	+2135	–935
col80	117	+2205	–935
col81	118	+2275	–935
col82	119	+2345	–935
col83	120	+2415	–935
col84	121	+2485	–935
col85	122	+2555	–935
col86	123	+2625	–935
col87	124	+2695	–935
col88	125	+2765	–935
col89	126	+2835	–935
col90	127	+2905	–935
col91	128	+2975	–935
col92	129	+3045	–935
col93	130	+3115	–935
col94	131	+3185	–935
col95	132	+3255	–935
col96	133	+3325	–935

SYMBOL	PAD	COORDINATES(1)	
		x	y
col97	134	+3395	–935
col98	135	+3465	–935
col99	136	+3535	–935
col100	137	+3605	–935
col101	138	+3675	–935
row50	139	+3815	–935
row49	140	+3885	–935
row48	141	+3955	–935
row47	142	+4025	–935
row46	143	+4095	–935
row45	144	+4165	–935
row44	145	+4235	–935
row43	146	+4305	–935
row42	147	+4375	–935
row41	148	+4445	–935
row40	149	+4515	–935
row39	150	+4585	–935
row38	151	+4655	–935
row37	152	+4725	–935
row36	153	+4795	–935
row35	154	+4865	–935
row34	155	+4935	–935
row33	156	+5005	–935
dummy pad	157	+5355	–935
dummy pad	158	+5320	+935
row51	159	+5180	+935
row52	160	+5110	+935
row53	161	+5040	+935
row54	162	+4970	+935
row55	163	+4900	+935
row56	164	+4830	+935
row57	165	+4760	+935
row58	166	+4690	+935
row59	167	+4620	+935
row60	168	+4550	+935
row61	169	+4480	+935
row62	170	+4410	+935
row63	171	+4340	+935
row64	172	+4270	+935

SYMBOL	PAD	COORDINATES(1)	
		x	y
dummy pad	173	+4050	+935
V_{DD1}	174	+3890	+935
V_{DD1}	175	+3810	+935
V_{DD1}	176	+3730	+935
V_{DD1}	177	+3650	+935
V_{DD1}	178	+3570	+935
V_{DD1}	179	+3490	+935
V_{DD3}	180	+3250	+935
V_{DD2}	181	+3090	+935
V_{DD2}	182	+3010	+935
V_{DD2}	183	+2930	+935
V_{DD2}	184	+2850	+935
V_{DD2}	185	+2770	+935
V_{DD2}	186	+2690	+935
V_{DD2}	187	+2610	+935
V_{DD2}	188	+2530	+935
V_{DD2}	189	+2450	+935
V_{DD2}	190	+2370	+935
V_{DD2}	191	+2290	+935
V_{DD2}	192	+2210	+935
V_{DD2}	193	+2130	+935
SCLK	194	+1890	+935
SDIN	195	+1650	+935
DC_B	196	+1410	+935
SCE_B	197	+1170	+935
T2	198	+930	+935
OSC	199	+690	+935
V_{SS2}	200	+530	+935
V_{SS2}	201	+450	+935
V_{SS2}	202	+370	+935
V_{SS2}	203	+290	+935
V_{SS2}	204	+210	+935
V_{SS2}	205	+130	+935
V_{SS2}	206	+50	+935
V_{SS2}	207	–30	+935
V_{SS2}	208	–110	+935
V_{SS2}	209	–190	+935
V_{SS2}	210	–270	+935
V_{SS2}	211	–350	+935

SYMBOL	PAD	COORDINATES(1)	
		x	y
V_{SS2}	212	−430	+935
V_{SS2}	213	−510	+935
V_{SS1}	214	−670	+935
V_{SS1}	215	−750	+935
V_{SS1}	216	−830	+935
V_{SS1}	217	−910	+935
T1	218	−1150	+935
T5	219	−1630	+935
T4	220	−2030	+935
V_{SS1}	221	−2110	+935
V_{SS1}	222	−2190	+935
T3	223	−2270	+935
V_{LCDIN}	224	−2510	+935
V_{LCDIN}	225	−2590	+935
V_{LCDIN}	226	−2670	+935
V_{LCDIN}	227	−2750	+935
V_{LCDIN}	228	−2830	+935
V_{LCDIN}	229	−2910	+935
V_{LCDOUT}	230	−3070	+935
V_{LCDOUT}	231	−3150	+935
V_{LCDOUT}	232	−3230	+935
V_{LCDOUT}	233	−3310	+935
V_{LCDOUT}	234	−3390	+935
V_{LCDOUT}	235	−3470	+935
V_{LCDOUT}	236	−3550	+935
$V_{LCDSENSE}$	237	−3630	+935
Alignment marks			
Circle 1		−5185	−910
Circle 2		+5185	−910
Circle 3		+4160	+910
Circle 4		−4160	+910

Note

1. All x/y coordinates (in μm) are referenced to the centre of the chip (see Fig.20).

Table 9 Bonding pad dimensions

NAME	DIMENSION
Pad pitch	70 μm
Pad size, aluminium	62 × 100 μm
Bump dimensions	50 × 90 × 17.5 (±5) μm
Wafer thickness (including bumps)	maximum 430 μm
Wafer thickness (without bumps)	typical 380 μm

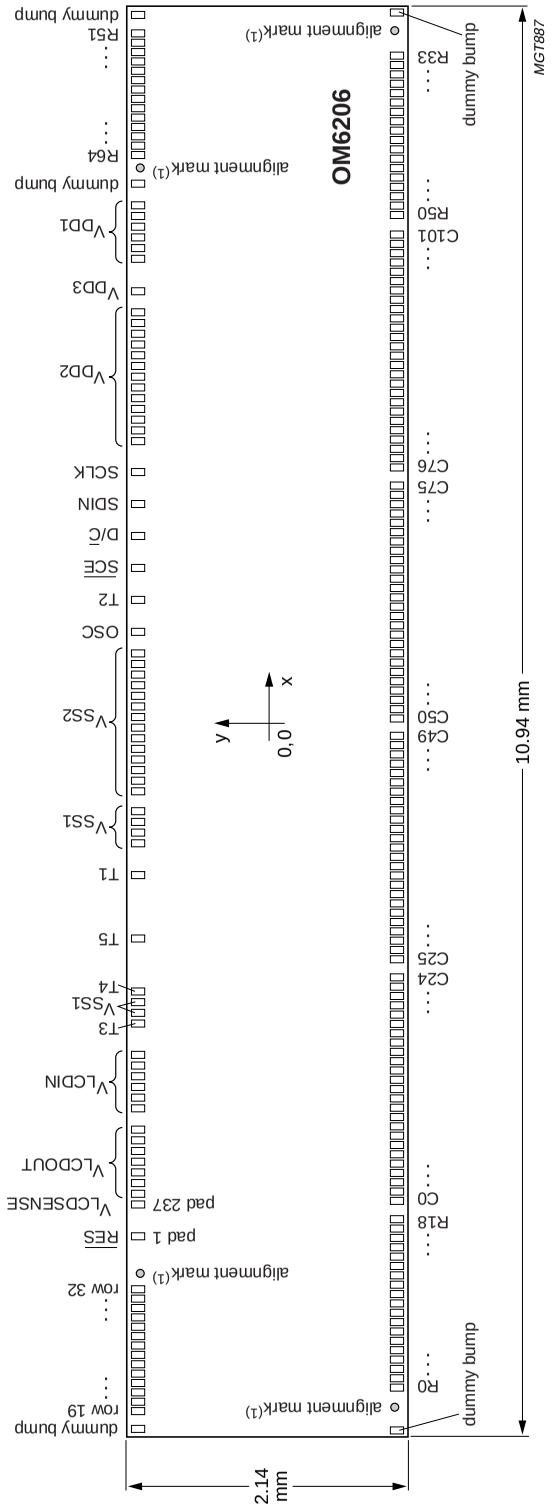
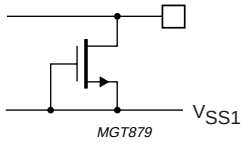
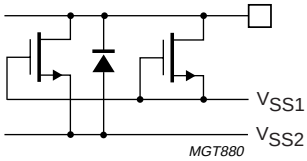
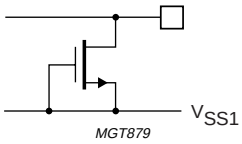
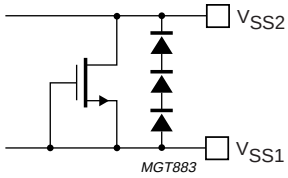
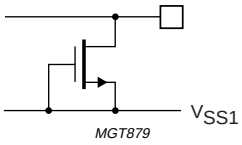
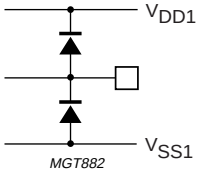
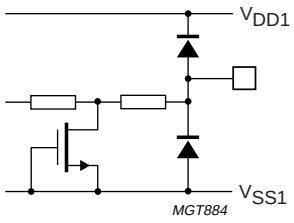
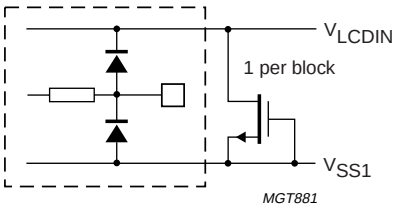


Fig.20 Bonding pad locations.

(1) The alignment marks are circles with a diameter of 100 µm.

15 DEVICE PROTECTION CIRCUITS

SYMBOL	PAD	INTERNAL CIRCUIT
V_{DD1}	174 to 179	
V_{DD2}	181 to 193	
V_{DD3}	180	
V_{SS1}	214 to 217, 221, 222	
V_{SS2}	200 to 213	
V_{LCDIN}	224 to 229	
$V_{LCDSENSE}$	237	
V_{LCDOUT}	230 to 236	
T2	198	
T3	223	

SYMBOL	PAD	INTERNAL CIRCUIT
SDIN	195	
SCLK	194	
$\overline{SCE}$	197	
D/$\overline{C}$	196	
OSC	199	
$\overline{RES}$	1	
T1	217	
T4	218	
T5	220	
R0 to R64	2 to 15, 18 to 36, 139 to 156, 159 to 172	
C0 to C101	37 to 138	

16 TRAY INFORMATION

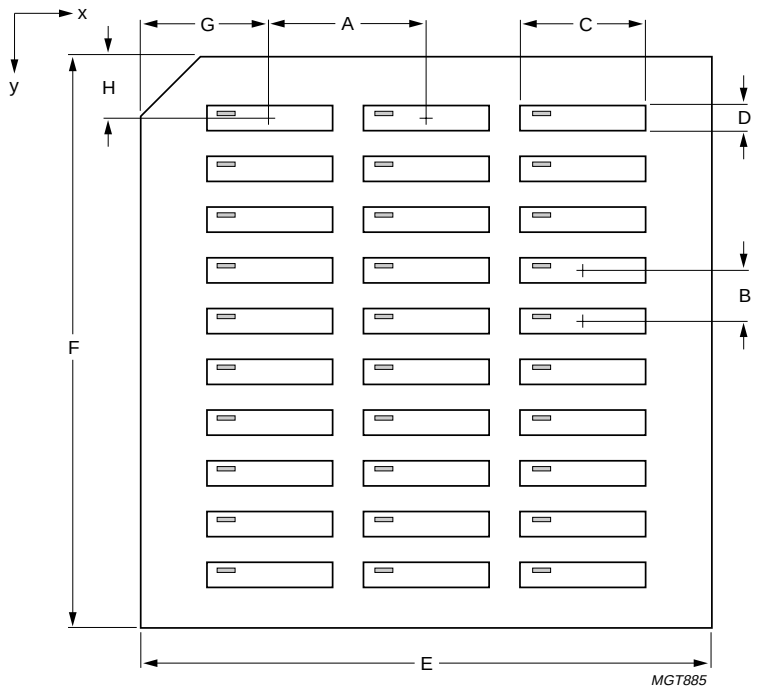
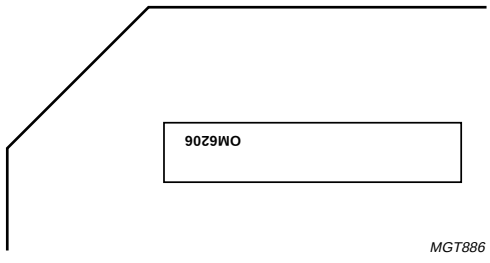


Fig.21 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.22 Tray alignment.

Table 10 Tray dimensions

DIMENSIONS	DESCRIPTION	VALUE
A	pocket pitch; in the x direction	13.77 mm
B	pocket pitch; in the y direction	4.45 mm
C	pocket width; in the x direction	11.04 mm
D	pocket width; in the y direction	2.24 mm
E	tray width; in the x direction	50.8 mm
F	tray width; in the y direction	50.8 mm
G	distance from cut corner to pocket centre	11.63 mm
H	distance from cut corner to pocket centre	5.41 mm
x	number of pockets in the x direction	3
y	number of pockets in the y direction	10

17 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES