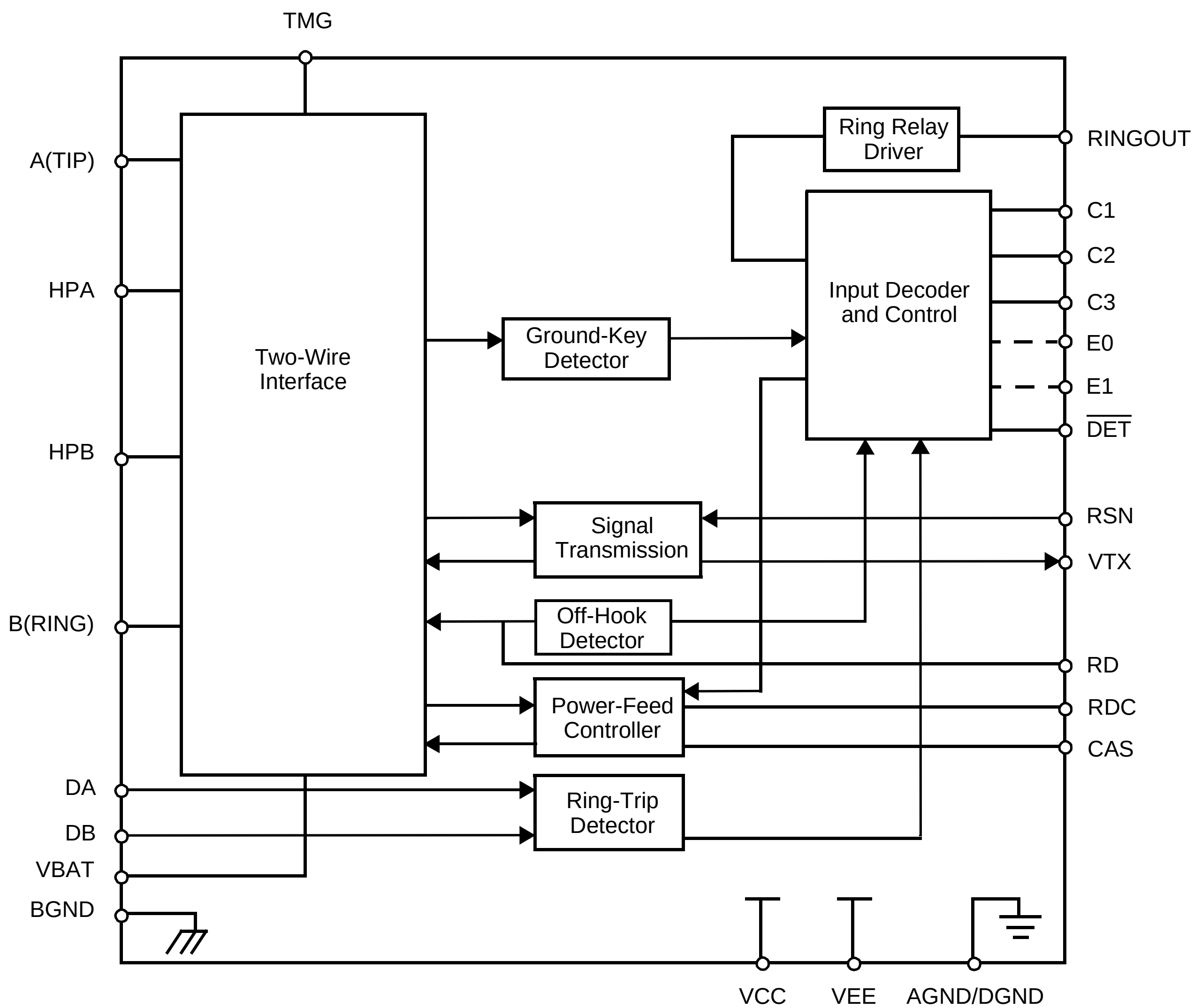
Am7945

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Programmable constant-current feed**
- **Current gain = 200**
- **Programmable loop-detect threshold**
- **Low power Standby state**
- **Ground-key detector**
- **Tip Open state for ground-start lines**
- **–19 V to –56.5 V battery operation**
- **On-chip Thermal Management (TMG) feature**
- **Two-wire impedance set by single external impedance**
- **On-hook transmission**
- **On-chip ring relay driver and relay snubber circuit**
- **Ideal for low cost PABX and key telephone systems**

BLOCK DIAGRAM



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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am7945 **J** **C**

TEMPERATURE RANGE
C = Commercial (0°C to 70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)

DEVICE NUMBER/DESCRIPTION
Am7945
Subscriber Line Interface Circuit

Valid Combinations	
Am7945	JC

Valid Combinations

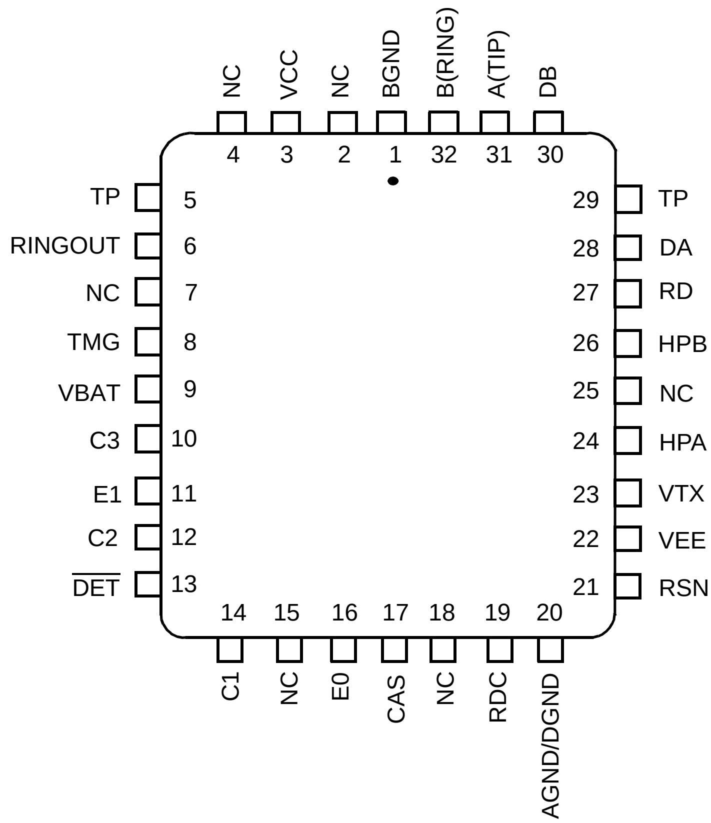
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:
** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAM

Top View

32-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*
3. *NC = No Connect*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and digital ground
A(TIP)	Output	Output of A(TIP) power amplifier
BGND	Gnd	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-Trip Negative. Negative input to ring-trip comparator.
DB	Input	Ring-Trip Positive. Positive input to ring-trip comparator.
$\overline{DET}$	Output	Switchhook Detector. When enabled, a logic Low indicates the selected detector is tripped. The detect condition is selected by the logic inputs (C3–C1, E0, E1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E0	Input	Ground-Key Enable. A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$ (PLCC only).
E1	Input	Ground-Key Enable. E1 = Low connects the ground-key or ring-trip detector to $\overline{DET}$. E1 = High connects the off-hook or ring-trip detector to $\overline{DET}$ (PLCC only).
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
RD	Resistor	Detect Resistor. Threshold modification and filter point for the off-hook detector.
RDC	Resistor	DC Feed Resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. Networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
TMG	—	Thermal Management. Connect an external resistor between this pin and the VBAT pin to reduce on-chip power dissipation in the normal polarity, Active state only. See Table 2.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.
VBAT	Battery	Battery supply
VCC	Power	+5 V power supply
VEE	Power	–5 V power supply
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . –55°C to +150°C

With respect to AGND/DGND:

V_{CC}. . . . . –0.4 V to +7.0 V

V_{EE}. . . . . +0.4 V to –7.0 V

V_{BAT}

Continuous . . . . +0.4 V to –70 V
10 ms . . . . +0.4 V to –75 V

BGND. . . . . +3 V to –3 V

A(TIP) or B(RING) with respect to BGND:

Continuous . . . . –70 V to +1 V
10 ms (f = 0.1 Hz) . . . . –70 V to +5 V
1 ms (f = 0.1 Hz) . . . . –80 V to +8 V
10 µs (f = 0.1 Hz) . . . . –100 V to +12 V

Current from A(TIP) or B(RING). . . . . ±150 mA

Current from TMG . . . . 100 mA

Voltage on RINGOUT:

During transient . . . . BGND to +10 V
During steady state. . . . . BGND to +7 V

Current through relay drivers . . . . 60 mA

DA and DB inputs

Voltage on ring-trip inputs . . . . V_{BAT} to 0 V
Current into ring-trip inputs . . . . ±10 mA

C3–C1, E0, E1
to AGND/DGND . . . . –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, T_A = 85°C
No heat sink (See note):

In 32-pin PLCC package. . . . . 1.4 W

Thermal data . . . . θ_{JA}

In 32-pin PLCC package. . . . . 43°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . 0°C to +70°C*

V_{CC} . . . . 4.75 V to 5.25 V

V_{EE} . . . . –4.75 V to –5.25 V

V_{BAT} . . . . –19 V to –56.5 V

AGND/DGND . . . . 0 V

BGND with respect to
AGND/DGND . . . . –100 mV to +100 mV

Load resistance on VTX to GND . . . . 10 kΩ min

The Operating Ranges define those limits over which the functionality of the device is guaranteed by production testing.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

The Am7945 device is tested under the following conditions unless otherwise noted: BAT = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 900 Ω. The device is not tested in Polarity Reversal state.

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog output (V_{TX}) impedance			3		Ω	
Analog output (V_{TX}) offset	0°C to +70°C –40°C to +85°C	–37 –40		+37 +40	mV	 4
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	Ω	4
Longitudinal impedance at A or B				35	Ω	
Overload level	4-wire and 2-wire, Active state	–2.5		+2.5	Vpk	2a
	On hook, R_{LAC} = 900 Ω, Active or OHT state	0.95			Vrms	2b
Transmission Performance						
2-wire return loss (See Test Circuit D)	200 to 3.4 kHz	26			dB	4, 8
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); R_L = 740 Ω at BAT = 48 V						
Longitudinal to metallic L-T, L-4 normal polarity	200 Hz to 1 kHz 0°C to +70°C –40°C to +85°C	52 50			dB	 4
	1 kHz to 3.4 kHz 0°C to +70°C –40°C to +85°C	52 50			dB	 4
Longitudinal signal generation 4-L	300 Hz to 800 Hz, normal polarity	40			dB	
Longitudinal current per pin	Active state and OHT state	20	27		mArms	
Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B) BAT = –48 V, R_L = 900 Ω						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	–0.15 –0.20		+0.15 +0.20	dB	 4
Gain accuracy, OHT state	–10 dBm, On hook, R_{LAC} = 900 Ω	–1.0		+1.0	dB	4
Variation with frequency	300 to 3.4 kHz, relative to 1 kHz 0°C to +70°C –40°C to +85°C	 –0.10 –0.15		 +0.10 +0.15	dB	 4
Gain tracking	+7 dBm to –55 dBm, reference 0 dBm 0°C to +70°C –40°C to +85°C	 –0.10 –0.15		 +0.10 +0.15	dB	 4 4
Balance Return Signal (4- to 4-Wire, See Test Circuit B) BAT = –48 V, R_L = 900 Ω						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	–0.15 –0.20		+0.15 +0.20	dB	3 4
Variation with frequency	300 to 3.4 kHz, relative to 1 kHz 0°C to +70°C –40°C to +85°C	 –0.10 –0.15		 +0.10 +0.15	dB	 3 4
Gain tracking	+3 dBm to –55 dBm, reference 0 dBm 0°C to +70°C –40°C to +85°C	 –0.10 –0.15		 +0.10 +0.15	dB	 3, 4 4
Group delay	f = 1 kHz			4	µs	4, 8
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire, See Test Circuits A and B) BAT = –48 V, R_L = 900 Ω						
Harmonic distortion 300 Hz to 3.4 kHz	2-wire level = 0 dBm 2-wire level = +7 dBm		–64 –55	–50 –40	dB	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Idle Channel Noise (2-Wire and 4-Wire)						
C-message weighted	2-wire, 0°C to +70°C –40°C to +85°C		+7 +7	+10 +12	dBrnc	4
	4-wire, 0°C to +70°C –40°C to +85°C		+7 +7	+10 +12		
Psophometric weighted	2-wire, 0°C to +70°C –40°C to +85°C		–83 –83	–78	dBmp	4
	4-wire, 0°C to +70°C –40°C to +85°C		–83 –83	–75		4
Line Characteristics, Active State (See Figure 1)						
Short loops, Active state	BAT = –48 V, R_{LDC} = 600 Ω	24.7		29.3	mA	
Long loops, Active state	BAT = –48 V, R_{LDC} = 1.9 kΩ	17.5				
OHT state	BAT = –48 V, R_{LDC} = 600 Ω	15.5		20.5		
Standby state	$I_L = \frac{\lvert V_{BAT} \rvert - 3\ V}{R_L + 1800}$ T_A = 25°C	$0.7I_L$	I_L	$1.3I_L$		
	R_L = 600 Ω, BAT = –48 V T_A = 70°C	15.0	17.4			
Loop current	Tip Open state, R_L = 0 Ω			100	µA	
	Disconnect state, R_L = 0 Ω			100		
	Tip Open state, Bwire to GND	21	30	44	mA	
	Tip Open state, Bwire = BAT + 6 V	20	30	45		
I_LLIM (I_{TIP} + I_{RING})	Tip and ring shorted to GND		100	130		
Ground-start signaling (tip voltage)	Active state, R_{TIP} to –48 V = 7.0 kΩ R_{RING} to GND = 100 kΩ	–7.5	–5.0		V	
Open circuit voltage	Active and OHT state, BAT = –48 V	40.5	42.0			
Power Dissipation, BAT = –48 V						
On hook, Open Circuit state			25	100	mW	
On hook, OHT state			120	210		
On hook, Active state	R_{TMG} = Open R_{TMG} = 1700 Ω		160 195	230 280		
On hook, Standby state			35	100		
Off hook, OHT state	R_L = 300 Ω, R_{TMG} = ∞, BAT = –48 V		735	1100		
Off hook, Active state	R_L = 300 Ω, R_{TMG} = ∞, BAT = –48 V R_L = 300 Ω, R_{TMG} = ∞		1.25 0.57	1.60 0.85	W	
Off hook, Standby state	R_L = 600 Ω, T_A = 25°C		0.68	1.0		

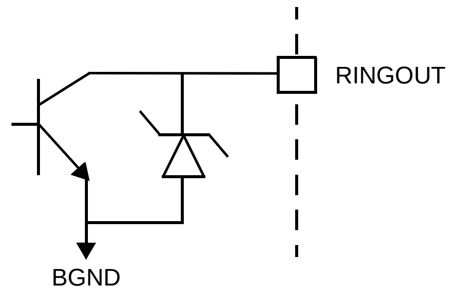
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents, BAT = –48 V						
V_{CC}, On-hook supply current	Open Circuit state OHT state Standby state Active state		1.7 4.9 2.2 6.3	2.5 7.5 3.0 8.5	mA	
V_{EE}, On-hook supply current	Open Circuit state OHT state Standby state Active state		0.7 2.0 0.77 2.1	2.0 3.5 2.0 5.0	mA	
V_{BAT}, On-hook supply current	Open Circuit state OHT state Standby state Active state		0.18 1.9 0.45 4.2	1.0 4.7 1.5 5.7	mA	
Power-Supply Rejection Ratio (V_{RIPPLE} = 50 mVrms), Active Normal State						
V_{CC}	50 Hz to 3.4 kHz	30	40		dB	5
V_{EE}	50 Hz to 3.4 kHz	28	35		dB	5
V_{BAT}	50 Hz to 3.4 kHz	28	50		dB	5
Effective internal resistance	CAS pin to GND	85	170	255	kΩ	4
RFI rejection	100 kHz to 30 MHz (See Figure E)			1.0	mVrms	4
Off-Hook Detector						
Current threshold	$I_{DET} = \frac{375}{R_D}$	–12		+12	%	
Ground-Key Detector Thresholds, Active State, BAT = –48 V						
Ground-key resistance threshold	B(RING) to GND	2.0	5.0	10.0	kΩ	
Ground-key current threshold	B(RING) to GND		9		mA	
Ring-Trip Detector Input						
Bias current		–0.5	–0.05		µA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Logic Inputs (C3–C1, E0, E1)						
Input High voltage		2.0			V	
Input Low voltage				0.8	V	
Input High current	All inputs except C3 and E1	–75		40	µA	
	Input C3	–75		200	µA	
	Input E1	–75		45	µA	
Input Low current		–0.4			mA	
Logic Output ($\overline{DET}$)						
Output Low voltage	I_{OUT} = 0.8 mA			0.4	V	
Output High voltage	I_{OUT} = –0.1 mA	2.4			V	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Relay Driver Output (RINGOUT)						
On voltage	35 mA sink		+0.25	+0.4	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	100 µA	6	7.2		V	
Zener On voltage	30 mA		10		V	

RELAY DRIVER SCHEMATIC

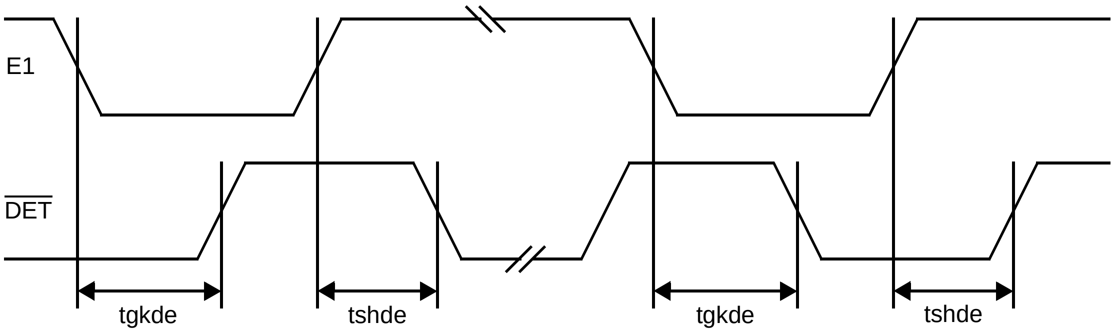


SWITCHING CHARACTERISTICS (32-Pin PLCC only)

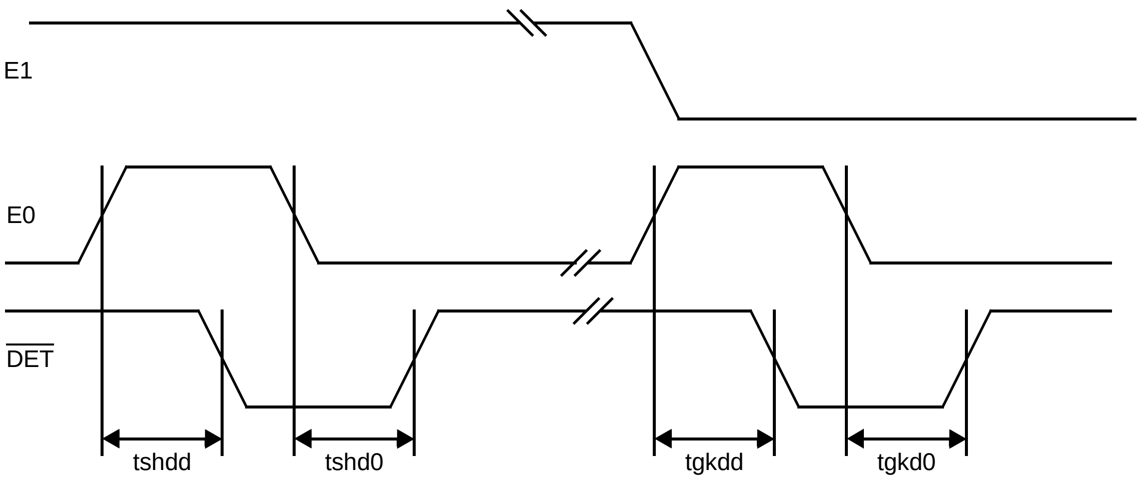
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C –40°C to +85°C			3.8 4.0	µs	4
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C –40°C to +85°C			1.1 1.6		
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)		0°C to +70°C –40°C to +85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to +70°C –40°C to +85°C			3.8 4.0		
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C –40°C to +85°C			1.2 1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C –40°C to +85°C			3.8 4.0		
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to +70°C –40°C to +85°C			1.1 1.6		
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to +70°C –40°C to +85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{DET}$



E0 to $\overline{DET}$

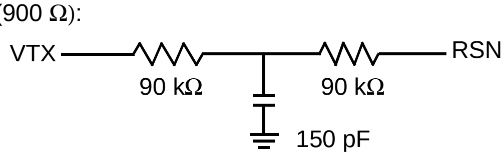


Note:
All delays measured at 1.4 V level.

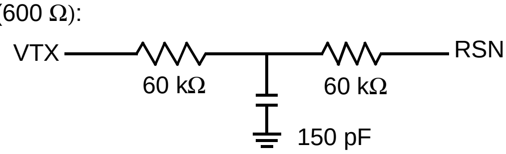
Notes:

1. *Unless otherwise noted, test conditions are V_{CC} = +5 V, V_{EE} = –5 V, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 9.26 kΩ, C_{DC} = 0.33 µF, R_D = 35.4 kΩ, C_{CAS} = 0.33 µF, no fuse resistors, BAT = –48 V, R_L = 900 Ω, and R_{TMG} = 1700 Ω.*
2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz with a termination impedance of 900 Ω and an R_L of 600 Ω in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Assumes the following Z_T networks:*

(900 Ω):



(600 Ω):



8. *Group delay can be considerably reduced by using a Z_T network such as that shown in Note 7 above. The network reduces the group delay to less than 2 µs. The effect of group delay on the linecard performance may be compensated for by using the QSLAC™ or DSLAC™ device.*

Table 1. SLIC Decoding

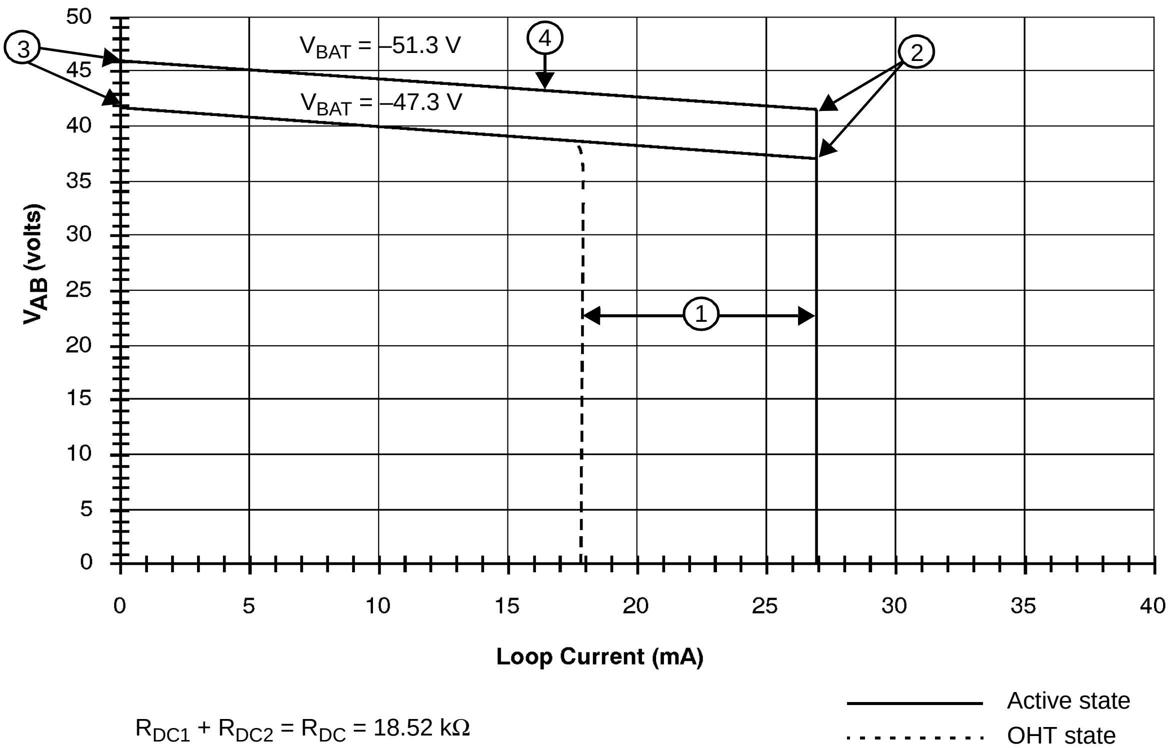
State	C3	C2	C1	2-Wire Status	$\overline{\text{DET}}$ Output E1 = 1	$\overline{\text{DET}}$ Output E1 = 0
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	On-Hook TX (OHT)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	Ground key
5	1	0	1	Standby	Loop detector	Ground key
6	1	1	0	Reserved		
7	1	1	1	Reserved		

Note:
E0 High enables $\overline{\text{DET}}$.

Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{200 \bullet Z_T}{Z_T + 200(Z_L + 2 \bullet R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5\ \text{ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{375}{I_T}, \quad C_D = \frac{0.5\ \text{ms}}{R_D}$	R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on hook and off hook.
$I_{OHT} = \frac{500\ \text{V} \bullet 0.66}{R_{DC1} + R_{DC2}}$	OHT loop current (constant-current region).
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cutoff frequency.
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \geq \frac{\lvert V_{BAT} \rvert - 6\ \text{V}}{I_{LOOP}}$	R_{TMG} is connected from T_{MG} to V_{BAT} and is used to limit power dissipation within the SLIC in Normal Active and Tip Open states only.
$P_{RTMG} = \frac{(\lvert V_{BAT} \rvert - 6\ \text{V} - (I_L \bullet R_L))^2}{R_{TMG}}$	Power dissipated in the T_{MG} resistor, R_{TMG}, during Active and Tip Open states.
$P_{SLIC} = \lvert V_{BAT} \rvert \bullet I_L - (P_{RTMG} - R_L(I_L)^2) + 0.12\ \text{W}$	Power dissipated in the SLIC while in Active and Tip Open states.

DC FEED CHARACTERISTICS



Notes:

1. *Constant-current region:*

Active state: $I_L = \frac{500}{R_{DC}}$

OHT state: $I_L = \frac{2}{3} \bullet \frac{500}{R_{DC}}$

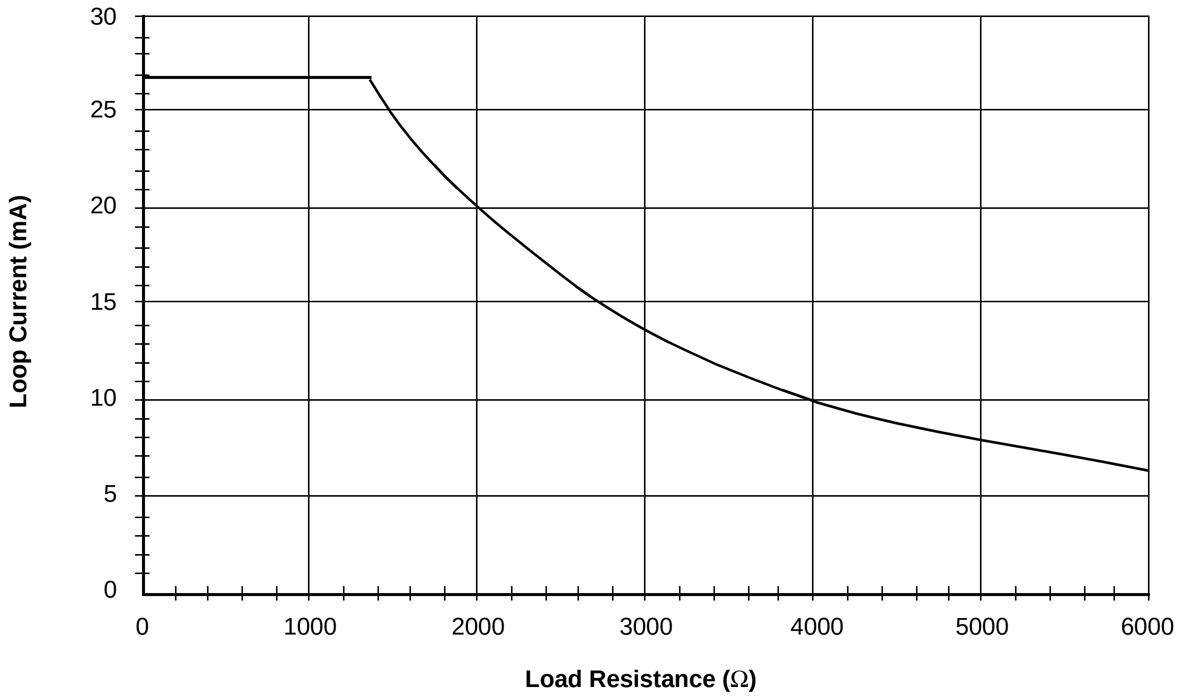
2. *Anti-sat (battery tracking) turn-on:* $V_{AB} = 1.017|V_{BAT}| - 10.7$

3. *Open circuit voltage:* $V_{AB} = 1.017|V_{BAT}| - 6.3$

4. *Anti-sat (battery tracking) region:* $V_{AB} = 1.017|V_{BAT}| - 6.3 - I_L \frac{R_{DC}}{120}$

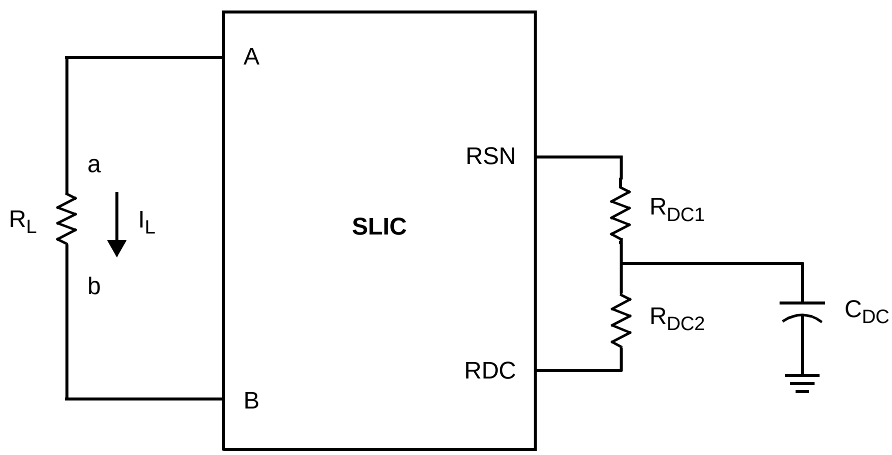
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



$R_{DC1} + R_{DC2} = R_{DC} = 18.52\ k\Omega$
$V_{BAT} = –47.3\ V$

b. Loop Current vs. Load Resistance (Typical)

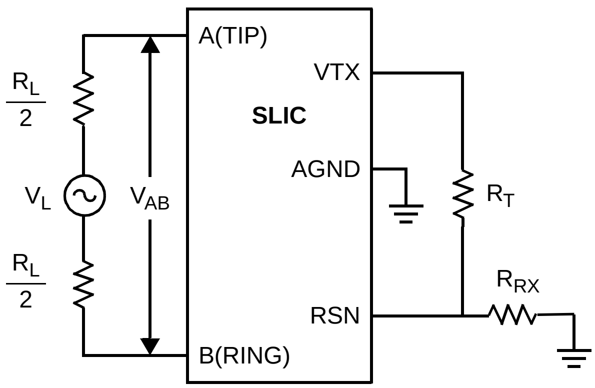


Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

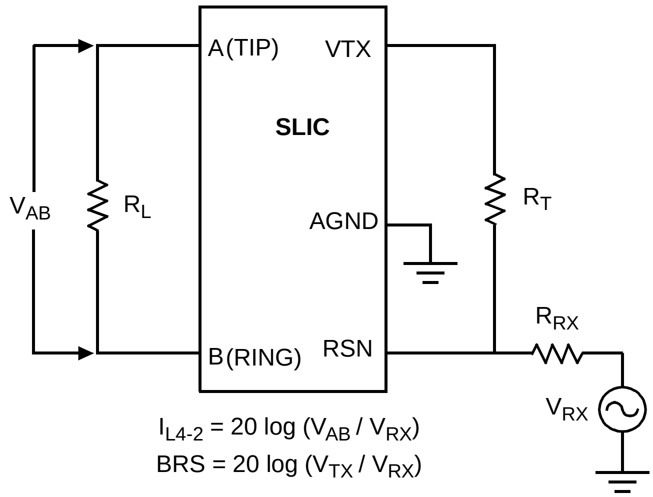
Figure 1. DC Feed Characteristics

TEST CIRCUITS



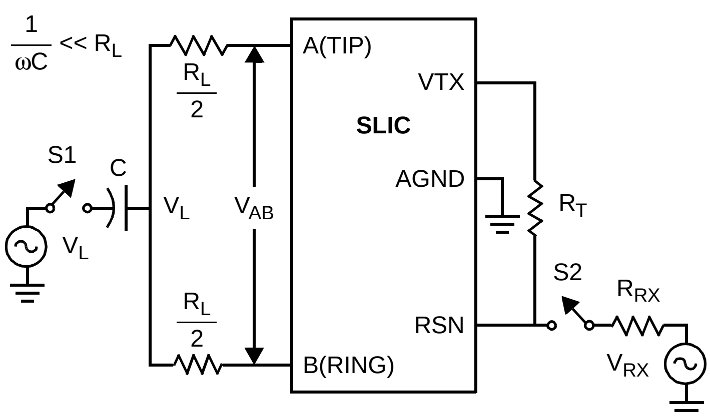
I_{L2-4} = 20 log (V_{TX} / V_{AB})

A. Two- to Four-Wire Insertion Loss



I_{L4-2} = 20 log (V_{AB} / V_{RX})
BRS = 20 log (V_{TX} / V_{RX})

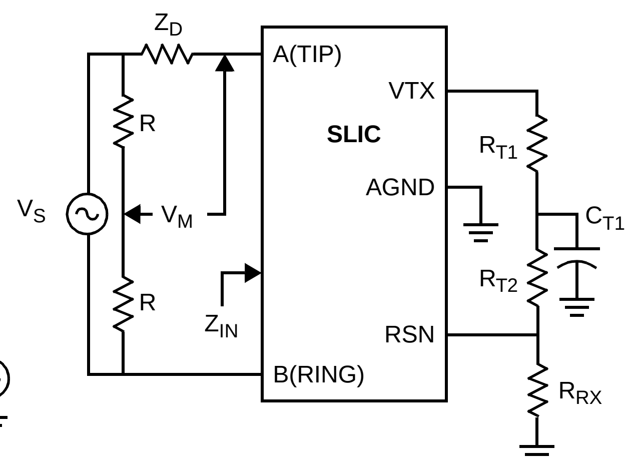
B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed
L-T Long. Bal. = 20 log (V_{AB} / V_L)
L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open
4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance

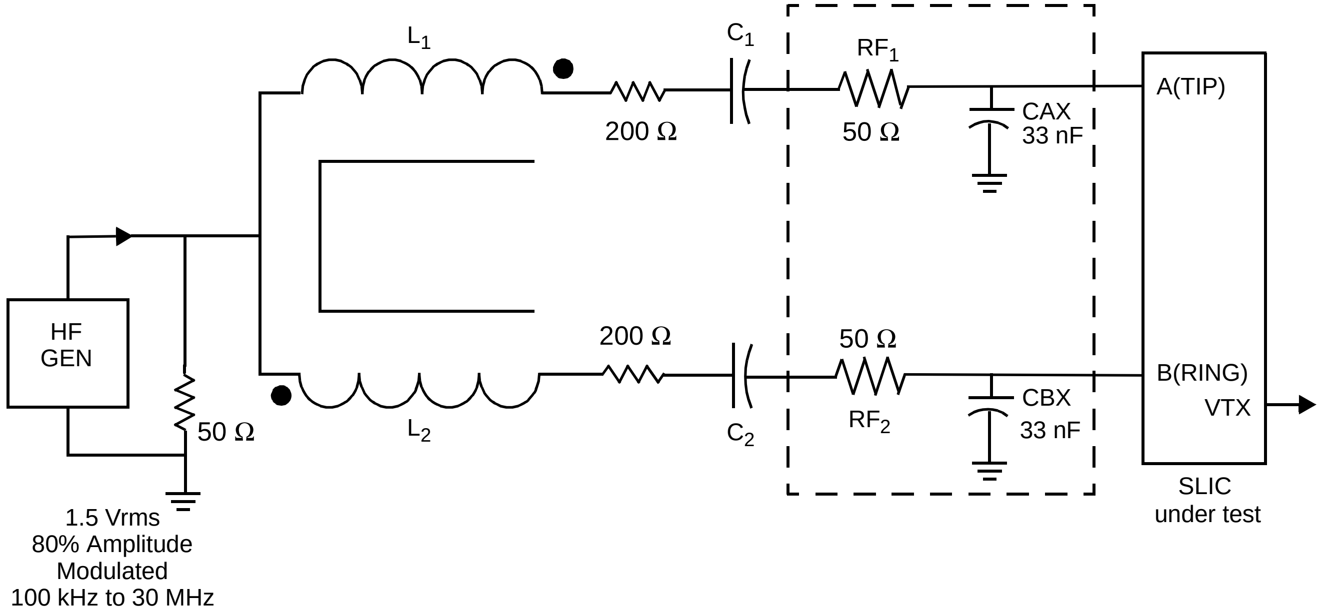


Note:
Z_D is the desired impedance (e.g., the characteristic impedance of the line).

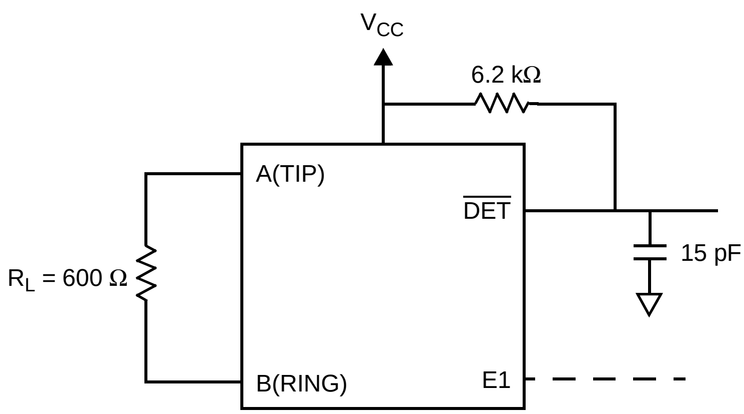
R_L = –20 log (2 V_M / V_S)

D. Two-Wire Return Loss Test Circuit

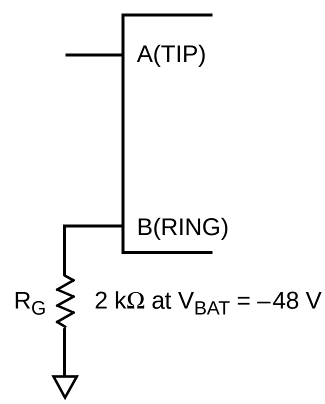
TEST CIRCUITS (continued)



E. RFI Test Circuit

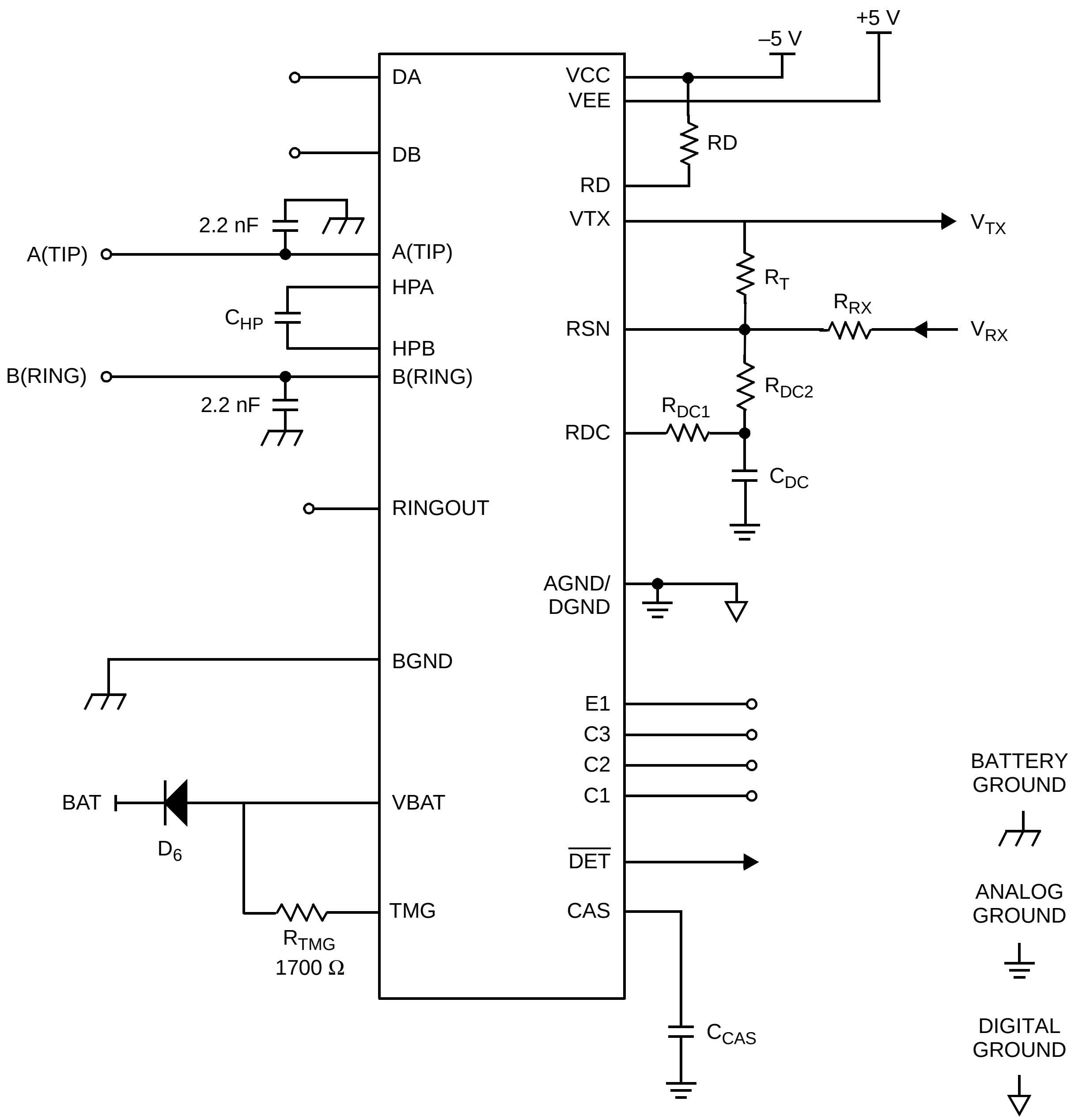


F. Loop-Detector Switching



G. Ground-Key Switching

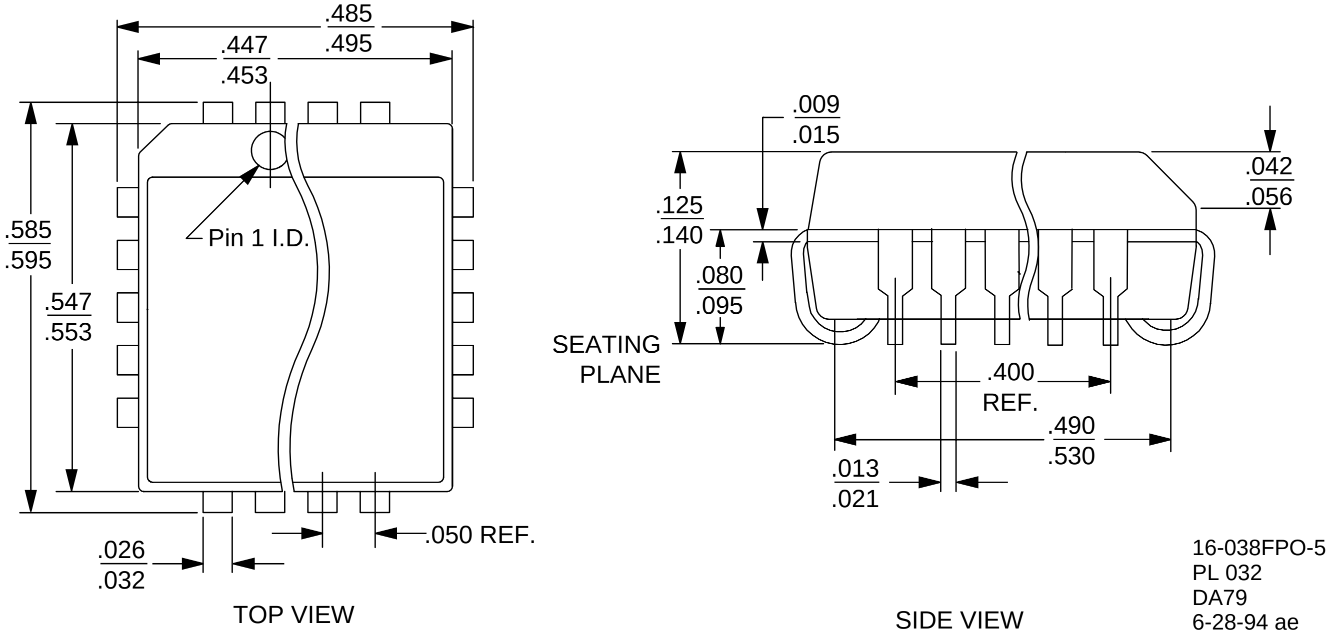
TEST CIRCUITS (continued)



H. Am7945 Test Circuit

PHYSICAL DIMENSION

PL032



REVISION SUMMARY

Revision A to B

- Minor changes were made to the data sheet style and format to conform to AMD standards.

Revision B to Revision C

- In the Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”

Revision C to Revision D

- Deleted information on the Ceramic DIP and Plastic DIP packages.
- The PL032 package was added to the new Physical Dimension section.
- Updated the Pin Description table to correct inconsistencies.