

# Triacs

## Silicon Bidirectional Triode Thyristors

... designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Quadrants

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage ( $T_J = -65$ to $+100^\circ\text{C}$ ) 1/2 Sine Wave 50 to 60 Hz, Gate Open 2N5571, 2N5573, 2N6145 2N5572, 2N5574, 2N6146 T4100M, T4110M, 2N6147	VDRM	200 400 600	Volts
*Peak Gate Voltage	VGM	20	Volts
*RMS On-State Current ( $T_C = -65$ to $+80^\circ\text{C}$ ) ( $T_C = +85^\circ\text{C}$ )	I <sub>T(RMS)</sub>	15 10	Amps
*Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceded and followed by rated current, $T_C = 85^\circ\text{C}$ )	I <sub>TSM</sub>	100	Amps
Circuit Fusing ( $T_C = -65$ to $+80^\circ\text{C}$ , $t = 1$ to 8.3 ms)	I <sup>2</sup> t	40	A <sup>2</sup> s
Peak Gate Power *( $T_C = 80^\circ\text{C}$ , Pulse Width = 1 $\mu\text{s}$ ) 2N5571 thru 2N5574 T4100M, T4110M *( $T_C = 80^\circ\text{C}$ , Pulse Width = 2 $\mu\text{s}$ ) 2N6145 thru 2N6147	PGM	16 16 20	Watts
*Average Gate Power ( $T_C = 80^\circ\text{C}$ , Pulse Width = 8.3 ms)	PG(AV)	0.5	Watt
*Peak Gate Current	I <sub>GM</sub>	2	Amps
*Operating Junction Temperature Range	T <sub>J</sub>	-65 to +100	°C
*Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Stud Torque *2N5573, 2N5574, T4110M *2N6145, 2N6146, 2N6147	—	30	in. lb.

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	R <sub>θJC</sub>	1	°C/W

\*Indicates JEDEC Registered Data.

**2N5571  
thru  
2N5574  
2N6145  
thru  
2N6147  
T4100M  
T4110M**

**TRIACS  
15 AMPERES RMS  
200 thru 600 VOLTS**



**CASE 174-04  
(TO-203)  
STYLE 3  
2N5571  
2N5572  
T4100M**



**CASE 175-03  
STYLE 3  
2N5573  
2N5574  
T4110M**



**CASE 311-02  
STYLE 2  
2N6145  
2N6146  
2N6147**

## 2N5571 thru 2N5574 • 2N6145 thru 2N6147 • T4100M • T4110M

ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ , and Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated $V_{DRM}$ or $V_{RRM}$ ) $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	$I_{DRM}$ , $I_{RRM}$	—	—	10 2	$\mu\text{A}$ mA
*Peak On-State Voltage ( $I_{TM} = 21$ A Peak, Pulse Width = 1 to 2 ms, Duty Cycle $\leq 2\%$ )	$V_{TM}$	—	1.3	1.8	Volts
Gate Trigger Current (Continuous dc), Note 1 ( $V_D = 12$ Vdc, $R_L = 30$ Ohms) MT2(+), G(+); MT2(-), G(-) MT2(+), G(-); MT2(-), G(+) *MT2(+), G(+); MT2(-), G(-), $T_C = -65^\circ\text{C}$ *MT2(+), G(-); MT2(-), G(+), $T_C = -65^\circ\text{C}$	$I_{GT}$	—	—	50 80 150 200	mA
Gate Trigger Voltage (Continuous dc) (All Quadrants) ( $V_D = 12$ Vdc, $R_L = 30$ Ohms) $T_C = 25^\circ\text{C}$ $*T_C = -65^\circ\text{C}$ $*(V_D = \text{Rated } V_{DRM}, R_L = 10 \text{ k ohms}, T_C = +100^\circ\text{C})$	$V_{GT}$	— — 0.2	— — —	2.5 4 —	Volts
Holding Current ( $V_D = 12$ Vdc, Gate Open) (Initiating Current = 500 mA) $T_C = 25^\circ\text{C}$ $*T_C = -65^\circ\text{C}$	$I_H$	— —	— —	75 300	mA
Gate Controlled Turn-On Time (Rated $V_{DRM}$ , $I_{TM} = 21$ A Peak, $I_{GT} = 160$ mA, Rise Time = 0.1 $\mu\text{s}$ , Pulse Width = 2 $\mu\text{s}$ )	$t_{gt}$	—	1	2	$\mu\text{s}$
*Critical Rate-of-Rise of Commutation Voltage (Rated $V_{DRM}$ , $I_{TM} = 21$ A Peak, Commutating $di/dt = 8$ A/ms, gate unenergized $T_C = 80^\circ\text{C}$ 2N5571 thru 2N5574, T4100M, T4110M $T_C = 75^\circ\text{C}$ 2N6145 thru 2N6147	$dv/dt(c)$	2 2	10 10	— —	$\text{V}/\mu\text{s}$
Critical Rate-of-Rise of Off-State Voltage (Rated $V_{DRM}$ , Exponential Voltage Rise, Gate Open, $T_C = 100^\circ\text{C}$ ) *2N5571, 2N5573, 2N6145 *2N5572, 2N5574, 2N6146 T4100M, T4110M, 2N6147	$dv/dt$	30 20 10	150 100 75	— — —	$\text{V}/\mu\text{s}$

\*Indicates JEDEC Registered Data.

Note 1. All Voltage polarities referenced to main terminal 1.

2N5571 thru 2N5574 • 2N6145 thru 2N6147 • T4100M • T4110M

FIGURE 1 - RMS CURRENT DERATING

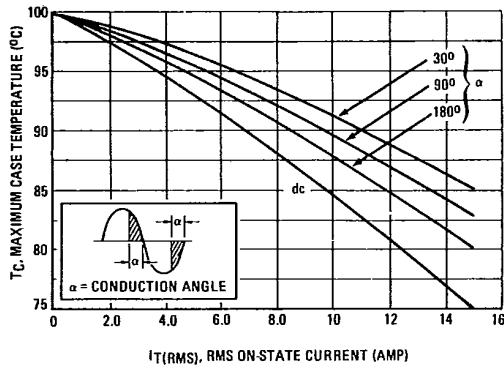


FIGURE 2 - ON-STATE POWER DISSIPATION

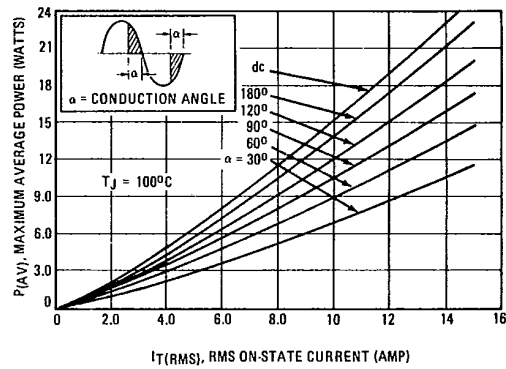


FIGURE 3 - TYPICAL GATE TRIGGER VOLTAGE

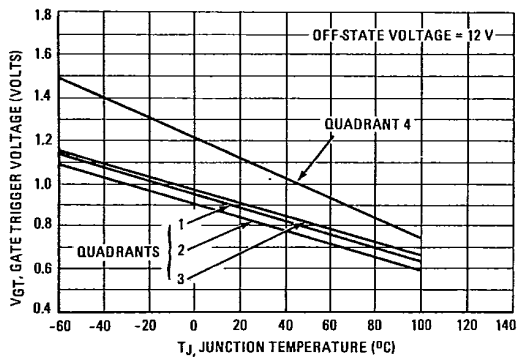
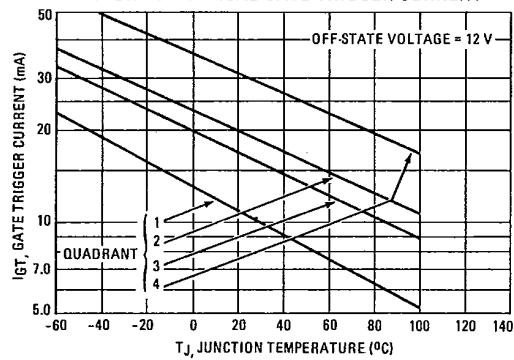


FIGURE 4 - TYPICAL GATE TRIGGER CURRENT



2N5571 thru 2N5574 • 2N6145 thru 2N6147 • T4100M • T4110M

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FIGURE 5 - MAXIMUM ON-STATE CHARACTERISTICS

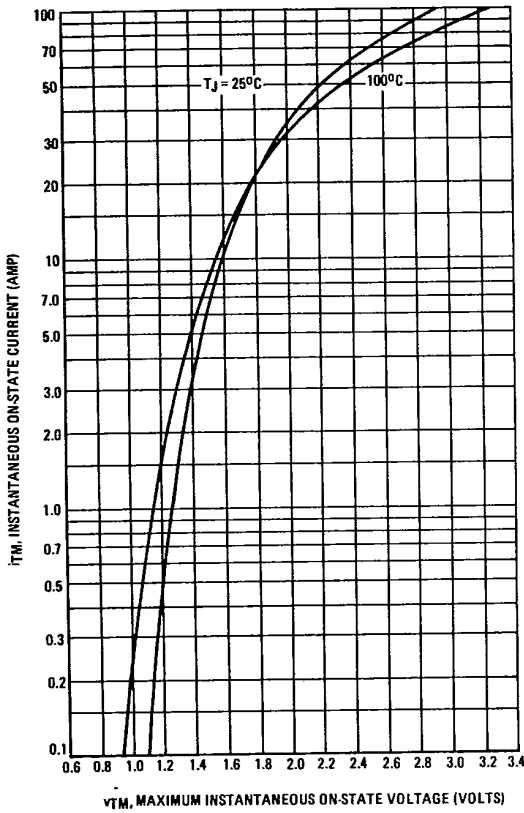


FIGURE 6 - TYPICAL HOLDING CURRENT

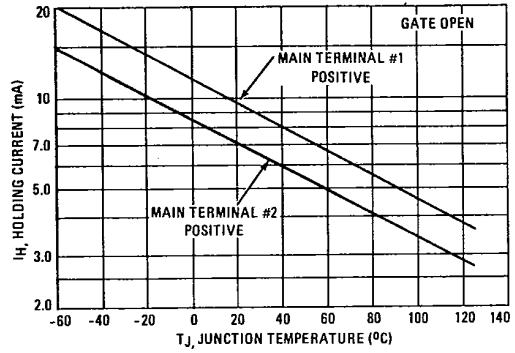


FIGURE 7 - MAXIMUM NON-REPETITIVE SURGE CURRENT

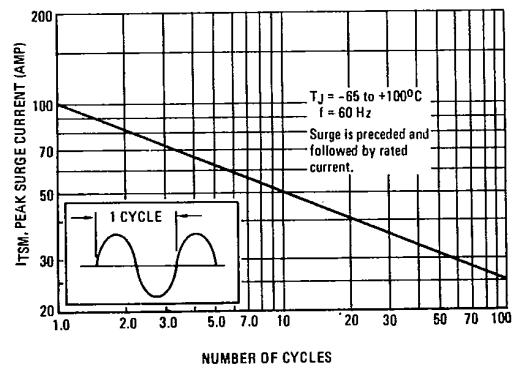


FIGURE 8 - TYPICAL THERMAL RESPONSE

