Preliminary Information[1] *(See Last Page)*

Dual Channel Supply Voltage Marginer and Active DC Output Controller

FEATURES & APPLICATIONS

- **Extremely accurate (±0.1%) Active DC Output Control (ADOC)**
- **ADOC Automatically adjusts supply output voltage level under all load conditions**
- **Capable of margining supplies with trim inputs using either positive or negative trim pin control**
- **Wide Margin/ADOC range from 0.3V to VDD**
- **Uses either an internal or external VREF**
- **Operates from any intermediate bus supply from 8V to 15V and from 2.7V to 5.5V**
- **Programmable START and READY pins**
- **Two programmable general purpose monitor sensors – UV and OV with FAULT Output Flag**
- **General Purpose 1k EEPROM with Write Protect**
- **I^2C 2-wire serial bus for programming configuration and monitoring status.**
- **28 lead QFN package**

Applications

- **In-system test and control of Point-of-Load (POL) Power Supplies for Multi-voltage Processors, DSPs and ASICs**
- **Enterprise and edge routers, servers, Storage Area Networks**

INTRODUCTION

The SMM205 actively controls the output voltage level of two DC/DC converters that use a Trim or VADJ/FB pin to adjust the output. An Active DC Output Control (ADOC) feature is used during normal operation to maintain extremely accurate settings of supply voltages and, during system test, to control margining of the supplies using I^2C commands. Total accuracy with a ±0.1% external reference is ±0.2%, and ±0.5% using the internal reference. The device can margin supplies with either positive or negative trim pin control within a range of 0.3V to VDD. The SMM105 supply can be from 12V, 8V, 5V or 3.3V to as low as 2.7V to accommodate any intermediate bus supply.

The voltage settings (margin high/low and nominal) are programmed into nonvolatile memory through the industry standard I^2C 2-wire data bus. The I^2C bus is also used to enable margin high, margin low, ADOC or normal operation. When margining, the SMM205 checks the voltage output of the converter and make adjustments to the trim pin via a feedback loop to bring the voltage to the margin setting. A margining status register is set to indicate that the system is ready for test. The SMM205 ADOC continues to monitor and adjust the channel output at the specified level.

SIMPLIFIED APPLICATIONS DRAWING

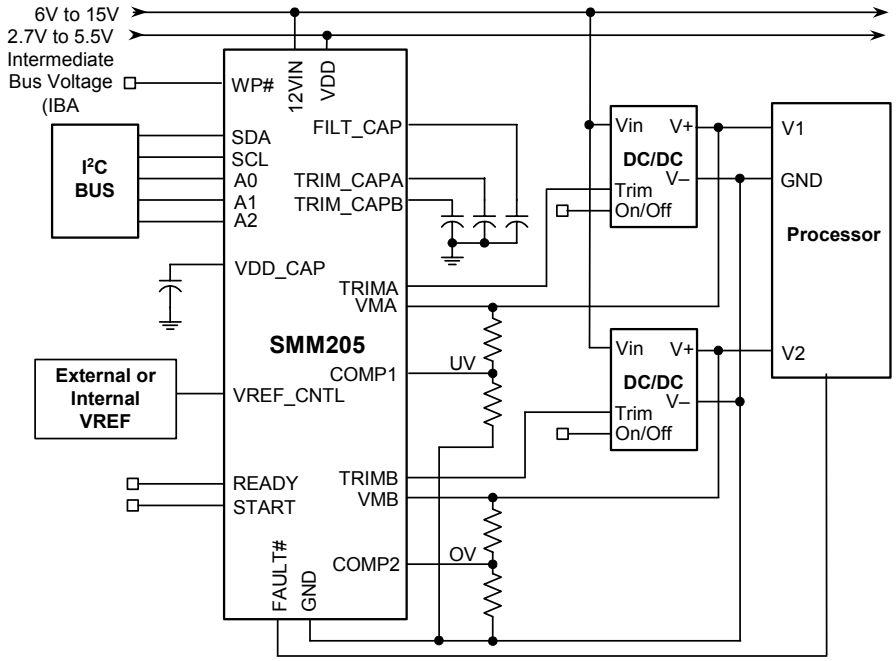


Figure 1 – Applications Schematic showing the SMM205 ADOC actively control the DC output level of 2 DC/DC Converters as well as provide margin control. The SMM205 can operate over a wide supply range

Note: This is an applications example only. Some pins, components and values are not shown.

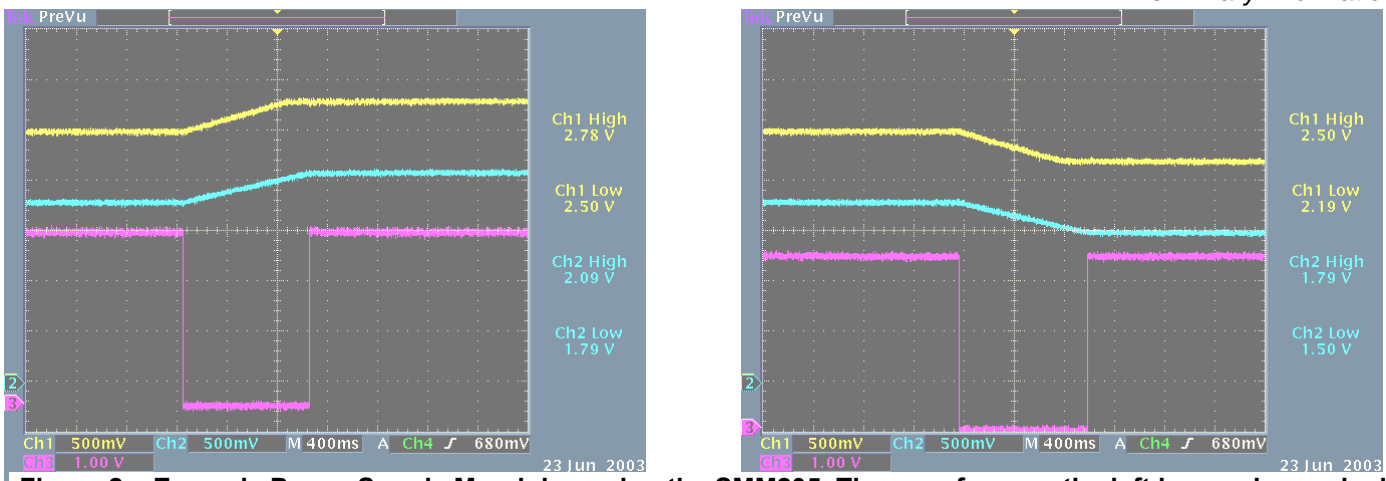


Figure 2 – Example Power Supply Margining using the SMM205. The waveform on the left is margin nominal to high from 2.5V to 2.8V and 1.8V to 2.1V. The waveform on the right is margin nominal to low from 2.5V to 2.2V and 1.8V to 1.5V. The bottom waveform is the READY signal indicating when margining is complete.

GENERAL DESCRIPTION

The SMM205 is capable of controlling and margining the DC output voltage of LDOs or DC/DC converters that use a trim/adjust pin and to automatically change the level using a unique Active DC Output Control (ADOC). The ADOC function is programmable over a standard 2-wire I^2C serial data interface and can be used to set the nominal DC output voltage as well as the margin high and low settings. The part actively controls the programmed set levels to maintain tight control over load variations and voltage drops at the point of load. The margin range will vary depending on the supply manufacturer and model but the normal range is 10% adjustment around the nominal output setting. However, the SMM205 has the capability to margin from VREF_CNTL to VDD.

The user can set the desired voltage settings (nominal, margin high and margin low) into the EE memory array for the device. Then, volatile registers are used to select one of these settings. The registers are accessed over the I^2C bus.

In normal operation, Active DC Output Control is set to adjust the nominal output voltage of one or two trimmed converters. Typical converters have ±2% accuracy ratings for their output voltage. Using the Active DC Output Control feature of the SMM205 can increase the accuracy to ±0.2%. This high accuracy control of a converter output voltage is extremely important in low voltage applications where deviations in power supply voltage can result in lower system performance. Active DC Output Control may be turned off by de-selecting the function in the Control Select Register. Active DC Output Control can also be used for margining a supply during system test.

When the SMM205 receives the command to margin the Active DC Output Control will adjust the supply to the selected margin voltage. Once the supply has reached its margined set point the Ready bit in the status register will set and the READY pin will go active. If Active DC Control is disabled a margined supply can return to its nominal voltage by writing to the margin command register.

In order to obtain maximum accuracy the SMM205 requires an external voltage reference. An external reference with ±0.1% accuracy will enable an overall ±0.2% accuracy for the device. A configuration option also exists so that an internal voltage reference can be used, but with less accuracy. Total accuracy using the internal reference is ±0.5%. The SMM205 can be powered from either a 12V or 8V input via an internal regulator, or the VDD input (Figure 3).

The SMM205 has two additional input pins and one additional output pin. The input pins, COMP1 and COMP2, are high impedance inputs, each connected to a comparator and compared against the VREF_CNTL input or the internal reference (VREF). Each comparator can be independently programmed to monitor for UV or OV. When either of the COMP1 or COMP2 inputs are in fault the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output during margining.

Programming of the SMM205 is performed over the industry standard I^2C 2-wire serial data interface. A status register is available to read the state of the part, and a Write Protect (WP#) pin is available to prevent writing to the configuration registers and EE memory.

INTERNAL BLOCK DIAGRAM

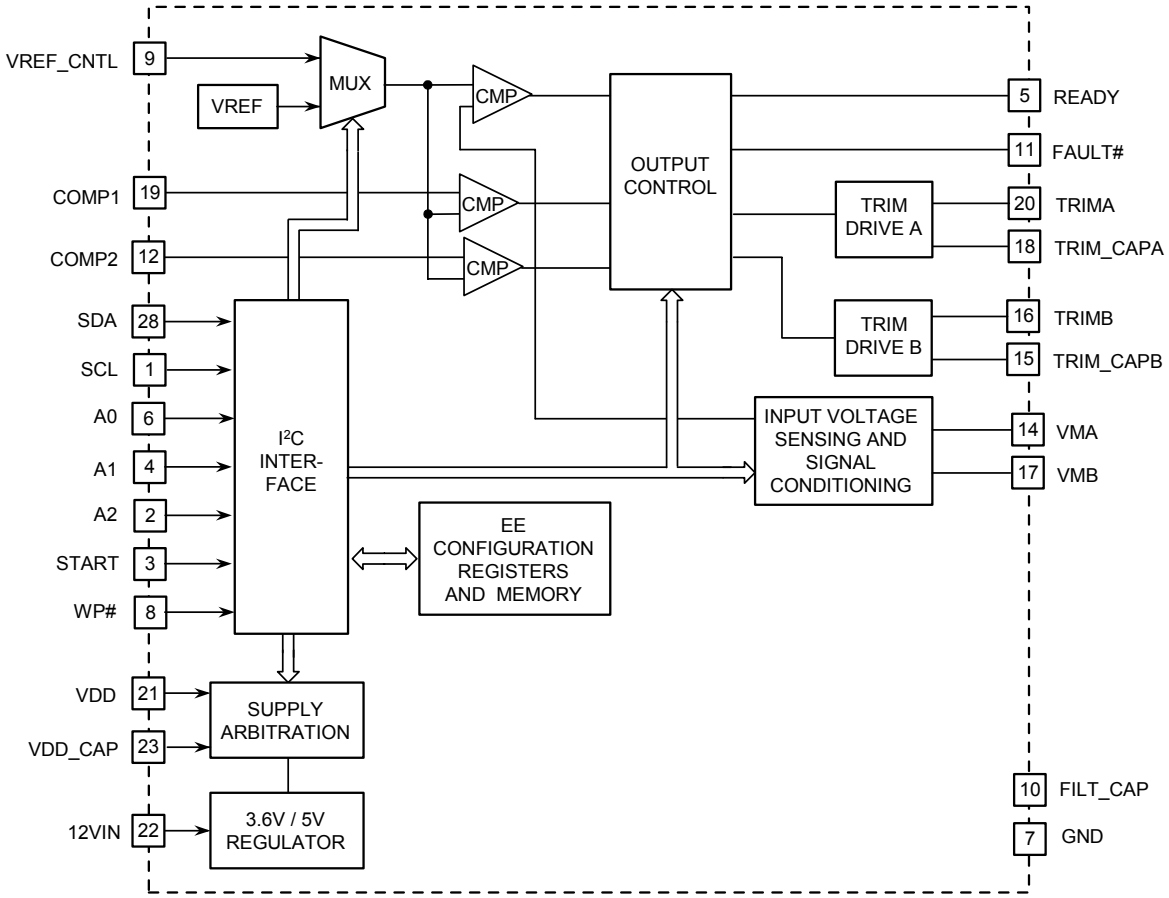
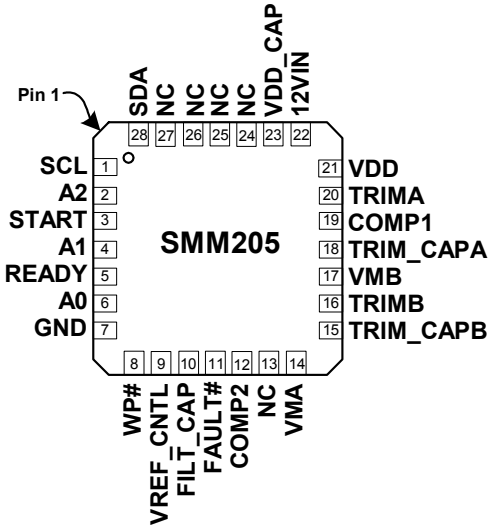


Figure 3 –Block Diagram.

PACKAGE AND PIN CONFIGURATION

28 Pin QFN
Top View



PIN DESCRIPTIONS

Pin Number	Pin Type	Pin Name	Pin Description
28	DATA	**SDA**	I^2C Bi-directional data line.
1	CLK	**SCL**	I^2C clock input.
2	I	**A2**	The address pins are biased either to VDD_CAP or GND. When communicating with the SMM205 over the 2-wire bus these pins provide a mechanism for assigning a unique bus address.
4	I	**A1**	
6	I	**A0**	
8	I	**WP#**	Write Protect active low input. When asserted writes to the configuration registers and general purpose EE are not allowed.
10	CAP	**FILT_CAP**	External capacitor input used to filter the VM inputs.
15, 18	CAP	**TRIM_CAPx**	External capacitor input used for Active Control and margining.
16, 20	O	**TRIMx**	Output voltage used to control and/or margin converter voltages. Connect to the converter trim input.
14, 17	I	**VMx**	Voltage monitor input. Connect to the DC/DC converter positive sense line or its +Vout pin.
9	I	**VREF_CNTL**	Voltage reference input used for DC output control and margining. VREF_CNTL can be programmed to output the internal 1.25V reference voltage. Pin should be left open if using VREF internal.
21	PWR	**VDD**	Power supply of the part.
7	GND	**GND**	Ground of the part. The SMM205 ground pin should be connected to the ground of the device under control or to a star point ground. PCB layout should take into consideration ground drops.
22	PWR	**12VIN**	12V power supply input internally regulated to either 3.6V or 5.5V. When using the 3.6V internal regulator option the voltage input can be as low as 8V. It can be as high as 15V using the 5.5V internal regulator.
3	I	**START**	Programmable active high/low input. The START input is used solely for enabling Active Control and/or margining.
5	I/O	**READY**	Programmable active high/low open drain output indicates that VM is at its set point. When programmed as an active high output READY can also be used as an input. When pulled low it will latch the state of the comparator inputs.
23	CAP	**VDD_CAP**	External capacitor input used to filter the internal supply rail.
19	I	**COMP1**	COMP1 and COMP2 are high impedance inputs, each connected internally to a comparator and compared against the VREF_CNTL input. Each comparator can be independently programmed to monitor for UV or OV. The monitor level is set externally with a resistive voltage divider.
12	I	**COMP2**	
11	O	**FAULT#**	When either of the COMP1 or COMP2 inputs are in fault the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output while the device is margining.
13, 24-27	NC	**NC**	No Connect. Leave floating; do not connect anything to the NC pins.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....–55°C to 125°C
Storage Temperature.....–65°C to 150°C
Terminal Voltage with Respect to GND:
VDD Supply Voltage .....–0.3V to 6.0V
12VIN Supply Voltage.....–0.3V to 15.0V
All Others .....–0.3V to V_{DD} + 0.7V
Output Short Circuit Current 100mA
Lead Solder Temperature (10 secs)…….300°C
Junction Temperature.....……...…..150°C
ESD Rating per JEDEC……..……..2000V
Latch-Up testing per JEDEC……..……...….±100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial) .....–40°C to +85°C
(Commercial).....–5°C to +70°C
VDD Supply Voltage..... 2.7V to 5.5V
12VIN Supply Voltage (1)..... 8.0V to 14.0V
VIN.....GND to VDD
VOUT.....GND to 15.0V
Package Thermal Resistance (θ_{JA})
28 Lead QFN……..…80°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020

Note (1) — Range depends on internal regulator set to 3.6V or 5.5V, see 12VIN specification below.

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
VDD	Supply Voltage		2.7	3.3	5.5	V
12VIN	Supply Voltage	Internally regulated to 5.5V	10		15	V
		Internally regulated to 3.6V	6		14	
VM	Positive Sense Voltage	VM pin	–0.3		VDD	V
I_{DD}	Power Supply Current from VDD	All TRIM pins and 12VIN floating		3	5	mA
I_{12VIN}	Power Supply Current from 12VIN	All TRIM pins and VDD floating		3	5	mA
I_{TRIM}	TRIM output current through 100Ω to 1.0V	TRIM Sourcing Max Current	1.5			mA
		TRIM Sinking Max Current	1.5			mA
V_{ADOC}	Margin Control/ADOC Range	Depends on Trim range of DC-DC Converter	VREF_CNTL		VDD	V
V_{IH}	Input High Voltage	VDD = 2.7V	0.9xVDD		VDD	V
		VDD = 5.0V	0.7xVDD		VDD	
V_{IL}	Input Low Voltage	VDD = 2.7V			0.1xVDD	V
		VDD = 5.0V			0.3xVDD	
V_{OL}	Programmable Open Drain Output (READY)	ISINK = TBD		0.2		V
OV/UV	Monitor Voltage Range	COMP1 and COMP2 pins	–0.3		VDD	V
V_{HYST}	Base DC Hysteresis	COMP1 and COMP2 pins, $V_{TH} – V_{TL}$ — Note 1	3	10		mV

Note 1 – The Base DC Hysteresis voltage is measured with a 1.25V external voltage source. The resulting value is determined by subtracting Threshold Low from Threshold High ($V_{TH} – V_{TL}$) while monitoring the FAULT# pin state. Base DC Hysteresis is measured with a 1.25V input. Actual DC Hysteresis is derived from the equation: (V_{IN}/V_{REF})(Base Hysteresis). For example, if V_{IN} = 2.5V and V_{REF} = 1.25V then Actual DC Hysteresis = (2.5V/1.25V) (0.003V) = 6mV.

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
VREF	1.25VREF Output Voltage	R_{LOAD} = 2KΩ to GND	1.24	1.25	1.26	V
V_{REF_CNTL}	External V_{REF} Voltage Range		0.25		VDD	V
$ADOC_{ACC}$	ADOC/Margin Accuracy	External VREF=1.25V, ±0.1%	-0.2		+0.2	%
		ADOC trimmed to internal VREF	-0.5		+0.5	%

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
$t_{DC\_CONTROl}$	Active DC Control sampling period	Update period for Active DC Control		1.7		ms
$T_{settling}$	Settling Time	± 10% change in voltage with 0.1% ripple		100		ms
T_{TRIM}	Trim Speed	Fast Margin, nom to high, TRIM_CAP=1μF		20		ms
		Slow Margin, nom to high, TRIM_CAP=1μF		200		ms

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100/400kHz

Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND. See Figure 4 Timing Diagram.

Symbol	Description	Conditions	100kHz			400kHz			
			Min	Typ	Max	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	0		400	KHz
t_{LOW}	Clock Low Period		4.7			1.3			µs
t_{HIGH}	Clock High Period		4.0			0.6			µs
t_{BUF}	Bus Free Time	Before New Transmission - Note 1/	4.7			1.3			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			0.6			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			0.6			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			0.6			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	0.2		0.9	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			0.2			µs
t_R	SCL and SDA Rise Time	Note 1/			1000			1000	ns
t_F	SCL and SDA Fall Time	Note 1/			300			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			150			ns
$t_{HD:DAT}$	Data In Hold Time		0			0			ns
TI	Noise Filter SCL and SDA	Noise suppression		100			100		ns
t_{WR}	Write Cycle Time				5			5	ms

Note: 1/ - Guaranteed by Design.

TIMING DIAGRAMS

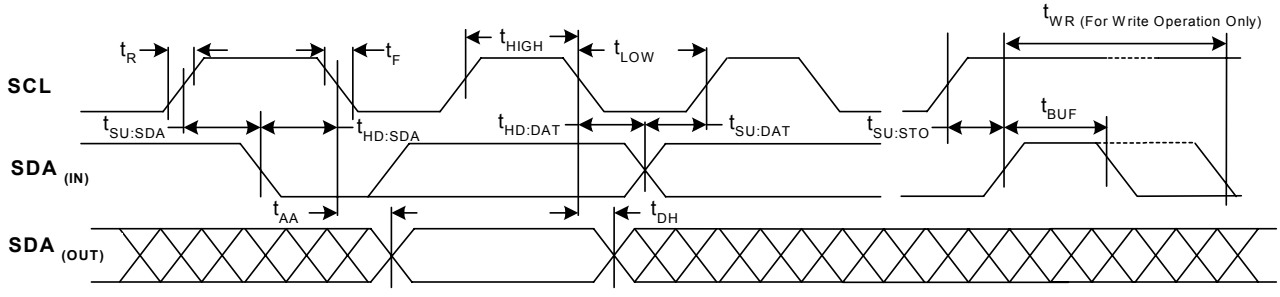


Figure 4 . Basic I²C Serial Interface Timing

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

The SMM205 can be powered by either an 8V to 15V input through the 12VIN pin or by a 2.7V to 5.5V input through the VDD pin. The 12VIN pin feeds an internal programmable regulator that internally generates either 5.5V or 3.6V. The internal regulator must be set to 3.6V if using an 8V supply. A voltage arbitration circuit allows the device to be powered by the highest voltage from either the regulator output or the VDD input. This voltage arbitration circuit continuously checks for these voltages to determine which will power the SMM205. The resultant internal power supply rail is connected to the VDD_CAP pin that allows both filtering and hold-up of the internal power supply.

VOLTAGE REFERENCE

The SMM205 can operate using either an internal or external voltage reference, VREF. The internal VREF is set to 1.25V. Total accuracy with a ±0.1% external reference is ±0.2%, and ±0.5% using the internal reference.

MODES OF OPERATION

The SMM205 has one key feature: Active DC Output Control (ADOC), and two basic modes of operation: UV/OV monitoring mode and supply margining mode. A detailed description of each feature and mode follows.

ACTIVE DC OUTPUT CONTROL (ADOC)

The SMM205 can control the DC output voltage of bricks or DC/DC converters that have a trim pin. The TRIM pin on the SMM205 is connected to the trim input pin on the power supply converter. A sense line from the channel's point-of-load connects to the VM input. The Active DC Control function cycles every 1.7ms making slight adjustments to the voltage on the TRIM output pin based on the voltage input on the VM pin. This voltage adjustment allows the SMM205 to control the output voltage of the power supply converter to within ±0.2% when using a ±0.1% external voltage reference.

The voltage on the TRIM_CAP pins is buffered and applied to the TRIM pin. The voltage adjustments on the TRIM pin cause a slight ripple of less than 1mV on the power supply voltage. The amplitude of this ripple is a function of the TRIM_CAP capacitor and the trim gain of the converter. Calculation of the TRIM_CAP capacitor to achieve a desired minimum ripple is detailed in Application Note 37.

The device can be programmed to either enable or disable the Active DC Control function. When disabled or not active the TRIM pin on the SMM205 is a high impedance input. The voltage on the TRIM pin is buffered and applied to the TRIM_CAP pin charging the capacitor. This allows a smooth transition from the converter's nominal voltage to the SMM205 controlling that voltage to the Active DC Control nominal setting.

There is a programmable Speed-Up Convergence option. As the name implies, this option decreases the time required to bring a supply voltage from the converter's nominal output voltage to the Active DC Output Control nominal voltage setting.

MONITORING

The SMM205 monitors the COMP1 and COMP2 inputs as well as the VM pins. COMP1 and COMP2 are high impedance inputs, each connected internally to a comparator and compared against the VREF_CNTL input. Each comparator can be independently programmed to monitor for either UV or OV. The monitor level is set externally with a resistive voltage divider. The part can be programmed to trigger the FAULT# pin when either COMPx comparator has exceeded the UV or OV range. The READY and FAULT# outputs of the SMM205 are active as long as the triggering limit remains in a fault condition. The READY pin is programmable active high/low open drain output indicates that VM is at its set point. When programmed as an active high output READY can also be used as an input. When pulled low it will latch the state of the comparator inputs. When either of the COMP1 or COMP2 inputs are in fault the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output while the device is in margining mode.

APPLICATIONS INFORMATION (CONTINUED)

STATUS REGISTER

A status register exists for I^2C polling of the status of the COMP1 and COMP2 inputs. Two bits in this status register reflect the current state of the inputs (1 = fault, 0 = no fault). Two additional bits show the state of the inputs latched by one of two events programmed in the configuration. The first event option is the FAULT# output going active. The second event option is the READY pin going low. The READY pin is an I/O. As an output the READY output pin goes active when the DC controlled voltages are at their set point. As an input programmed to active high it can be pulled low externally and latch the state of the COMP inputs. This second event option allows the state of the COMP inputs on multiple devices to be latched at the same time while a host monitors their FAULT# outputs.

MARGINING

The SMM205 has two additional Active DC Output Control voltage settings: margin high and margin low. The margin high and margin low settings can be as much as ±10% of the nominal setting depending on the manufacturer. The SMM205 range can be as large as VREF_CNTL to VDD. These settings are stored in the configuration registers and are loaded into the Active DC Output Control voltage setting by margin commands issued via the I^2C bus. The device must be enabled for Active DC Output Control in order to enable margining.

The margin command registers contain two bits that decode the commands to margin high, to margin low, or to control to the nominal setting. Once the SMM205 receives the command to margin the supply voltage it begins adjusting the supply voltage to move toward the desired setting. When this voltage setting is reached a bit is set in the margin status registers and the READY signal becomes active.

Note: Configuration writes or reads of registers 00_{HEX} to 03_{HEX} should not be performed while the SMM205 is margining.

WRITE PROTECTION

Write protection for the SMM205 is located in a volatile register where the power-on state is defaulted to write protect. There are separate write protect modes for the configuration registers and memory. In order to remove write protection the code 55_{HEX} is written to the write protection register. Other codes will also enable write protection. For example, writing 59_{HEX} will allow writes to the configuration register but not to the memory, while writing 35_{HEX} will allow writes to the memory but not to the configuration registers. The SMM205 also features a Write Protect pin (WP#) which, when asserted, prevents writing to the configuration registers and EE memory. In addition to these two forms of write protection there is also a configuration register lock bit which, once programmed, does not allow the configuration registers to be changed.

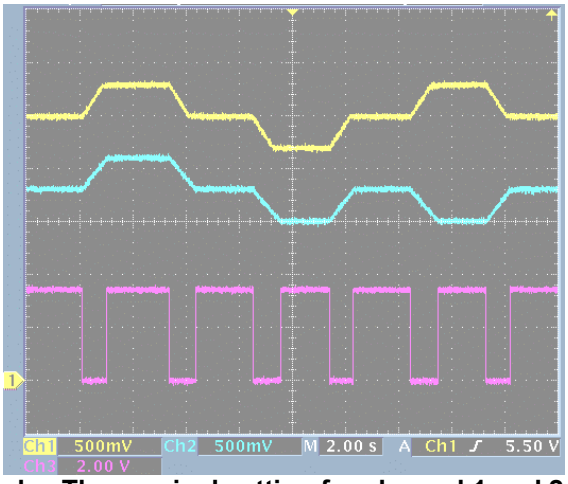


Figure 5 – SMM205 margin example. The nominal setting for channel 1 and 2 is 2.5V and 1.8V. The device margins the DC/DC converters from nominal to high (2.8V and 2.1) then to nominal, then to low (2.3V and 1.5V), then to nominal, then to channel 1 high and channel 2 low, and then back to nominal. The READY signals goes low when margining and high when complete.

APPLICATIONS INFORMATION (CONTINUED)

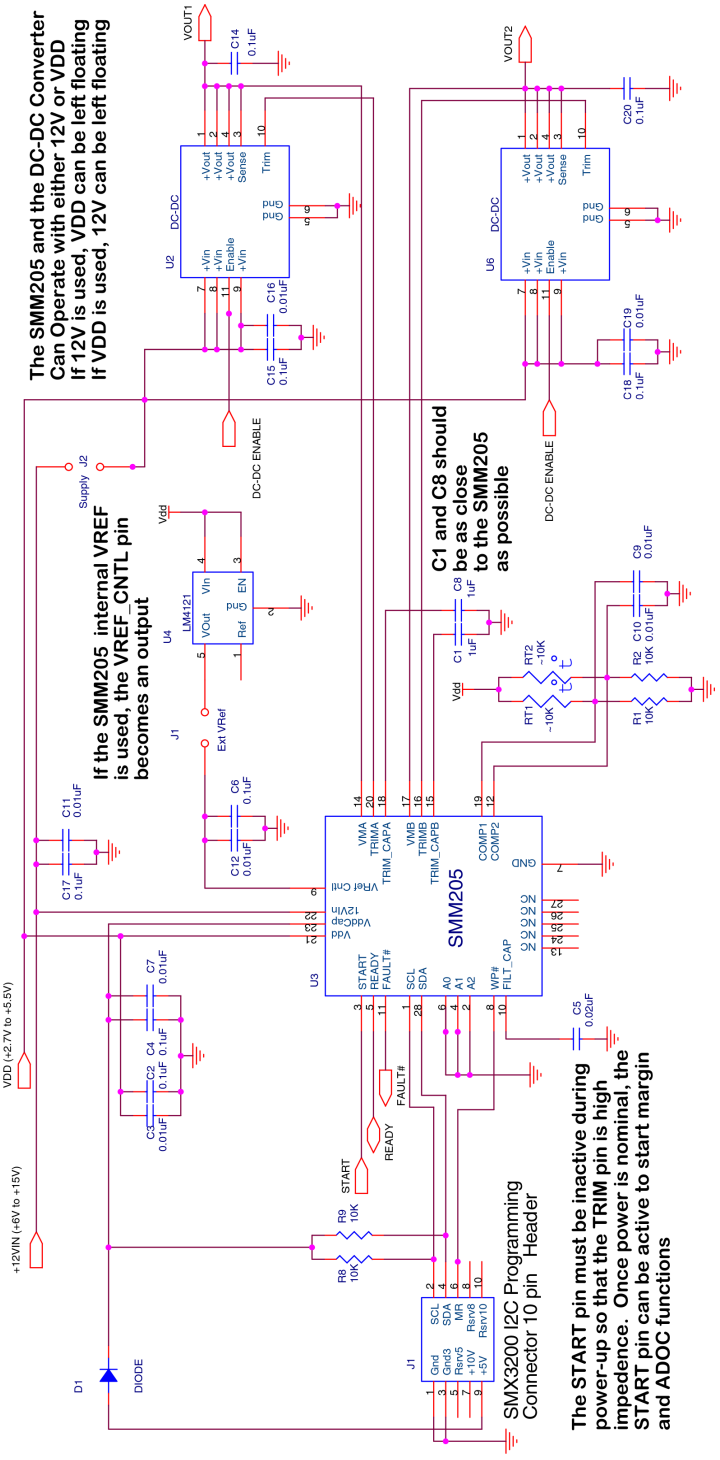


Figure 6 – SMM205 Applications schematic. The accuracy of the external (U4) or internal reference sets the accuracy of the ADOC function. Total accuracy with a ±0.1% external reference is ±0.2% and ±0.5% with the internal reference. The 12V supply can go as low as 8V if the internal regulator is set to 3.6V.

APPLICATIONS INFORMATION (CONTINUED)

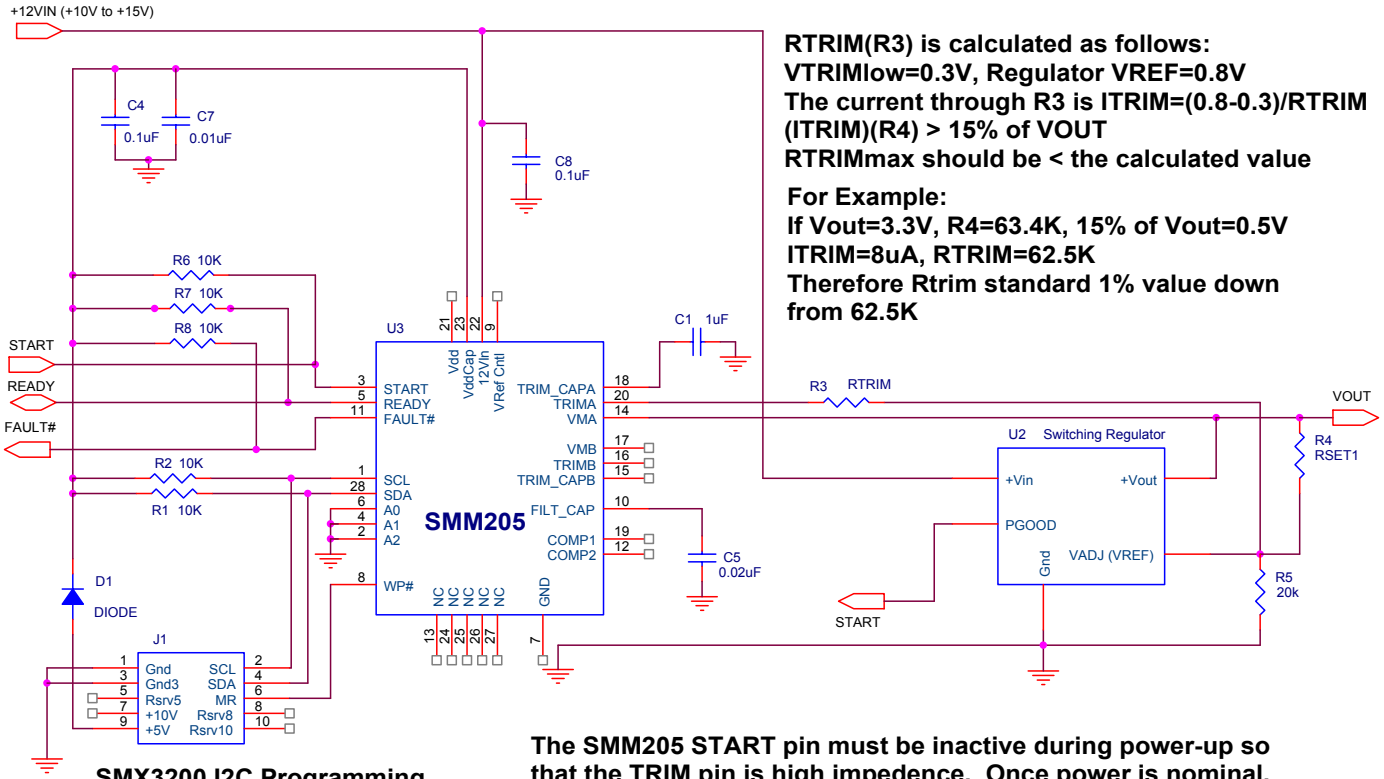


Figure 7 – SMM205 Applications schematic for an adjustable switching regulator (Full regulator circuit not shown).

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMM205 via the programming Dongle and cable. An example of the connection interface is shown in Figure 8.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

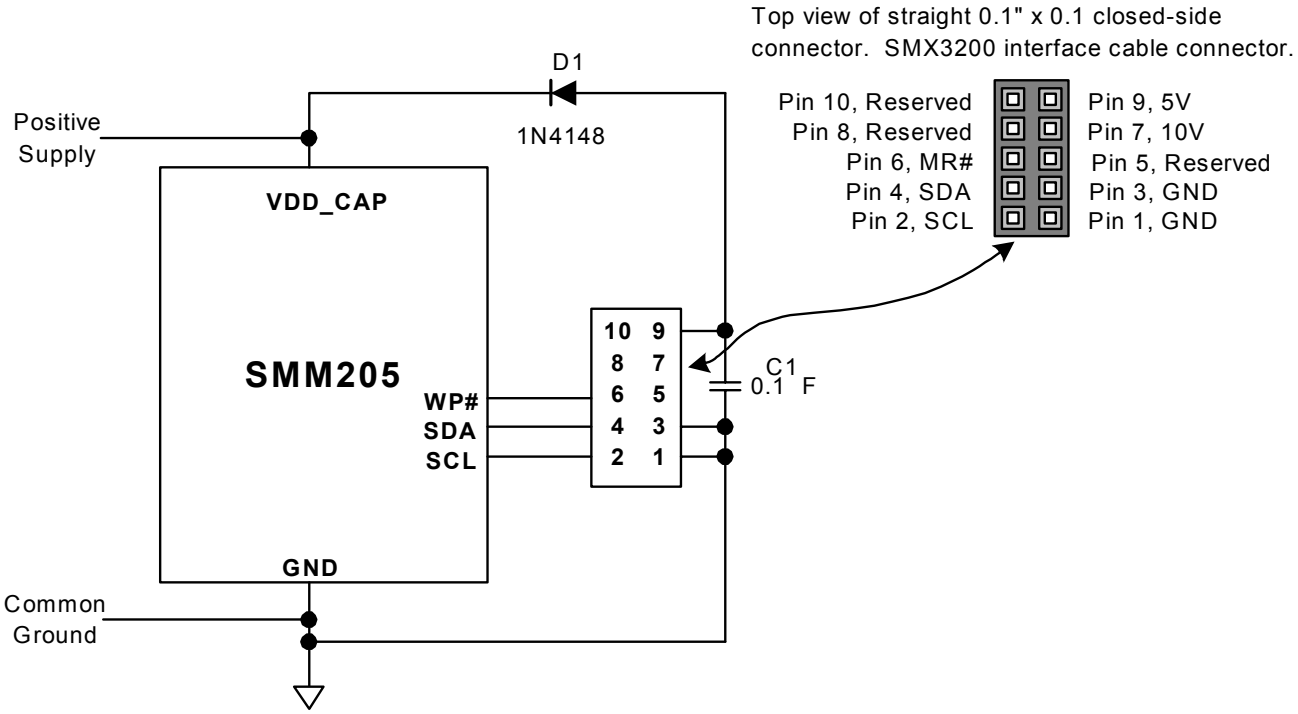


Figure 8– SMX3200 Programmer I^2C serial bus connections to program the SMM205. The SMM205 has a Write Protect pin (WP#) which, when asserted, prevents writing to the configuration registers and EE memory. In addition, there is a configuration register lock bit which, once programmed, does not allow the configuration registers to be changed.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition, while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 4-bit device type identifier (slave address) and a 3-bit bus address. The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMM205.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. It can be programmed to any four bit number 0000_{BIN} through 1111_{BIN}.

The bus address bits, A2, A1 and A0, are hard wired though pins 2, 4 and 6 (A2, A1 and A0). The bus address accessed in the address byte of the serial data stream must match the setting on the SMM205 address pins.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 9, 10, 11, 13, 14 and 16. A Start condition followed by the address byte is provided by the host; the SMM205 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMM205 responds with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page. After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the configuration registers, memory, command and status registers and ADC registers must be set before data can be read from the SMM205. This is accomplished by issuing a dummy write command, which is simply a write command that is not followed by a Stop condition. The dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figures 12, 15 and 17 for an illustration of the read sequence.

WRITE PROTECTION

The SMM205 powers up into a write protected mode. Writing a code to the volatile write protection register (write only) can disable the write protection. The write protection register is located at address 42_{HEX}. Writing to the write protection register is shown in Figure 9.

Writing 0101_{BIN} to bits [7:4] of the write protection register allows writes to the general-purpose memory while writing 0101_{BIN} to bits [3:0] allows writes to the configuration registers. The write protection can be re-enabled by writing other codes (not 0101_{BIN}) to the write protection register.

I²C PROGRAMMING INFORMATION (CONTINUED)

CONFIGURATION REGISTERS

The majority of the configuration registers are grouped with the general-purpose memory. Writing and reading the configuration registers is shown in Figures 10, 11 and 12.

Note: Configuration writes or reads of registers 00_{HEX} to 03_{HEX} should not be performed while the SMM205 is margining.

GENERAL-PURPOSE MEMORY

The 1k-bit general-purpose memory is located at any slave address. The bus address bits are hard wired by the address pins A2, A1 and A0. Memory writes and reads are shown in Figures 13, 14 and 15.

COMMAND AND STATUS REGISTERS

Writes and reads of the command and status registers are shown in Figures 16 and 17.

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMM205 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet and Application Note 38 simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMM205. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol. See figure 8 and the SMX3200 Data Sheet.

Slave Address	Bus Address	Register Type
ANY	A2 A1 A0	Configuration Registers are located in 00_{HEX} thru 45_{HEX}
		General-Purpose Memory is located in 80_{HEX} thru FF_{HEX}

Table 1 - Address bytes used by the SMM205.

I²C PROGRAMMING INFORMATION (CONTINUED)

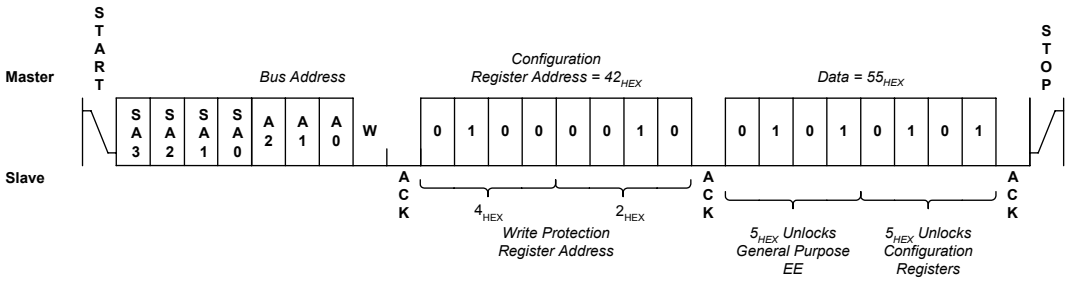


Figure 9 – Write Protection Register Write

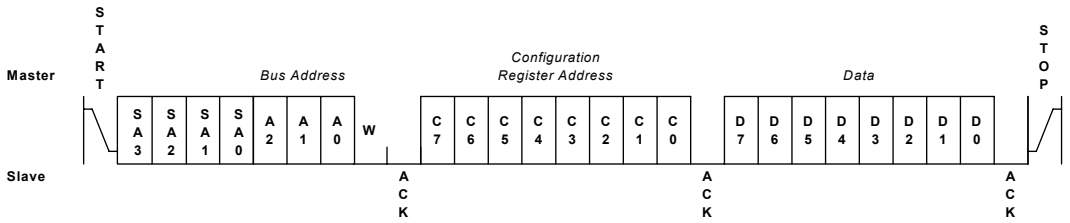


Figure 10 – Configuration Register Byte Write

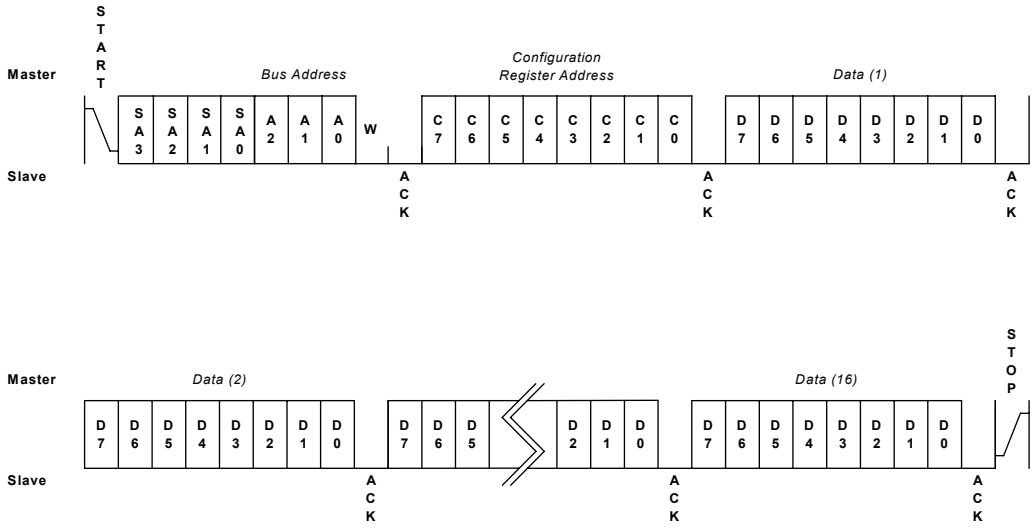


Figure 11 – Configuration Register Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

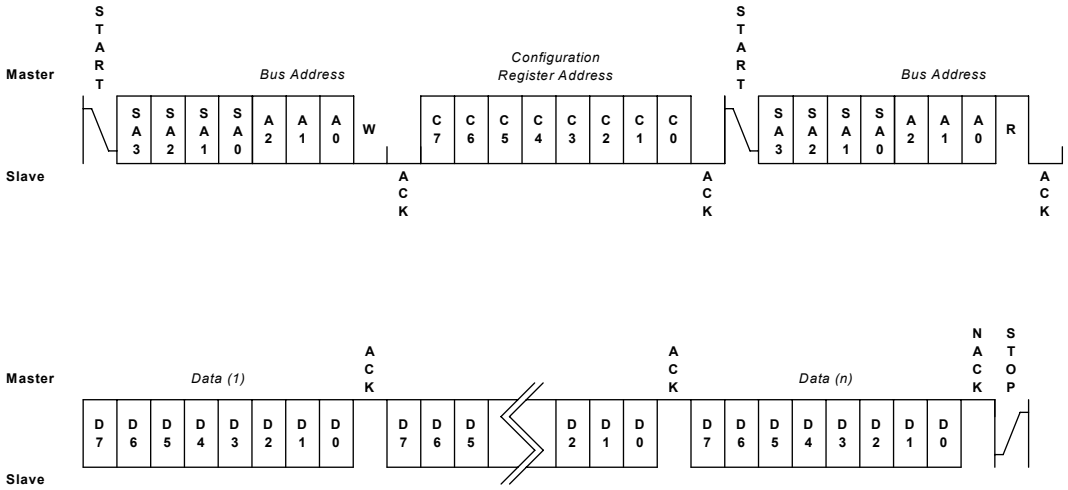


Figure 12 - Configuration Register Read

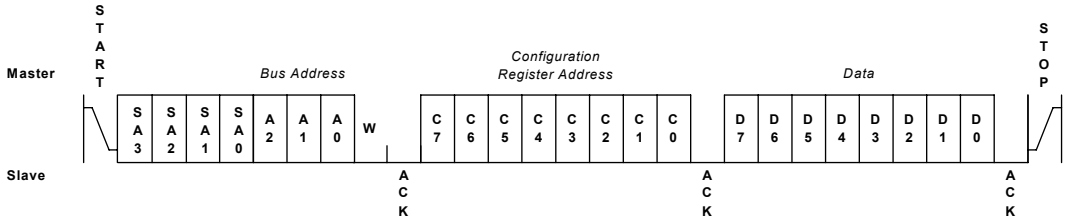


Figure 13 – General Purpose Memory Byte Write

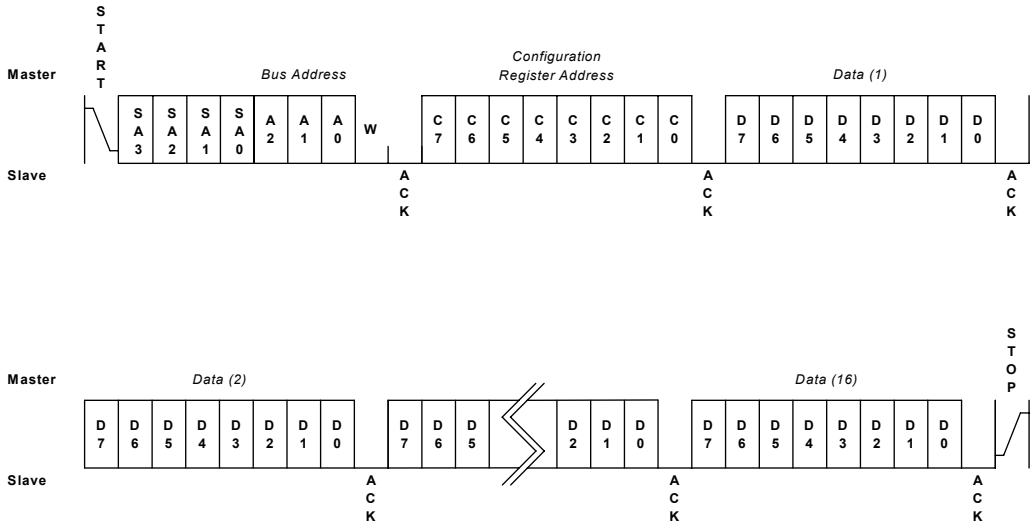


Figure 14 - General Purpose Memory Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

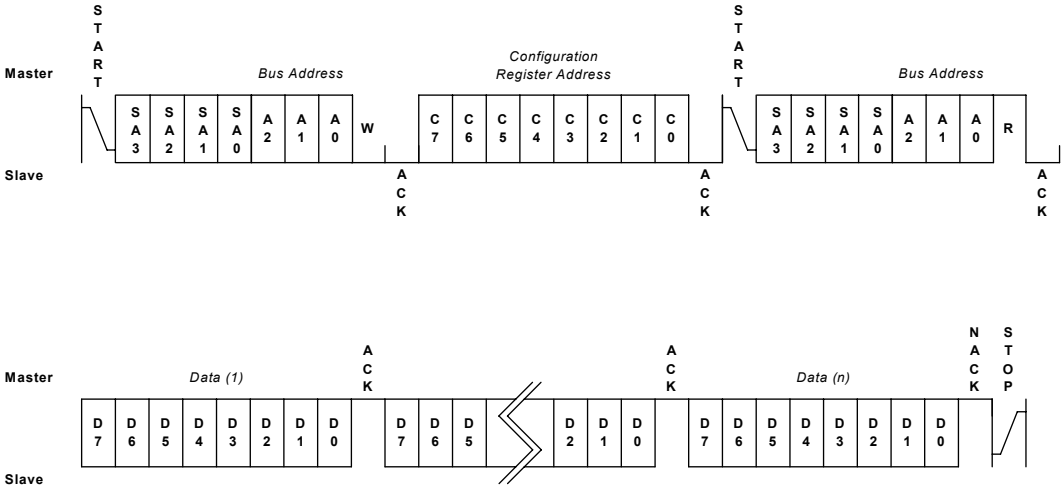


Figure 15 - General Purpose Memory Read

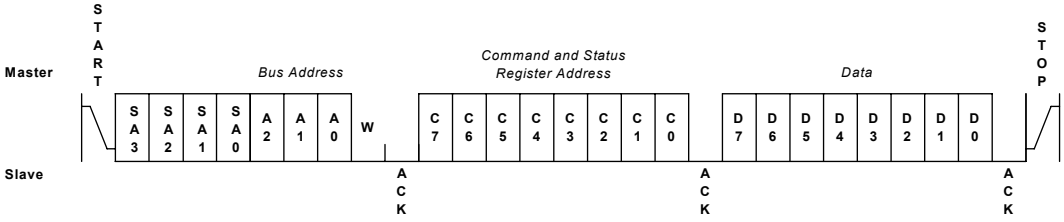


Figure 16 – Command and Status Register Write

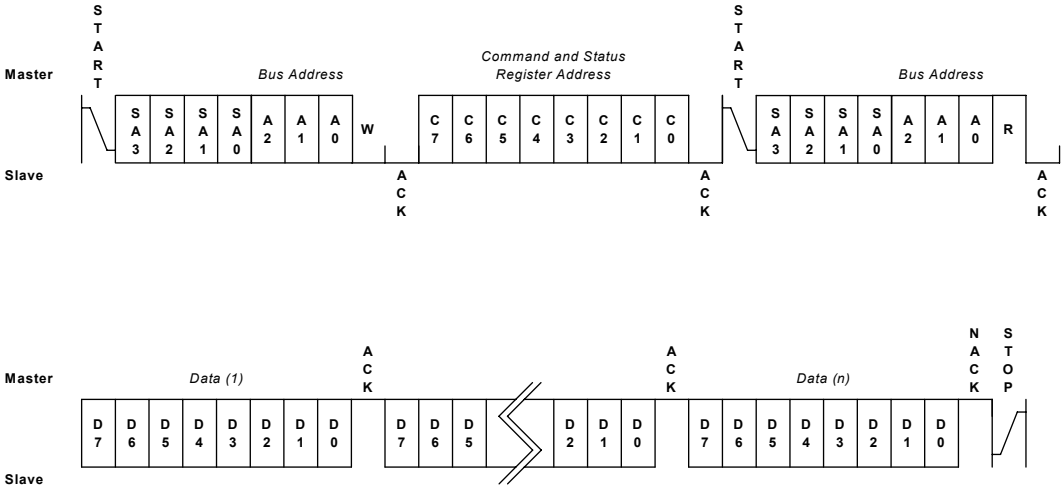


Figure 17 - Command and Status Register Read

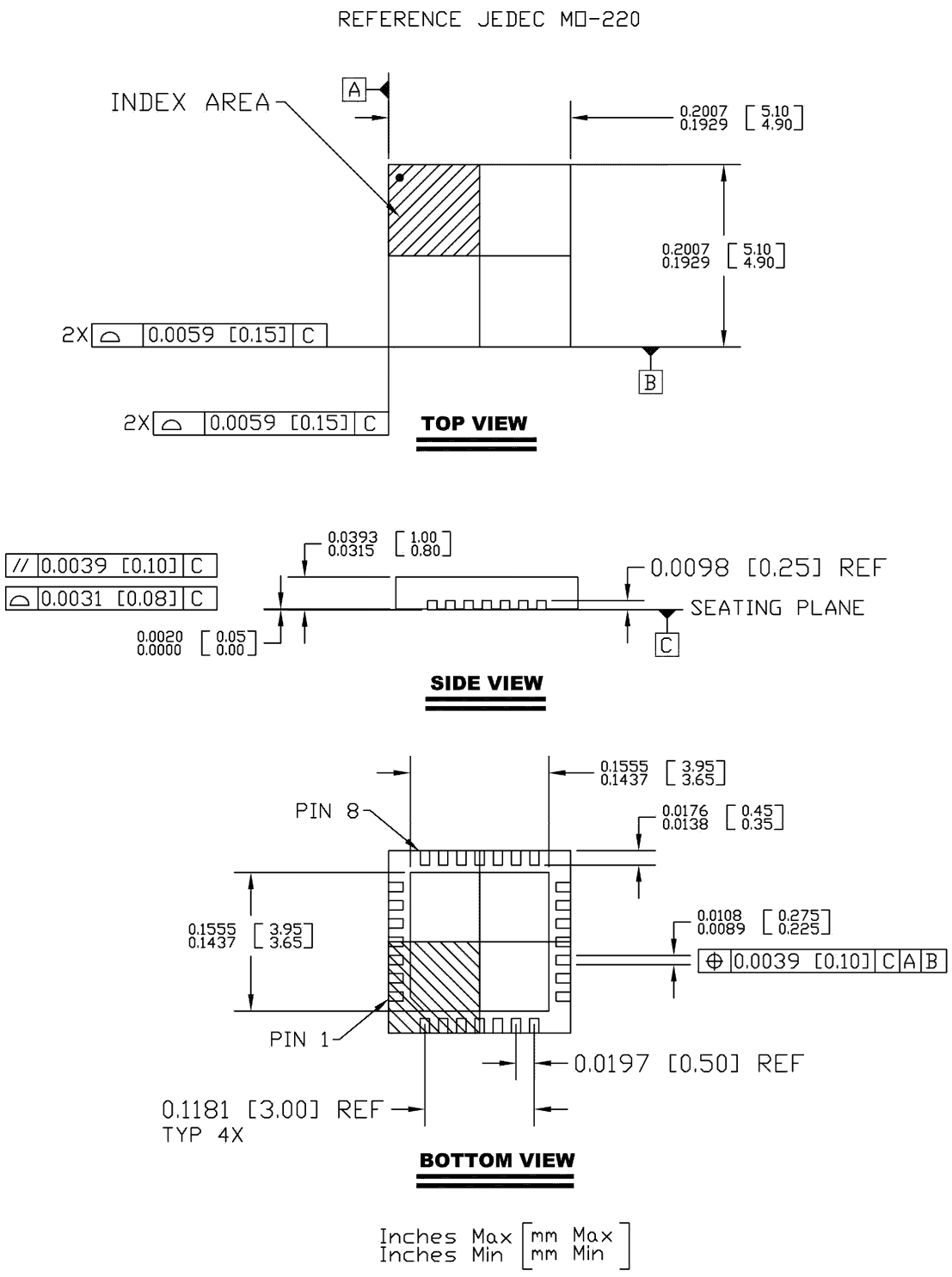
DEFAULT CONFIGURATION REGISTER SETTINGS – SMM205F-167

Register	Contents	Function
R00	01	Channel A Nominal Voltage is set to 2.503V (MSB)
R01	FF	Channel A Nominal Voltage is set to 2.503V (MSB)
R02	02	Channel B Nominal Voltage is set to 1.801V (MSB)
R03	C6	Channel B Nominal Voltage is set to 1.801V (MSB)
R04	AF	Channel A and B ADOC is enabled, Trim polarity is inverse, Fast Convergence, VREF External, Fault Latched by a Fault Condition
R05	05	Slave address is 0101
R06	28	No Write Command Required to Activate ADOC, Internal Regulator set to 3.6V, Fault Output Enabled While Margining, Configuration Registers Unlocked, COMP1 and COMP2 are set to sense UV
R08	00	Margin Command Bits
R0C	12	Stores VREF_CNTL value set to 1.25
R0D	50	Stores VREF_CNTL value set to 1.25
R20	01	Channel A - Margin High Voltage is set to 2.805V (MSB)
R21	C8	Channel A - Margin High Voltage is set to 2.805V (LSB)
R22	02	Channel B - Margin High Voltage is set to 2.100V (MSB)
R23	61	Channel B - Margin High Voltage is set to 2.100V (LSB)
R30	02	Channel A - Margin Low Voltage is set to 2.201V (MSB)
R31	45	Channel A - Margin Low Voltage is set to 2.201V (LSB)
R32	03	Channel B - Margin Low Voltage is set to 1.501V (MSB)
R33	54	Channel B - Margin Low Voltage is set to 1.501V (LSB)
R40	00	Margin Command Status Bits
R41	03	READY and START pin Polarities set to Active High
R42	FF	Write Protect
R44	00	Fault Status Bits

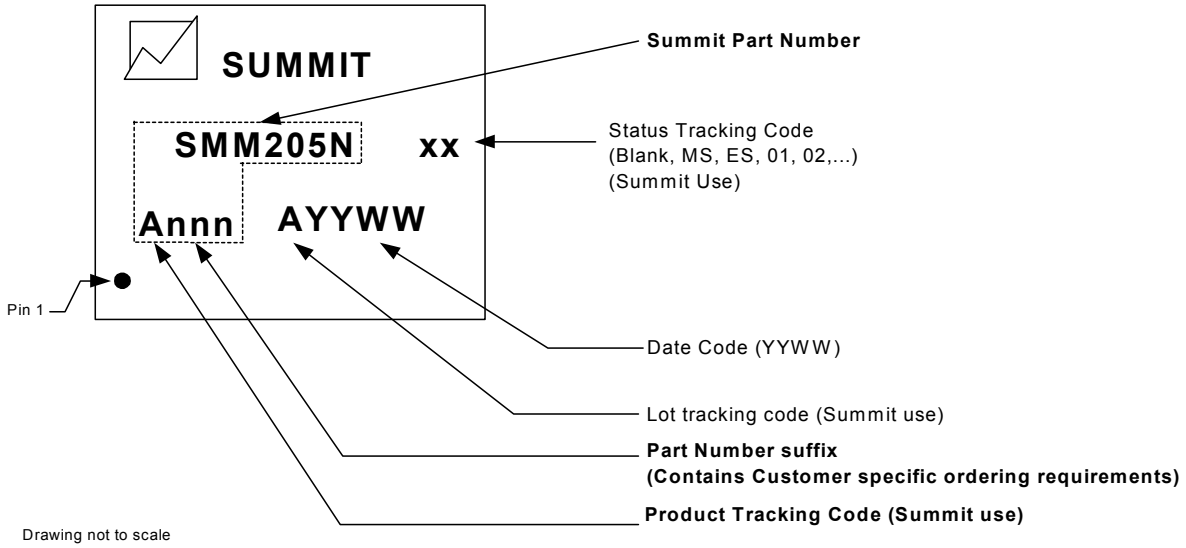
The default device ordering number — SMM205F-167 — is programmed as described above and tested over the commercial temperature range. Application Note 41 contains a complete description of the Windows GUI and the default settings of each of the 22 individual Configuration Registers.

PACKAGE

28 Pin QFN



PART MARKING



Drawing not to scale

ORDERING INFORMATION

SMM205 **N** **nnn**

Summit Part Number

Package
N=28 Lead QFN

Part Number Suffix (see page 18)
Specific requirements are contained in the suffix such as Commercial or Industrial Temp Range, Hex code, Hex code revision, etc.

NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

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