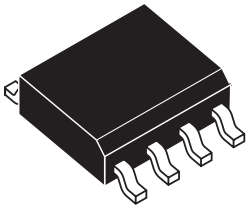
LCP1521

Application Specific Discretes
A.S.D.™

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

FEATURES

- Dual programmable transient suppressor
- Wide negative firing voltage range: V_{MGL} = -150 V max.
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 2 mA max
- Peak pulse current: I_{PP} = 30 A (10/1000 µs)
- Holding current: I_H = 150 mA



SO-8

DESCRIPTION

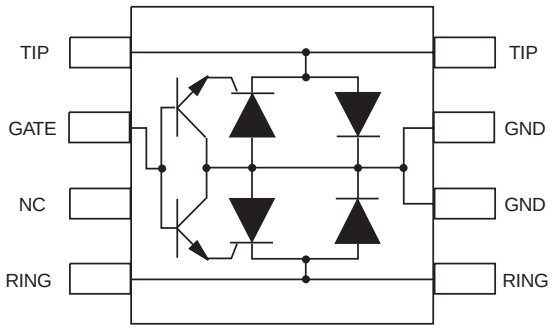
This device has been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clipped with 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

This component presents a very low gate triggering current (I_{GT}) in order to reduce the current consumption on printed circuit board during the firing phase.

A particular attention has been given to the internal wire bonding. The Kelvin method configuration ensures reliable protection, reducing the overvoltage introduced by the parasitic inductances of the wiring L x(dI/dt), especially for very fast transients.

FUNCTIONAL DIAGRAM



COMPLIES WITH THE FOLLOWING STANDARDS:	Peak Surge Voltage (V)	Voltage Waveform (µs)	Current Waveform (µs)	Admissible Ipp (A)	Necessary Resistor (Ω)
ITU-T K20	4000 1000	10/700 10/700	5/310 5/310	40 25	60 -
VDE0433	2000	10/700	5/310	40	10
VDE0878	2000	1.2/50	1/20	50	2
IEC1000-4-5	level 3 level 4	10/700 1.2/50	5/310 8/20	40 100	10 -
FCC Part 68 lightning surge type A	1500 800	10/160 10/560	10/160 10/560	50 35	22 15
FCC Part 68 lightning surge type B	1000	9/720	5/320	25	-
BELLCORE: NWT-001089-CORE First level	2500 1000	2/10 10/1000	2/10 10/1000	170 30	10 24
BELLCORE: NWT-001089-CORE Second level	5000	2/10	2/10	170	20

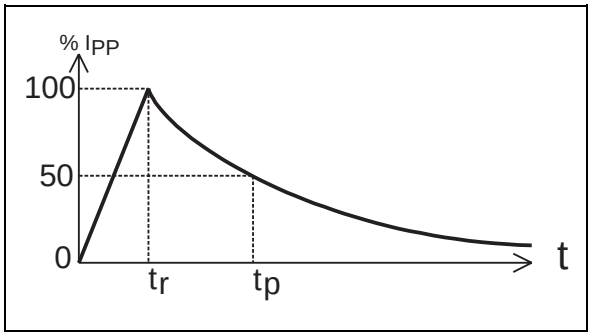
Note 1: the mentioned value of the series resistance is the minimum value needed to fulfill the standard requirement.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C, unless otherwise specified).

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current (see note1)	10/1000µs 5/310µs 2/10µs	30 40 170	A
I_{TSM}	Non repetitive surge peak on-state current (F = 50Hz)	t_p = 10ms t = 1s	20 5	A
I_{GSM}	Maximum gate current (half sine wave tp = 10ms)		2	A
V_{MLG} V_{MGL}	Maximum voltage LINE/GND Maximum voltage GATE/LINE	-40°C < Tamb < +85°C -40°C < Tamb < +85°C	-150 -150	V
T_{stg} Tj	Storage temperature range Maximum junction temperature		- 55 to + 150 150	°C
T_L	Maximum lead temperature for soldering during 10s		260	°C

Note 1: Pulse waveform

10 / 1000 µs	tr = 10 µs	tp = 1000 µs
5 / 310 µs	tr = 5 µs	tp = 310 µs
2 / 10 µs	tr = 2 µs	tp = 10 µs

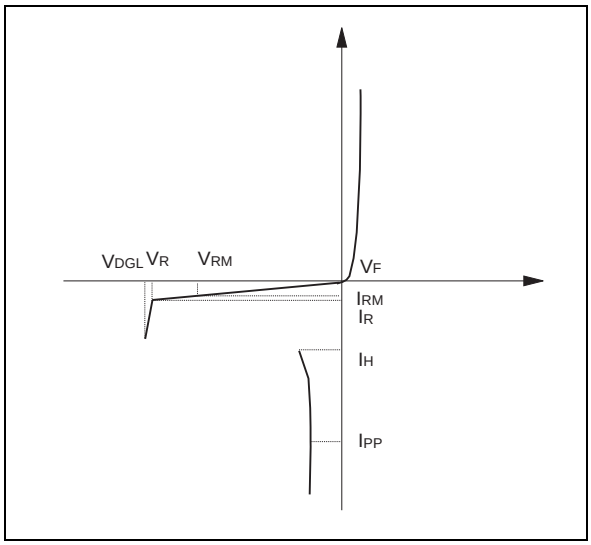


THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
Rth (j-a)	Junction to ambient	170	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
I_{GT}	Gate triggering current
I_H	Holding current
I_{RM}	Reverse leakage current LINE / GND
I_{RG}	Reverse leakage current GATE / LINE
V_{RM}	Reverse voltage LINE / GND
V_{GT}	Gate triggering voltage
V_F	Forward drop voltage LINE / GND
V_{FP}	Peak forward voltage LINE / GND
V_{DGL}	Dynamic switching voltage GATE / LINE
V_{GATE}	GATE / GND voltage
V_{RG}	Reverse voltage GATE / LINE
C	Capacitance LINE / GND



1 - PARAMETERS RELATED TO THE DIODE LINE / GND (T_{amb} = 25°C)

Symbol	Test conditions			Max	Unit
V_F	Square pulse : t_p = 500µs I_F = 5A			2	V
V_{FP} (note 1)	10/700µs 1.2/50µs 2/10µs	1.5kV 1.5kV 2.5kV	R_P = 10Ω R_P = 10Ω R_P = 62Ω	5 7 12	V

Note 1: see test circuit for VFP; RP is the protection resistor located on the line card.

2 - PARAMETERS RELATED TO THE PROTECTION THYRISTOR (T_{amb} = 25°C)

Symbol	Test conditions	Min	Max	Unit
I_{GT}	$V_{GND / LINE}$ = -48V	0.1	2	mA
I_H	V_{GATE} = -48V (see note 2)	150		mA
V_{GT}	at I_{GT}		1.5	V
I_{RG}	Tc=25°C V_{RG} = -150V Tc=85°C V_{RG} = -150V		5 50	µA
V_{DGL}	V_{GATE} = -48V (see note 3) 10/700µs 1kV R_P = 10Ω I_{PP} = 30A 1.2/50µs 1.5kV R_P = 10Ω I_{PP} = 30A 2/10µs 2.5kV R_P = 62Ω I_{PP} = 38A		7 10 25	V

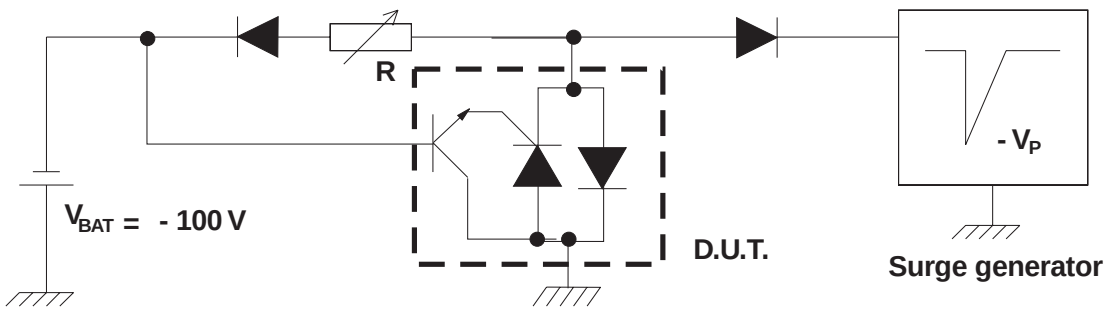
Note 2: see functional holding current (I_H) test circuit

Note 3: see test circuit for V_{DGL}
The oscillations with a time duration lower than 50ns are not taken into account

3 - PARAMETERS RELATED TO DIODE AND PROTECTION THYRISTOR (T_{amb} = 25°C)

Symbol	Test conditions	Max	Unit
I_{RM}	Tc=25°C $V_{GATE / LINE}$ = -1V V_{RM} = -150V Tc=85°C $V_{GATE / LINE}$ = -1V V_{RM} = -150V	5 50	µA
C	V_R = -3V F = 1MHz V_R = -48V F = 1MHz	100 50	pF

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT : GO-NO GO TEST

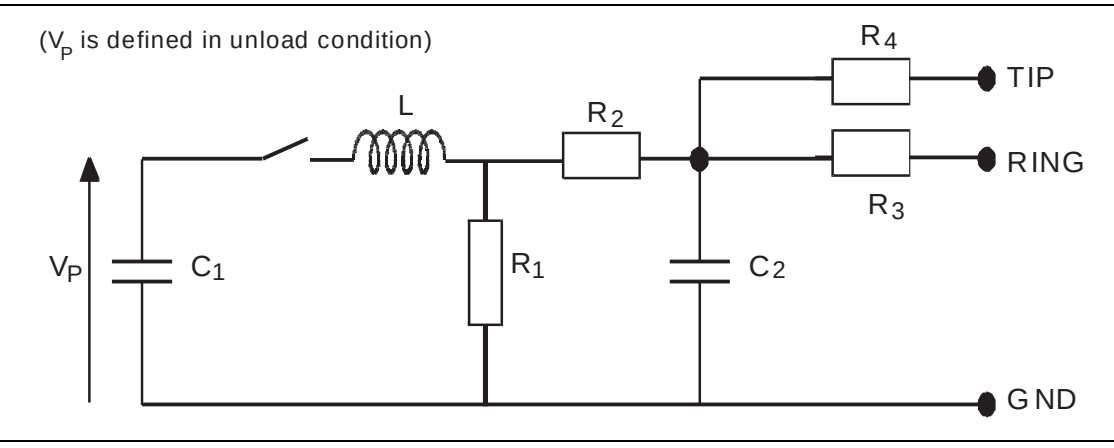


This is a GO-NO GO test which allows to confirm the holding current (I_H) level in a functional test circuit.

TEST PROCEDURE :

- Adjust the current level at the I_H value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current : I_{PP} = 10A, 10/1000µs.
- The D.U.T. will come back to the off-state within a duration of 50ms max.

TEST CIRCUIT FOR V_{FP} AND V_{DGL} PARAMETERS



Pulse (µs)		V_p	C_1	C_2	L	R_1	R_2	R_3	R_4	I_{PP}	R_p
t_r	t_p	(V)	(µF)	(nF)	(µH)	(Ω)	(Ω)	(Ω)	(Ω)	(A)	(Ω)
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62

TECHNICAL INFORMATION

Fig. A1: LCP1521 concept behavior.

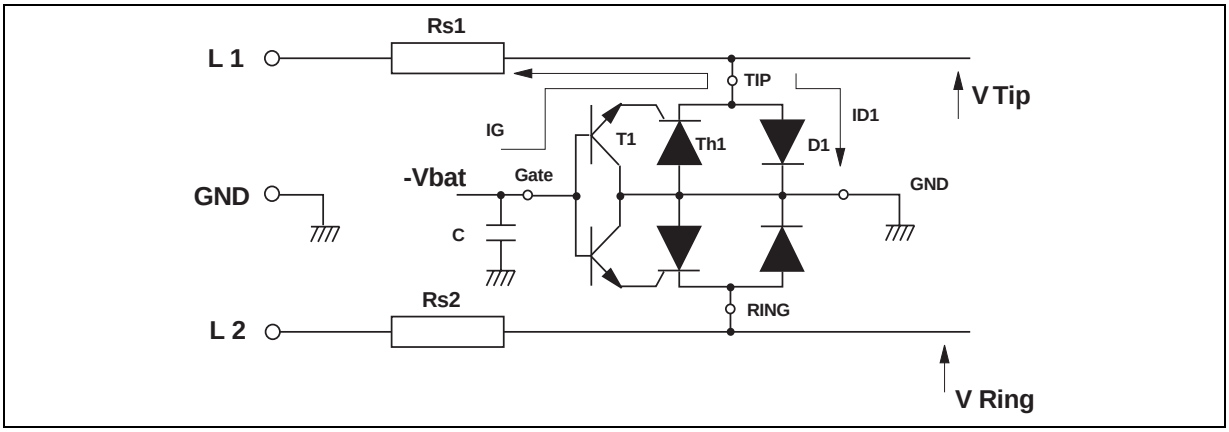
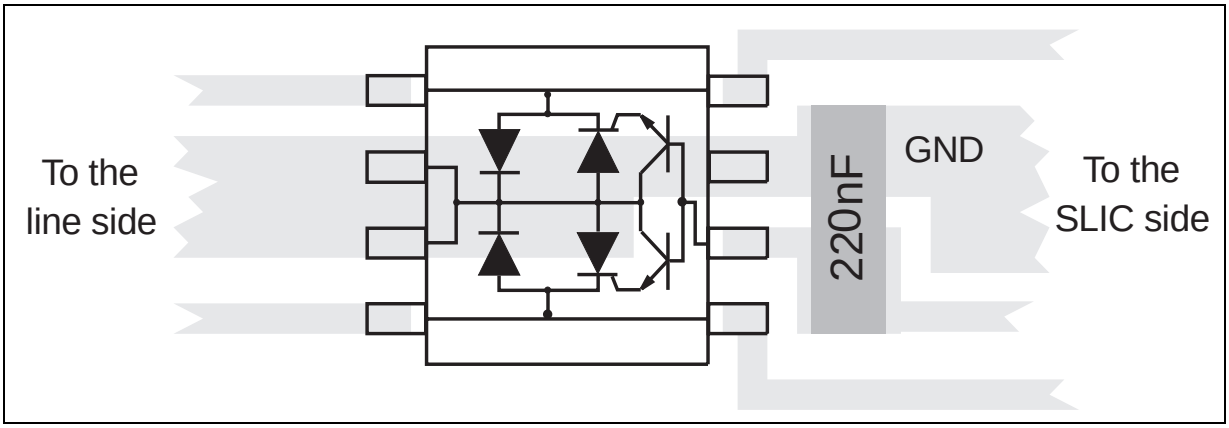


Figure A1 shows the classical protection circuit using the LCP1521 crowbar concept. This topology has been developed to protect the new high voltage SLIC's, it allows to program the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example) a current Ign flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current I_H, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example) the diode D1 conducts and the surge current flows through the ground.

Fig. A2: Example of PCB layout based on LCP1521 protection.



In order to minimize the remaining voltage across the SLIC inputs during the surge, the TIP and RING pins of the LCP1521 are doubled (Pins 1 and 8 for TIP / Pins 4 and 5 for RING).
This fact allows the board designer to connect the track like designed in figure A2. With such a PCB design, the extra voltages caused by track stray inductance (LdI / dt) remain located on the line side of the LCP and do not affects its SLIC side.
The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.
This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast strikes.
Please note that this capacitor is generally present around the SLIC - Vbat pin.
So to be efficient it has be as close as possible from the LCP1521 Gate pin and from the reference ground track (or plan) (see Fig. A2). The optimized value for C is 220nF.

The series resitors Rs1 and Rs2 designed in figure 1 represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power inductance tests imposed by the different country standards. Taking into account this fact the actual lightning surge current flowing through the LCP is equal to:

I surge = V surge / (Rg + Rs)

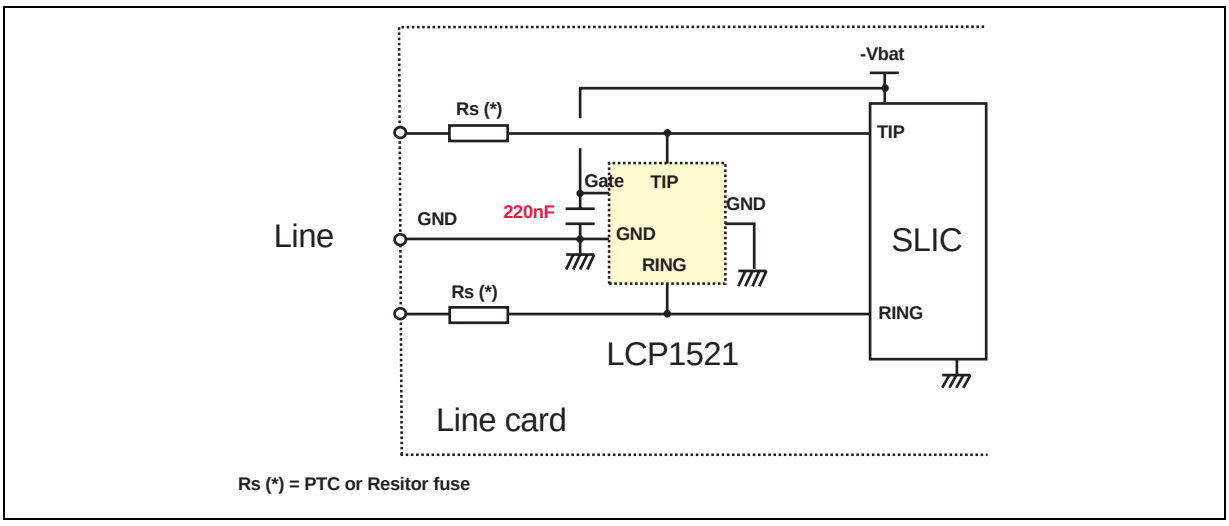
With V surge = peak surge voltage imposed by the standard.
Rg = series resistor of the surge generator
Rs = series resistor of the line card (e.g. PTC)

e.g. For a line card with 30Ω of series resistors which has to be qualified under Bellcore 1000V 10/1000µs surge, the actual current through the LCP1521 is equal to:

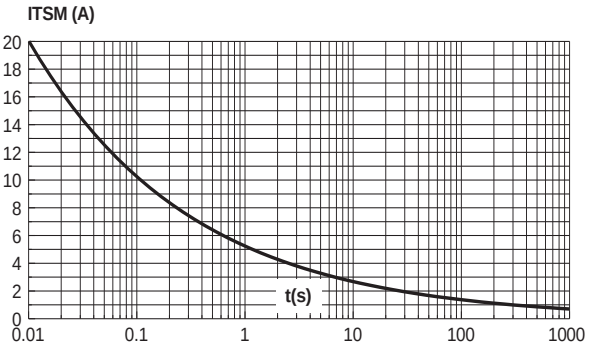
I surge = 1000 / (10 + 30) = **25A**

The LCP1521 is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the decentralized central office for example. These short line applications need smaller operating voltages than the long line applications and then allow the use of high voltage SLIC's operating without ring relay. The schematics of figure A3 gives the most frequent topology used for these emergent applications.

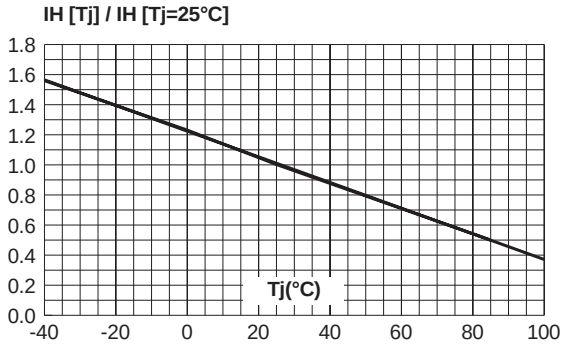
Fig. A3: Protection of high voltage SLIC.



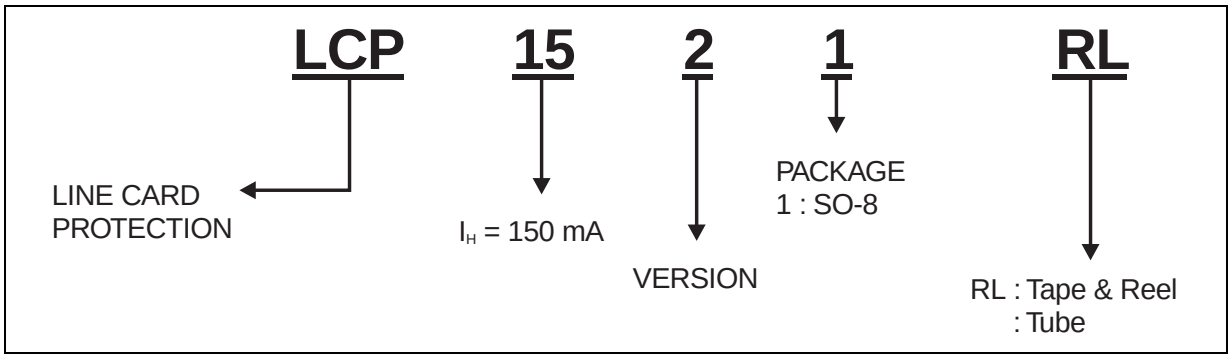
Surge peak current versus overload duration.



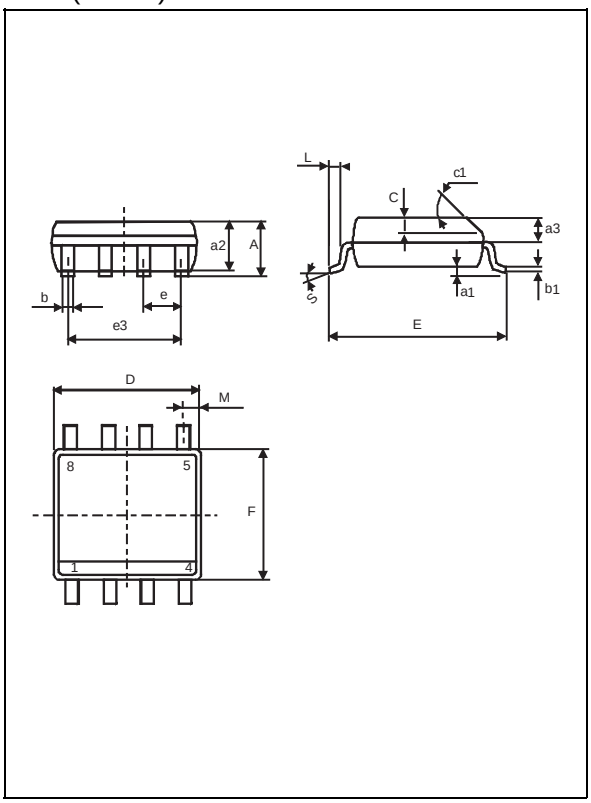
Relative variation of holding current versus junction temperature



ORDER CODE



PACKAGE MECHANICAL DATA
SO-8 (Plastic)



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25	0.50	0.50	0.010		0.020
c1	45° (typ)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max)					

Order code	Marking	Package	Weight	Base qty	Delivery mode
LCP1521	151DHV	SO-8	0.08 g	2500	Tube
LCP1521RL	151DHV	SO-8	0.08 g	2000	Tape & Reel