

Advanced PWM and Dual Linear Power Controller

General Description

The RT9228 is a 3-in-one power controller optimized for high-performance microprocessor and computer applications. The IC integrates a synchronous buck PWM controller, a linear regulator, and a linear controller as well as monitoring and protection functions into a 24-pin SOP package. The PWM controller regulates the microprocessor core voltage. The linear regulator provides power for the clock driver circuit and the linear controller regulates power for the GTL bus.

The RT9228 features an Intel-compatible, TTL 5-bit programmable DAC that adjusts the core voltage from 2.1V to 3.5V in 0.1V increments and from 1.3V to 2.05V in 0.05V steps. The 5-bit DAC has a typical $\pm 1\%$ tolerance. The linear regulator uses an internal drive device to provide $2.5V \pm 2.5\%$ output voltage. The linear controller drives an external N-channel MOSFET or a low cost NPN bipolar transistor to provide $1.5V \pm 2.5\%$.

The RT9228 monitors all the output voltages. A Power-good signal is issued when the core voltage is within $\pm 10\%$ of the DAC setting and the other levels are above their under-voltage levels. Additional build-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltage above 115% of the DAC setting. The PWM over-current function monitors the output current using the voltage drop across the upper MOSFET's $R_{DS(ON)}$, which eliminates the need for a current sensing resistor.

Ordering Information

RT9228□ □

- Package type
S : SOP-24
- Operating temperature range
C: Commercial standard

Features

- 3-in-one Regulated Voltages for Microprocessor Core, Clock, and GTL
- Compatible with HIP6018B
- Power-good Output Voltage Monitor

Switching section

- 5-bit DAC Programmable from 1.3V to 3.5V
- $\pm 1\%$ DAC Accuracy
- Fast Transient Response
- Full 0% to 100% Duty Cycle Driver
- Fixed 200kHz Switching Frequency
- Adaptive Non-overlapping Gate Driver
- Over-current Monitor Uses MOSFET $R_{DS(ON)}$
- Over-voltage Protection Uses Lower MOSFET

Linear Section

- User-adjustable Linear Regulator Output Voltage
- MOSFET or NPN Driving Capability
- Ultra Fast Response Speed
- Under-voltage Protection
- Internal Thermal Shutdown

Applications

- Full Motherboard Power Regulation for Computer
- Low-voltage Distribution Power Supplies

Pin Configurations

Part Number	Pin Configurations	
RT9228CS (Plastic SOP-24)	TOP VIEW	
	VCC	1
	VID4	2
	VID3	3
	VID2	4
	VID1	5
	VID0	6
	PGOOD	7
	FAULT	8
	SS	9
	NC	10
	FB2	11
	VIN2	12
	24	UGATE1
	23	PHASE1
	22	LGATE1
	21	PGND
	20	OCSET1
	19	VSEN1
	18	FB1
	17	NC
	16	FB3
	15	GATE3
	14	GND
	13	VOT2

Absolute Maximum Ratings

Supply Voltage	+15V
PGOOD, FAULT and GATE Voltage	GND–0.3V to $V_{CC}+0.3V$
Input, Output or I/O Voltage	GND–0.3V to 7V
Ambient Temperature Range	0°C to +70°C
Junction Temperature Range	0°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Package Thermal Resistance SOP-24, θ_{JA}	75°C/W

Recommended Operating Conditions

Supply Voltage	+12V±10%
Ambient Temperature Range	0°C to 70°C
Junction Temperature Range	0°C to 125°C

CAUTION:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

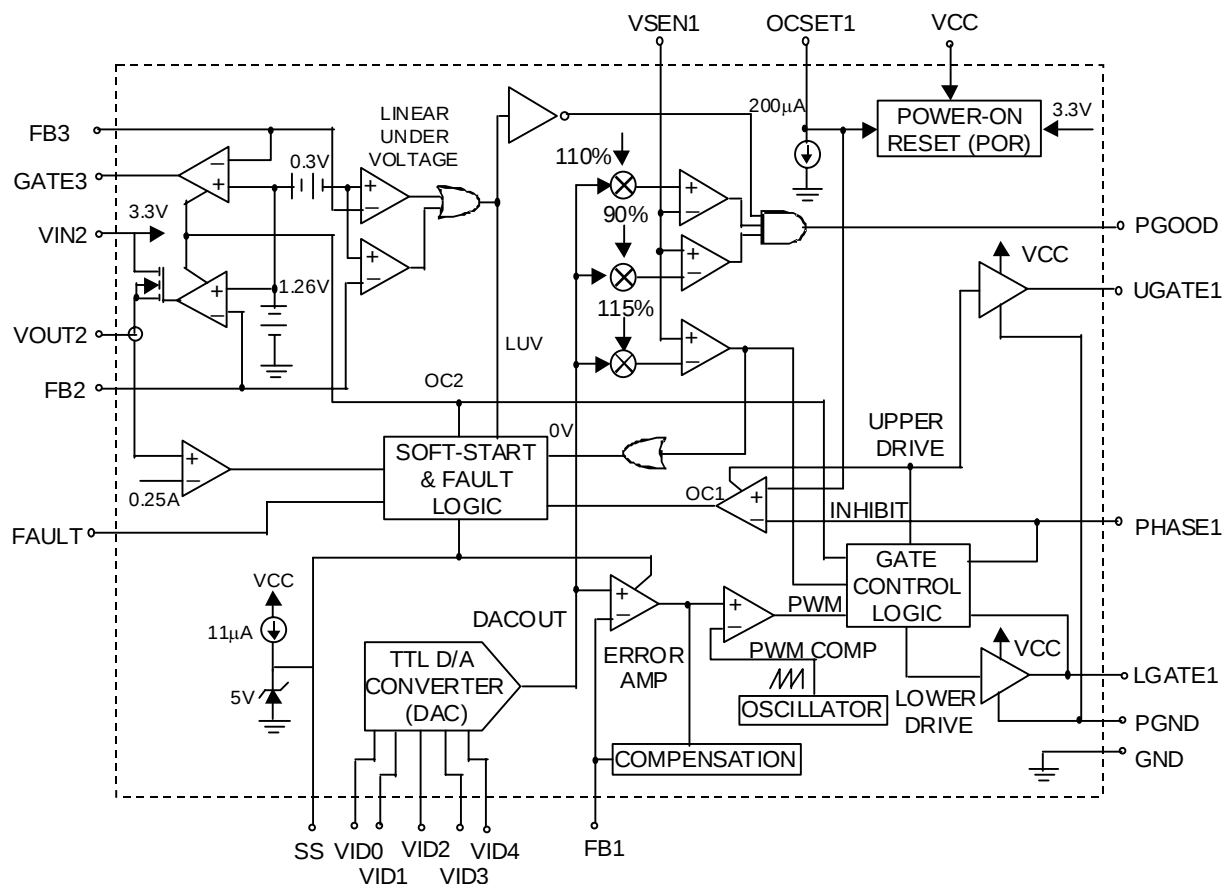
($V_{CC} = 12V$, $PGND = 0V$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Current						
Nominal Supply Current	I_{CC}	UGATE1, GATE3, LGATE1, and VOUT2 Open	--	10	--	mA
Power-On Reset						
VCC Rising Threshold		$V_{OCSET1} = 4.5V$	7.5	--	9.5	V
VCC Falling Threshold		$V_{OCSET1} = 4.5V$	7	--	9	V
Rising VIN2 Under-voltage Threshold			--	2.8	--	V
VIN2 Under-voltage Hysteresis			--	0.5	--	V
Rising V_{OCSET1} Threshold			--	1.25	--	V
Oscillator						
Free Running Frequency			180	200	225	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.9	--	V_{P-P}

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reference and DAC						
DAC (VID0-VID4) Input Low Voltage			--	--	0.8	V
DAC (VID0-VID4) Input High Voltage			2.0	--	--	V
DACOUT Voltage Accuracy		DACOUT = 2.05 ~ 3.50V	-1	--	1	%
DACOUT Voltage Accuracy		DACOUT = 1.30 ~ 2.00V	-1%	--	20mV	-
Reference Voltage (Pin FB2 and FB3)	V _{REF}		1.240	1.265	1.290	V
Linear Regulator						
Regulation		10mA < I _{VOUT2} < 150mA	-2.5	--	2.5	%
Under-voltage Level		FB2 Rising	--	75	87	%
Under-voltage Hysteresis			--	100	--	mV
Over-current Protection	I _{ovp}		180	230	--	mA
Over-current Protection During Start-up			--	700	--	mA
Linear Controller						
Regulation		VSEN3 = GATE3 0 < I _{GATE3} < 20mA	-2.5	--	2.5	%
Under-voltage Level		FB3 Rising	--	75	87	%
Under-voltage Hysteresis			--	100	--	mV
Output Drive Current		VIN2 – VOUT3 > 1.5V	20	40	--	mA
PWM Controller Error Amplifier						
DC Gain			--	65	--	dB
PWM Controller Gate Driver						
UGATE Source	R _{UGATE1}	VCC = 12V VCC - V _{UGATE1} = 1V	--	3	7	Ω
UGATE Sink	R _{UGATE1}	V _{UGATE1} = 1V	--	3	7	Ω
LGATE Source	I _{LGATE1}	VCC = 12V V _{LGATE1} = 2V	--	1	--	A
LGATE Sink	R _{LGATE1}	V _{LGATE1} = 1V	--	2	6	Ω
Protection						
V _{OUT1} Over-voltage Trip		VSEN1 Rising	112	115	120	%
FAULT Souring Current	I _{ovp}	V _{FAULT} = 8V	10	14	--	mA
OCSET1 Current Source	I _{ocset}	V _{OCSET1} = 4.5V	170	200	230	μA
Soft-start Current	I _{ss}	V _{SS} = 1V	--	11	--	μA
Power Good						
V _{OUT1} Upper Threshold		VSEN1 Rising	108	--	112	%
V _{OUT1} Under Voltage		VSEN1 Rising	89	--	95	%
V _{OUT1} Hysteresis (VSEN1/DACOUT)		Upper/Lower Threshold	--	2	--	%
PGOOD Voltage Low		I _{PGOOD} = -4mA	--	--	0.5	V

Function Block Diagram



Functional Pin Description

VCC (Pin 1)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC.

VID0, VID1, VID2, VID3, VID4 (Pin 6, 5, 4, 3, and 2)

VID0~4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference, DACOUT. The level of DACOUT sets the core converter output voltage. It also sets the core PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage of 32 combinations of VID levels.

PGOOD (Pin 7)

PGOOD is an open collector output used to indicate the status of the output voltage. This pin is pulled low when the core output is not within $\pm 10\%$ of the

DACOUT reference voltage and the other outputs are below their under-voltage thresholds.

The PGOOD output is open for '11111' VID codes that inhibit operation. See table 1.

FAULT (Pin 8)

This pin is low during normal operation, but it is pulled to about 8V ($V_{CC} = 12V$) in the event of an over-voltage or over-current condition.

SS (Pin 9)

Connect a capacitor from this pin to ground. This capacitor, along with an internal $11\mu A$ ($V_{SS} > 1V$) current source, sets the soft-start interval of the converter.

FB2 (Pin 11)

Connect this pin to a resistor divider to set the linear regulator output voltage. VIN2 (Pin 12) this pin supplies power to the internal regulator. Connect this pin to a suitable 3.3V source.

Additionally, this pin is used to monitor the 3.3V supply. If, following a startup cycle, the voltage drops below 2.8V (typically), the chip shuts down. A new soft-start cycle is initiated upon return of the 3.3V supply above the under-voltage threshold.

VOUT2 (Pin 13)

Output of the linear regulator. Supplies current up to 230mA.

GND (Pin 14)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

GATE3 (Pin 15)

Connect this pin to drive gate of an external MOSFET or NPN. This pin provides the drive for the linear controller's pass transistor.

FB3 (Pin 16)

Connect this pin to a resistor divider to set the linear controller output voltage.

FB1 (Pin 18)

The FB1 pin is the inverting input of the error amplifier.

VSEN1 (Pin 19)

This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over voltage protection.

OCSET1 (Pin 20)

Connect a resistor (R_{OCSET1}) from this pin to the drain of the upper MOSFET. R_{OCSET1} , an internal $200\mu A$ current source (I_{OCSET1}), and the upper MOSFET on-resistance ($R_{DS(ON)}$) set the PWM

converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET1} \times R_{OCSET1}}{R_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

Sustaining an over-current for 2 soft-start intervals shuts down the controller.

PGND (Pin 21)

This is the power ground of UGATE1 and LGATE1. Tie the PWM converter's lower MOSFET source to this pin.

LGATE1 (Pin 22)

Connect LGATE1 to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

PHASE1 (Pin 23)

Connect the PHASE1 pin to the PWM converter's upper MOSFET source. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection.

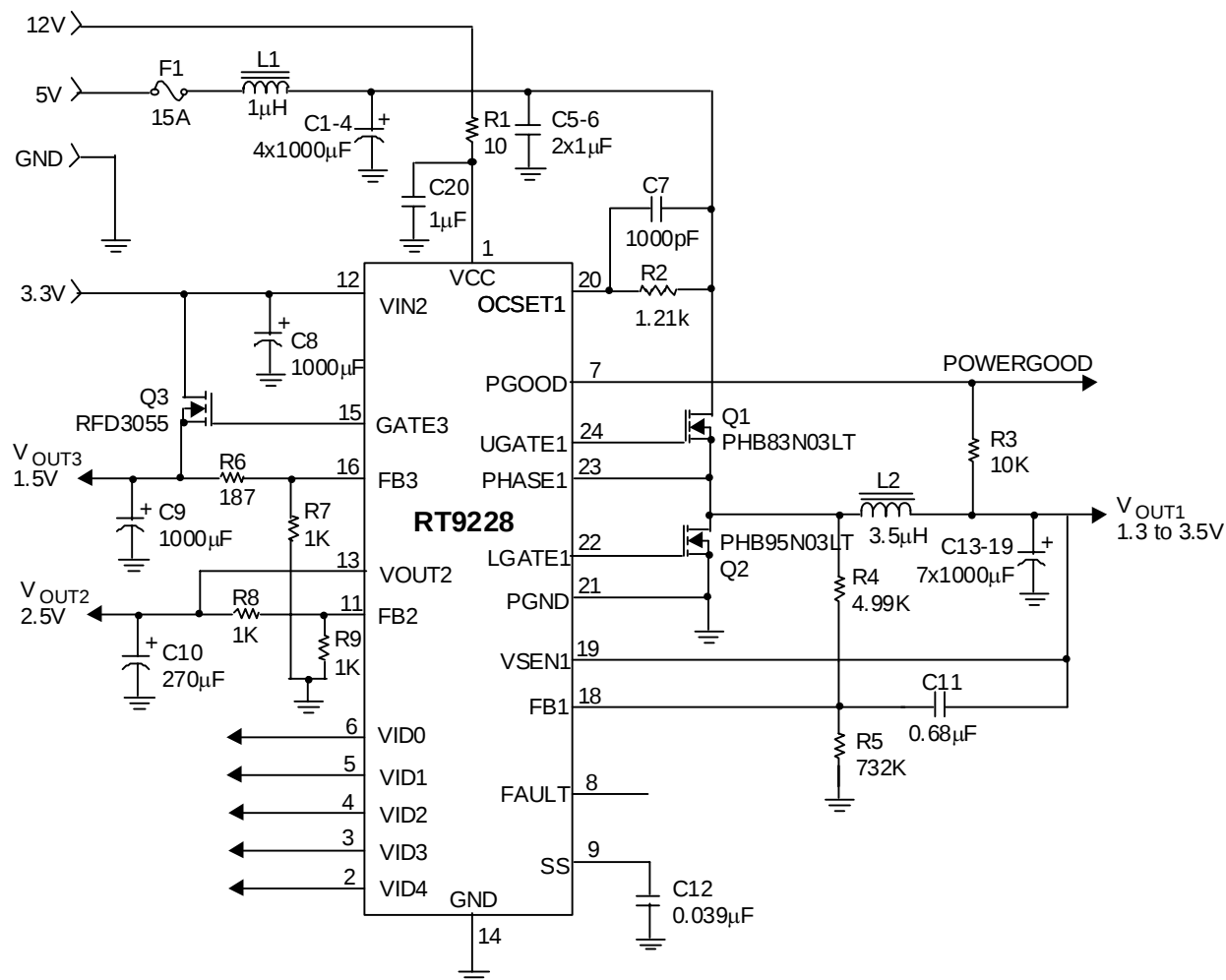
UGATE1 (Pin 24)

Connect UGATE1 pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

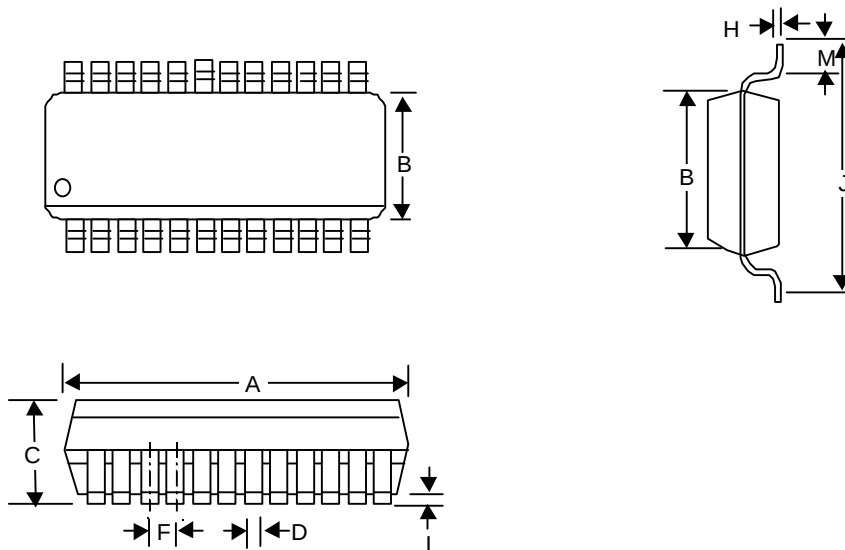
Table 1. VOUT1 Voltage Program

Pin Name					Normal OUT1 Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	INHIBIT
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60
1	1	0	0	0	2.70
1	0	1	1	1	2.80
1	0	1	1	0	2.90
1	0	1	0	1	3.00
1	0	1	0	0	3.10
1	0	0	1	1	3.30
1	0	0	1	0	3.30
1	0	0	0	1	3.40
1	0	0	0	0	3.50

Typical Application Circuit



Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	15.189	15.596	0.598	0.614
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

