



## NVRAM CONTROLLER for up to TWO LPSRAM

- CONVERT LOW POWER SRAMs into NVRAMs
- PRECISION POWER MONITORING and POWER SWITCHING CIRCUITRY
- AUTOMATIC WRITE-PROTECTION when  $V_{CC}$  is OUT-OF-TOLERANCE
- CHOICE of SUPPLY VOLTAGES and POWER-FAIL DESELECT VOLTAGES:
  - M40Z111:
    - $V_{CC} = 4.5V$  to  $5.5V$
    - $THS = V_{SS}$   $4.5V \leq V_{PFD} \leq 4.75V$
    - $THS = V_{OUT}$   $4.2V \leq V_{PFD} \leq 4.5V$
  - M40Z111W:
    - $V_{CC} = 3.0V$  to  $3.6V$
    - $THS = V_{SS}$   $2.8V \leq V_{PFD} \leq 3.0V$
    - $V_{CC} = 2.7V$  to  $3.3V$
    - $THS = V_{OUT}$   $2.5 \leq V_{PFD} \leq 2.7V$
- LESS THAN 15ns CHIP ENABLE ACCESS PROPAGATION DELAY (for 5.0V device)
- PACKAGING INCLUDES a 28-LEAD SOIC and SNAPHAT® TOP (to be Ordered Separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT TOP which CONTAINS the BATTERY

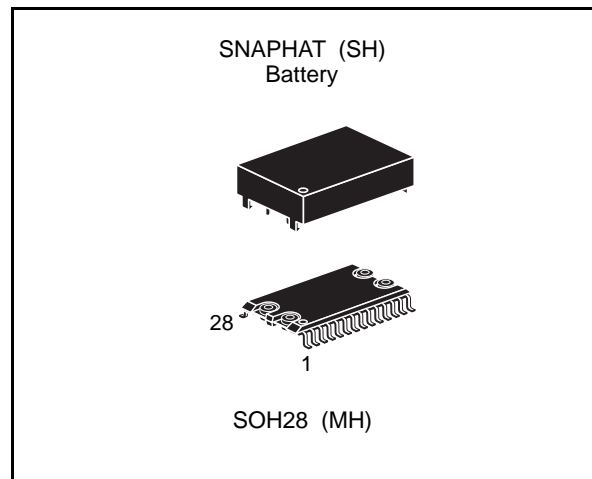
### DESCRIPTION

The M40Z111/111W NVRAM Controller is a self-contained device which converts a standard low-power SRAM into a non-volatile memory.

A precision voltage reference and comparator monitors the  $V_{CC}$  input for an out-of-tolerance condition.

**Table 1. Signal Names**

$THS$	Threshold Select Input
$\bar{E}$	Chip Enable Input
$\bar{E}_{CON}$	Conditioned Chip Enable Output
$V_{OUT}$	Supply Voltage Output
$V_{CC}$	Supply Voltage
$V_{SS}$	Ground



**Figure 1. Logic Diagram**

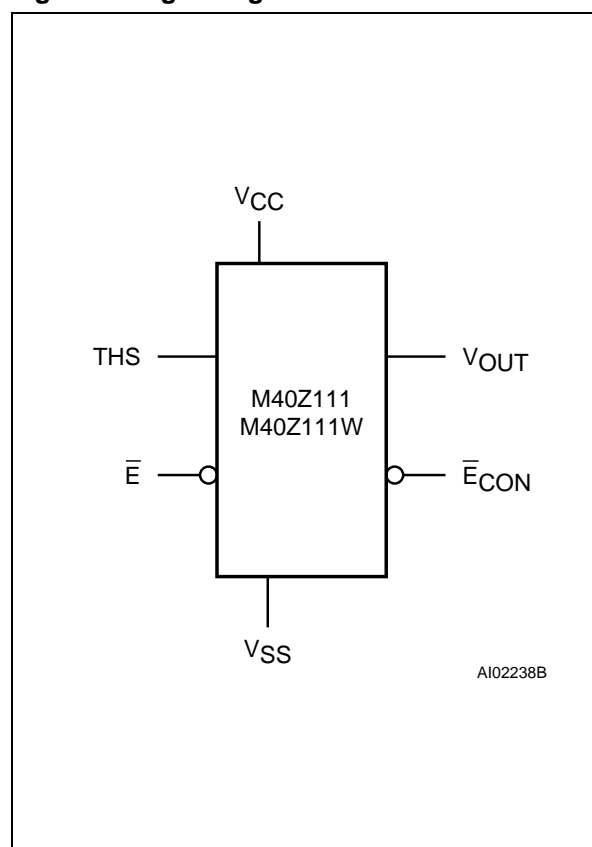


Table 2. Absolute Maximum Ratings <sup>(1)</sup>

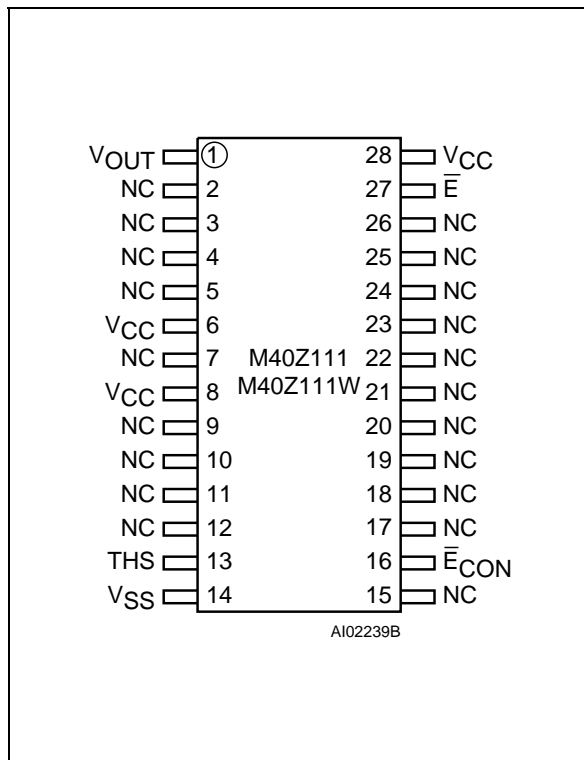
Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature	0 to 70	°C
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off)      SNAPHAT SOIC	-40 to 85 -55 to 125	°C
T <sub>SLD</sub> <sup>(2)</sup>	Lead Solder Temperature for 10 seconds	260	°C
V <sub>IO</sub>	Input or Output Voltages	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>CC</sub>	Supply Voltage	-0.3 to 7	V
I <sub>O</sub>	Output Current	20	mA
P <sub>D</sub>	Power Dissipation	1	W

**Notes:** 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.  
2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

**CAUTION:** Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

**CAUTION:** Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

Figure 2. SOIC Pin Connections



**Warning:** NC = Not Connected.

**DESCRIPTION** (cont'd)

When an invalid V<sub>CC</sub> condition occurs, the conditioned chip enable ( $\bar{E}_{CON}$ ) output is forced inactive to write-protect the stored data in the SRAM.

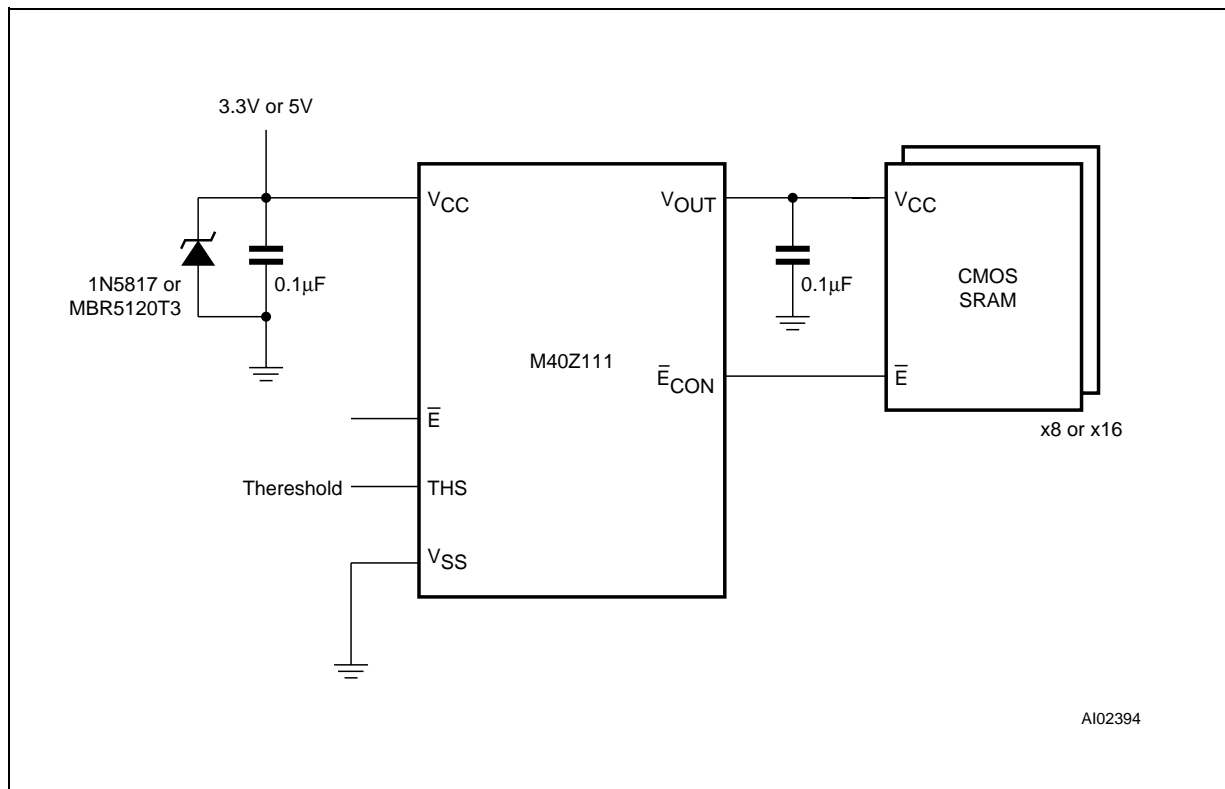
During a power failure, the SRAM is switched from the V<sub>CC</sub> pin to the lithium cell within the SNAPHAT to provide the energy required for data retention. On a subsequent power-up, the SRAM remains write protected until a valid power condition returns.

The 28 pin 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion. The SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28 lead SOIC, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1" or "M4Z32-BR00SH1" (See Table 7).

**OPERATION**

The M40Z111/111W, as shown in Figure 4, can control up to two standard low-power SRAMs. These SRAMs must be configured to have the chip enable input disable all other input signals. Most slow, low-power SRAMs are configured like this, however many fast SRAMs are not. During normal operating conditions, the conditioned chip enable ( $\bar{E}_{CON}$ ) output pin follows the chip enable ( $\bar{E}$ ) input pin with timing shown in Table 6. An internal switch connects V<sub>CC</sub> to V<sub>OUT</sub>. This switch has a voltage drop of less than 0.3V (I<sub>OUT1</sub>).

Figure 3. Hardware Hookup



When  $V_{CC}$  degrades during a power failure,  $\bar{E}_{CON}$  is forced inactive independently of  $\bar{E}$ . In this situation, the SRAM is unconditionally write protected as  $V_{CC}$  falls below an out-of-tolerance threshold ( $V_{PFD}$ ). The power fail detection value associated with  $V_{PFD}$  is selected by the THS pin and is shown in Table 5. (Note: THS pin must be connected to either  $V_{SS}$  or  $V_{OUT}$ ). If chip enable access is in progress during a power fail detection, that memory cycle continues to completion before the memory is write protected. If the memory cycle is not terminated within time  $t_{WP}$ ,  $\bar{E}_{CON}$  is unconditionally driven high, write protecting the SRAM.

A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the SRAM's contents. At voltages below  $V_{PFD}(\min)$ , the user can be assured the memory will be write protected provided the  $V_{CC}$  fall time exceeds  $t_F$ .

As  $V_{CC}$  continues to degrade, the internal switch disconnects  $V_{CC}$  and connects the internal battery to  $V_{OUT}$ . This occurs at the switchover voltage ( $V_{SO}$ ). Below the  $V_{SO}$ , the battery provides a voltage  $V_{OHV}$  to the SRAM and can supply current  $I_{OUT2}$  (see Table 5). When  $V_{CC}$  rises above  $V_{SO}$ ,  $V_{OUT}$  is switched back to the supply voltage. Output

$\bar{E}_{CON}$  is held inactive for  $t_{ER}$  (200ms maximum) after the power supply has reached  $V_{PFD}$ , independent of the  $\bar{E}$  input, to allow for processor stabilization (see Figure 6).

#### DATA RETENTION LIFETIME CALCULATION

Most low power SRAMs on the market today can be used with the M40Z111/111W NVRAM Controller. There are, however some criteria which should be used in making the final choice of which SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M40Z111/111W and SRAMs to be Don't Care once  $V_{CC}$  falls below  $V_{PFD}(\min)$ . The SRAM should also guarantee data retention down to  $V_{CC} = 2.0V$ . The chip enable access time must be sufficient to meet the system needs with the chip enable propagation delays included. If the SRAM includes a second chip enable pin ( $\bar{E}2$ ), this pin should be tied to  $V_{OUT}$ . If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0V.

**Table 3. AC Measurement Condition**

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

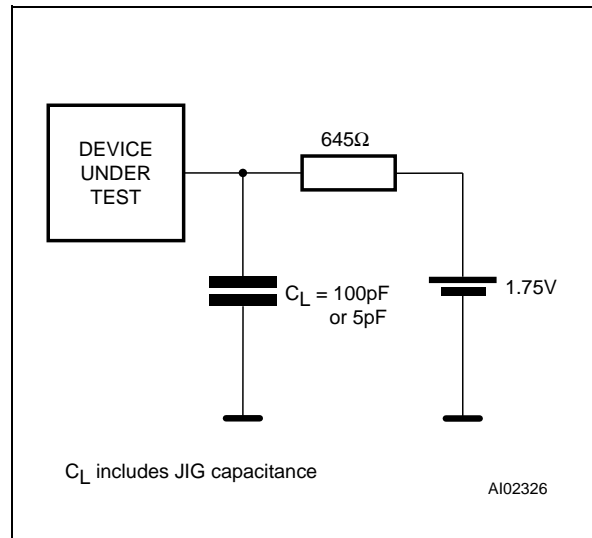
Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I<sub>CCDR</sub> value of the M40Z111/111W to determine the total current requirements for data retention.

The available battery capacity for the SNAPHAT of your choice can then be divided by this current to determine the amount of data retention available (see Table 7). For more information on Battery Storage Life refer to the Application Note AN1012.

**V<sub>CC</sub> NOISE AND NEGATIVE-GOING TRANSIENTS**

I<sub>CC</sub> transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V<sub>CC</sub> bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V<sub>CC</sub> bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur.

**Figure 4. AC Testing Load Circuit**



A ceramic bypass capacitor value of 0.1μF (as shown in Figure 4) is recommended in order to provide the needed filtering. In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V<sub>CC</sub> that drive it to values below V<sub>SS</sub> by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V<sub>CC</sub> to V<sub>SS</sub> (cathode connected to V<sub>CC</sub>, anode to V<sub>SS</sub>).

**Table 4. Capacitance <sup>(1)</sup>**  
(T<sub>A</sub> = 25°C; f = 1MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V		8	pF
C <sub>OUT</sub> <sup>(2)</sup>	Output Capacitance	V <sub>OUT</sub> = 0V		10	pF

**Note:** 1. Sampled only, not 100% tested.  
2. Outputs deselected.

**Table 5A. DC Characteristics for M40Z111**  
 ( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ )

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$I_{LI}^{(1)}$	Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{LO}^{(1)}$	Output Leakage Current	$0\text{V} \leq V_{OUT} \leq V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{CC}$	Supply Current	Outputs open		3	6	mA
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$V_{IH}$	Input High Voltage		2.2		$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 4.0\text{mA}$			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -2.0\text{mA}$	2.4			V
$V_{OHB}$	$V_{OH}$ Battery Back-up	$I_{OUT2} = 1.0\mu\text{A}$	2.0	2.9	3.6	V
$I_{OUT1}$	$V_{OUT}$ Current (Active)	$V_{OUT} > V_{CC} - 0.3$			160	mA
		$V_{OUT} > V_{CC} - 0.2$			100	mA
$I_{OUT2}$	$V_{OUT}$ Current (Battery Back-up)	$V_{OUT} > V_{BAT} - 0.3$		100		$\mu\text{A}$
$I_{CCDR}$	Data Retention Mode Current				150	nA
$V_{PFD}$	Power-fail Deselect Voltage (THS = 0)		4.5	4.6	4.75	V
	Power-fail Deselect Voltage (THS = 1)		4.2	4.35	4.5	V
$V_{SO}$	Battery Back-up Switchover Voltage			3.0		V

**Note:** 1. Outputs deselected.

## M40Z111, M40Z111W

**Table 5B. DC Characteristics for M40Z111W**  
( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 3\text{V}$  to  $3.6\text{V}$  or  $2.7\text{V}$  to  $3.3\text{V}$ )

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$I_{LI}^{(1)}$	Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{LO}^{(1)}$	Output Leakage Current	$0\text{V} \leq V_{OUT} \leq V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{CC}$	Supply Current	Outputs open		2	4	mA
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 4.0\text{mA}$			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -2.0\text{mA}$	2.4			V
$V_{OHB}$	$V_{OH}$ Battery Back-up	$I_{OUT2} = 1.0\mu\text{A}$	2.0	2.9	3.6	V
$I_{OUT1}$	$V_{OUT}$ Current (Active)	$V_{OUT} > V_{CC} - 0.3$			100	mA
		$V_{OUT} > V_{CC} - 0.2$			65	mA
$I_{OUT2}$	$V_{OUT}$ Current (Battery Back-up)	$V_{OUT} > V_{BAT} - 0.3$		100		$\mu\text{A}$
$I_{CCDR}$	Data Retention Mode Current				150	nA
$V_{PFD}$	Power-fail Deselect Voltage (THS = 0)		2.8	2.9	3.0	V
	Power-fail Deselect Voltage (THS = 1)		2.5	2.6	2.7	V
$V_{SO}$	Battery Back-up Switchover Voltage			2.5		V

**Note:** 1. Outputs deselected.

**Table 6. Power Down/Up AC Characteristics**  
( $T_A = 0$  to  $70^\circ\text{C}$ )

Symbol	Parameter	Min	Max	Unit
$t_F^{(1)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ $V_{CC}$ Fall Time	300		$\mu\text{s}$
$t_{FB}^{(2)}$	$V_{PFD}(\text{min})$ to $V_{SO}$ $V_{CC}$ Fall Time	10		$\mu\text{s}$
$t_R$	$V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ $V_{CC}$ Rise Time	10		$\mu\text{s}$
$t_{EDL}$	Chip Enable Propagation Delay	M40Z111	15	ns
		M40Z111W	20	ns
$t_{EDH}$	Chip Enable Propagation Delay	M40Z111	10	ns
		M40Z111W	20	ns
$t_{ER}$	Chip Enable Recovery	40	200	ms
$t_{WP}$	Write Protect Time	M40Z111	40	$\mu\text{s}$
		M40Z111W	40	$\mu\text{s}$

**Notes:** 1.  $V_{PFD}(\text{max})$  to  $V_{PFD}(\text{min})$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until  $200 \mu\text{s}$  after  $V_{CC}$  passes  $V_{PFD}(\text{min})$ .  
2.  $V_{PFD}(\text{min})$  to  $V_{SO}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

**Figure 5. Power Down Timing**

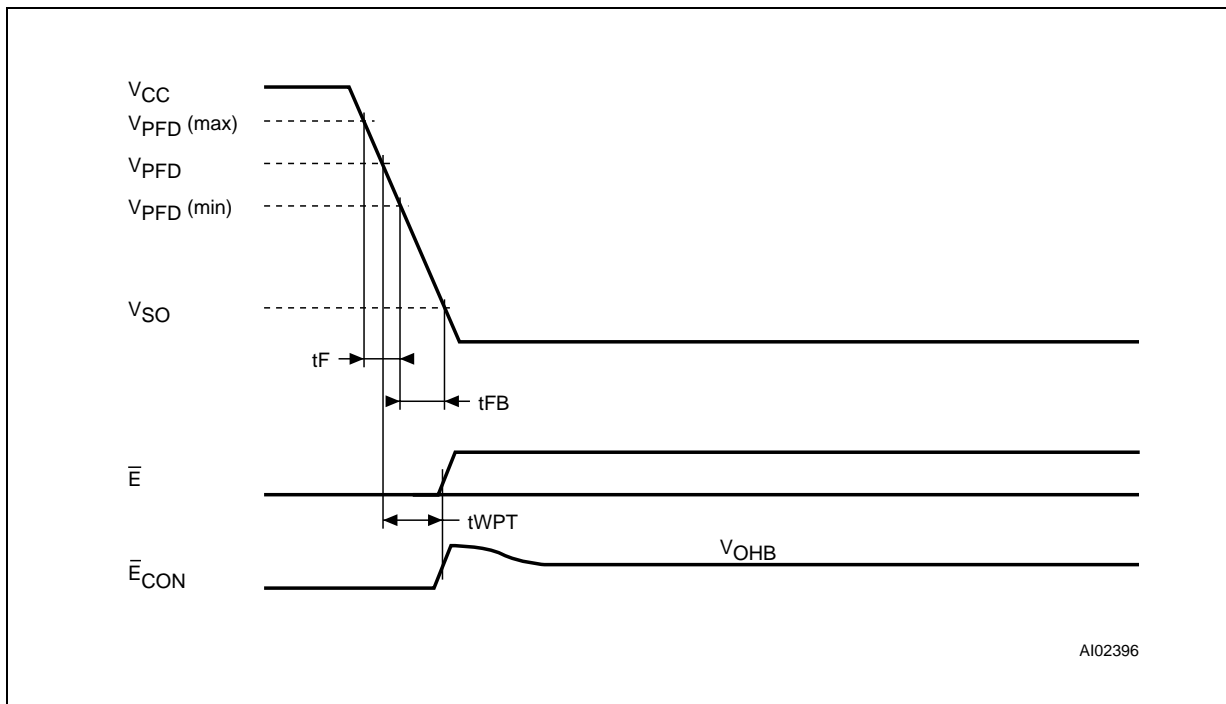


Figure 6. Power Up Timing

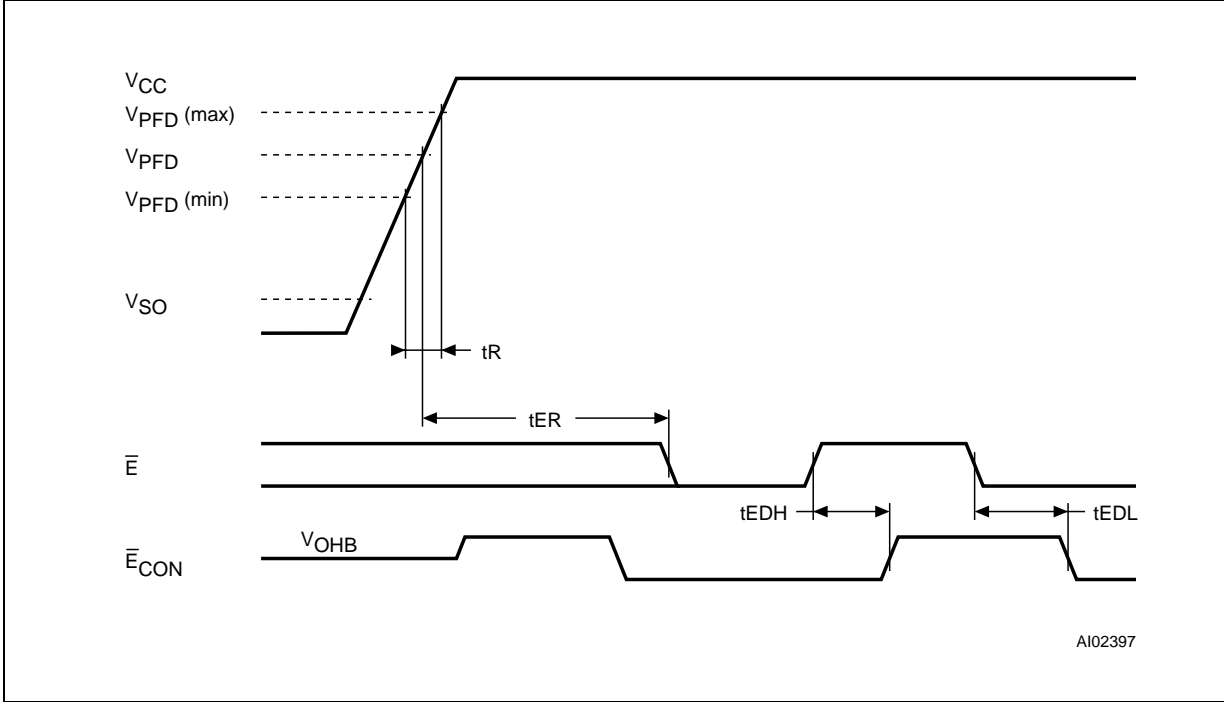
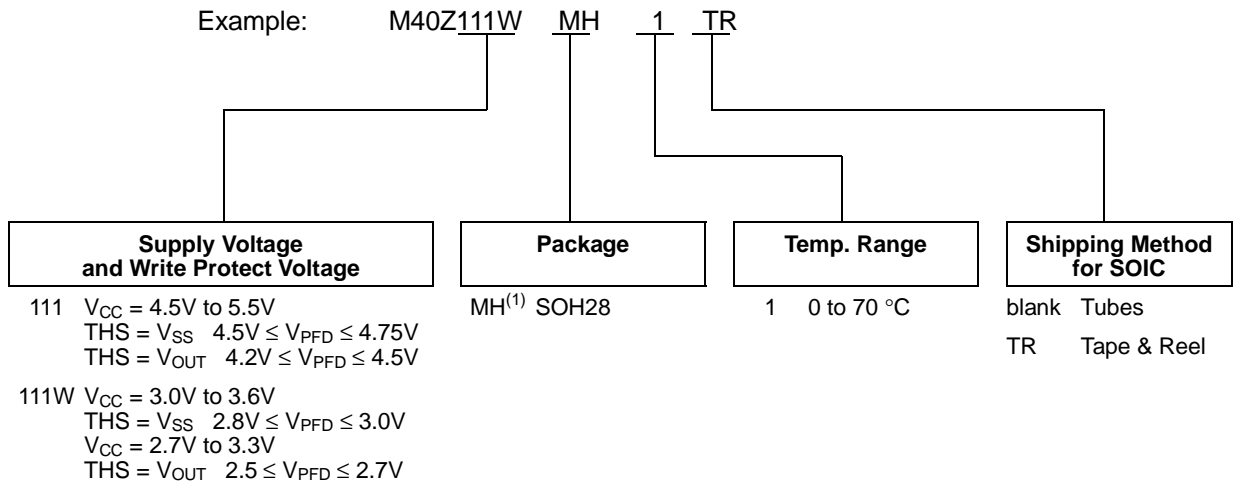


Table 7. Battery Table

Part Number	Description	Package
M4Z28-BR00SH1	Lithium Battery (50mAh) SNAPHAT	SH
M4Z32-BR00SH1	Lithium Battery (130mAh) SNAPHAT	SH



**ORDERING INFORMATION SCHEME**



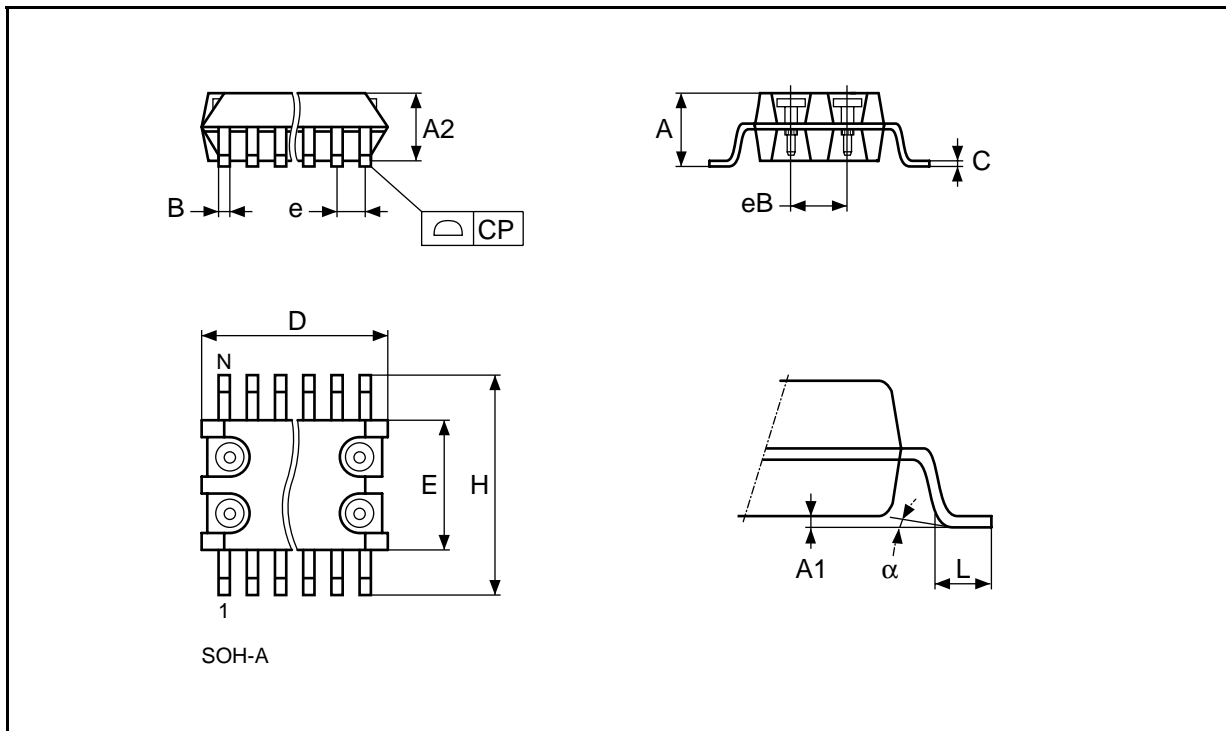
**Note:** 1. The SOIC package (SOH28) requires the battery package (SNAPHAT) which is ordered separately under the part number "M4ZxxBR00SH1" in plastic tube or "M4Zxx-BR00SH1TR" in Tape & Reel form.

**Caution:** Do not place the SNAPHAT battery package "M4Zxx-BR00SH1" in conductive foam since will drain the lithium button-cell battery.

For a list of available options (Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

**SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT**

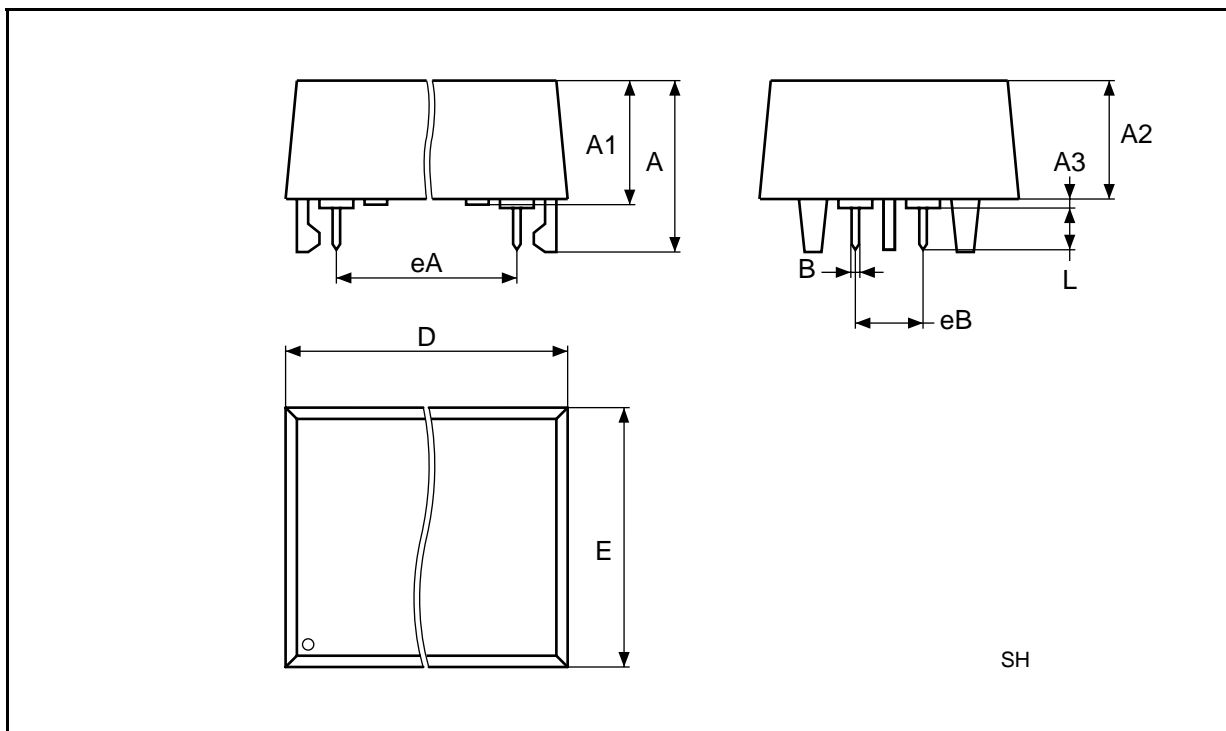
Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
$\alpha$		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004



Drawing is not to scale.

### SH - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090



Drawing is not to scale.

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