

LRS1329

Stacked Chip

16M Flash and 2M SRAM

(Model No.: LRS1329)

Spec No.: MFM2-J11601

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 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliances
 - Communication equipment other than for trunk lines

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

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Part 1 Overview

1. Description

The LRS1329 is a combination memory organized as 1M x16/2M x8 bit flash memory and 256K x8 bit static RAM in one package.

Features

- Power supply 2.7 V to 3.6 V
- Operating temperature -25 °C to +85 °C
- Not designed or rated as radiation hardened
- 72 pin CSP (LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

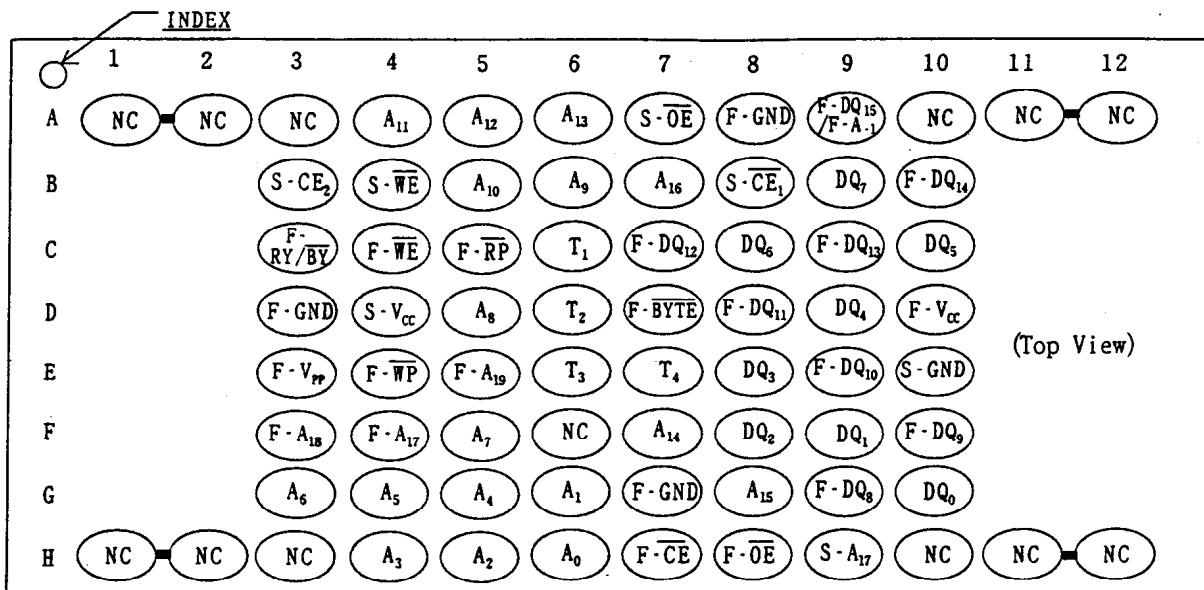
Flash Memory

- Access Time 100 ns (Max.)
- Operating current (The current for F-V_{CC} pin)
 - Read 25 mA (Max. t_{CYCLE}=200ns)
 - Word/Byte write 17 mA (Max.)
 - Block erase 17 mA (Max.)
- Deep power down current (The current for F-V_{CC} pin) 10 μA (Max. F- $\overline{\text{CE}} \geq \text{F-V}_{\text{CC}} - 0.2\text{V}$,
F-RP $\leq 0.2\text{V}$, F-V_{PP} $\leq 0.2\text{V}$)
- Optimized Array Blocking Architecture
 - Two 4K-word/8K-byte Boot Blocks/ Six 4K-word/8K-byte Parameter Blocks/
Thirty-one 32K-word/64K-byte Main Blocks/ Top Boot Location
- Extended Cycling Capability
 - 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
 - Word/Byte write Suspend to Read
 - Block Erase Suspend to Word/Byte write
 - Block Erase Suspend to Read

SRAM

- Access Time 85 ns (Max.)
- Operating current 30 mA (Max.)
 - 3 mA (Max. t_{RC}, t_{WC}=1 μs)
- Standby current 15 μA (Max.)
- Data retention current 15 μA (Max.)

2. Pin Configuration



Notes: All F-GND and S-GND pins must connect to GND.
 Two NC pins at the corner are connected.
 From T₁ to T₄ pins need to be open.

| Pin | Description | |
|---|--|--|
| A ₀ to A ₁₆ | Address Inputs (Common) | |
| F-A ₁ , F-A ₁₇ to F-A ₁₈ | Address Inputs (Flash) F-A ₁ : Not used in x16 mode. | |
| S-A ₁₇ | Address Input (SRAM) | |
| F-CE | Chip Enable (Flash) | |
| S-CE ₁ , S-CE ₂ | Chip Enable (SRAM) | |
| F-WE | Write Enable (Flash) | |
| S-WE | Write Enable (SRAM) | |
| F-OE | Output Enable (Flash) | |
| S-OE | Output Enable (SRAM) | |
| F-RP | Reset/Deep Power Down (Flash) Block erase and Word/Byte Write: V _{IH} or V _{HH} Read: V _{IH} or V _{HH} Deep Power Down: V _{IL} | |
| F-WP | Write Protect (Flash) Two Boot Blocks Locked: V _{IL} (With F-RP=V _{HH} Erase/Write can operate to all block) | |
| F-BYTE | Byte Enable (Flash); x8 mode: V _{IL} , x16 mode: V _{IH} | |
| F-RY/BY | Ready/Busy (Flash) During an Erase or Write operation: V _{OL} Block Erase and Word/Byte Write Suspend: High-Z Deep Power Down: V _{OH} | |
| DQ ₀ to DQ ₇ | Data Input/Outputs (Common) | |
| F-DQ ₈ to F-DQ ₁₅ | Data Inputs/Outputs (Flash); Not used in x8 mode. | |
| F-V _{CC} | Power Supply (Flash) | |
| S-V _{CC} | Power Supply (SRAM) | |
| F-V _{PP} | Write, Erase Power Supply (Flash) Block Erase and Word/Byte Write: F-V _{PP} =V _{PPLK} All Blocks Locked: F-V _{PP} <V _{PPLK} | |
| F-GND | GND (Flash) | |
| S-GND | GND (SRAM) | |
| NC | No Connect | |
| T ₁ to T ₄ | Test pins (Should be open) | |

3. Truth Table (*1)

| Flash | SRAM | Note | F- \overline{CE} | F- \overline{RP} | F- \overline{OE} | F- \overline{WE} | S- \overline{CE}_1 | S- \overline{CE}_2 | S- \overline{OE} | S- \overline{WE} | F-BYTE | DQ ₀ to DQ ₇ | F-DQ ₈ to F-DQ ₁₅ |
|------------------|----------------|----------|--------------------|--------------------|--------------------|--------------------|----------------------|----------------------|--------------------|--------------------|--------|------------------------------------|---|
| Read | Standby | *4.5 | L | H | L | H | *7 | X | X | X | H | DOUT | High-Z |
| | | | | | H | DOUT | | | | | | | |
| Output Disable | Standby | | L | H | H | L | *7 | X | X | X | H | High-Z | High-Z |
| | | | | | L | High-Z | | | | | | | |
| Write | Standby | *2, 3, 4 | L | H | H | L | *7 | X | X | X | H | DIN | High-Z |
| | | | | | L | DIN | | | | | | | |
| Standby | Read | *6 | H | H | X | X | L | H | L | H | X | DOUT | High-Z |
| | Output Disable | *6 | | | | | | | | | | High-Z | |
| | Write | *6 | | | | | | | | | | DIN | |
| Reset Power Down | Read | *6 | X | L | X | X | L | H | L | H | X | DOUT | High-Z |
| | Output Disable | *6 | | | | | | | | | | High-Z | |
| | Write | *6 | | | | | | | | | | DIN | |
| Standby | Standby | *6 | H | H | X | X | *7 | X | X | X | X | High-Z | |
| | | *6 | X | L | | | | | | | | | |

Notes) *1. L= V_{IL} , H= V_{IH} , X=H or L. Refer to DC Characteristics.

*2. Command writes involving block erase or word/byte write are reliably executed when $F-V_{pp}=V_{ppH}$ and $F-V_{cc}=2.7V$ to $3.6V$. Block erase or word/byte write with $V_{IH} < F-RP < V_{IH}$ produce spurious results and should not be attempted.

*3. Refer Section 5. Flash Memory Command Definition for valid DIN during a write operation.

*4. Never hold F- \overline{OE} low and F- \overline{WE} low at the same timing.

*5. F-A₁ set to V_{IL} or V_{IH} in byte mode (F-BYTE= V_{IL}).

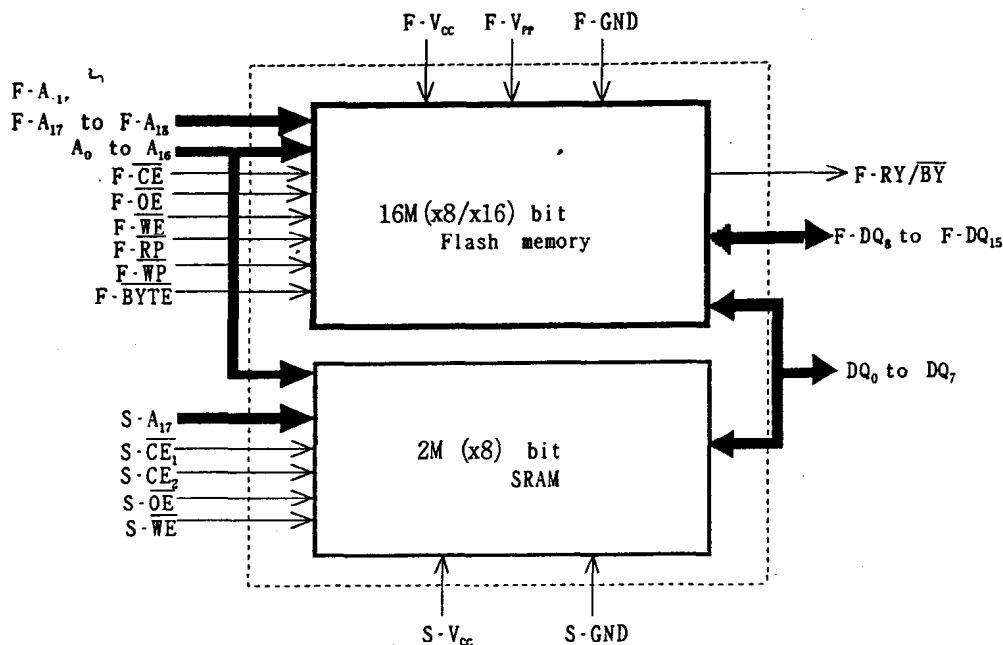
*6. F-WP set to V_{IL} or V_{IH} .

*7. See the following SRAM Standby mode.

SRAM Standby Mode

| Mode | S- \overline{CE}_1 | S- \overline{CE}_2 |
|---------|----------------------|----------------------|
| SRAM | H | X |
| Standby | X | L |

4. Block Diagram



5 Command Definitions for Flash Memory (*1)

| Command | Bus Cycles Req'd. | Note | First Bus Cycle | | | Second Bus Cycle | | |
|---|-------------------|------|-----------------|--------------|------------|------------------|--------------|-----------|
| | | | Oper (*2) | Address (*3) | Data (*3) | Oper (*2) | Address (*3) | Data (*3) |
| Read Array/Reset | 1 | | Write | XA | FFH | | | |
| Read Identifier Codes | ≥2 | *4 | Write | XA | 90H | Read | IA | ID |
| Read Status Register | 2 | | Write | XA | 70H | Read | XA | SRD |
| Clear Status Register | 1 | | Write | XA | 50H | | | |
| Block Erase | 2 | *5 | Write | BA | 20H | Write | BA | DOH |
| Word/Byte Write | 2 | *5 | Write | WA | 40H or 10H | Write | WA | WD |
| Block Erase and Word/Byte Write Suspend | 1 | *5 | Write | XA | BOH | | | |
| Block Erase and Word/Byte Write Resume | 1 | *5 | Write | XA | DOH | | | |

Note)

- *1. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
- *2. BUS operations are defined in 3. Truth Table.
- *3. XA=Any valid address within the device.
IA=Identifier Code Address.
BA=Address within the block being erased.
WA=Address of memory location to be written.
SRD=Data read from status register (See the next page "Status Register Definition").
WD=Data to be written at location WA. Data is latched on the rising edge of F-WE or F-CE (whichever goes high first).
ID=Data read from identifier codes.
- *4. See the Following Identifier Codes.
- *5. See the following Write Protection Alternatives.

Identifier Codes

| Codes | Address [A ₁₈ -A ₀] | Data [DQ ₇ -DQ ₀] |
|------------------|--|--|
| Manufacture Code | 00000H | BOH |
| Device Code | 00001H | 48H |

Write Protection Alternatives

| Operation | F-V _{PP} | F-RP | F-WP | Effect |
|--------------------------------------|--------------------|-----------------|-----------------|-----------------------|
| Block Erase or Word/Byte Write | V _{IL} | X | X | All Blocks Locked. |
| | >V _{PPLK} | V _{IL} | X | All Blocks Locked. |
| | | V _{IH} | X | All Blocks Unlocked. |
| | | V _{IH} | V _{IL} | 2 Boot Blocks Locked. |
| | | V _{IH} | V _{IH} | All Blocks Unlocks. |

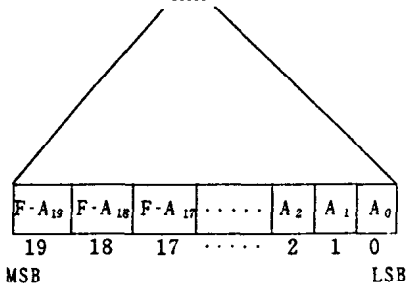
6. Status Register Definition

| | | | | | | | |
|------|-----|----|------|------|-------|-----|---|
| WSMS | ESS | ES | WBWS | VPPS | WBWSS | DPS | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

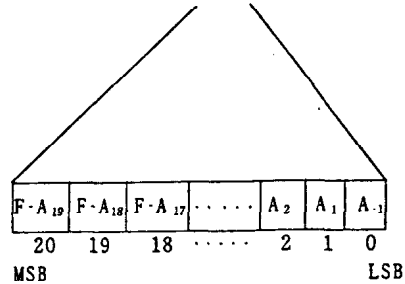
| | |
|---|---|
| <p>S R. 7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>S R. 6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>S R. 5 = ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful Block Erase</p> <p>S R. 4 = WORD/BYTE WRITE STATUS (WBWS) 1 = Error in Word/Byte Write 0 = Successful Word/Byte Write</p> <p>S R. 3 = V_{pp} STATUS (VPPS) 1 = F-V_{pp} Low Detect, Operation Abort 0 = F-V_{pp} OK</p> <p>S R. 2 = WORD/BYTE WRITE SUSPENDED STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed</p> <p>S R. 1 = DEVICE PROTECT STATUS (DPS) 1 = F-\overline{WP} or F-\overline{RP} Lock Detected, Operation Abort 0 = Unlock</p> <p>S R. 0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> | <p>NOTES:</p> <p>Check RY/\overline{BY} or SR.7 to determine block erase or word/byte write completion. SR.6-0 are invalid while SR.7="0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of F-V_{pp} level. The WSM interrogates and indicates the F-V_{pp} level only after Block Erase or Word/ByteWrite command sequences. SR.3 is not guaranteed to reports accurate feedback only when F-V_{pp} ≠ V_{ppH1/2}.</p> <p>The WSM interrogates the F-\overline{WP} and F-\overline{RP} only after Block Erase or Word/ByteWrite command sequences. It informs the system, depending on the attempted operation, if the F-\overline{WP} is not V_{IH}, F-\overline{RP} is not V_{IH}.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p> |
|---|---|

7. Memory Map for Flash Memory

| Address [A ₁₉ -A ₀] | Top Boot | Address [A ₁₉ -A ₁] |
|---|---------------------------------|---|
| FFFFF | 4K-word/8K-byte Boot Block | 1FFFFF |
| FF000 | 4K-word/8K-byte Boot Block | 1FE000 |
| FEFFF | 4K-word/8K-byte Boot Block | 1FDFFF |
| FE000 | 4K-word/8K-byte Parameter Block | 1FC000 |
| FDFFF | 4K-word/8K-byte Parameter Block | 1FBFFF |
| FD000 | 4K-word/8K-byte Parameter Block | 1FA000 |
| FCFFF | 4K-word/8K-byte Parameter Block | 1F9FFF |
| FC000 | 4K-word/8K-byte Parameter Block | 1F8000 |
| FBFFF | 4K-word/8K-byte Parameter Block | 1F7FFF |
| FB000 | 4K-word/8K-byte Parameter Block | 1F6000 |
| FAFFF | 4K-word/8K-byte Parameter Block | 1F5FFF |
| FA000 | 4K-word/8K-byte Parameter Block | 1F4000 |
| F9FFF | 4K-word/8K-byte Parameter Block | 1F3FFF |
| F9000 | 4K-word/8K-byte Parameter Block | 1F2000 |
| F8FFF | 4K-word/8K-byte Parameter Block | 1F1FFF |
| F8000 | 4K-word/8K-byte Parameter Block | 1F0000 |
| F7FFF | 32K-word/64K-byte Main Block | 1EFFFF |
| F0000 | 32K-word/64K-byte Main Block | 1E0000 |
| EFFFF | 32K-word/64K-byte Main Block | 1DFFFF |
| E8000 | 32K-word/64K-byte Main Block | 1D0000 |
| E7FFF | 32K-word/64K-byte Main Block | 1CFFFF |
| E0000 | 32K-word/64K-byte Main Block | 1C0000 |
| DFFFF | 32K-word/64K-byte Main Block | 1BFFFF |
| D8000 | 32K-word/64K-byte Main Block | 1B0000 |
| D7FFF | 32K-word/64K-byte Main Block | 1AFFFF |
| D0000 | 32K-word/64K-byte Main Block | 1A0000 |
| CFFFF | 32K-word/64K-byte Main Block | 19FFFF |
| C8000 | 32K-word/64K-byte Main Block | 190000 |
| C7FFF | 32K-word/64K-byte Main Block | 18FFFF |
| C0000 | 32K-word/64K-byte Main Block | 180000 |
| BFFFF | 32K-word/64K-byte Main Block | 17FFFF |
| B8000 | 32K-word/64K-byte Main Block | 170000 |
| B7FFF | 32K-word/64K-byte Main Block | 16FFFF |
| B0000 | 32K-word/64K-byte Main Block | 160000 |
| AFFFF | 32K-word/64K-byte Main Block | 15FFFF |
| A8000 | 32K-word/64K-byte Main Block | 150000 |
| A7FFF | 32K-word/64K-byte Main Block | 14FFFF |
| A0000 | 32K-word/64K-byte Main Block | 140000 |
| 9FFFF | 32K-word/64K-byte Main Block | 13FFFF |
| 98000 | 32K-word/64K-byte Main Block | 130000 |
| 97FFF | 32K-word/64K-byte Main Block | 12FFFF |
| 90000 | 32K-word/64K-byte Main Block | 120000 |
| 8FFFF | 32K-word/64K-byte Main Block | 11FFFF |
| 88000 | 32K-word/64K-byte Main Block | 110000 |
| 87FFF | 32K-word/64K-byte Main Block | 10FFFF |
| 80000 | 32K-word/64K-byte Main Block | 100000 |
| 7FFFF | 32K-word/64K-byte Main Block | 0FFFFF |
| 78000 | 32K-word/64K-byte Main Block | 0F0000 |
| 77FFF | 32K-word/64K-byte Main Block | 0EFFFF |
| 70000 | 32K-word/64K-byte Main Block | 0E0000 |
| 6FFFF | 32K-word/64K-byte Main Block | 0DFFFF |
| 68000 | 32K-word/64K-byte Main Block | 0D0000 |
| 67FFF | 32K-word/64K-byte Main Block | 0CFFFF |
| 60000 | 32K-word/64K-byte Main Block | 0C0000 |
| 5FFFF | 32K-word/64K-byte Main Block | 0BFFFF |
| 58000 | 32K-word/64K-byte Main Block | 0B0000 |
| 57FFF | 32K-word/64K-byte Main Block | 0AFFFF |
| 50000 | 32K-word/64K-byte Main Block | 0A0000 |
| 4FFFF | 32K-word/64K-byte Main Block | 09FFFF |
| 48000 | 32K-word/64K-byte Main Block | 090000 |
| 47FFF | 32K-word/64K-byte Main Block | 08FFFF |
| 40000 | 32K-word/64K-byte Main Block | 080000 |
| 3FFFF | 32K-word/64K-byte Main Block | 07FFFF |
| 38000 | 32K-word/64K-byte Main Block | 070000 |
| 37FFF | 32K-word/64K-byte Main Block | 06FFFF |
| 30000 | 32K-word/64K-byte Main Block | 060000 |
| 2FFFF | 32K-word/64K-byte Main Block | 05FFFF |
| 28000 | 32K-word/64K-byte Main Block | 050000 |
| 27FFF | 32K-word/64K-byte Main Block | 04FFFF |
| 20000 | 32K-word/64K-byte Main Block | 040000 |
| 1FFFF | 32K-word/64K-byte Main Block | 03FFFF |
| 18000 | 32K-word/64K-byte Main Block | 030000 |
| 17FFF | 32K-word/64K-byte Main Block | 02FFFF |
| 10000 | 32K-word/64K-byte Main Block | 020000 |
| 0FFFF | 32K-word/64K-byte Main Block | 01FFFF |
| 08000 | 32K-word/64K-byte Main Block | 010000 |
| 07FFF | 32K-word/64K-byte Main Block | 00FFFF |
| 00000 | 32K-word/64K-byte Main Block | 000000 |



X8 Mode



X16 Mode

8. Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---------------------------------|--------------------|---------------------------|------|
| Supply voltage (*1, 2) | V_{CC} | -0.2 to +4.6 | V |
| Input voltage (*1, 3) | V_{IN} | -0.2 (*4) to $V_{CC}+0.3$ | V |
| Operating temperature | T_{opr} | -25 to +85 | °C |
| Storage temperature | T_{stg} | -65 to +125 | °C |
| F- V_{PP} voltage (*1) | F- V_{PP} | -0.2 (*4) to +14.0(*5) | V |
| F- \overline{RP} voltage (*1) | F- \overline{RP} | -0.5 (*4) to +14.0(*5) | V |

Notes) *1. The maximum applicable voltage on any pins with respect to GND.

*2. Except F- V_{PP} .

*3. Except F- \overline{RP} .

*4. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

*5. +14.0V overshoot is allowed when the pulse width is less than 20nsec.

9. Recommended DC Operating Conditions

($T_i = -25\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------|---------------|-----------|------|-------------------|------|
| Supply voltage | V_{CC} | 2.7 | 3.0 | 3.6 | V |
| Input voltage | V_{IH} | 2.2 | | $V_{CC}+0.3$ (*1) | V |
| | V_{IL} | -0.2 (*2) | | 0.8 | V |
| | V_{IH} (*3) | 11.4 | | 12.6 | V |

Notes) *1. V_{CC} is the lower one of S- V_{CC} and F- V_{CC} .

*2. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

*3. This voltage is applicable to F- \overline{RP} Pin only.

10. Pin Capacitance

($T_i = 25\text{ }^\circ\text{C}$, $f = 1\text{MHz}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------|-----------|----------------|------|------|------|------|
| Input capacitance | C_{IN} | $V_{IN} = 0V$ | | | 20 | pF |
| I/O capacitance | $C_{I/O}$ | $V_{I/O} = 0V$ | | | 22 | pF |

*1

*1

Note) *1 Sampled but not 100% tested

11. DC Characteristics

DC Characteristics ($T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

| Parameter | Symbol | Conditions | Min. | Typ. (*1) | Max. | Unit | |
|---|---|--|--|--|----------|---------------|---------------|
| Input leakage current (I_{LI}) | I_{LI} | $V_{IN} = V_{CC}$ or GND | -1.5 | | +1.5 | μA | |
| Output leakage current (I_{LO}) | I_{LO} | $V_{OUT} = V_{CC}$ or GND | -1.5 | | +1.5 | μA | |
| F- V_{CC} V_{CC} Standby Current | I_{CCS} (*2, 7) | $F\text{-}\overline{CE} = F\text{-}\overline{RP} = F\text{-}V_{CC} \pm 0.2\text{V}$ $F\text{-}\overline{WP} = F\text{-}V_{CC} \pm 0.2\text{V}$ or $F\text{-}GND \pm 0.2\text{V}$ | | 25 | 50 | μA | |
| | | $F\text{-}\overline{CE} = F\text{-}\overline{RP} = V_{IH}$ $F\text{-}\overline{WP} = V_{IH}$ or V_{IL} | | 0.2 | 2 | mA | |
| | Deep Power-Down Current | I_{CCD} (*7) | $F\text{-}\overline{RP} = F\text{-}GND \pm 0.2\text{V}$, $I_{OUT} (F\text{-}RY/BY) = 0\text{mA}$ | | 5 | 10 | μA |
| | V_{CC} Read Current | I_{CCR} (*3, 4) | CMOS Input $F\text{-}\overline{CE} = F\text{-}GND$, $f = 5\text{MHz}$, $I_{OUT} = 0\text{mA}$ | | | 25 | mA |
| TTL Input $F\text{-}\overline{CE} = F\text{-}GND$, $f = 5\text{MHz}$, $I_{OUT} = 0\text{mA}$ | | | | | 30 | mA | |
| V_{CC} Word/Byte Write Current | I_{CCW} | $F\text{-}V_{PP} = V_{PPH}$ | | | 17 | mA | |
| V_{CC} Block Erase Current | I_{CCE} | $F\text{-}V_{PP} = V_{PPH}$ | | | 17 | mA | |
| V_{CC} Word/Byte Write Block Erase Suspend Current | I_{CCWS} I_{CCES} | $F\text{-}\overline{CE} = V_{IH}$ | | | 6 | mA | |
| F- V_{PP} V_{PP} Standby or Read Current | I_{PPS} I_{PPR} | $F\text{-}V_{PP} = F\text{-}V_{CC}$ | | ± 2 | ± 15 | μA | |
| | | $F\text{-}V_{PP} > F\text{-}V_{CC}$ | | 10 | 200 | μA | |
| | V_{PP} Deep Power-Down Current | I_{PPD} | $F\text{-}\overline{RP} = F\text{-}GND \pm 0.2\text{V}$ | | 0.1 | 5 | μA |
| | V_{PP} Word/Byte Write Current | I_{PPW} | $F\text{-}V_{PP} = V_{PPH}$ | | 12 | 40 | mA |
| | V_{PP} Block Erase Current | I_{PPE} | $F\text{-}V_{PP} = V_{PPH}$ | | 8 | 25 | mA |
| | V_{PP} Word/Byte Write or Block Erase Suspend Current | I_{PPWS} I_{PPES} | $F\text{-}V_{PP} = V_{PPH}$ | | 10 | 200 | μA |
| S- V_{CC} Standby Current | I_{SB} | $S\text{-}\overline{CE}_1, S\text{-}\overline{CE}_2 \geq S\text{-}V_{CC} - 0.2\text{V}$ or $S\text{-}\overline{CE}_2 \leq 0.2\text{V}$ | | | 15 | μA | |
| | | $S\text{-}\overline{CE}_1 = V_{IH}$ or $S\text{-}\overline{CE}_2 = V_{IL}$ | | | 3.0 | mA | |
| | Operation Current | I_{CC1} I_{CC2} | $S\text{-}\overline{CE}_1 = V_{IL}$, $S\text{-}\overline{CE}_2 = V_{IH}$ $V_{IN} = V_{IL}$ or V_{IH} | $t_{CYCLE} = \text{Min.}$ $I_{I/O} = 0\text{mA}$ | | 30 | mA |
| | | | $S\text{-}\overline{CE}_1 = 0.2\text{V}$, $S\text{-}\overline{CE}_2 = S\text{-}V_{CC} - 0.2\text{V}$ $V_{IN} = S\text{-}V_{CC} - 0.2\text{V}$ or 0.2V | $t_{CYCLE} = 1\mu\text{s}$ $I_{I/O} = 0\text{mA}$ | | 3 | mA |

DC Characteristics (Continue)

 $(T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{cc} = 2.7\text{ V}$ to 3.6 V)

| Parameter | Symbol | Test Conditions | Min. | Typ (*1) | Max. | Unit |
|--|-----------------|--------------------------------|------|-------------|----------------|------|
| Input Low Voltage | V_{IL} | | -0.2 | | 0.8 | V |
| Input High Voltage | V_{IH} | | 2.2 | | $V_{cc} + 0.3$ | V |
| Output Low Voltage | V_{OL} (*2) | $I_{OL} = 2.0\text{ mA}$ | | | 0.4 | V |
| Output High Voltage | V_{OH} (*2) | $I_{OH} = -1.0\text{ mA}$ | 2.4 | | | V |
| F- V_{PP} Lockout during Normal Operations | V_{PPLK} (*5) | | | | 1.5 | V |
| F- V_{PP} Word/Byte Write or Block Erase Operations | V_{PPH} | | 2.7 | | 3.6 | V |
| F- V_{CC} Lockout Voltage | V_{LKO} | | 1.5 | | | V |
| F- \overline{RP} Unlock Voltage | V_{RH} (*6) | Unavailable F- \overline{WP} | 11.4 | | 12.6 | V |

Notes)

- Reference values at $V_{cc}=3.0\text{ V}$ and $T_a=+25^\circ\text{C}$.
- Includes F-RY/ \overline{BY} .
- Automatic Power Savings (APS) for Flash Memory reduces typical I_{CCR} to 3mA at 2.7V V_{cc} in static operation.
- CMOS inputs are either $V_{cc} \pm 0.2\text{ V}$ or $\text{GND} \pm 0.2\text{ V}$. TTL inputs are either V_{IL} or V_{IH} .
- Block erases and word/byte writes are inhibited when $F\text{-}V_{PP} \leq V_{PPLK}$ and not guaranteed in the range between $V_{PPLK}(\text{max})$ and $V_{PPH}(\text{min})$, and above $V_{PPH}(\text{max})$.
- F- \overline{RP} connection to a V_{RH} supply is allowed for a maximum cumulative period of 80 hours.
- F- \overline{BYTE} is $V_{cc} \pm 0.2\text{ V}$ in word mode and is $\text{GND} \pm 0.2\text{ V}$ in byte mode.
F- \overline{WP} is $V_{cc} \pm 0.2\text{ V}$ or $\text{GND} \pm 0.2\text{ V}$.

12. Flash memory AC Characteristics

AC Test Conditions

| | |
|------------------------------------|----------------------------|
| Input pulse level | 0 V to 2.7 V |
| Input rise and fall time | 5 ns |
| Input and Output timing Ref. level | 1.35 V |
| Output load | 1TTL+C _L (30pF) |

Read Cycle (T_i = -25°C to +85°C, V_{CC} = 2.7V to 3.6V)

| Parameter | Sym. | Min. | Max. | Unit |
|---|-------------------|------|------|------|
| Read Cycle Time | t _{AVAV} | 100 | | ns |
| Address to Output Delay | t _{AVOQ} | | 100 | ns |
| F- $\overline{\text{CE}}$ to Output Delay | t _{ELQV} | | 100 | ns |
| F- $\overline{\text{RP}}$ High to Output Delay | t _{PHOV} | | 10 | μs |
| F- $\overline{\text{OE}}$ to Output Delay | t _{GLQV} | | 45 | ns |
| F- $\overline{\text{CE}}$ to Output in Low Z | t _{ELQX} | 0 | | ns |
| F- $\overline{\text{CE}}$ High to Output in High Z | t _{EHQZ} | | 45 | ns |
| F- $\overline{\text{OE}}$ to Output in Low Z | t _{GLQX} | 0 | | ns |
| F- $\overline{\text{OE}}$ High to Output in High Z | t _{GHQZ} | | 20 | ns |
| Output Hold from Address, F- $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ Change, Whichever Occurs First | t _{OH} | 0 | | ns |
| F-BYTE and A ₁ to Output Delay | t _{FVQV} | | 90 | ns |
| F-BYTE Low to Output in High Z | t _{FLOZ} | | 30 | ns |
| F- $\overline{\text{CE}}$ to F-BYTE High Z or Low | t _{ELFV} | | 5 | ns |

*1
*1

Notes) *1. F- $\overline{\text{OE}}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of F- $\overline{\text{OE}}$ without impact on t_{ELQV}.

Write Cycle (F- $\overline{\text{WE}}$ Controlled) (*2) (T_i = -25°C to +85°C, V_{CC} = 2.7V to 3.6V)

| Parameter | Sym. | Min. | Max. | Unit |
|--|--------------------|------|------|------|
| Write Cycle Time | t _{AVAV} | 100 | | ns |
| F- $\overline{\text{RP}}$ High Recovery to F- $\overline{\text{WE}}$ going to Low | t _{PHWL} | 10 | | μs |
| F- $\overline{\text{CE}}$ Setup to F- $\overline{\text{WE}}$ Going Low | t _{ELWL} | 0 | | ns |
| F- $\overline{\text{WE}}$ Pulse Width | t _{WLWH} | 50 | | ns |
| F- $\overline{\text{RP}}$ V _{IH} Setup to F- $\overline{\text{WE}}$ Going High | t _{PHHWH} | 100 | | ns |
| F- $\overline{\text{WP}}$ V _{IH} Setup to F- $\overline{\text{WE}}$ Going High | t _{SHWH} | 100 | | ns |
| F-V _{PP} Setup to F- $\overline{\text{WE}}$ Going High | t _{VPWH} | 100 | | ns |
| Address Setup to F- $\overline{\text{WE}}$ Going High | t _{AVWH} | 50 | | ns |
| Data Setup to F- $\overline{\text{WE}}$ Going High | t _{DVWH} | 50 | | ns |
| Data Hold from F- $\overline{\text{WE}}$ High | t _{WHDX} | 0 | | ns |
| Address Hold from F- $\overline{\text{WE}}$ High | t _{WHAX} | 0 | | ns |
| F- $\overline{\text{CE}}$ Hold from F- $\overline{\text{WE}}$ High | t _{WHEH} | 0 | | ns |
| F- $\overline{\text{WE}}$ Pulse Width High | t _{WHWL} | 30 | | ns |
| F- $\overline{\text{WE}}$ High to F-RY/ $\overline{\text{BY}}$ Going Low | t _{WHRL} | | 100 | ns |
| Write Recovery before Read | t _{WHGL} | 0 | | ns |
| F-V _{PP} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High Z | t _{QVVL} | 0 | | ns |
| F- $\overline{\text{RP}}$ V _{IH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High Z | t _{QVPH} | 0 | | ns |
| F- $\overline{\text{WP}}$ V _{IH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High | t _{QVSL} | 0 | | ns |
| F-BYTE Setup to F- $\overline{\text{WE}}$ Going High | t _{FVWH} | 50 | | ns |
| F-BYTE Hold from F- $\overline{\text{WE}}$ High | t _{WHFV} | 100 | | ns |

*3
*3

Write Cycle (F-CE Controlled) (*2)

(T_i = -25°C to +85°C , V_{cc} = 2.7V to 3.6V)

| Parameter | Symb. | Min. | Max. | Unit |
|--|--------------------|------|------|------|
| Write Cycle Time | t _{AVAV} | 100 | | ns |
| F- \overline{RP} High Recovery to F- \overline{CE} going to Low | t _{PHL} | 10 | | μs |
| F- \overline{WE} Setup to F- \overline{CE} Going Low | t _{WLEL} | 0 | | ns |
| F- \overline{CE} Pulse Width | t _{LEFH} | 70 | | ns |
| F- \overline{RP} V _{IH} Setup to F- \overline{CE} Going High | t _{PHIHH} | 100 | | ns |
| F- \overline{WP} V _{IH} Setup to F- \overline{CE} Going High | t _{SHEH} | 100 | | ns |
| F-V _{PP} Setup to F- \overline{CE} Going High | t _{VPEH} | 100 | | ns |
| Address Setup to F- \overline{CE} Going High | t _{AVEH} | 50 | | ns |
| Data Setup to F- \overline{CE} Going High | t _{DVEH} | 50 | | ns |
| Data Hold from F- \overline{CE} High | t _{EHDX} | 0 | | ns |
| Address Hold from F- \overline{CE} High | t _{EHAX} | 0 | | ns |
| F- \overline{WE} Hold from F- \overline{CE} High | t _{ENWH} | 0 | | ns |
| F- \overline{CE} Pulse Width High | t _{EHHL} | 25 | | ns |
| F- \overline{CE} High to F-RY/ \overline{BY} Going Low | t _{EHRL} | | 100 | ns |
| Write Recovery before Read | t _{ENGL} | 0 | | ns |
| F-V _{pp} Hold from Valid SRD, F-RY/ \overline{BY} High Z | t _{QVVL} | 0 | | ns |
| F- \overline{RP} V _{IH} Hold from Valid SRD, F-RY/ \overline{BY} High Z | t _{QVPH} | 0 | | ns |
| F- \overline{WP} V _{IH} Hold from Valid SRD, F-RY/ \overline{BY} High | t _{QVSL} | 0 | | ns |
| F-BYTE Setup to F- \overline{CE} Going High | t _{FVEH} | 50 | | ns |
| F-BYTE Hold from F- \overline{CE} High | t _{ENFV} | 100 | | ns |

*3

*3

Notes) *2. Read timing characteristics during block erase and word/byte write operations are the same as during read-only operations. Refer to AC Characteristics for Read Cycle.

*3. Refer to Section 5. Flash Memory Command Definition for valid AIN and DIN for block erase or word/byte write.

Block Erase and Word/Byte Write Performance

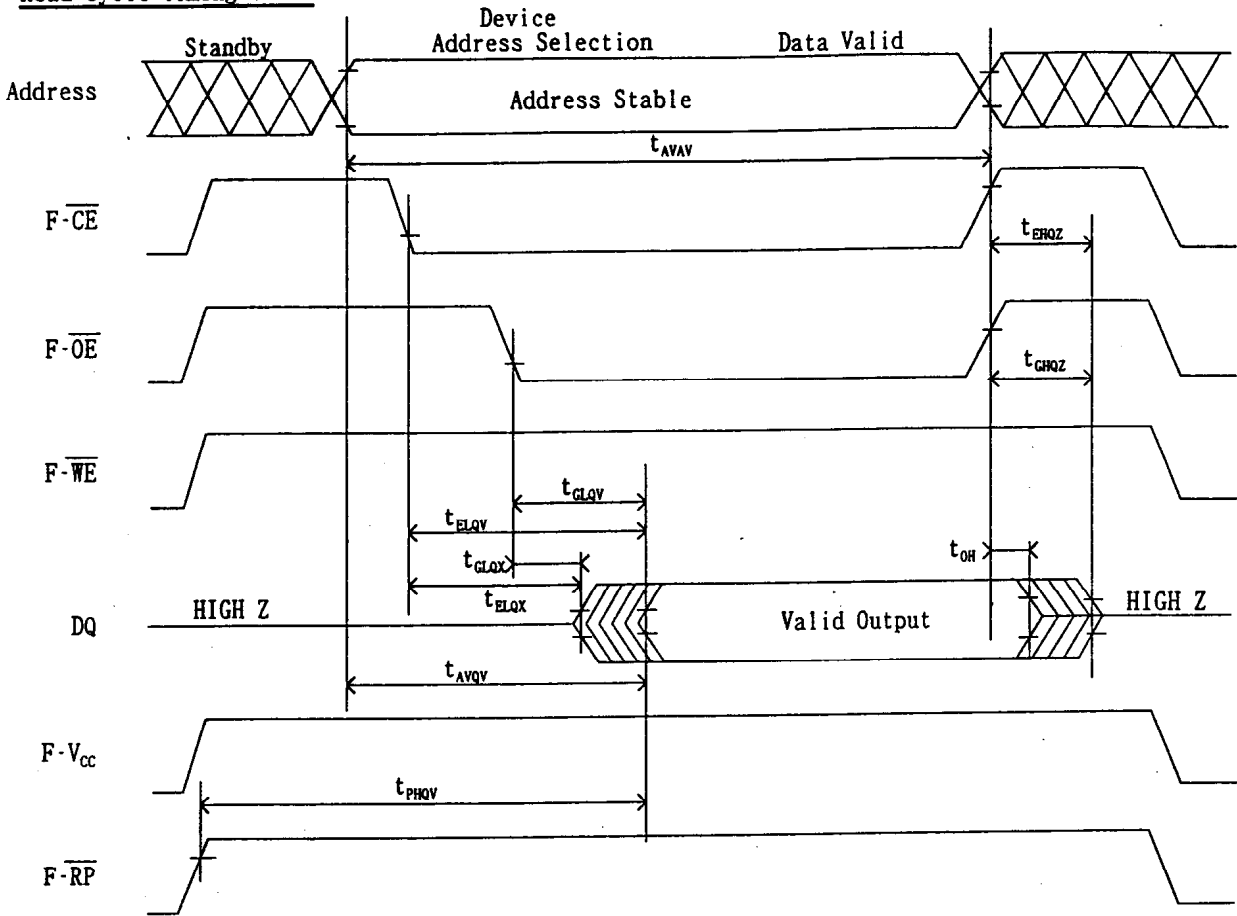
($T_s = -25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{ V}$ to 3.6 V)

| Sym. | Parameter | | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | | | Unit | |
|----------------------------|--|--------------------------------|---|---------------------|------|----------------|----|
| | | | Min. | Typ. ^(*) | Max. | | |
| t_{WHQV1} t_{EHQV1} | Word/Byte Write Time | 32K-word Block /64K-byte Block | | 55 | | $\mu\text{ s}$ | *5 |
| | | 4K-word Block /8K-byte Block | | 60 | | $\mu\text{ s}$ | *5 |
| | Block Write Time (at word mode) | 32K-word Block | | 1.8 | | s | *5 |
| | | 4K-word Block | | 0.3 | | s | *5 |
| | Block Write Time (at byte mode) | 64K-byte Block | | 3.6 | | s | *5 |
| | | 8K-byte Block | | 0.6 | | s | *5 |
| t_{WHQV2} t_{EHQV2} | Block Erase Time | 32K-word Block | | 1.2 | | s | *5 |
| | | 64K-byte Block | | | | s | *5 |
| | | 4K-word Block /8K-byte Block | | 0.5 | | s | *5 |
| t_{WHRZ1} t_{EHRZ1} | Word/Byte Write Suspend Latency Time to Read | | | 7.5 | 8.6 | $\mu\text{ s}$ | |
| t_{WHRZ2} t_{EHRZ2} | Erase Suspend Latency Time to Read | | | 19.3 | 23.6 | $\mu\text{ s}$ | |

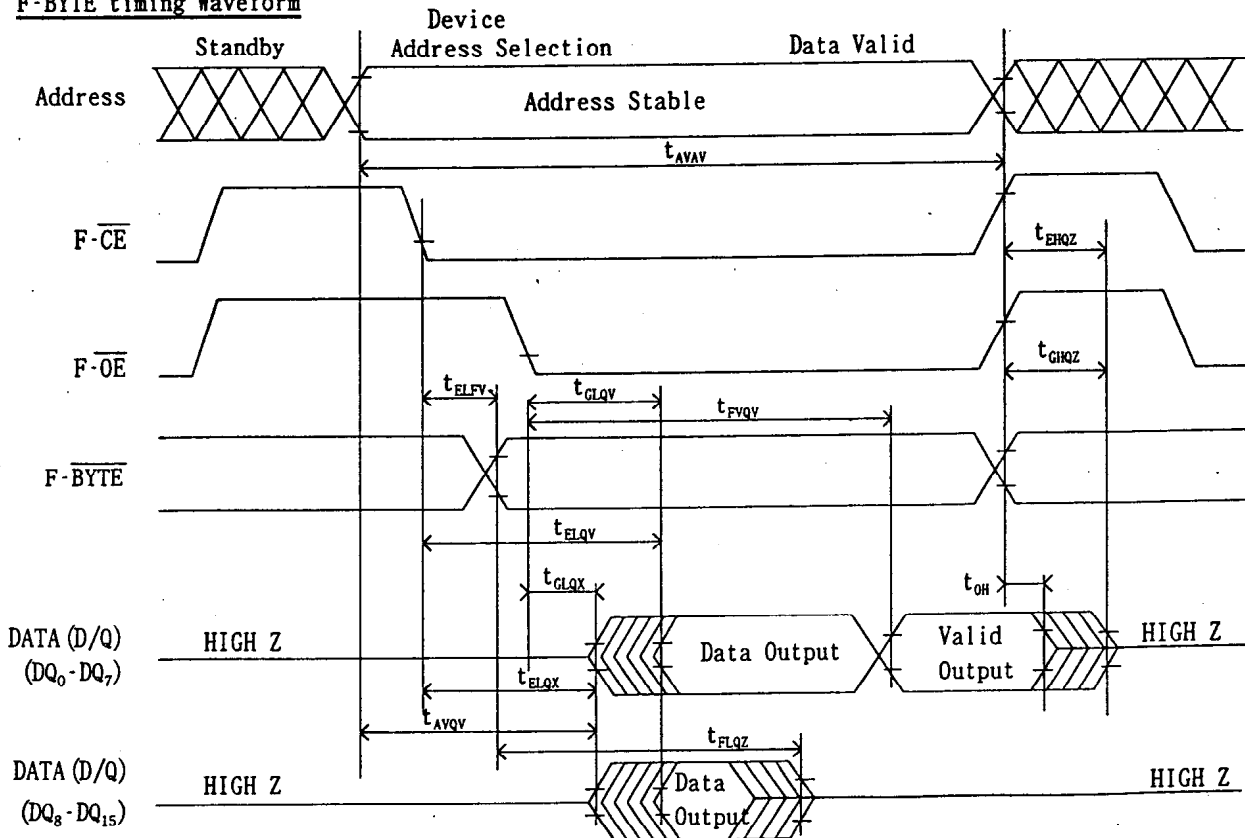
Notes) *4. Reference values at $T_s = +25^{\circ}\text{C}$ and $V_{CC} = 3.0\text{ V}$, $V_{PP} = 3.0\text{ V}$.

*5. Excludes system-level overhead.

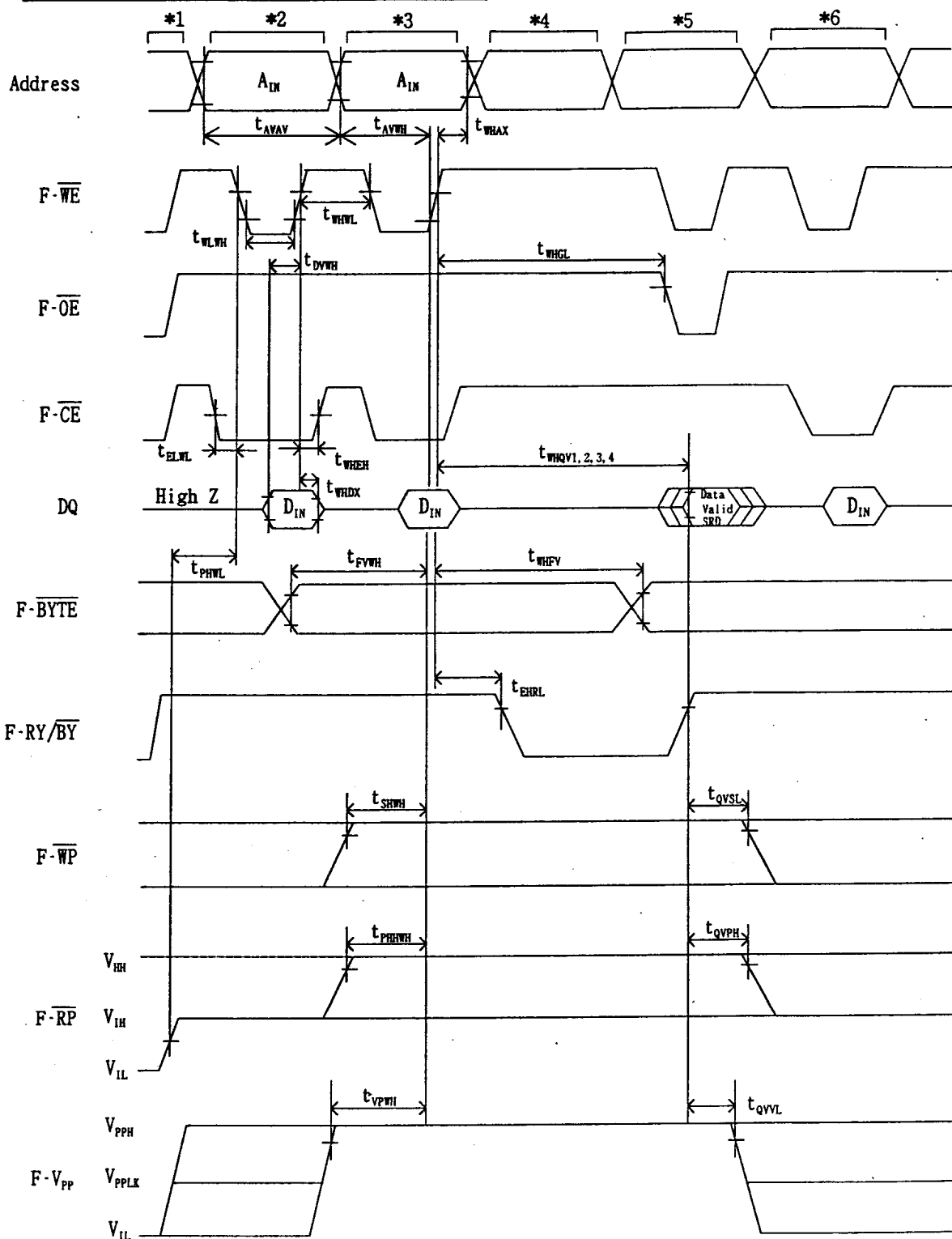
Flash Memory AC Characteristic Timing Chart
Read Cycle timing chart



F-BYTE timing Waveform



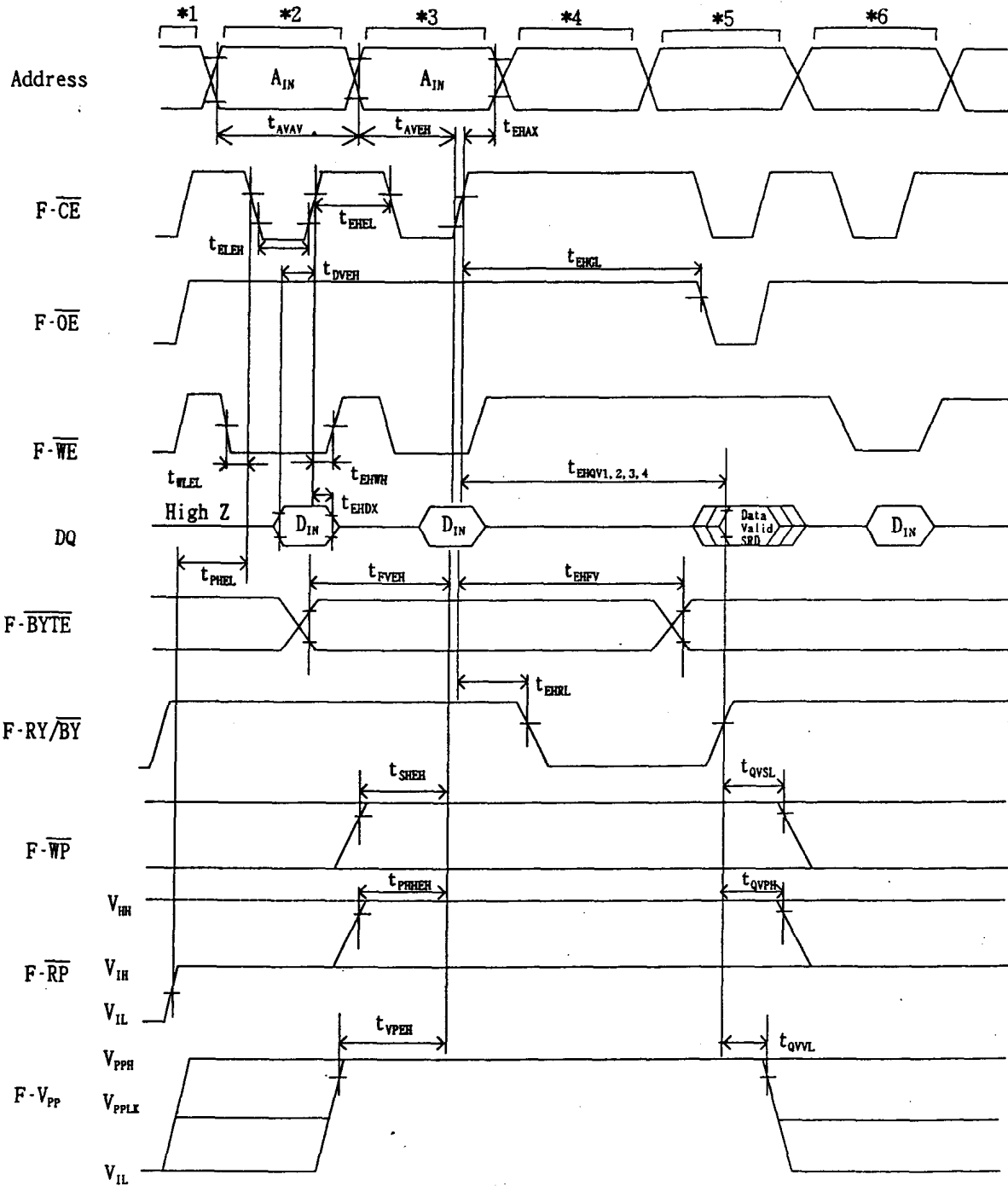
Write cycle timing chart (F-WE controlled)



Notes:

- *1. V_{CC} Power-up and standby.
- *2. Write block erase or word/byte write setup.
- *3. Write block erase confirm or valid address and data.
- *4. Automated erase or program delay.
- *5. Read status register data.
- *6. Write Read Array command.

Write cycle timing chart (F- \overline{CE} controlled)



Notes:

- *1. V_{CC} Power-up and standby.
- *2. Write block erase or word/byte write setup.
- *3. Write block erase confirm or valid address and data.
- *4. Automated erase or program delay.
- *5. Read status register data.
- *6. Write Read Array command.

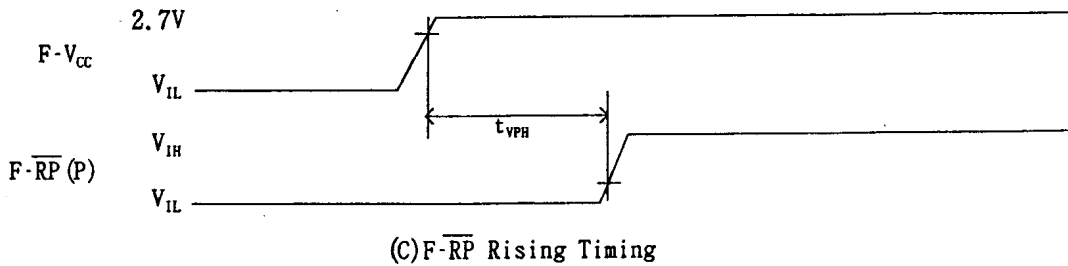
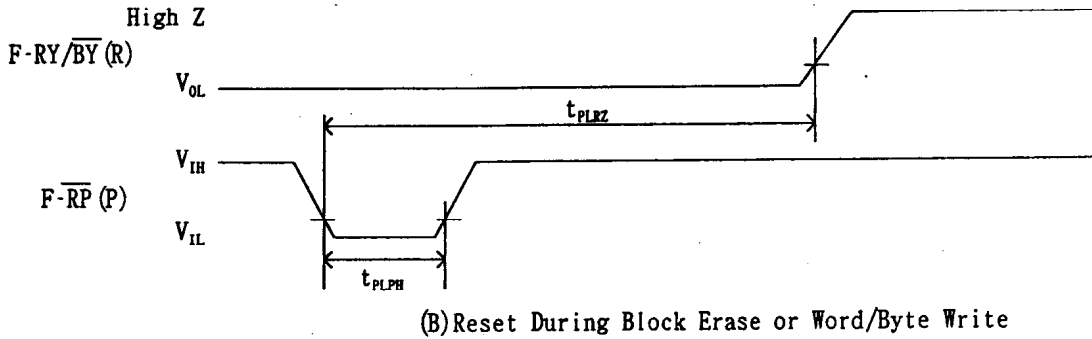
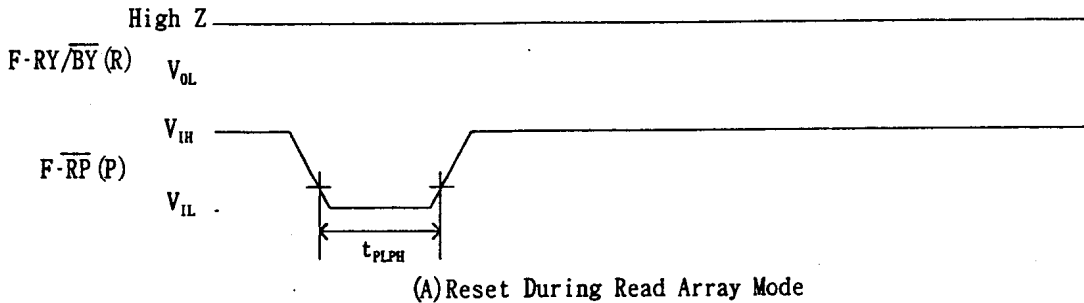
Reset Operations

($T_s = -25\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

| Parameter | Sym. | Min. | Max. | Unit | |
|--|------------|------|------|---------------|-------|
| F- $\overline{\text{RP}}$ Pulse Low Time (If F- $\overline{\text{RP}}$ is tied to V_{CC} , this specification is not applicable.) | t_{PLPH} | 100 | | ns | |
| F- $\overline{\text{RP}}$ Low to Reset during Block Erase or Write | t_{PLRZ} | | 23.6 | μs | *1, 2 |
| F- V_{CC} 2.7V to F- $\overline{\text{RP}}$ High | t_{VPH} | 100 | | ns | *3 |

- Notes)*1. If F- $\overline{\text{RP}}$ is asserted while a block erase or word/byte write operation is not executing, the reset will complete with 100ns.
 *2. A reset time, t_{PHOV} , is required from the later of F-RY/ $\overline{\text{BY}}$ going High Z or F- $\overline{\text{RP}}$ going high until outputs are valid.
 *3. When the device power-up, holding F- $\overline{\text{RP}}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



13. SRAM AC Electrical Characteristics

SRAM AC Test Conditions

| | |
|------------------------------------|---------------------------------|
| Input pulse level | 0.4 V to 2.2 V |
| Input rise and fall time | 5 ns |
| Input and Output timing Ref. level | 1.5 V |
| Output load | 1TTL+C _L (30pF) (*1) |

Note) *1. Including scope and jig capacitance.

Read Cycle

(T_a = -25 °C to +85 °C , V_{cc} = 2.7 V to 3.6 V)

| Parameter | Sym. | Min. | Max. | Unit | |
|---|-------------------|------|------|------|----|
| Read Cycle Time | t _{RC} | 85 | | ns | |
| Address access time | t _{AA} | | 85 | ns | |
| Chip enable access time (S- \overline{CE}_1) | t _{ACE1} | | 85 | ns | |
| (S- \overline{CE}_2) | t _{ACE2} | | 85 | ns | |
| Output enable to output valid | t _{OE} | | 40 | ns | |
| Output hold from address change | t _{OH} | 10 | | ns | |
| S- \overline{CE}_1 , S- \overline{CE}_2 Low (S- \overline{CE}_1) | t _{LZ1} | 10 | | ns | *2 |
| to output active (S- \overline{CE}_2) | t _{LZ2} | 10 | | ns | *2 |
| S- \overline{OE} Low to output active | t _{OLZ} | 5 | | ns | *2 |
| S- \overline{CE}_1 , S- \overline{CE}_2 High to (S- \overline{CE}_1) | t _{HZ1} | 0 | 25 | ns | *2 |
| output in High impedance (S- \overline{CE}_2) | t _{HZ2} | 0 | 25 | ns | *2 |
| S- \overline{OE} High to output in High impedance | t _{OHZ} | 0 | 25 | ns | *2 |

Write Cycle

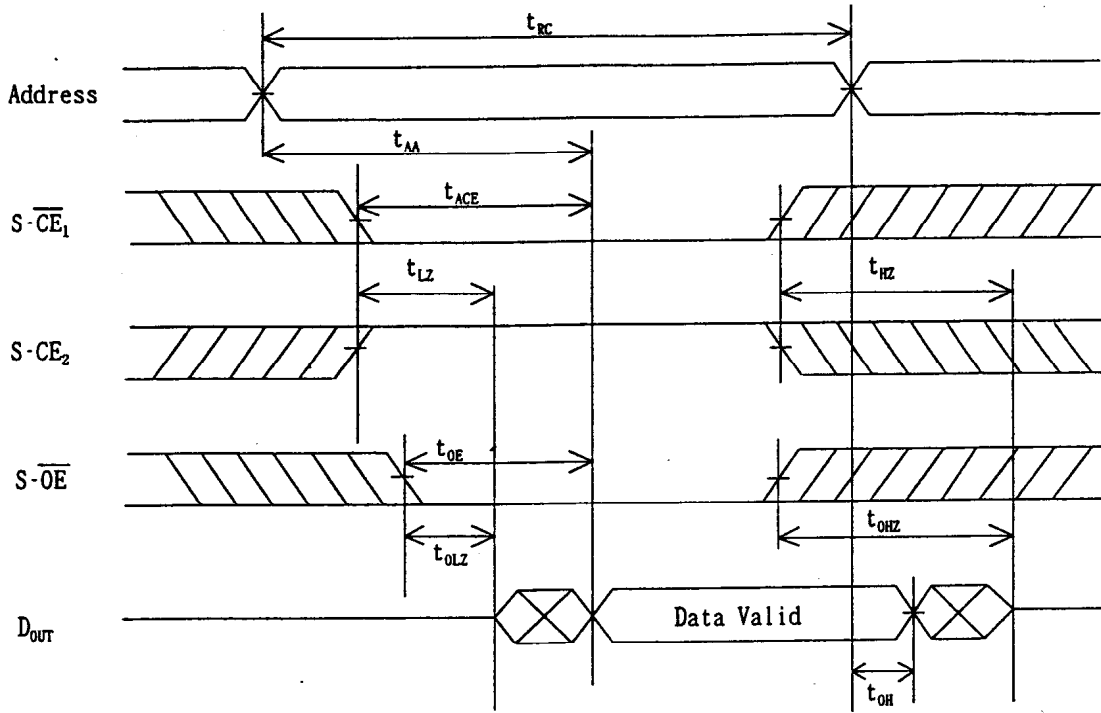
(T_a = -25 °C to +85 °C , V_{cc} = 2.7 V to 3.6 V)

| Parameter | Sym. | Min. | Max. | Unit | |
|--|------------------|------|------|------|----|
| Write cycle time | t _{WC} | 85 | | ns | |
| Chip enable to end of write | t _{CEW} | 70 | | ns | |
| Address valid to end of write | t _{AV} | 70 | | ns | |
| Address setup time | t _{AS} | 0 | | ns | |
| Write pulse width | t _{WP} | 55 | | ns | |
| Write recovery time | t _{WR} | 0 | | ns | |
| Input data setup time | t _{DW} | 35 | | ns | |
| Input data hold time | t _{DH} | 0 | | ns | |
| S- \overline{WE} High to output active | t _{OW} | 5 | | ns | *2 |
| S- \overline{WE} Low to output in High impedance | t _{OZ} | 0 | 25 | ns | *2 |

*2. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

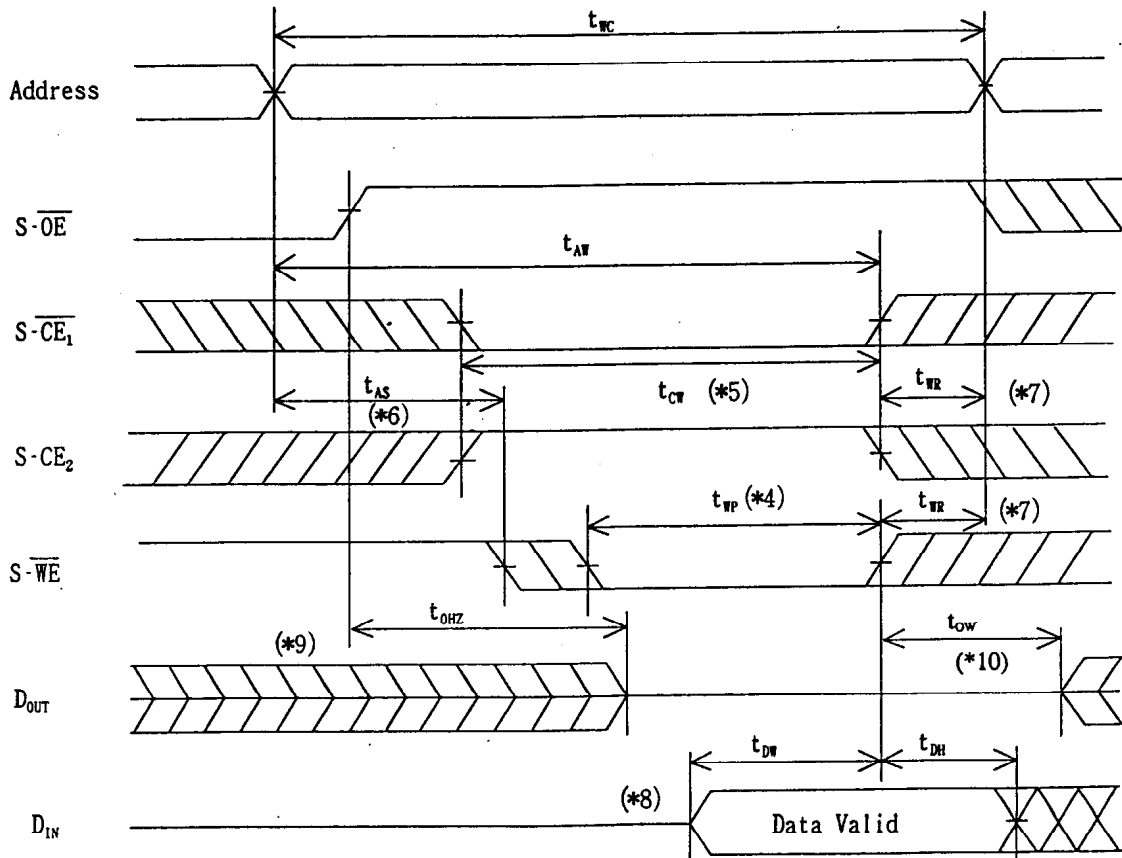
SRAM AC Characteristics Timing Chart

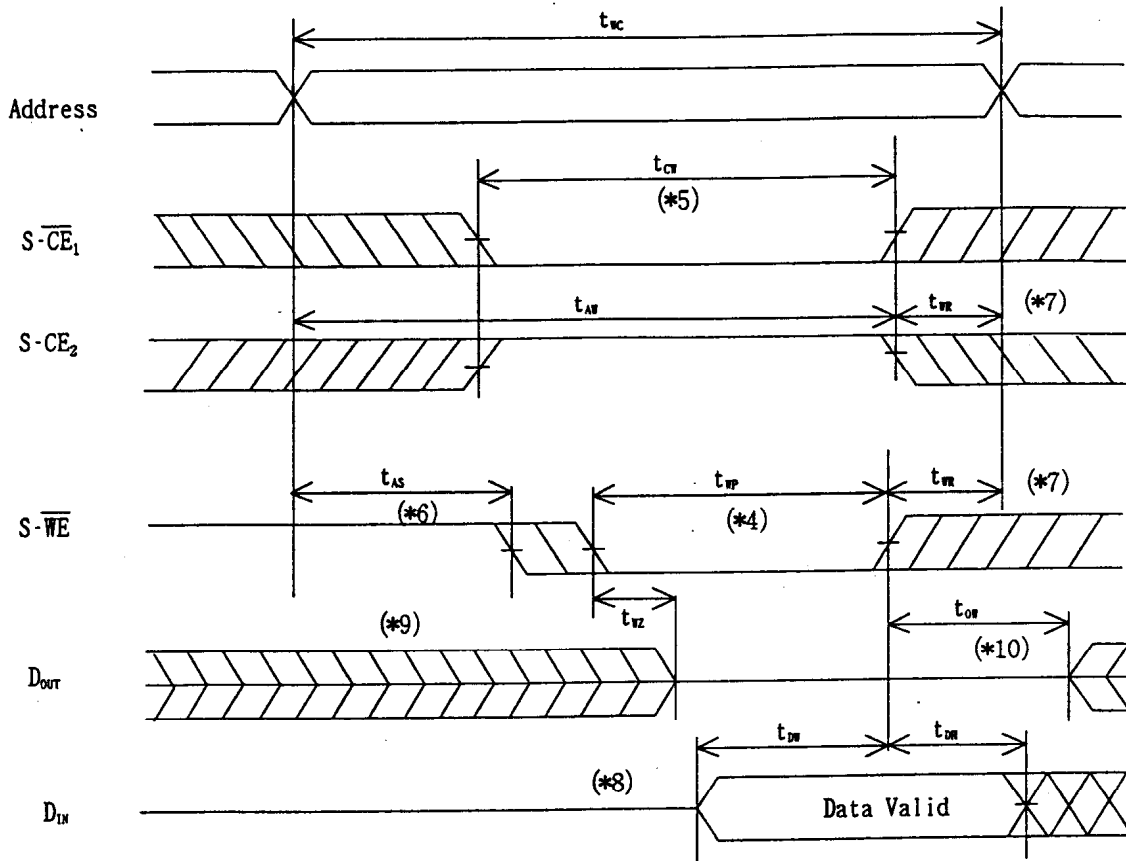
Read cycle timing chart - (*3)



*3 S-WE is high for Read cycle.

Write cycle timing chart - (S-OE Controlled)



Write cycle timing chart—(S- \overline{OE} Low fixed)

Notes)

- *4. A write occurs during the overlap of a low S- \overline{CE}_1 , a high S- \overline{CE}_2 and a low S- \overline{WE} . A write begins at the latest transition among S- \overline{CE}_1 going low, S- \overline{CE}_2 going high and S- \overline{WE} going low. A write ends at the earliest transition among S- \overline{CE}_1 going high, S- \overline{CE}_2 going low and S- \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- *5. t_{CW} is measured from the later of S- \overline{CE}_1 going low or S- \overline{CE}_2 going high to the end of write.
- *6. t_{AS} is measured from the address valid to the beginning of write.
- *7. t_{WR} is measured from the end of write to the address change.
- *8. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- *9. If S- \overline{CE}_1 goes low or S- \overline{CE}_2 goes high simultaneously with S- \overline{WE} going low or after S- \overline{WE} going low, the outputs remain in high impedance state.
- *10. If S- \overline{CE}_1 goes high or S- \overline{CE}_2 goes low simultaneously with S- \overline{WE} going high or S- \overline{WE} going high, the outputs remain in high impedance state.

14. SRAM Data Retention Characteristics

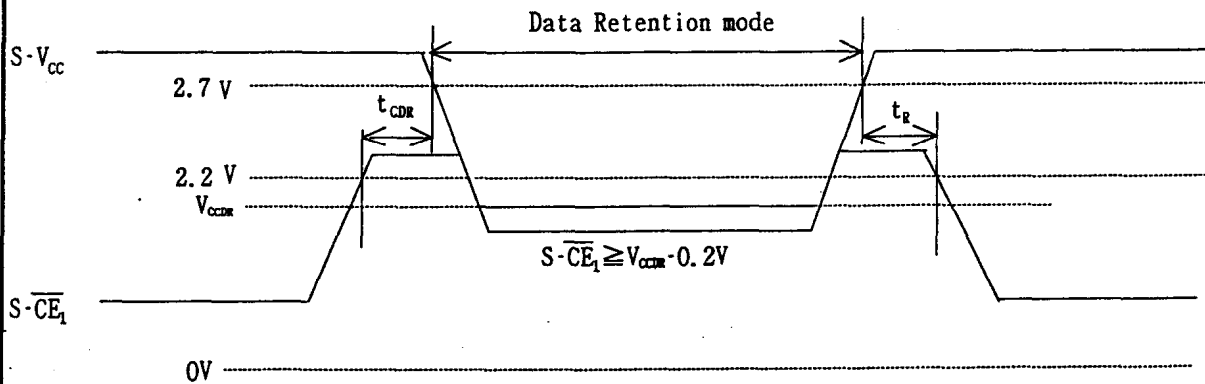
($T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Sym. | Conditions | Min. | Typ. (*1) | Max. | Unit |
|----------------------------------|------------|---|------|-----------|------|---------------|
| Data Retention Supply voltage | V_{CCDR} | $S\text{-CE}_2 \leq 0.2\text{V}$ or $S\text{-}\overline{\text{CE}}_1 \geq V_{CCDR} - 0.2\text{V}$ (*2) | 2.0 | | 3.6 | V |
| Data Retention Supply current | I_{CCDR} | $V_{CCDR} = 3\text{V}$ $S\text{-CE}_2 \leq 0.2\text{V}$ or $S\text{-}\overline{\text{CE}}_1 \geq V_{CCDR} - 0.2\text{V}$ (*2) | | 0.2 | 15 | μA |
| Chip enable setup time | t_{CDR} | | 0 | | | ns |
| Chip enable hold time | t_R | | 5 | | | ms |

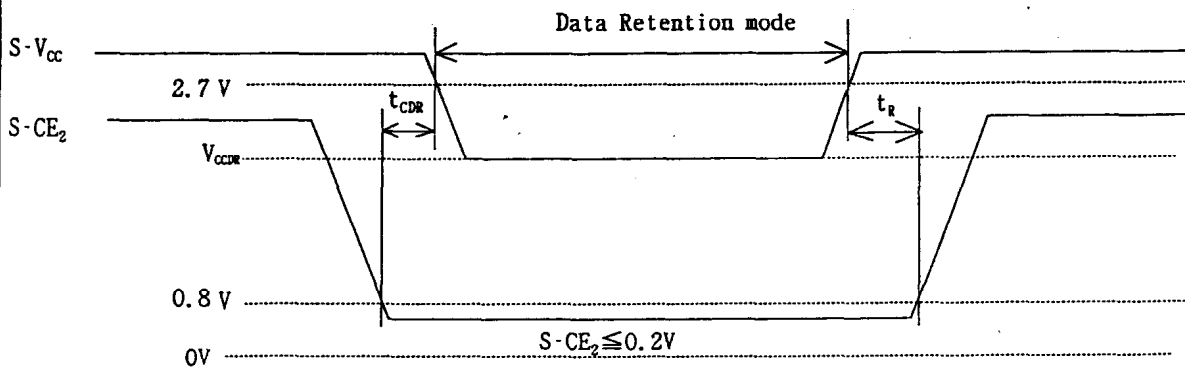
Notes) *1. Reference value at $T_a = 25^\circ\text{C}$, $S\text{-}V_{CC} = 3.0\text{V}$.

*2. $S\text{-}\overline{\text{CE}}_1 \geq V_{CC} - 0.2\text{V}$, $S\text{-CE}_2 \geq V_{CC} - 0.2\text{V}$ ($S\text{-}\overline{\text{CE}}_1$ controlled) or $S\text{-CE}_2 \leq 0.2\text{V}$ ($S\text{-CE}_2$ controlled)

Data Retention timing chart ($S\text{-}\overline{\text{CE}}_1$ Controlled) (*3)



Data Retention timing chart ($S\text{-CE}_2$ Controlled)



Note) *3. To control the data retention mode at $S\text{-}\overline{\text{CE}}_1$, fix the input level of $S\text{-CE}_2$ between V_{CCDR} and $V_{CCDR} - 0.2\text{V}$ or 0V or 0.2V and during the data retention mode.

15. Notes

This product is a stacked CSP package that a 16M (x8/x16) bit Flash Memory and a 2M (x8) bit SRAM are assembled into.

Supply Power

Maximum difference (between $F-V_{CC}$ and $S-V_{CC}$) of the voltage is less than 0.3V.

Power Supply and Chip Enable of Flash Memory and SRAM

$S-\overline{CE}_1$ should not be LOW and $S-CE_2$ should not be HIGH when $F-\overline{CE}$ is LOW simultaneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both $F-V_{CC}$ and $S-V_{CC}$ are needed to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

Power UP Sequence

When turning on Flash memory power supply, keep $F-\overline{RP}$ LOW. After $F-V_{CC}$ reaches over 2.7V, keep $F-\overline{RP}$ LOW for more than 100nsec.

Device Decoupling

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals ($F-\overline{CE}$, $S-\overline{CE}_1$, $S-CE_2$).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.

Such noises, when induced onto $\overline{F\text{-WE}}$ signal or power supply may be interpreted as false commands, causing undesired memory updating.

To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block

By setting a $\overline{F\text{-WP}}$ to low, only the boot block can be protected against overwriting.

Parameter and main blocks cannot be locked.

System program, etc., can be locked by storing them in the boot block.

When a high voltage is applied to $\overline{F\text{-RP}}$, overwrite operation is enabled for all blocks.

For further information on setting/resetting of block bit, and controlling of $\overline{F\text{-WP}}$ and $\overline{F\text{-RP}}$, refer to the specification. (See 5. Command Definitions P.5)

2) Data protection through V_{pp}

When the level of V_{pp} is lower than V_{PPLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.

For the lockout voltage, refer to the specification. (See Chapter 11. DC Characteristics P.10)

Data protection during voltage transition

1) Data protection thorough $\overline{F\text{-RP}}$

When the $\overline{F\text{-RP}}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.

For the details of $\overline{F\text{-RP}}$ control, refer to the specification. (See chapter 12. Flash Memory AC Electrical Characteristics)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a $0.1\mu\text{F}$ ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. Low inductance capacitors should be placed as close as possible to package leads.

2. V_{PP} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power Supply trace. Use similar trace widths and layout considerations given to the V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programmed "1".

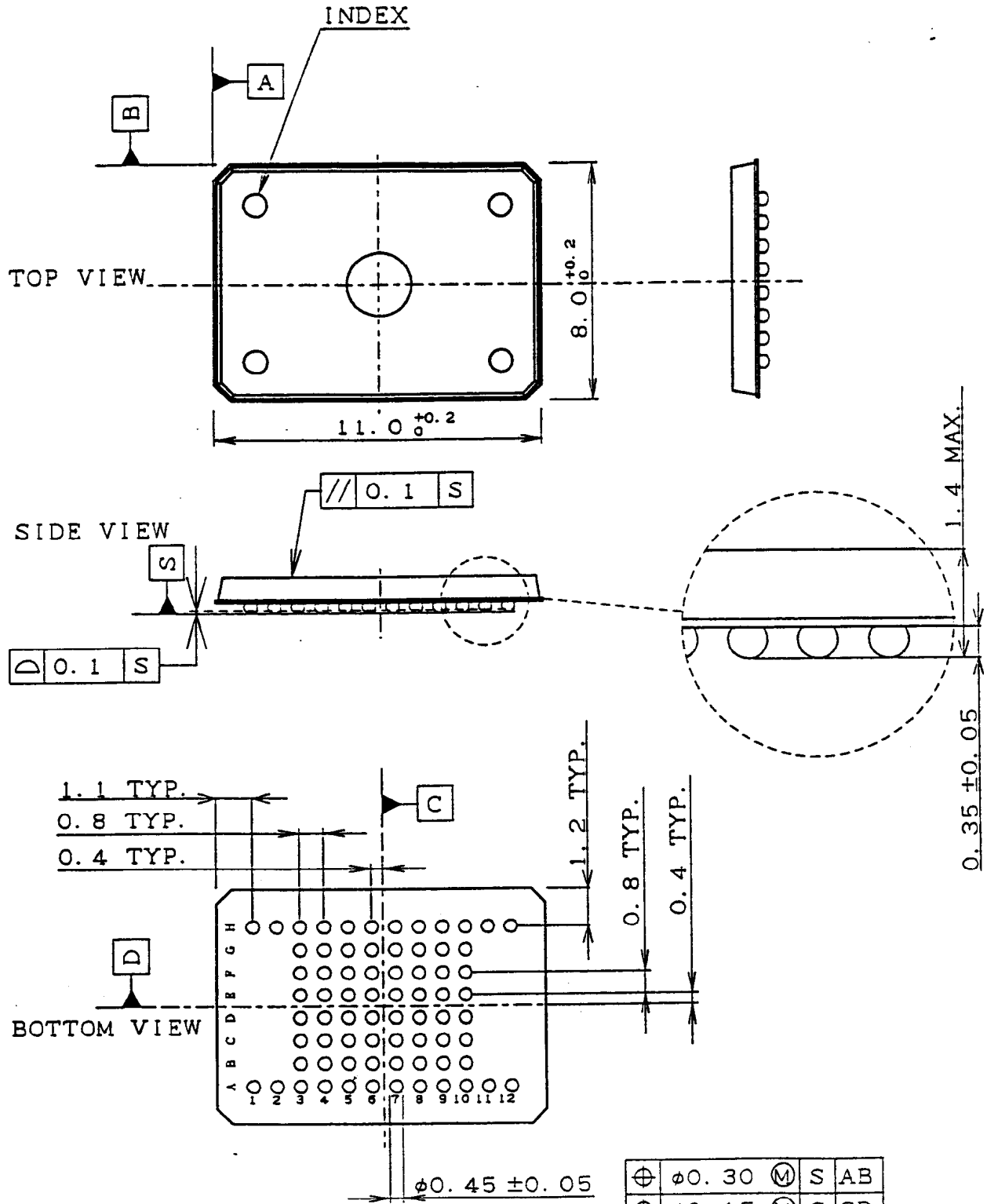
- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "111011111111110" programming.

4. Power Supply

Block erase, full chip erase, word/byte write and lock-bit configuration with an invalid V_{PP} (See 11. DC Characteristics) produce spurious results and should not be attempted. Device operations at invalid V_{CC} voltage (see 11. DC Characteristics) produce spurious results and should not be attempted.

SHARP



| | | | | | |
|-------------|-------------|----------------|-------------|--|-------------------------|
| | | 尺度 SCALE | 単位 UNIT | 適用機種 | 16M FLASH MEMORY(X1638) |
| | | 5/1 | 1=1/1mm | APPLICABLE MODEL | +2M SRAM (X8) |
| | | 端子マトリクス MATRIX | 12 X 8 | 名称 | LCSP072-P-0811 |
| | | 端子数 COUNTS | 72 | NAME | (LFBGA072-P-0811) |
| 改訂日 DATE | 改訂記事 REVISE | 担当 CHARGE | 端子ピッチ PITCH | コード | LCSP072-P-0811 |
| 1998. 2. 10 | | | 0.8 | CODE | -0811 |
| 設計 DESIGN | 製図 DRAW | 写図 TRACE | 承認 APPROVE | 図番 | |
| | | | | DRAWING No. | AA2078 |
| SOTA | SOTA | | | SHARP CORPORATION TENRI IC GROUP 超LSI開発研究所 VLSI DEVELOPMENT LABORATORIES 生産技術開発部 PRODUCTION ENGINEERING DEPT. | |