

SANYO	No. 4354	LB1890M
FDD Spindle Motor Driver		

Overview

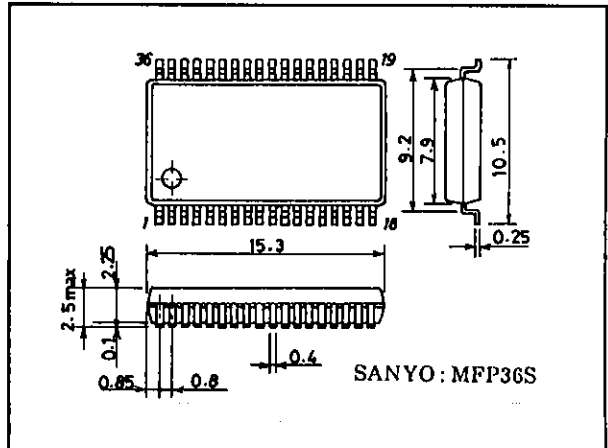
The LB1890M is a 3-phase DD motor driver IC and is an ideal FDD spindle motor driver for 3.5 inch applications.

Functions and Features

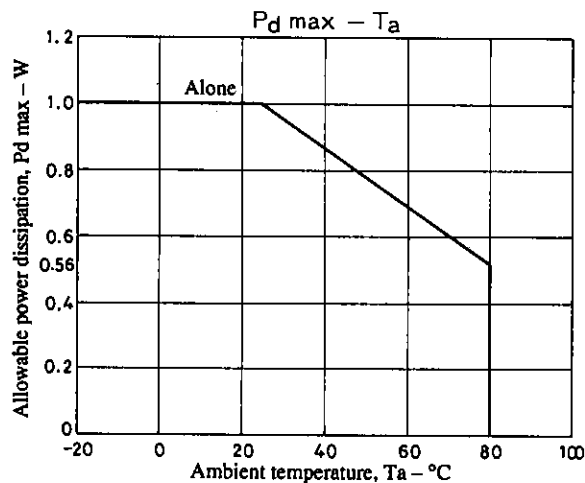
- Three phase total wave linear driver
- Eliminates need for output electrolytic capacitor (however, depending on the motor, this may not apply)
- On-chip digital speed control
- Start/stop circuit
- Current limiter circuit
- On-chip index comparator (single HYS)
- On-chip index delay circuit
- AGC circuit
- Temperature protection circuit

Package Dimensions

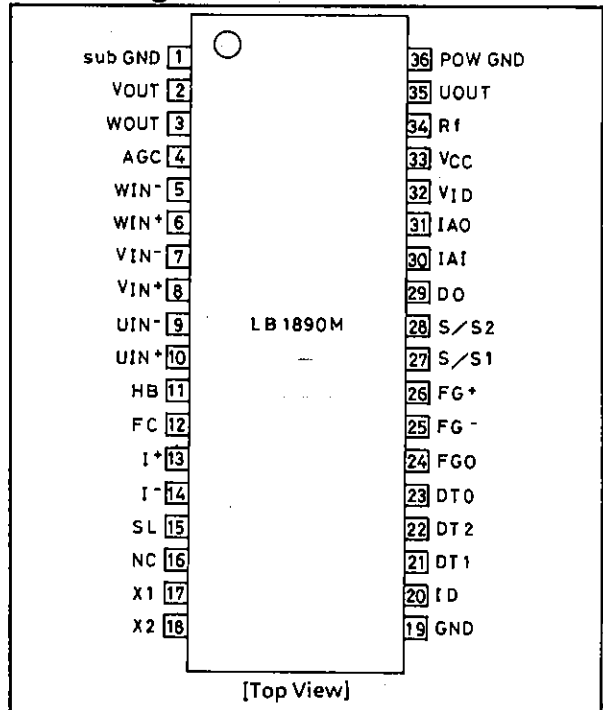
unit : mm
3129-MFP36S



Allowable power dissipation vs. ambient temperature



Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C

				unit
Maximum supply voltage	V _{CC} max		7.0	V
Maximum output current	I _O max1	t ≤ 0.5sec	1.0	A
Steady Maximum output current	I _O max2		0.7	A
Allowable power dissipation	Pd max	IC alone	1	W
Operating temperature	T _{opr}		-20 to +80	°C
Storage temperature range	T _{stg}		-40 to +150	°C

Allowable Operating Conditions at Ta = 25°C

				unit
Supply voltage	V _{CC}		4.2 to 6.5	V

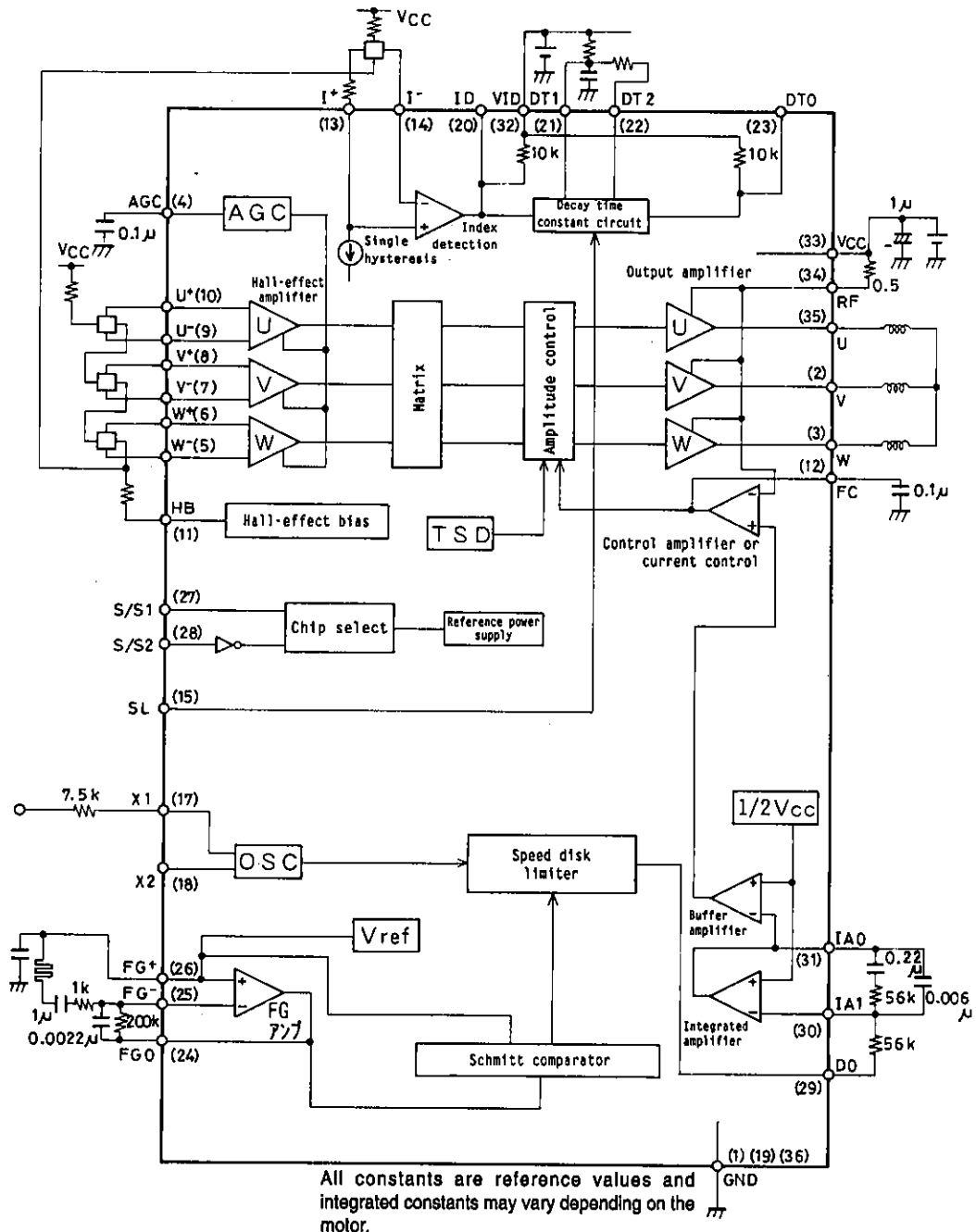
Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

			min	typ	max	unit	note
Current consumption	I _{CCO1}	V _{CC} = 5.0V (Stop)			0.2	mA	
	I _{CC1}	V _{CC} = 5.0V (Steady)		20	30	mA	
Time changeover bias current	I _{SL}				0.4	mA	
Time changeover input voltage 1	V _{SLL}		0		0.8	V	
Time changeover input voltage 2	V _{SLH}		2.0		V _{CC}	V	
S/S1 bias current	I _{S/S1}				0.4	mA	
S/S1 start voltage	V _{S/S1}		2.0		V _{CC}	V	
S/S1 stop voltage	V _{S/S1}		0		0.8	V	
S/S2 bias current	I _{S/S2}				0.1	mA	
S/S2 start voltage	V _{S/S2}		0		0.8	V	
S/S2 stop voltage	V _{S/S2}		2.0		V _{CC}	V	
Hall-effect bias amplifier input current	I _{HB}				20	μA	
In-phase input voltage range	V _h		2.2		V _{CC} - 0.7	V	
Differential input voltage range	V _{dif}		70		250	mVp-p	*2
Input offset voltage	V _{ho}				±1.0	mV	*1
Hall-Effect output voltage	V _H	I _H = 5mA		1.5	1.8	V	
Leak current	I _{HL}	Stop			±10	μA	
Output saturation voltage	V _{sat1}	I _O = 0.35A, V _{CC} = 4.2V		1.2	1.4	V	
Sink plus source	V _{sat2}	I _O = 0.70A, V _{CC} = 4.2V		1.5	2.0	V	
Output leak current	I _{OL}				±1.0	mA	
Current limiter	V _{ref1}		0.27	0.30	0.33	V	
Control amplifier voltage gain	G _C			-6		dB	
Voltage gain phase differential	ΔG _C				±1	dB	
Integrated amplifier internal reference voltage	V _{ref2}			V _{CC} /2		V	
Integrated amplifier bias current	I _{ib}				±1	μA	
Integrated output voltage amplitude	V _{i+}	I _i = -0.5 mA with reference of V _{ref2}		0.75		V	
	V _{i-}	I _i = 0.5 mA with reference of V _{ref2}		-1.4		V	
Gain band width				1000		kHz	*1
FG amplifier input voltage	V _{FG}		5		100	mVp-p	
FG amplifier voltage gain	G _{FG}	Open loop		60		dB	*1
FG amplifier input offset	V _{FG0}				±10	mV	
FG amplifier internal reference voltage	V _{FGB}		2.20	2.50	2.80	V	
Schmitt hysteresis width	ΔV _{sh1}	"H" → "L"		25		mV	*1
	ΔV _{sh2}	"L" → "H"		25		mV	*1
Schmitt input operation level	V _{sh}		1		V _{CC} - 1	V	
Speed disk recount number	N			992			
Disk recount out "L" level voltage	V _{DL}	I _D = -0.5mA			0.3	V	
Disk recount out "H" level voltage	V _{DH}	I _D = 0.5mA		V _{CC} - 0.4		V	
Disk recount out leak current	I _{DI}				±1.0	μA	
Disk recount operation frequency	F _D				1.0	MHz	*1
Oscillation range	F _{OSC}				1.0	MHz	*1
Index bias current	I _{IDB}				±10	μA	
In-phase input voltage range	V _{ID}		1.5		V _{CC} - 0.5	V	
Hysteresis setting current range	I _{IDO}		5	10	15	μA	
Index output "L" level voltage	V _{IDL}	V _{ID} = 5V			0.4	V	
Index output "H" level voltage	V _{IDH}	V _{ID} = 5V	4.5			V	
Break-down voltage	V _{DLDC}	V _{ID} = 5V		2.50		V	
Delay output "L" level voltage	V _{DLL}	V _{ID} = 5V			0.4	V	
Delay output "H" level voltage	V _{DLH}	V _{ID} = 5V	4.5			V	
Excessive heat protected operating temperature	TSD		150	180		°C	*1
Hysteresis width	ΔTSD			40		°C	*1

Note: *1) Marked values (*1) are guaranteed by the design itself and therefore do not require measurement.

*2) When hall-effect input becomes larger, kick-back occurs to the output waveform and for this reason, 200 mVp-p or less is recommended.

Block Diagram



Unit (resistance: Ω, capacitance: F)

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Pin Description

Unit (resistance: Ω)

Pin Number	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
5 6 7 8 9 10	W- W+ V- V+ U- U+	2.2V min $V_{CC} - 0.7V$ max		<ul style="list-style-type: none"> W-phase hall-effect input pin. W+ > W- is established when logic is at an "H" level. V-phase hall-effect input pin. V+ > V- is established when logic is at an "H" level. U-phase hall-effect input pin. U+ > U- is established when logic is at an "H" level.
11	HB	1.5V typ ($I_H = 5mA$)		<ul style="list-style-type: none"> Minus pin for hall-effect bias. When stopped, switches open and hall-effect bias severs.
12	FC			<ul style="list-style-type: none"> Frequency characteristics revision pin By installing a capacitor between this pin and GND, close-loop oscillation for the current control system halts.
13 14	I+ I-	1.5V min $V_{CC} - 0.5V$ max		<ul style="list-style-type: none"> Index input pin. When the I+ pin is at an "L" level, I1 operates with the fixed current of $I1 = 10 \mu A$ and when at an "H" level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I+ pin.
15	SL	"L": 0.8V max "H": 2.0V min		<ul style="list-style-type: none"> Time changeover pin. 1 : 1.2 "L" level : "H" level
17	X1			<ul style="list-style-type: none"> Reference clock generating pin.
18	X2			
19	GND			<ul style="list-style-type: none"> Ground pin. Grounded as with pins 1 and 36.

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Unit (resistance: Ω)

Pin Number	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
20	ID	"L": 0.4V max "H": 4.5V min (When V_{ID} equals 5 V)		• Index pulse output pin.
21	DT1			• Pin connecting the external CR for the delay time constant circuit.
22	DT2			• Break-down current setting pin for the delay time constant circuit.
23	DTO	"L": 0.4V max "H": 4.5V min (When V_{ID} equals 5 V)		• Index delay pulse output pin.
24	FG0			• FG amplifier output pin.
25	FG-			• FG amplifier negative input pin.
26	FG+	2.48V (When V_{ID} equals 5 V)		• FG amplifier positive input pin. Generates reference voltage within IC.
27	S/S1	"L": 0.8V max "H": 2.0V min		• Start/stop changeover pin. "H" level active.
28	S/S2	"L": 0.8V max "H": 2.0V min		• Start/stop changeover pin. "L" level active.

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Unit (resistance: Ω).

Pin Number	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
29	DO			• Speed discriminator output pin.
30	IAI			• Integrated amplifier input pin.
31	IAO			• Integrated amplifier output pin.
32	VID			• Index pulse output and index delay pulse output power supply pin. For applications when V_{CC} equals 5 V, $V_{CC} = V_{ID} = 5$ V.
33	V_{CC}			• Total power supply voltage pin except for V_{ID} . Voltage must be stable and free of ripple and noise interference.
34	R_f			• Output current detection pin. By installing an R_f resistor between this pin and V_{CC} , output current is detected as voltage. Voltage detection at this pin activates the current limiter.
35	U_{OUT}			• U-phase output pin.
36	Pow GND			• Output transistor ground pin.
1	Sub GND			• Ground pin. Grounded as with pins 19 and 36.
2	V_{OUT}			• V-phase output pin.
3	W_{OUT}			• W-phase output pin.
4	AGC			• AGC pin. Controls hall-effect amplifier gain in response to hall-effect input frequency.

Truth Table

	Source → Sink	Hall-Effect Input		
		U	V	W
1	V-phase → W-phase	H	H	L
2	V-phase → U-phase	L	H	L
3	W-phase → U-phase	L	H	H
4	W-phase → V-phase	L	L	H
5	U-phase → V-phase	H	L	H
6	U-phase → W-phase	H	L	L

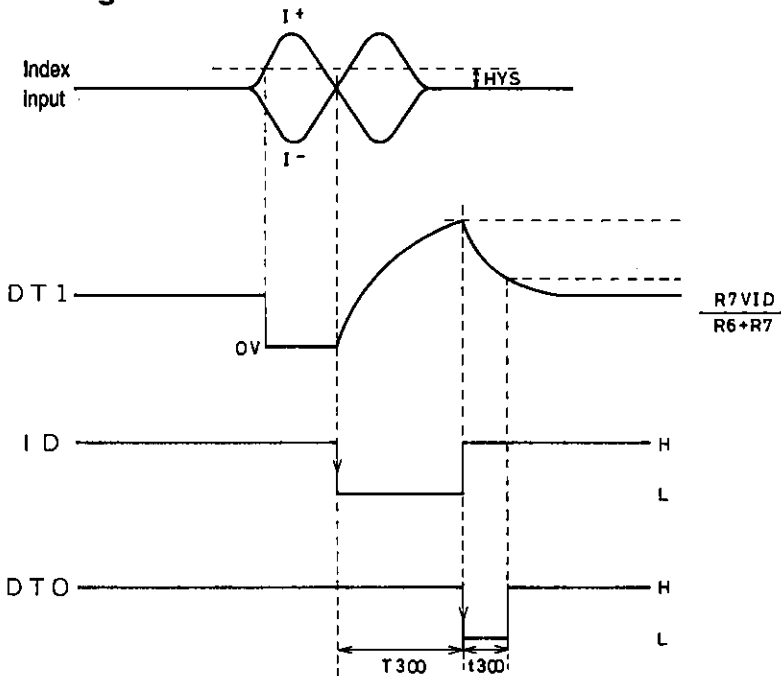
When an "H" level exists for hall-effect input,

$$U^+ > U^-$$

$$V^+ > V^-$$

$$W^+ > W^-$$

Index and Timing Chart



When SL equals an "H" level,

$$\bullet T' \approx 0.693CR6$$

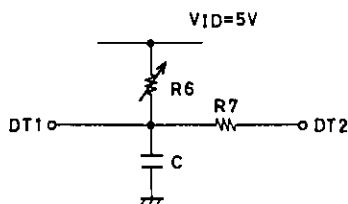
$$\bullet t' \approx \frac{CR6R7}{R6 + R7} \left\{ 0.405 + \ln \left(\frac{R6 - R7}{R6 - 2R7} \right) \right\}$$

When SL equals an "L" level,

$$\bullet T' \approx 0.577CR6$$

$$\bullet t' \approx \frac{CR6R7}{R6 + R7} \left\{ 0.522 + \ln \left(\frac{0.781R6 - R7}{R6 - 2R7} \right) \right\}$$

Using only the ID pulse involves shorting DT1 and DT2.



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