Ordering number : ENN6498

CMOS IC

LC651432N/F/L, 651431N/F/L

Four-Bit CMOS Microcontrollers for Small-Scale Control Applications

Overview

The LC651431N/F/L and LC651432N/F/L are the small-scale control models in Sanyo's LC6500 Series of 4-bit microcontrollers and feature the same basic architecture and instruction set. These microcontrollers are appropriate for a wide range of applications, from applications that require only a limited number of circuits and controls and were previously implemented in standard logic to larger application such as audio equipment, including tape decks and disc players, office equipment, communication equipment, automotive equipment, and home appliances. Furthermore, since these products have equivalent basic functions (although there are differences in some functions and characteristics) and are pin compatible with the earlier LC6543N/F/L and LC6546N/F/L products, they can be used to replace those devices.

Features

- Fabricated in a CMOS process for low power operation (Standby mode can be controlled by CPU instructions.)
- ROM/RAM
  LC651432N/F/L
  —ROM: 2 K × 8 bits, RAM: 128 × 4 bits
  LC651431N/F/L
  —ROM: 1 K × 8 bits, RAM: 64 × 4 bits
- Instruction set: The 80-instruction set common to the whole LC6500 Series
- Wide operating supply voltage range of 2.2 to 6.0 V (L versions)
- Instruction cycle time of 0.92 µs (F versions)
- On-chip serial I/O function
- Highly flexible I/O ports
  Number of ports
  — 7 ports (Up to 25 pins)
  All ports
  — Can be used for either input or output
  — Voltage handling capability (input and output): 15 V maximum (For open-drain specification ports)
  — Output current: 20 mA maximum sink current (Capable of directly driving an LED.)
  I/O port options to match application requirements:
  — Open-drain output and pull-up resistor specification: Can be specified for all ports in bit units.
  — Output level at reset specification: Either a high or low level can be specified for ports C and D in 4-bit units each.
- Interrupts
  Timer overflow vector interrupt (can also be tested by CPU instructions)
  $\overline{\text{INT}}$ pin or serial I/O full/empty vector interrupt (can also be tested by CPU instructions)
- Stack levels: 4 levels (also used by interrupts)
- Timers: 8-bit programmable timer with 4-bit prescaler
- Clock oscillator options to match application requirements:
  Oscillator circuit option:
  — Two-pin RC oscillator (N and L versions)
    Two-pin ceramic oscillator or single external clock input pin (N, F, and L versions)
  — Divider circuit option: No divider, built-in divide-by-three circuit, built-in divide-by-four circuit (N and L versions)
- Continuous square-wave output with a period 64 times the cycle time.

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co.,Ltd. Semiconductor Company
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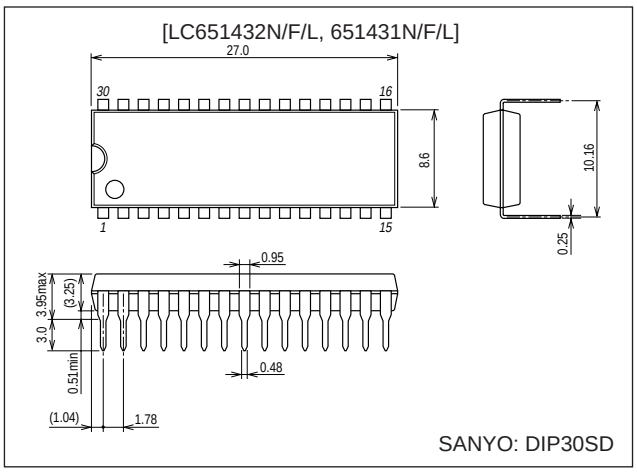
Package Dimensions

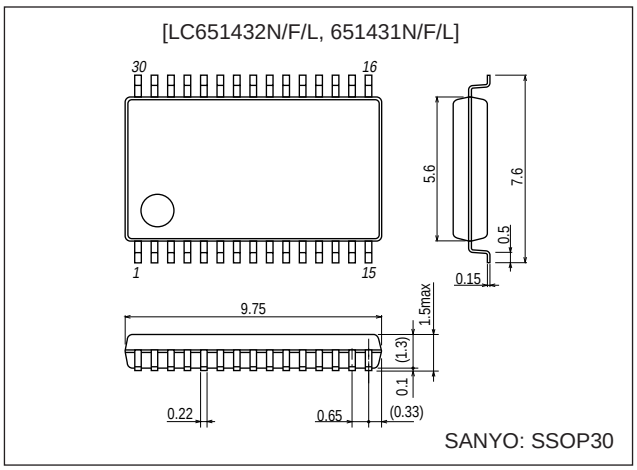
unit : mm

3196A-DIP30SD



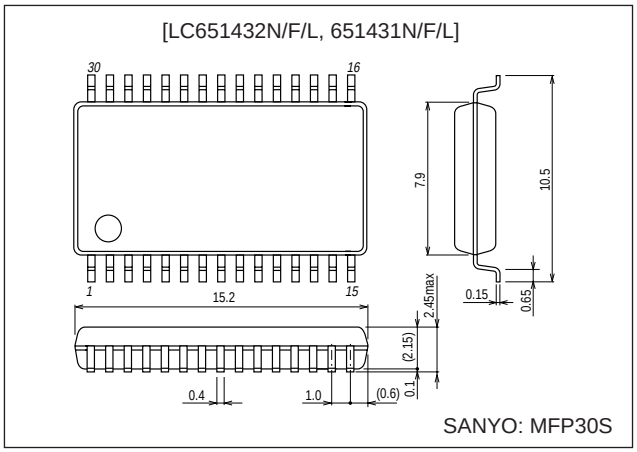
unit : mm

3191A-SSOP30



unit : mm

3216B-MFP30S



Function Overview

Parameter		LC651432N/1431N	LC651432F/1431F	LC651432L/1431L
Memory	ROM	2048 × 8 bits (1432N/F/L) 1024 × 8 bits (1431N/F/L)		
	RAM	128 × 4 bits (1432N/F/L) 64 × 4 bits (1431N/F/L)		
Instructions	Instruction set	80		
	Table reference	Provided		
On-chip functions	Interrupts	One external, one internal		
	Timers	8-bit timer with 4-bit prescaler		
	Stack levels	4		
	Standby function	HALT instruction based standby function Provided		
I/O ports	Number of ports	Up to 25 I/O pins		
	Serial ports	I/O in 4-bit or 8-bit units		
	I/O voltage	15 V max.		
	Output current	10 mA typ. 20 mA max.		
	I/O circuit types	Open drain (n channel) or built-in pull-up resistor output can be specified in 1-bit units.		
	Output level at reset	High or low can be specified in port units (C and D ports only)		
	Square-wave output	Possible		
Characteristics	Minimum cycle time	2.77 µs (V_{DD} ≥ 3 V)	0.92 µs (V_{DD} ≥ 3 V)	3.84 µs (V_{DD} ≥ 2.2 V)
	Supply voltage	3 to 6 V	3 to 6 V	2.2 to 6 V
	Supply current	1 mA typ.	1.5 mA typ.	1 mA typ.
Oscillator	Oscillator element	RC oscillator (400 or 800 kHz typical) Ceramic oscillator (400 kHz, 800 kHz, 1 MHz, or 4 MHz)	Ceramic oscillator: 4 MHz	RC oscillator (400 kHz typical) Ceramic oscillator (400 kHz or 4 MHz)
	Divider circuit option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4
Other features	Package	DIP30S-D, MFP30S, SSOP30		

Note: Sanyo will be providing details on oscillator elements and oscillator circuit constants as recommended circuits are developed. Contact your Sanyo representative for more information.

Differences between the LC651432N/LC651431N and the LC6543N/LC6546N

This table lists the points that require care when replacing the LC6543N/LC6546N with the LC651432N/LC651431N in completes end products.

Parameter		LC651432N/1431N	LC6543N/46N
Allowable power dissipation	Pdmax(1) : DIP	310 mW	250 mW
	Pdmax(2) : MFP	220 mW	150 mW
	Pdmax(3) : SSOP	160 mW	(This package not available.)
I/O voltage (PIO)	V_{IO}(3) added	–0.3 to V_{DD} + 0.3	–0.3 to +15 V (When open-drain output is used.) –0.3 to V_{DD} + 0.3 (When a pull-up resistor is used.)
High-level input voltage	V_{IH}(n)	V_{IH}(1) to V_{IH}(7) (Associated with the I/O voltage (PI0) changes mentioned above.)	V_{IH}(1) to V_{IH}(6)
High-level input current	I_{IH}(n)	I_{IH}(1) to I_{IH}(3) (Associated with the I/O voltage (PI0) changes mentioned above.)	I_{IH}(1) to I_{IH}(2)
Oscillator characteristics Ceramic oscillator Oscillator frequency 2-pin RC oscillator Oscillator frequency	f_{CFOSC} [OSC1, OSC2]	Oscillator frequency precision: ±2% Recommended oscillator circuit constants (under evaluation)	Oscillator frequency precision: ±4%
	f_{MOSC} [OSC1, OSC2]	800 kHz typical (V_{DD} = 3 to 6 V) Circuit constant changes: Rext = 6.8 kΩ ±1% Sample-to-sample frequency variation: 595 to 1274 kHz	850 kHz typical (V_{DD} = 4 to 6 V) Circuit constant changes: Rext = 4.7 kΩ ±1% Sample-to-sample frequency variation: 619 to 1144 kHz
		400 kHz typical (V_{DD} = 3 to 6 V) Sample-to-sample frequency variation: 284 to 790 kHz	400 kHz typical (V_{DD} = 3 to 6 V) Sample-to-sample frequency variation: 305 to 546 kHz
Current drain	I_{DD}	1 mA typ.	2 mA typ.
Serial clock input clock cycle time	t_{CKCY}(1)[$\overline{SCK}$]	min. 2.0 µs	min 3.0 µs
Package		DIP30S-D, MFP30S, SSOP30 added	DIP30S-D, MFP30S

Differences between the LC651432F/LC651431F and the LC6543F/LC6546F

This table lists the points that require care when replacing the LC6543F/LC6546F with the LC651432F/LC651431F in completes end products.

Parameter		LC651432F/1431F	LC6543F/46F
Allowable power dissipation	Pdmax(1) : DIP	310 mW	250 mW
	Pdmax(2) : MFP	220 mW	150 mW
	Pdmax(3) : SSOP	160 mW	(This package not available.)
Operating supply voltage	V_{DD}	3 to 6 V	4.5 to 6 V
I/O voltage (PI0)	V_{IO}(3) added	–0.3 to V_{DD} + 0.3	–0.3 to +15 V (When open-drain output is used.) –0.3 to V_{DD} + 0.3 (When a pull-up resistor is used.)
High-level input voltage	V_{IH}(n)	V_{IH}(1) to V_{IH}(7) (Associated with the I/O voltage (PI0) changes mentioned above.)	V_{IH}(1) to V_{IH}(6)
High-level input current	I_{IH}(n)	I_{IH}(1) to I_{IH}(3) (Associated with the I/O voltage (PI0) changes mentioned above.)	I_{IH}(1) to I_{IH}(2)
Low-level input voltage	V_{IL}(n)	I_{IH}(1) to I_{IH}(3) Specifications when V_{DD} = 4 to 6 V Specifications added for V_{DD} = 3 to 6 V	Specifications when V_{DD} = 4 to 6 V
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC} [OSC1, OSC2]	Oscillator frequency precision: ±2%	Oscillator frequency precision: ±4%
Current drain	I_{DD}	1.5 mA typ.	2.5 mA typ.
Serial clock input clock cycle time	t_{CKCY}(1)[$\overline{SCK}$]	min. 2.0 µs	min 3.0 µs
Package		DIP30S-D, MFP30S, SSOP30 added	DIP30S-D, MFP30S

Differences between the LC651432L/LC651431L and the LC6543L/LC6546L

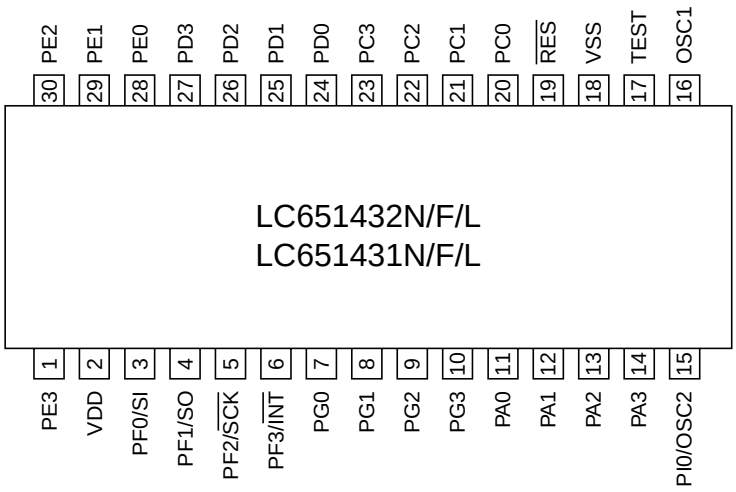
This table lists the points that require care when replacing the LC6543L/LC6546L with the LC651432L/LC651431L in completes end products.

Parameter		LC651432L/1431L	LC6543L/46L
Allowable power dissipation	Pdmax(1) : DIP	310 mW	250 mW
	Pdmax(2) : MFP	220 mW	150 mW
	Pdmax(3) : SSOP	160 mW	(This package not available.)
I/O voltage (PI0)	V_{IO}(3) added	–0.3 to V_{DD} + 0.3	–0.3 to +15 V (When open-drain output is used.) –0.3 to V_{DD} + 0.3 (When a pull-up resistor is used.)
High-level input voltage	V_{IH}(n)	V_{IH}(1) to V_{IH}(7) (Associated with the I/O voltage (PI0) changes mentioned above.)	V_{IH}(1) to V_{IH}(6)
High-level input current	I_{IH}(n)	I_{IH}(1) to I_{IH}(3) (Associated with the I/O voltage (PI0) changes mentioned above.)	I_{IH}(1) to I_{IH}(2)
Oscillator characteristics Ceramic oscillator Oscillator frequency 2-pin RC oscillator Oscillator frequency	f_{CFOSC} [OSC1, OSC2]	Oscillator frequency precision: ±2% Recommended oscillator circuit constants (under evaluation)	Oscillator frequency precision: ±4%
	f_{MOSC} [OSC1, OSC2]	400 kHz typical (V_{DD} = 2.2 to 6 V) Circuit constant changes: Rext = 15 kΩ ±1% Sample-to-sample frequency variation: 200 to 790 kHz	400 kHz typical (V_{DD} = 2.2 to 6 V) Circuit constant changes: Rext = 12 kΩ ±1% Sample-to-sample frequency variation: 284 to 546 kHz
Current drain	I_{DD}	1 mA typ.	2 mA typ.
Package		DIP30S-D, MFP30S, SSOP30 added	DIP30S-D, MFP30S

Caution: Always test the end product thoroughly after changing the microcontroller used.

Pin Assignment

The same pin assignment is used for the DIP, MFP, and SSOP packages.



Pin Nomenclature

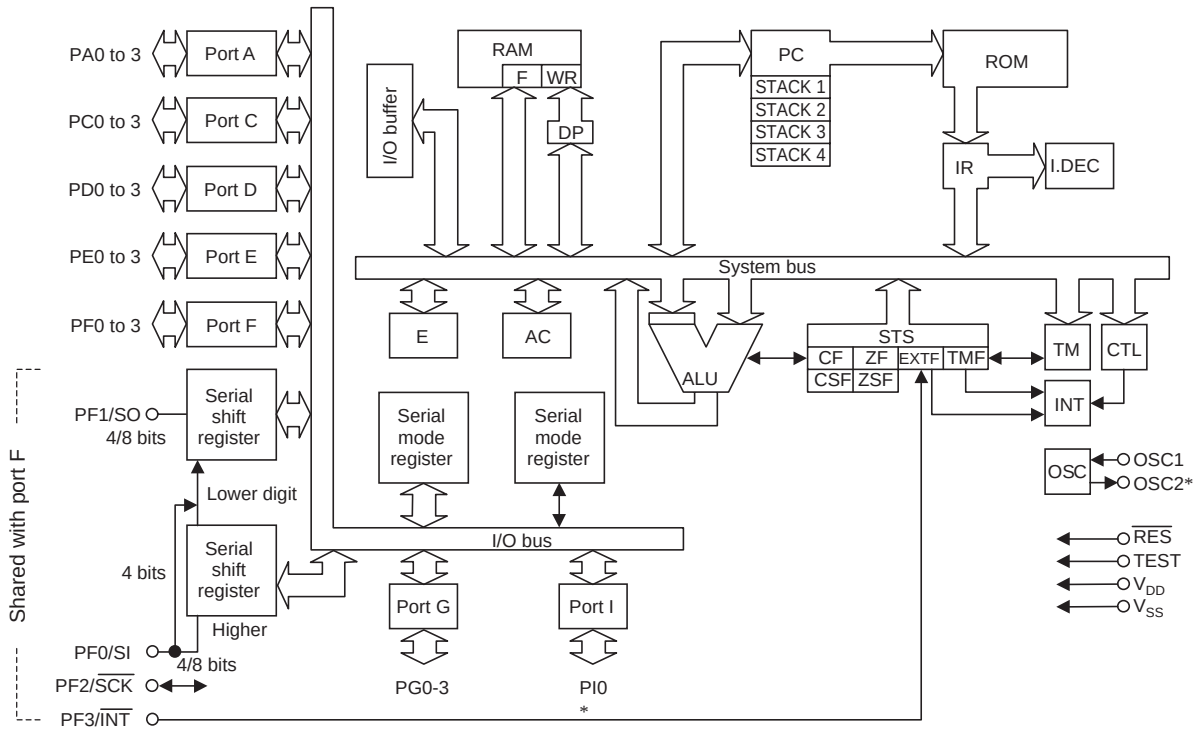
OSC1, OSC2: Connections for capacitor and resistor oscillator components or a ceramic oscillator element.

PG0 to 3:	Shared-function I/O port G0 to 3	PI0:	Shared-function I/O port IO
$\overline{\text{RES}}$:	Reset	TEST:	Test
PA0 to 3:	Shared-function I/O port A0 to 3	$\overline{\text{INT}}$:	Interrupt request
PC0 to 3:	Shared-function I/O port C0 to 3	SI:	Serial input
PD0 to 3:	Shared-function I/O port D0 to 3	SO:	Serial output
PE0 to 3:	Shared-function I/O port E0 to 3	$\overline{\text{SCK}}$:	Serial clock input or output pin
PF0 to 3:	Shared-function I/O port F0 to 3		

Notes: 1. The SI, SO, $\overline{\text{SCK}}$, and $\overline{\text{INT}}$ pins are shared-function pins also used as PF0 to 3.
2. OSC2 and PIO are a single pin set exclusively to one or the other function as a user option.

System Block Diagram

LC651432N/F/L, LC651431N/F/L



Note: * OSC2 and PIO are a single pin set exclusively to one or the other function as a user option.

RAM:	Data memory	ROM:	Program memory
F:	Flags	PC:	Program counter
WR:	Working register	INT:	Interrupt control
AC:	Accumulator	IR:	Instruction register
ALU:	Arithmetic and logic unit	I.DEC:	Instruction decoder
DP:	Data pointer	CF, CSF:	Carry flag, carry save flag
E:	E register	ZF, ZSF:	Zero flag, zero save flag
CTL:	Control register	EXTF:	External interrupt request flag
OSC:	Oscillator circuit	TMF:	Internal interrupt request flag
TM:	Timer		
STS:	Status register		

Development Support

The following are available to support the development of LC651431 and LC651432 applications.

- User's manual
  "LC6543/46 User's Manual" No. E71
- Development tool manual
  See the "EVA86000 Development Tool Manual for 4-Bit Microcontrollers."
- Software manual
  "LC65/66 Series Software Manual"
- Development tools
  Program development: EVA86000 System
  Program evaluation: LC65E43 on-chip EPROM microcontroller

Pins Functions

Count	Pin	I/O	Function	Options	Reset state	Handling when unused
1 1	V_{DD} V_{SS}	— —	Power supply	—	—	—
1	OSC1	Input	• Connection for the external system clock RC or ceramic oscillator element • When a single pin is used for external clock input, the PI0/OSC2 pin is used as the PI0 I/O port. • When a 2-pin RC oscillator or a 2-pin ceramic oscillator is used, the PI0/OSC2 pin is used as the OSC2 oscillator pin.	1. Single-pin external clock input 2. 2-pin RC oscillator 3. 2-pin ceramic oscillator 4. Divider circuit option • No divider • Divide-by-three circuit • Divide-by-four circuit	—	—
4	PA0 to PA3	I/O	• I/O port A0 to 3 Input in 4-bit units (IP instruction) Output in 4-bit units (OP instruction) Test in single-bit units (BP and BNP instructions) Set/reset in single-bit units (SPB and RPB instructions) • PA3 (Any one of PA0 to 3 can be selected) is used for standby mode control. • Applications must assure that key bounce or similar noise does not occur on PA3 (or PA0 to 3) during a HALT instruction execution cycle.	1. Open-drain output 2. Built-in pull-up resistor Options 1 and 2 may be specified in bit units.	• High-level output (with the output n-channel transistor off)	The open-drain output option must be selected and the pin connected to V_{SS}.
4	PC0 to PC3	I/O	• I/O port C0 to 3 Provides the same functions as PA0 to 3. (See note.) • The output level at reset can be specified to be either high or low. Note: This port does not have the standby mode control function.	1. Open-drain output 2. Built-in pull-up resistor 3. High-level output at reset 4. Low-level output at reset • Options 1 and 2 may be specified in bit units. • Options 3 and 4 are specified in a single 4-bit group	• High-level output • Low-level output (Specified as a user option.)	The same as that for PC0 to 3
4	PD0 to PD3	I/O	• I/O port D0 to 3 Provides the same functions as PC0 to 3.	The same as those for PC0 to 3.	The same as those for PC0 to 3.	The same as those for PC0 to 3.

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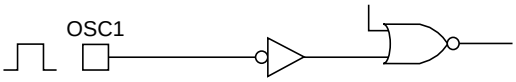
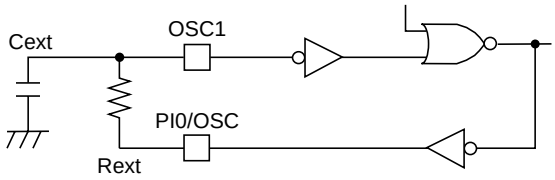
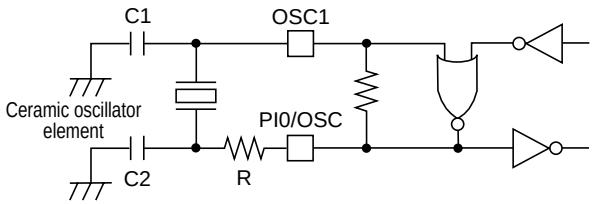
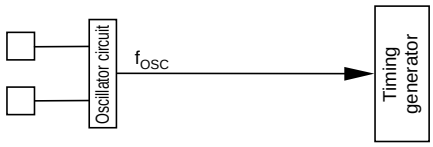
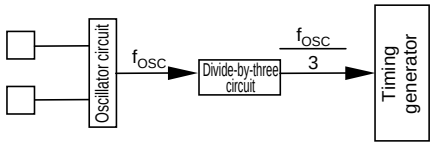
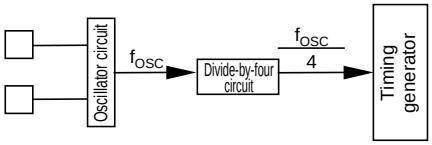
Count	Pin	I/O	Function	Options	Reset state	Handling when unused
4	PE0 to PE3	I/O	• I/O port E0 to 3 Input in 4-bit units (IP instruction) Output in 4-bit units (OP instruction) Set/reset in single-bit units (SPB and RPB instructions) Test in single-bit units (BP and BNP instructions) • PE0 also has a continuous pulse (64Tcyc) output function.	1. Open-drain output 2. Built-in pull-up resistor Options 1 and 2 may be specified in bit units.	• High-level output (with the output n-channel transistor off)	The same as that for PA0 to 3.
4	PF0/SI PF1/$\overline{\text{SO}}$ PF2/$\overline{\text{SCK}}$ PF3/$\overline{\text{INT}}$	I/O	• I/O port F0 to 3 Functions and options identical to PE0 to 3. (See note.) • PF0 to 3 have shared functions as the serial interface pins and the $\overline{\text{INT}}$ input. Either function can be selected under program control. SI ... Serial input port $\overline{\text{SO}}$ ... Serial output port $\overline{\text{SCK}}$ ... Serial clock input or output $\overline{\text{INT}}$ ... Interrupt request input Serial input/output is switched between 4-bit and 8-bit units under program control. Note: This port does not have a continuous pulse output function.	The same as those for PE0 to 3.	The same as that for PE0 to 3. The serial port is disabled and $\overline{\text{INT}}$ is the interrupt source.	The same as that for PA0 to 3.
4	PG0 to PG3	I/O	• I/O port G0 to 3 Functions and options identical to PE0 to 3. (See note.) Note: This port does not have a continuous pulse output function.	The same as those for PE0 to 3.	The same as those for PE0 to 3.	The same as that for PA0 to 3.
1	PI0/OSC2	I/O Output	• I/O port IO Functions and options identical to PG0 to 3. • However, consists of a single bit. • When a 2-pins oscillator is used, this pin functions as the OSC2 pin, and the I/O port function is not available.	The same as those for PG0 to 3.	The same as those for PG0 to 3.	The same as that for PA0 to 3.
1	$\overline{\text{RES}}$	Input	• System reset input • Connect an external capacitor to implement a power-on reset. • The reset start operation requires that a low level be held for at least 4 clock cycles.	—	—	—
1	TEST	Input	• IC test pin This pin must be connected to V_{SS} during normal operation.	—	—	This pin must be connected to V_{SS}.

Oscillator Circuit Options

Option	Circuit	Conditions and notes
External clock		The PI0/OSC2 pin is used as the PI0 pin.
Two-pin RC oscillator		The PI0/OSC2 pin is used as the OSC2 pin and the port function is unavailable.
Ceramic oscillator		The PI0/OSC2 pin is used as the OSC2 pin and the port function is unavailable.

Divider Circuit Options

Option	Circuit	Conditions and notes
No divider circuit (1/1)		• Applicable to all three oscillator options. • The oscillator frequency or the external clock must not exceed 1444 kHz. (LC651431N and LC651432N) • The oscillator frequency or the external clock must not exceed 4330 kHz. (LC651431F and LC651432F) • The oscillator frequency or the external clock must not exceed 1040 kHz. (LC651431L and LC651432L)
Divide-by-three circuit (1/3)		• Only applicable to the external clock and the ceramic oscillator option. • The oscillator frequency or the external clock must not exceed 4330 kHz.
Divide-by-four circuit (1/4)		• Only applicable to the external clock and the ceramic oscillator option. • The oscillator frequency or the external clock must not exceed 4330 kHz.

Caution: The following table summarizes the oscillator and divider option combinations. Use care when selecting these options.

Oscillator Divider Options for the LC651431N/LC651432N, LC651431F/LC651432F, and LC651431L/LC651432L

LC651432N, LC651431N

Oscillator type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	400 kHz	1/1 (10 µs)	3 to 6 V	The divide-by-three and divide-by-four circuits cannot be used.
	800 kHz	1/1 (5 µs)	3 to 6 V	
		1/3 (15 µs)	3 to 6 V	
		1/4 (20 µs)	3 to 6 V	
	1 MHz	1/1 (4 µs)	3 to 6 V	
		1/3 (12 µs)	3 to 6 V	
		1/4 (16 µs)	3 to 6 V	
	4 MHz	1/3 (3 µs)	3 to 6 V	The no-divider (1/1) option cannot be used.
		1/4 (4 µs)	3 to 6 V	
Single-pin external clock input	200 to 1444 kHz	1/1 (20 to 2.77 µs)	3 to 6 V	
	600 to 4330 kHz	1/3 (20 to 2.77 µs)	3 to 6 V	
	800 to 4330 kHz	1/4 (20 to 3.70 µs)	3 to 6 V	
External clock provided by a 2-pin RC oscillator circuit	As above			
2-pin RC oscillator	Using the no-divider (1/1) option and the recommended circuit constants. If the use of circuit values other than the recommended values is unavoidable, the frequencies, divider options, and V_{DD} ranges specified for the single-pin external clock input option must be strictly observed.		3 to 6 V	
External clock used with the ceramic oscillator option	The IC cannot be driven by an external clock with this option. If external clock drive is required, select either the external clock option or the 2-pin RC oscillator option			

LC651432F, LC651431F

Oscillator type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	4 MHz	1/1 (1 µs)	3 to 6 V	
Single-pin external clock input	200 to 4330 kHz	1/1 (20 to 0.92 µs)	3 to 6 V	
External clock used with the ceramic oscillator circuit	The IC cannot be driven by an external clock with this option. If external clock drive is required, select the external clock option.			

LC651432L, LC651431L

Oscillator type	Frequency	Divider option (cycle time)	V_{DD} range	Notes
Ceramic oscillator	400 kHz	1/1 (10 µs)	2.2 to 6 V	The divide-by-three and divide-by-four circuits cannot be used.
	4 MHz	1/4 (4 µs)	2.2 to 6 V	The no-divider (1/1) and divide-by-three option cannot be used.
Single-pin external clock input	200 to 1040 kHz	1/1 (20 to 3.84 µs)	2.2 to 6 V	
	600 to 3120 kHz	1/3 (20 to 3.84 µs)	2.2 to 6 V	
	800 to 4160 kHz	1/4 (20 to 3.84 µs)	2.2 to 6 V	
External clock provided by a 2-pin RC oscillator circuit	As above			
2-pin RC oscillator	Using the no-divider (1/1) option and the recommended circuit constants. If the use of circuit values other than the recommended values is unavoidable, the frequencies, divider options, and V_{DD} ranges specified for the single-pin external clock input option must be strictly observed.		2.2 to 6 V	
External clock used with the ceramic oscillator option	The IC cannot be driven by an external clock with this option. If external clock drive is required, select either the external clock option or the 2-pin RC oscillator option			

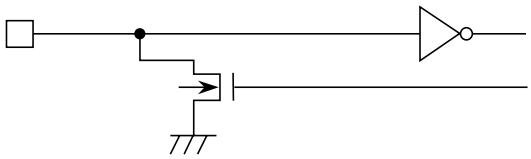
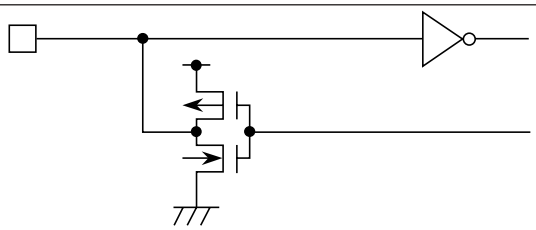
Port C and D Output Level at Reset Option

One of the following two options for the output level at reset may be chosen for the I/O ports C and D in 4-bit group units.

Option	Conditions and notes
High-level output at reset	Ports C and D in 4-bit units
Low-level output at reset	Ports C and D in 4-bit units

Port Output Circuit Type Option

One of the following two options for the circuit type can be selected for the I/O ports in bit units.

Option	Circuit	Applicable ports
Open-drain output		• Not applicable to the PI0/OSC2 pin if either the 2-pin RC oscillator or the ceramic oscillator is selected as the oscillator circuit.
Built-in pull-up resistor output		

Specifications

LC651432N, 651431N

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Voltages up to the voltage generated are allowed.	V
Input voltage	V_I(1)		OSC1 *1	–0.3 to V_{DD} +0.3	V
	V_I(2)		TEST, $\overline{RES}$	–0.3 to V_{DD} +0.3	V
I/O voltage	V_{IO}(1)		Ports with open-drain specifications	–0.3 to +15	V
	V_{IO}(2)		Ports with pull-up resistor specifications	–0.3 to V_{DD} +0.3	V
	V_{IO}(3)		PI0	–0.3 to V_{DD} +0.3	V
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Per single pin, the average over a 100 ms period	I/O ports	–2 to +20	mA
	ΣI_{OA}(1)	The total current for PC0 to 3, PD0 to 3, and PE0 to 3*2	PC0 to 3 PD0 to 3 PE0 to 3	–15 to +100	mA
	ΣI_{OA}(2)	The total current for PF0 to 3, PG0 to 3, PA0 to 3, and PI0*2	PF0 to 3, PI0 PG0 to 3 PA0 to 3	–15 to +100	mA
Allowable power dissipation	Pd max(1)	Ta = –40 to +85°C (DIP package)		310	mW
	Pd max(2)	Ta = –40 to +85°C (MFP package)		220	mW
	Pd max(3)	Ta = –40 to +85°C (SSOP package)		160	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to 125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	3.0		6.0	V
Standby supply voltage	V_{ST}	RAM and register contents retained. *3	V_{DD}	1.8		6.0	V
High-level input voltage	V_{IH}(1)	With the n-channel output transistors off	Ports with open-drain specifications (except for I0)	0.7 V_{DD}		13.5	V
	V_{IH}(2)	With the n-channel output transistors off	Ports with pull-up resistor specifications (except for I0)	0.7 V_{DD}		V_{DD}	V
	V_{IH}(3)	With the n-channel output transistors off	Port I0	0.7 V_{DD}		V_{DD}	V
	V_{IH}(4)	With the n-channel output transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with open-drain specifications	0.8 V_{DD}		13.5	V
	V_{IH}(5)	With the n-channel output transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with pull-up resistor specifications	0.8 V_{DD}		V_{DD}	V
	V_{IH}(6)	V_{DD} = 1.8 to 6 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	V
	V_{IH}(7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	V

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Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Low-level input voltage	$V_{IL}(1)$	With the n-channel output transistors off V_{DD} = 4 to 6 V	Port	V_{SS}		0.3 V_{DD}	V
	$V_{IL}(2)$	With the n-channel output transistors off 3 to 6 V	Port	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(3)$	With the n-channel output transistors off V_{DD} = 4 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(4)$	With the n-channel output transistors off 3 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.2 V_{DD}	V
	$V_{IL}(5)$	External clock specifications V_{DD} = 4 to 6 V	OSC1	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(6)$	External clock specifications 3 to 6 V	OSC1	V_{SS}		0.2 V_{DD}	V
	$V_{IL}(7)$	V_{DD} = 4 to 6 V	TEST	V_{SS}		0.3 V_{DD}	V
	$V_{IL}(8)$	3 to 6 V	TEST	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(9)$	V_{DD} = 4 to 6 V	$\overline{RES}$	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(10)$	3 to 6 V	$\overline{RES}$	V_{SS}		0.2 V_{DD}	V
Operating frequency (cycle time)	fop (Tcyc)	A clock frequency of up to 4.33 MHz may be used when either the divide-by-three circuit or the divide-by-four circuit is used.		200 (20)		1444 (2.77)	kHz (µs)
External clock conditions		See figure 1.					
Frequency	text	The divide-by-three circuit or the divide-by-four circuit must be used if the clock frequency exceeds 1.444 MHz.	OSC1	200		4330	kHz
Pulse width	textH, textL		OSC1	69			ns
Rise and fall time	textR, textF		OSC1			50	ns
Recommended oscillator circuit constants							
Two-pin RC oscillator	Cext Rext	See figure 2.	OSC1, OSC2		220 ± 5% 12 ±1%		pF kΩ
	Cext Rext	See figure 2.	OSC1, OSC2		220 ±5% 6.8 ±1%		pF kΩ
Ceramic oscillator*4		See figure 3.			See table 1.		

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
High-level input current	I_{IH}(1)	• With the output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = 13.5 V	Open-drain specification ports (except I0)			5.0	µA
	I_{IH}(2)	• With the output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = V_{DD}	The I0 port with open-drain specifications			1.0	µA
	I_{IH}(3)	• External clock mode • V_{IN} = V_{DD}	OSC1			1.0	µA
Low-level input current	I_{IL}(1)	• With the output n-channel transistors off • V_{IN} = V_{SS}	Open-drain specification ports	–1.0			µA
	I_{IL}(2)	• With the output n-channel transistors off • V_{IN} = V_{SS}	Built-in pull-up resistor specification ports	–1.3	–0.35		mA
	I_{IL}(3)	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
	I_{IL}(4)	• External clock mode • V_{IN} = V_{SS}	OSC1	–1.0			µA
High-level output voltage	V_{OH}(1)	• I_{OH} = –50 µA • V_{DD} =4.0 to 6.0 V	Built-in pull-up resistor specification ports	V_{DD} – 1.2			V
	V_{OH}(2)	• I_{OH} = –10 µA	Built-in pull-up resistor specification ports	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}(1)	• I_{OL} = 10 mA • V_{DD} = 4.0 to 6.0 V	Ports			1.5	V
	V_{OL}(2)	I_{OL} = 1 mA, when I_{OL} for all ports is less than or equal to 1 mA.	Ports			0.5	V
Schmitt characteristics: Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, and OSC1 with Schmitt trigger specifications*5		0.1 V_{DD}		V
Schmitt characteristics: High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	V
Schmitt characteristics: Low-level threshold voltage	V_{tL}			0.2 V_{DD}		0.6 V_{DD}	V
Current drain*6 Two-pin RC oscillator	I_{DDOP}(1)	• While operating, with the output n-channel transistors off • Port voltage = V_{DD} • Figure 2, fosc = 800 kHz (typical)	V_{DD}		1	3	mA
Ceramic oscillator	I_{DDOP}(2)	See figure 2. fosc = 400 kHz (typical)	V_{DD}		0.8	2.5	mA
External clock	I_{DDOP}(3)	• Figure 3, 4 MHz, divide-by-three circuit used.	V_{DD}		1	3	mA
	I_{DDOP}(4)	• Figure 3, 4 MHz, divide-by-four circuit used.	V_{DD}		1	3	mA
Standby mode	I_{DDOP}(5)	See figure 3. 400 kHz	V_{DD}		1	2.5	mA
	I_{DDOP}(6)	See figure 3. 800 kHz	V_{DD}		1	3	mA
	I_{DDOP}(7)	• 200 to 1444 kHz, no divider • 600 to 4330 kHz, divide-by-three circuit used • 800 to 4330 kHz, divide-by-four circuit used	V_{DD}		1	4	mA
	I_{DDst}	Output n-channel transistors off, V_{DD} = 6 V Port voltage = V_{DD}, V_{DD} = 3 V	V_{DD} V_{DD}		0.05 0.025	10 5	µA µA

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Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Oscillator characteristics							
Ceramic oscillator Oscillator frequency	f_{CFOSC}*7	• Figure 3, fo = 400 kHz • Figure 3, fo = 800 kHz • Figure 3, fo = 1 MHz • Figure 3, fo = 4 MHz, divide-by-three or divide-by-four circuit used.	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	392 784 980 3920	400 800 1000 4000	408 816 1020 4080	kHz kHz kHz kHz
Oscillator stabilization time*8	t_{CFS}	• Figure 4, fo = 400 kHz • Figure 4, fo = 800 kHz, 1 MHz, or 4 MHz, divide-by-three or divide-by-four circuit used.				10 10	ms ms
Two-pin RC oscillator Oscillator frequency	f_{MOSC}	• Figure 2, Cext = 220 pF ±5% • Figure 2, Rext = 6.8 kΩ ±1%	OSC1, OSC2	595	800	1274	kHz
		• Figure 2, Cext = 220 pF ±5% • Figure 2, Rext = 12 kΩ ±1%	OSC1, OSC2	284	400	790	kHz
Built-in pull-up resistor I/O ports $\overline{RES}$	RPP	• Output n-channel transistors off • $V_{IN} = V_{SS}$, V_{DD} = 5 V	Ports with built-in pull-up resistor specifications	8	14	30	kΩ
	Ru	• $V_{IN} = V_{SS}$, V_{DD} = 5 V	$\overline{RES}$	200	500	800	kΩ
External reset characteristics Reset time	t_{RST}				See figure 5.		
Pin capacitance	Cp	• f = 1 MHz • With all pins except the pin being tested at $V_{IN} = V_{SS}$.			10		pF
Serial clock							
Input clock cycle time	t_{CKCY}(1)	See figure 6.	$\overline{SCK}$	2.0			µs
Output clock cycle time	t_{CKCY}(2)	See figure 6.	$\overline{SCK}$		64 × T_{CYC}*9		µs
Input clock low-level pulse width	t_{CKL}(1)	See figure 6.	$\overline{SCK}$	1.0			µs
Output clock low-level pulse width	t_{CKL}(2)	See figure 6.	$\overline{SCK}$		32 × T_{CYC}		µs
Input clock high-level pulse width	t_{CKH}(1)	See figure 6.	$\overline{SCK}$	1.0			µs
Output clock high-level pulse width	t_{CKH}(2)	See figure 6.	$\overline{SCK}$		32 × T_{CYC}		µs
Serial input							
Data setup time	t_{ICK}	Stipulated with respect to the $\overline{SCK}$ rising edge.	SI	0.5			µs
Data hold time	t_{CKI}	See figure 6.	SI	0.5			µs
Serial output							
Output delay time	t_{CKO}	• Stipulated with respect to the $\overline{SCK}$ falling edge. • With external 1 kΩ resistors and 50 pF capacitors on the n-channel open-drain outputs only. • See figure 6.	SO			0.5	µs

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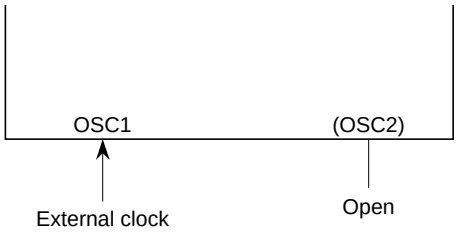
Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Pulse output Period	t_{PCY}	• See figure 7 • T_{CYC} = 4 × <system clock period> • With external 1 kΩ resistors and external 50 pF capacitors on the n-channel open-drain outputs only.	PE0		64 × T_{CYC}		µs
High-level pulse width	t_{PH}		PE0		32 × T_{CYC} ±10%		µs
Low-level pulse width	t_{PL}		PE0		32 × T_{CYC} ±10%		µs

Notes: 1. Voltages up to the generated oscillation amplitude are allowed with internal drive using the oscillator circuit of figure 3 and the recommended circuit constants.
2. The average over a 100 ms period.
3. Applications must hold the operating supply voltage V_{DD} level from the point a HALT instruction is executed until the IC enters the standby state. Also, switch bounce and similar noise must not appear on PA3 (or PA0 to 3) during the HALT instruction execution cycle.
4. The recommended circuit constants for which stable oscillation has been verified with the manufacturer of the oscillator element using the Sanyo specified oscillator characteristics evaluation board.
5. The OSC1 pin has Schmitt trigger characteristics when either 2-pin RC oscillator or external clock input is specified as the oscillator option.
6. The result of measurement when the recommended external circuit constants are used with the Sanyo characteristics evaluation board. The current due to the IC output transistors and pull-up resistor transistors is not included.
7. Indicates the frequency when f_{CFOSC} is due to the use of the recommended circuit constants in table 1.
8. Indicates the required time for oscillation to stabilize starting from the point when V_{DD} first exceeds the lower limit of the operating supply voltage range. (See figure 4.)
9. T_{CYC} = 4 × <system clock period>



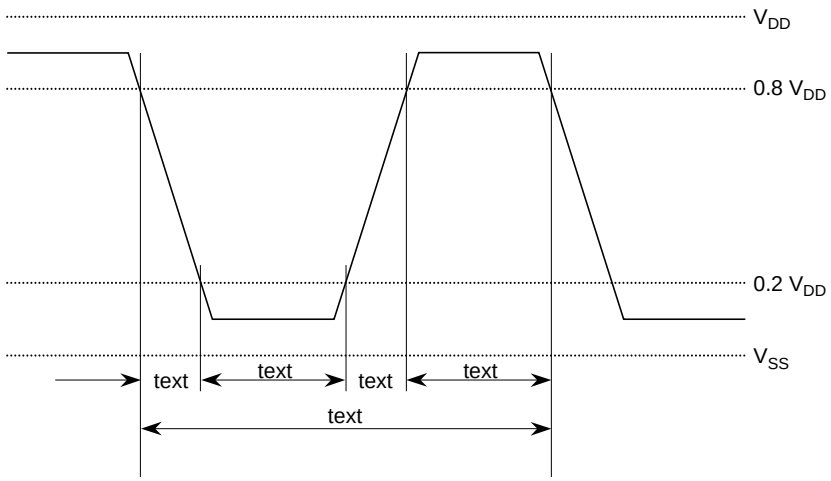


Figure 1 External Clock Input Waveform

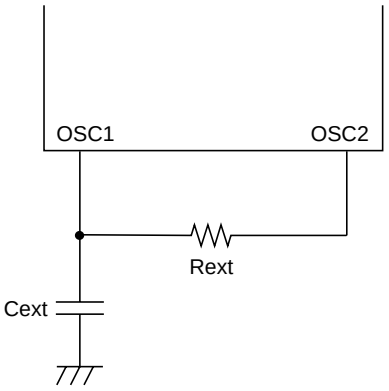


Figure 2 Two-Pin RC Oscillator Circuit

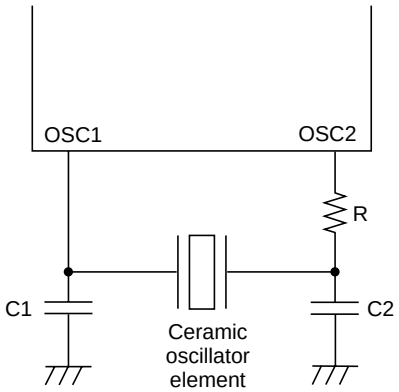


Figure 3 Ceramic Oscillator Circuit

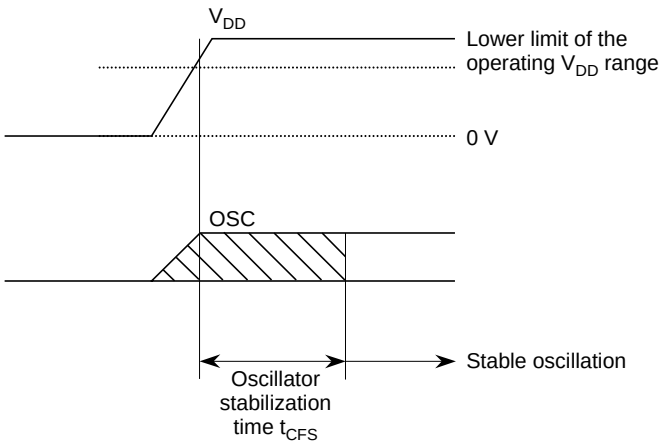


Figure 4 Oscillator Stabilization Time

Table 1 Ceramic Oscillator Recommended Circuit Constants

4 MHz (Murata Mfg. Co., Ltd.)	C1	33 pF ±10%
CSA4.00MG	C2	33 pF ±10%
CST4.00MGW (Built-in capacitor)	R	0 Ω
4 MHz (Kyocera Corporation)	C1	33 pF ±10%
KBR4.0MSB	C2	33 pF ±10%
KBR4.0MKC (Built-in capacitor)	R	0 Ω
1 MHz (Murata Mfg. Co., Ltd.)	C1	100 pF ±10%
CSB1000J	C2	100 pF ±10%
	R	2.2 kΩ
800 kHz (Murata Mfg. Co., Ltd.)	C1	100 pF ±10%
CSB800J	C2	100 pF ±10%
	R	2.2 kΩ
400 kHz (Murata Mfg. Co., Ltd.)	C1	220 pF ±10%
CSB400P	C2	220 pF ±10%
	R	2.2 kΩ

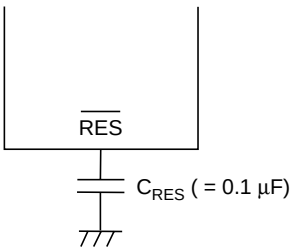


Figure 5 Reset Circuit

Note: When the power supply rise time is effectively zero, the reset time for a C_{RES} of 0.1 μF will be between 10 and 100 ms. If the power supply rise time is relatively long, increase the value of C_{RES} so that the reset time is over 10 ms.

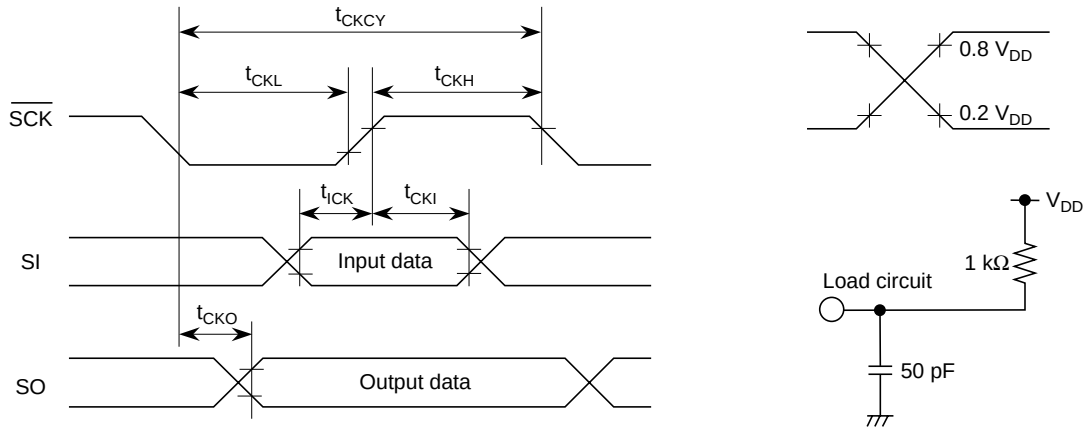
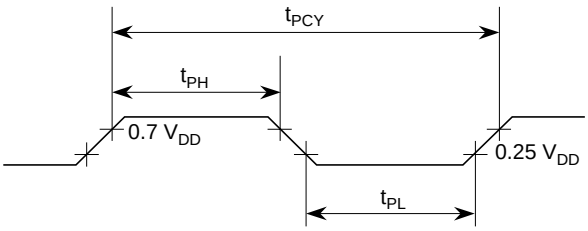


Figure 6 Serial I/O Timing



The load conditions are the same as those in figure 6.

Figure 7 Port PE0 Pulse Output Timing

LC651431N and LC651432N RC Oscillator Characteristics

Figure 8 shows the LC651431N and LC651432N RC oscillator characteristics.
However, the LC651431N and LC651432N have the following RC oscillator frequency sample-to-sample variations.

1) V_{DD} = 3.0 to 6.0 V, Ta = –40 to 85°C
   When the external circuit constants are: Cext = 220 pF, and
   Rext = 12 kΩ, the frequency range will be:
   284 kHz ≤ f_{MOSC} ≤ 790 kHz
2) V_{DD} = 3.0 to 6.0 V, Ta = –40 to 85°C
   When the external circuit constants are: Cext = 220 pF, and
   Rext = 6.8 kΩ, the frequency range will be:
   595 kHz ≤ f_{MOSC} ≤ 1274 kHz

   Note that only the above circuit constants are guaranteed.

   If using other values for these constants is unavoidable, use values in the following ranges.
   Cext = 150 to 390 pF
   Rext = 3 to 20 kΩ
   (See figure 8.)

Notes: 10. The oscillator frequency must be in the range 350 to 750 kHz when V_{DD} = 5.0 V and Ta = 25°C.
11. Applications must assure adequate margins so that oscillator frequency falls in the operating clock frequency range (in the oscillator divider option table) for the ranges V_{DD} = 3.0 to 6.0 V and Ta = –40 to 85°C.

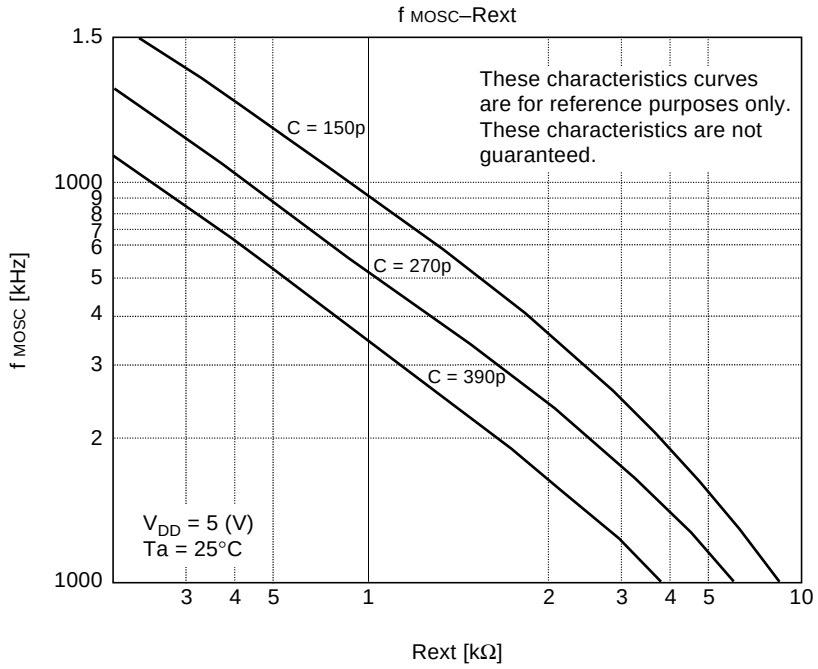


Figure 8 RC Oscillator Frequency Data (representative values)

LC651432F, 651431F

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Voltages up to the voltage generated are allowed.	V
Input voltage	V_I(1)		OSC1 *1	–0.3 to V_{DD} +0.3	V
	V_I(2)		TEST, $\overline{RES}$	–0.3 to V_{DD} +0.3	V
I/O voltage	V_{IO}(1)		Ports with open-drain specifications	–0.3 to +15	V
	V_{IO}(2)		Ports with pull-up resistor specifications	–0.3 to V_{DD} +0.3	V
	V_{IO}(3)		PI0	–0.3 to V_{DD} +0.3	V
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Per single pin, the average over a 100 ms period	I/O ports	–2 to +20	mA
	ΣI_{OA}(1)	The total current for PC0 to 3, PD0 to 3, and PE0 to 3*2	PC0 to 3 PD0 to 3 PE0 to 3	–15 to +100	mA
	ΣI_{OA}(2)	The total current for PF0 to 3, PG0 to 3, PA0 to 3, and PI0*2	PF0 to 3, PI0 PG0 to 3 PA0 to 3	–15 to +100	mA
Allowable power dissipation	Pd max(1)	Ta = –40 to +85°C (DIP package)		310	mW
	Pd max(2)	Ta = –40 to +85°C (MFP package)		220	mW
	Pd max(3)	Ta = –40 to +85°C (SSOP package)		160	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to 125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	3.0		6.0	V
Standby supply voltage	V_{ST}	RAM and register contents retained.*3	V_{DD}	1.8		6.0	V
High-level input voltage	V_{IH}(1)	With the n-channel output transistors off	Ports with open-drain specifications (except for I0)	0.7 V_{DD}		13.5	V
	V_{IH}(2)	With the n-channel output transistors off	Ports with pull-up resistor specifications (except for I0)	0.7 V_{DD}		V_{DD}	V
	V_{IH}(3)	With the n-channel output transistors off	Port I0	0.7 V_{DD}		V_{DD}	V
	V_{IH}(4)	With the n-channel output transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with open-drain specifications	0.8 V_{DD}		13.5	V
	V_{IH}(5)	With the n-channel output transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with pull-up resistor specifications	0.8 V_{DD}		V_{DD}	V
	V_{IH}(6)	V_{DD} = 1.8 to 6 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	V
	V_{IH}(7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	V

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Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Low-level input voltage	$V_{IL}(1)$	With the n-channel output transistors off V_{DD} = 4 to 6 V	Port	V_{SS}		0.3 V_{DD}	V
	$V_{IL}(2)$	With the n-channel output transistors off 3 to 6 V	Port	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(3)$	With the n-channel output transistors off V_{DD} = 4 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(4)$	With the n-channel output transistors off 3 to 6 V	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.2 V_{DD}	V
	$V_{IL}(5)$	External clock specifications V_{DD} = 4 to 6 V	OSC1	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(6)$	External clock specifications 3 to 6 V	OSC1	V_{SS}		0.2 V_{DD}	V
	$V_{IL}(7)$	V_{DD} = 4 to 6 V	TEST	V_{SS}		0.3 V_{DD}	V
	$V_{IL}(8)$	3 to 6 V	TEST	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(9)$	V_{DD} = 4 to 6 V	$\overline{RES}$	V_{SS}		0.25 V_{DD}	V
	$V_{IL}(10)$	3 to 6 V	$\overline{RES}$	V_{SS}		0.2 V_{DD}	V
Operating frequency (cycle time)	fop (Tcyc)			200 (20)		4330 (0.92)	kHz (µs)
External clock conditions							
Frequency	text	See figure 1.	OSC1	200		4330	kHz
Pulse width	textH, textL		OSC1	69			ns
Rise and fall time	textR, textF		OSC1			50	ns
Recommended oscillator circuit constants Ceramic oscillator*4		See figure 2.		See table 1.			

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
High-level input current	I_{IH}(1)	• With the output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = 13.5 V	Open-drain specification ports (except I0)			5.0	µA
	I_{IH}(2)	• With the output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = V_{DD}	The I0 port with open-drain specifications			1.0	µA
	I_{IH}(3)	External clock mode V_{IN} = V_{DD}	OSC1			1.0	µA
Low-level input current	I_{IL}(1)	• With the output n-channel transistors off • V_{IN} = V_{SS}	Open-drain specification ports	–1.0			µA
	I_{IL}(2)	• With the output n-channel transistors off • V_{IN} = V_{SS}	Built-in pull-up resistor specification ports	–1.3	–0.35		mA
	I_{IL}(3)	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
	I_{IL}(4)	External clock mode V_{IN} = V_{SS}	OSC1	–1.0			µA
High-level output voltage	V_{OH}(1)	• I_{OH} = –50 µA	Built-in pull-up resistor specification ports	V_{DD} – 1.2			V
	V_{OH}(2)	• I_{OH} = –10 µA	Built-in pull-up resistor specification ports	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}(1)	• I_{OL} = 10 mA	Ports			1.5	V
	V_{OL}(2)	I_{OL} = 1 mA, when I_{OL} for all ports is less than or equal to 1 mA.	Ports			0.5	V
Schmitt characteristics: Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, and OSC1 with Schmitt trigger specifications*5		0.1 V_{DD}		V
Schmitt characteristics: High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	V
Schmitt characteristics: Low-level threshold voltage	V_{tL}			0.2 V_{DD}		0.6 V_{DD}	V
Current drain*6 Ceramic oscillator External clock	I_{DDOP}(1)	• Figure 2, 4 MHz* • 200 to 4330 kHz* *: Operating, with the output n-channel transistors off, port voltage = V_{DD}	V_{DD}		1.5	4	mA
	I_{DDOP}(2)		V_{DD}		1	4	mA
Standby mode	I_{DDst}	With the output n-channel transistors off, V_{DD} = 6 V Port voltage = V_{DD}, V_{DD} = 3 V	V_{DD} V_{DD}		0.05 0.025	10 5	µA µA

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Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Oscillator characteristics Ceramic oscillator Oscillator frequency	f_{CFOSC}	• Figure 2, fo = 4 MHz*7	OSC1, OSC2	3920	4000	4080	kHz
Oscillator stabilization time*8	t_{CFS}	• Figure 3, fo = 4 MHz				10	ms
Built-in pull-up resistor I/O ports RES	RPP	• Output n-channel transistors off • $V_{IN} = V_{SS}$, V_{DD} = 5 V	Ports with built-in pull-up resistor specifications	8	14	30	kΩ
	Ru	• $V_{IN} = V_{SS}$, V_{DD} = 5 V	$\overline{RES}$	200	500	800	kΩ
External reset characteristics Reset time	t_{RST}			See figure 4.			
Pin capacitance	Cp	• f = 1 MHz • With all pins except the pin being tested at $V_{IN} = V_{SS}$.			10		pF
Serial clock Input clock cycle time	$t_{CKCY}(1)$	See figure 5.	$\overline{SCK}$	2.0			µs
Output clock cycle time	$t_{CKCY}(2)$	See figure 5.	$\overline{SCK}$		64 × T_{CYC}*9		µs
Input clock low-level pulse width	$t_{CKL}(1)$	See figure 5.	$\overline{SCK}$	1.0			µs
Output clock low-level pulse width	$t_{CKL}(2)$	See figure 5.	$\overline{SCK}$		32 × T_{CYC}		µs
Input clock high-level pulse width	$t_{CKH}(1)$	See figure 5.	$\overline{SCK}$	1.0			µs
Output clock high-level pulse width	$t_{CKH}(2)$	See figure 5.	$\overline{SCK}$		32 × T_{CYC}		µs
Serial input Data setup time	t_{ICK}	Stipulated with respect to the $\overline{SCK}$ rising edge.	SI	0.5			µs
Data hold time	t_{CKI}	See figure 5.	SI	0.5			µs
Serial output Output delay time	t_{CKO}	• Stipulated with respect to the $\overline{SCK}$ falling edge. • With external 1 kΩ resistors and 50 pF capacitors on the n-channel open-drain outputs only. • See figure 5	SO			0.5	µs
Pulse output Period	t_{PCY}	• See figure 6 • T_{CYC} = 4 × <system clock period> • With external 1 kΩ resistors and external 50 pF capacitors on the n-channel open-drain outputs only.	PE0		64 × T_{CYC}		µs
High-level pulse width	t_{PH}		PE0		32 × T_{CYC} ±10%		µs
Low-level pulse width	t_{PL}		PE0		32 × T_{CYC} ±10%		µs

Notes: 1. Voltages up to the generated oscillation amplitude are allowed with internal drive using the oscillator circuit of figure 2 and the recommended circuit constants.
2. The average over a 100 ms period.
3. Applications must hold the operating supply voltage V_{DD} level from the point a HALT instruction is executed until the IC enters the standby state. Also, switch bounce and similar noise must not appear on PA3 (or PA0 to 3) during the HALT instruction execution cycle.
4. The recommended circuit constants for which stable oscillation has been verified with the manufacturer of the oscillator element using the Sanyo specified oscillator characteristics evaluation board.
5. The OSC1 pin has Schmitt trigger characteristics when external clock is specified as the oscillator option.
6. The result of measurement when the recommended external circuit constants are used with the Sanyo characteristics evaluation board. The current due to the IC output transistors and pull-up resistor transistors is not included.
7. Indicates the frequency when f_{CFOSC} is due to the use of the recommended circuit constants in table 1.
8. Indicates the required time for oscillation to stabilize starting from the point when V_{DD} first exceeds the lower limit of the operating supply voltage range. (See figure 3.)
9. T_{CYC} = 4 × <system clock period>

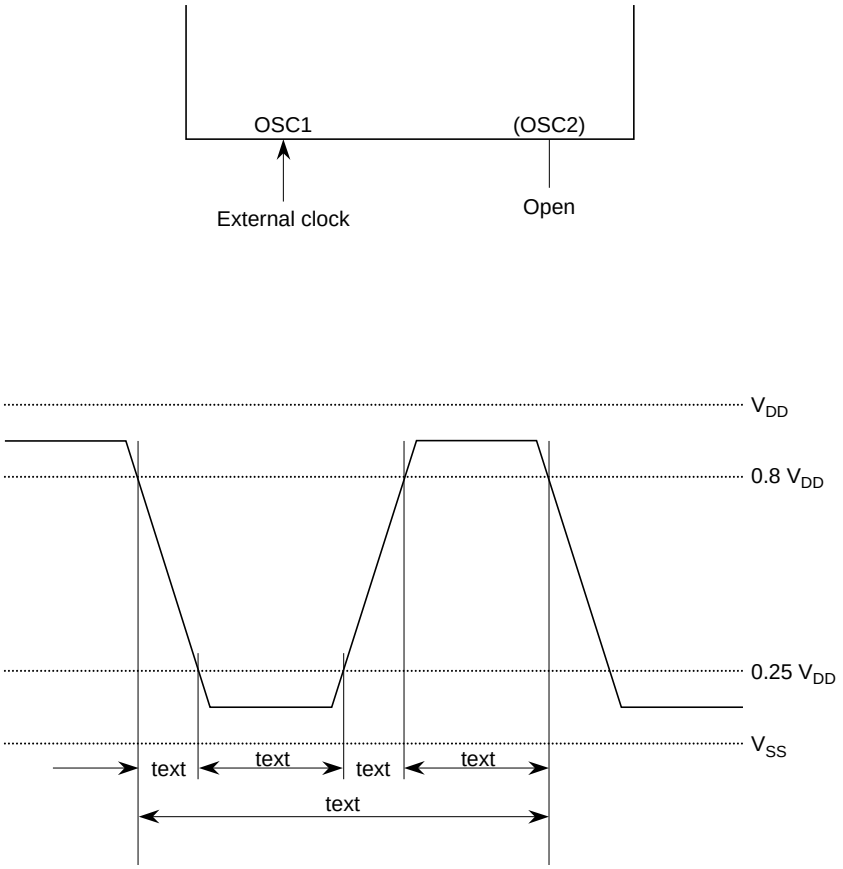


Figure 1 External Clock Input Waveform

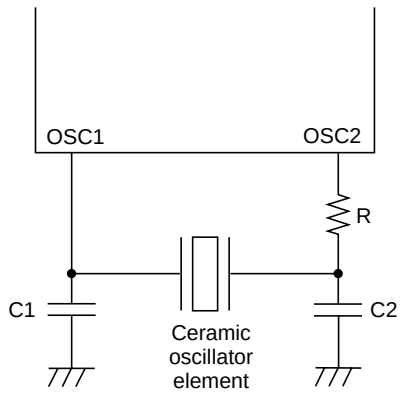


Figure 2 Ceramic Oscillator Circuit

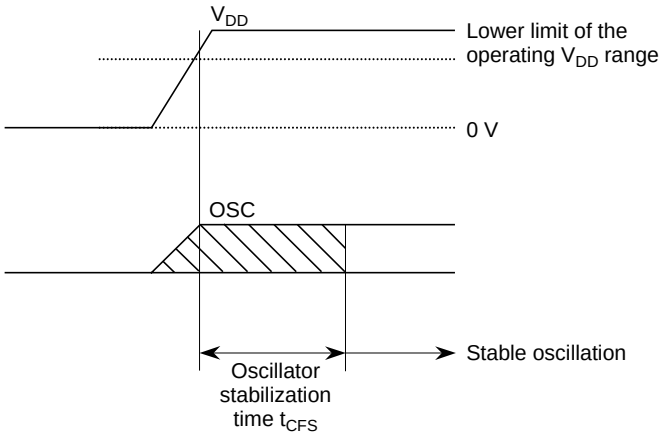


Figure 3 Oscillator Stabilization Time

Table 1 Ceramic Oscillator Recommended Circuit Constants

4 MHz (Murata Mfg. Co., Ltd.)	C1	33 pF ±10%
CSA4.00MG	C2	33 pF ±10%
CST4.00MGW (Built-in capacitor)	R	0 Ω
4 MHz (Kyocera Corporation)	C1	33 pF ±10%
KBR4.0MSB	C2	33 pF ±10%
KBR4.0MKC (Built-in capacitor)	R	0 Ω

Sanyo is currently requesting evaluation of oscillator element products and recommended circuit constants from Kyocera Corporation for their products, and thus these recommendations are subject to change. Contact your Sanyo representative before using these devices.

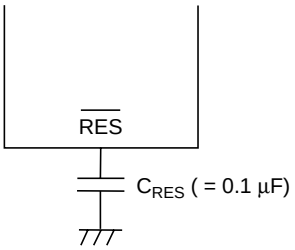


Figure 4 Reset Circuit

Note: When the power supply rise time is effectively zero, the reset time for a C_{RES} of 0.1 μF will be between 10 and 100 ms. If the power supply rise time is relatively long, increase the value of C_{RES} so that the reset time is over 10 ms.

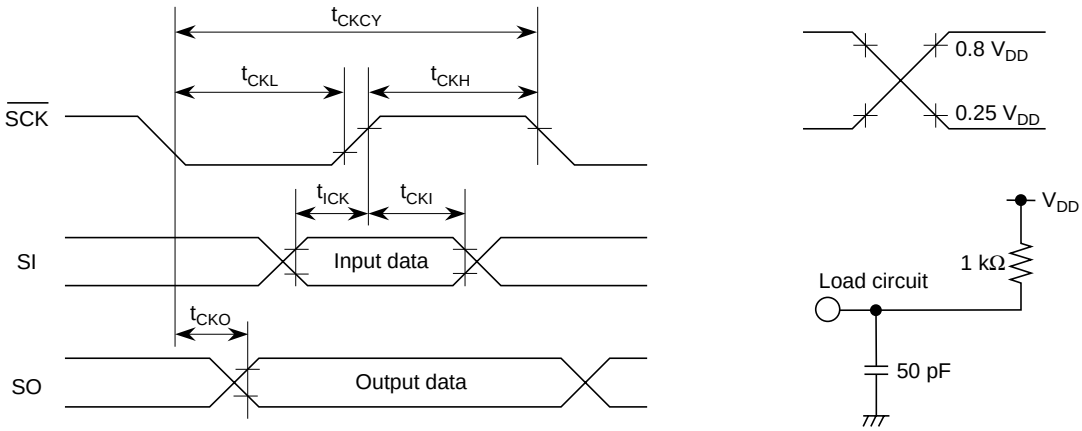
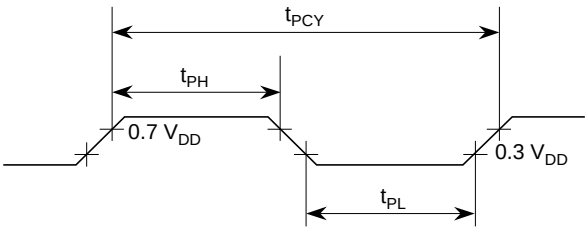


Figure 5 Serial I/O Timing



The load conditions are the same as those in figure 5.

Figure 6 Port PE0 Pulse Output Timing

LC651432L, 651431L

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Voltages up to the voltage generated are allowed.	V
Input voltage	V_I(1)		OSC1 *1	–0.3 to V_{DD} +0.3	V
	V_I(2)		TEST, $\overline{RES}$	–0.3 to V_{DD} +0.3	V
I/O voltage	V_{IO}(1)		Ports with open-drain specifications	–0.3 to +15	V
	V_{IO}(2)		Ports with pull-up resistor specifications	–0.3 to V_{DD} +0.3	V
	V_{IO}(3)		PI0	–0.3 to V_{DD} +0.3	V
Peak output current	I_{OP}		I/O ports	–2 to +20	mA
Average output current	I_{OA}	Per single pin, the average over a 100 ms period	I/O ports	–2 to +20	mA
	ΣI_{OA}(1)	The total current for PC0 to 3, PD0 to 3, and PE0 to 3*2	PC0 to 3 PD0 to 3 PE0 to 3	–15 to +100	mA
	ΣI_{OA}(2)	The total current for PF0 to 3, PG0 to 3, PA0 to 3, and PI0*2	PF0 to 3, PI0 PG0 to 3 PA0 to 3	–15 to +100	mA
Allowable power dissipation	Pd max(1)	Ta = –40 to +85°C (DIP package)		310	mW
	Pd max(2)	Ta = –40 to +85°C (MFP package)		220	mW
	Pd max(3)	Ta = –40 to +85°C (SSOP package)		160	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to 125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.2 to 6.0 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	2.2		6.0	V
Standby supply voltage	V_{ST}	RAM and register contents retained. *2	V_{DD}	1.8		6.0	V
High-level input voltage	V_{IH}(1)	With the n-channel output transistors off	Ports with open-drain specifications (except for I0)	0.7 V_{DD}		13.5	V
	V_{IH}(2)	With the n-channel output transistors off	Ports with pull-up resistor specifications (except for I0)	0.7 V_{DD}		V_{DD}	V
	V_{IH}(3)	With the n-channel output transistors off	Port I0	0.7 V_{DD}		V_{DD}	V
	V_{IH}(4)	With the n-channel output transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with open-drain specifications	0.8 V_{DD}		13.5	V
	V_{IH}(5)	With the n-channel output transistors off	The $\overline{INT}$, $\overline{SCK}$, and SI pins with pull-up resistor specifications	0.8 V_{DD}		V_{DD}	V
	V_{IH}(6)	V_{DD} = 1.8 to 6 V	$\overline{RES}$	0.8 V_{DD}		V_{DD}	V
	V_{IH}(7)	External clock specifications	OSC1	0.8 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}(1)	With the n-channel output transistors off	Ports	V_{SS}		0.2 V_{DD}	V
	V_{IL}(2)	With the n-channel output transistors off	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.2 V_{DD}	V
	V_{IL}(3)	External clock specifications	OSC1	V_{SS}		0.15 V_{DD}	V
	V_{IL}(4)		TEST	V_{SS}		0.22 V_{DD}	V
	V_{IL}(5)		$\overline{RES}$	V_{SS}		0.15 V_{DD}	V

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Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Operating frequency (cycle time)	fop (Tcyc)	When the built-in divide-by-four circuit is selected, the clock frequency upper limit is 4.16 MHz.		200 (20)		1040 (3.84)	kHz (µs)
External clock conditions		Figure 1. If the clock frequency exceeds 1.040 MHz, either the divide-by-three or the divide-by-four divider circuit option must be selected.					
Frequency	text		OSC1	200		4160	kHz
Pulse width	textH, textL		OSC1	120			ns
Rise and fall time	textR, textF		OSC1			100	ns
Recommended oscillator circuit constants							
Two-pin RC oscillator	Cext	See figure 2.	OSC1, OSC2		220 ± 5%		pF
	Rext				12 ±1%		kΩ
Ceramic oscillator*4		See figure 3.			See table 1.		

Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.2 to 6.0 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
High-level input current	$I_{IH}(1)$	• With the output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = 13.5 V	Open-drain specification ports (except I0)			5.0	µA
	$I_{IH}(2)$	• With the output n-channel transistors off (Including the n-channel transistor off leakage current.) • V_{IN} = V_{DD}	The I0 port with open-drain specifications			1.0	µA
	$I_{IH}(3)$	External clock mode V_{IN} = V_{DD}	OSC1			1.0	µA
Low-level input current	$I_{IL}(1)$	• With the output n-channel transistors off • V_{IN} = V_{SS}	Open-drain specification ports	–1.0			µA
	$I_{IL}(2)$	• With the output n-channel transistors off • V_{IN} = V_{SS}	Built-in pull-up resistor specification ports	–1.3	–0.35		mA
	$I_{IL}(3)$	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
	$I_{IL}(4)$	External clock mode V_{IN} = V_{SS}	OSC1	–1.0			µA
High-level output voltage	V_{OH}	• I_{OH} = –10 µA	Built-in pull-up resistor	V_{DD} – 0.5			V
Low-level output voltage	$V_{OL}(1)$	• I_{OL} = 3 mA	Ports			1.5	V
	$V_{OL}(2)$	I_{OL} = 1 mA, when I_{OL} for all ports is less than or equal to 1 mA.	Ports			0.4	V
Schmitt characteristics: Hysteresis voltage	V_{HIS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, and OSC1 with Schmitt trigger specifications*5		0.1 V_{DD}		V
Schmitt characteristics: High-level threshold voltage	V_{tH}			0.4 V_{DD}		0.8 V_{DD}	V
Schmitt characteristics: Low-level threshold voltage	V_{tL}			0.2 V_{DD}		0.6 V_{DD}	V
Current drain*6 Two-pin RC oscillator	$I_{DDOP}(1)$	• While operating, with the output n-channel transistors off • Port voltage = V_{DD} • Figure 2, fosc = 400 kHz (typical)	V_{DD}		0.8	2.5	mA
Ceramic oscillator	$I_{DDOP}(2)$	• Figure 3, 4 MHz, divide-by-four circuit used.	V_{DD}		1	3	mA
External clock	$I_{DDOP}(3)$	• Figure 3, 4 MHz, divide-by-four circuit used. V_{DD} = 2.2 V	V_{DD}		0.3	1	mA
Standby mode	$I_{DDOP}(4)$	See figure 3. 400 kHz	V_{DD}		1	2.5	mA
	$I_{DDOP}(5)$	• 200 to 1024 kHz, no divider • 600 to 3120 kHz, divide-by-three circuit used • 800 to 4160 kHz, divide-by-four circuit used	V_{DD}		1.5	4	mA
	I_{DDst}	Output n-channel transistors off, V_{DD} = 6 V Port voltage = V_{DD}, V_{DD} = 2.2 V	V_{DD} V_{DD}		0.05 0.025	10 5	µA µA

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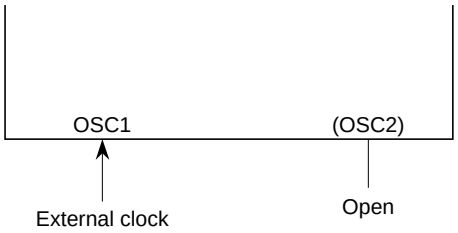
Parameter	Symbol	Conditions	Applicable pins	Ratings			Unit
				min	typ	max	
Oscillator characteristics							
Ceramic oscillator Oscillator frequency	f_{CFOSC}*7	• Figure 3, fo = 400 kHz • Figure 3, fo = 4 MHz, divide-by-four circuit used.	OSC1, OSC2 OSC1, OSC2	392 3920	400 4000	408 4080	kHz kHz
Oscillator stabilization time*8	t_{CFS}	• Figure 4, fo = 400 kHz • Figure 4, fo = 800 kHz, 1 MHz, or 4 MHz, divide-by-four circuit used.				10 10	ms ms
Two-pin RC oscillator Oscillator frequency	f_{MOSC}	• Figure 2, Cext = 220 pF ±5% • Figure 2, Rext = 12 kΩ ±1%	OSC1, OSC2	200	400	790	kHz
Built-in pull-up resistor I/O ports $\overline{RES}$	RPP	• Output n-channel transistors off • $V_{IN} = V_{SS}$, V_{DD} = 5 V	Ports with built-in pull-up resistor specifications	8	14	30	kΩ
	Ru	• $V_{IN} = V_{SS}$, V_{DD} = 5 V	$\overline{RES}$	200	500	800	
External reset characteristics Reset time	t_{RST}			See figure 5.			
Pin capacitance	Cp	• f = 1 MHz • With all pins except the pin being tested at $V_{IN} = V_{SS}$.			10		pF
Serial clock							
Input clock cycle time	t_{CKCY}(1)	See figure 6.	$\overline{SCK}$	12.0			µs
Output clock cycle time	t_{CKCY}(2)	See figure 6.	$\overline{SCK}$		64 × T_{CYC}*9		µs
Input clock low-level pulse width	t_{CKL}(1)	See figure 6.	$\overline{SCK}$	4.0			µs
Output clock low-level pulse width	t_{CKL}(2)	See figure 6.	$\overline{SCK}$		32 × T_{CYC}		µs
Input clock high-level pulse width	t_{CKH}(1)	See figure 6.	$\overline{SCK}$	4.0			µs
Output clock high-level pulse width	t_{CKH}(2)	See figure 6.	$\overline{SCK}$		32 × T_{CYC}		µs
Serial input							
Data setup time	t_{ICK}	Stipulated with respect to the $\overline{SCK}$ rising edge.	SI	0.5			µs
Data hold time	t_{CKI}	See figure 6.	SI	0.5			µs
Serial output							
Output delay time	t_{CKO}	• Stipulated with respect to the $\overline{SCK}$ falling edge. • With external 1 kΩ resistors and 50 pF capacitors on the n-channel open-drain outputs only. • See figure 6	SO			2.0	µs
Pulse output							
Period	t_{PCY}	• See figure 7 • T_{CYC} = 4 × <system clock period> • With external 1 kΩ resistors and external 50 pF capacitors on the n-channel open-drain outputs only.	PE0		64 × T_{CYC}		µs
High-level pulse width	t_{PH}		PE0		32 × T_{CYC} ±10%		µs
Low-level pulse width	t_{PL}		PE0		32 × T_{CYC} ±10%		µs

Notes: 1. Voltages up to the generated oscillation amplitude are allowed with internal drive using the oscillator circuit of figure 3 and the recommended circuit constants.
2. The average over a 100 ms period.
3. Applications must hold the operating supply voltage V_{DD} level from the point a HALT instruction is executed until the IC enters the standby state. Also, switch bounce and similar noise must not appear on PA3 (or PA0 to 3) during the HALT instruction execution cycle.
4. The recommended circuit constants for which stable oscillation has been verified with the manufacturer of the oscillator element using the Sanyo specified oscillator characteristics evaluation board.
5. The OSC1 pin has Schmitt trigger characteristics when either 2-pin RC oscillator or external clock input is specified as the oscillator option.
6. The result of measurement when the recommended external circuit constants are used with the Sanyo characteristics evaluation board. The current due to the IC output transistors and pull-up resistor transistors is not included.
7. Indicates the frequency when f_{CFOSC} is due to the use of the recommended circuit constants in table 1.
8. Indicates the required time for oscillation to stabilize starting from the point when V_{DD} first exceeds the lower limit of the operating supply voltage range. (See figure 4.)
9. $T_{CYC} = 4 \times$ <system clock period>



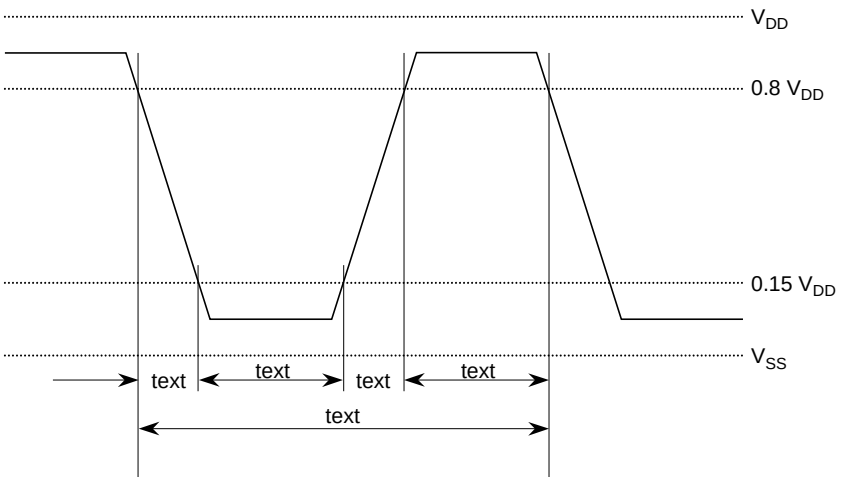


Figure 1 External Clock Input Waveform

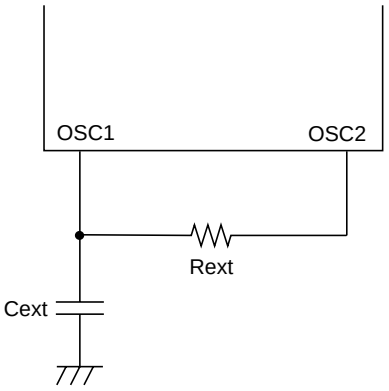


Figure 2 Two-Pin RC Oscillator Circuit

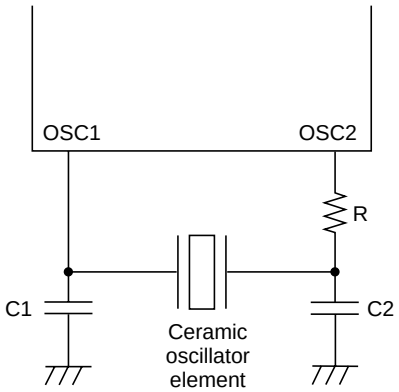


Figure 3 Ceramic Oscillator Circuit

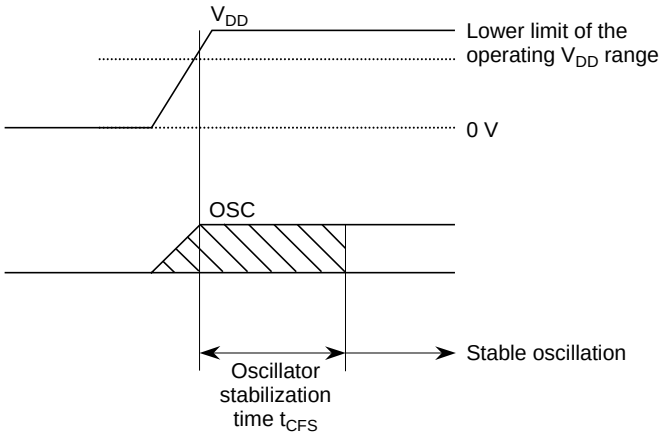


Figure 4 Oscillator Stabilization Time

Table 1 Ceramic Oscillator Recommended Circuit Constants

4 MHz (Murata Mfg. Co., Ltd.)	C1	33 pF ±10%
CSA4.00MGU	C2	33 pF ±10%
CST4.00MGWU (Built-in capacitor)	R	0 Ω
400 kHz (Murata Mfg. Co., Ltd.)	C1	330 pF ±10%
CSB400P	C2	330 pF ±10%
	R	3.3 kΩ

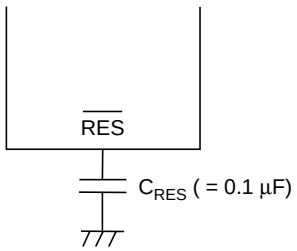


Figure 5 Reset Circuit

Note: When the power supply rise time is effectively zero, the reset time for a C_{RES} of 0.1 µF will be between 10 and 100 ms. If the power supply rise time is relatively long, increase the value of C_{RES} so that the reset time is over 10 ms.

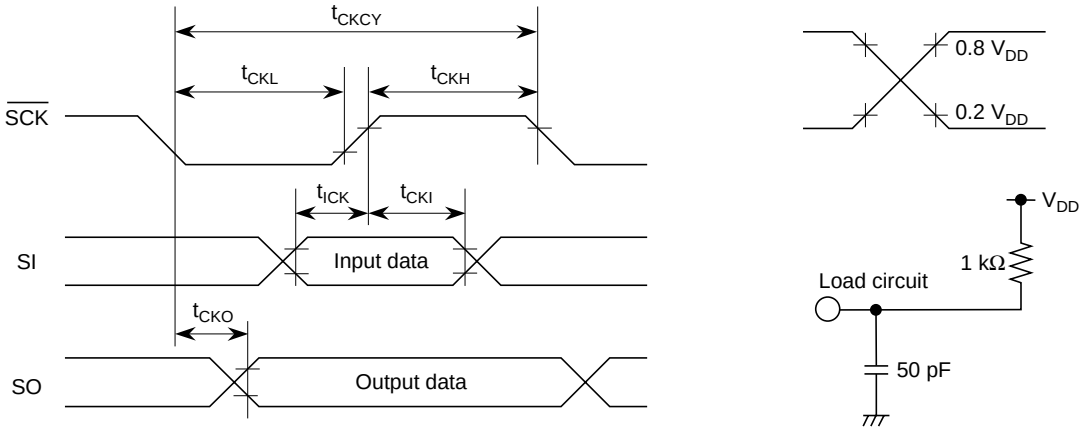
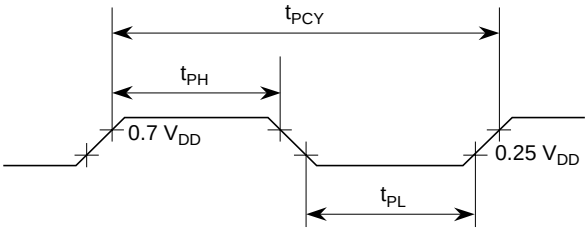


Figure 6 Serial I/O Timing



The load conditions are the same as those in figure 6.

Figure 7 Port PE0 Pulse Output Timing

LC651431L and LC651432L RC Oscillator Characteristics

Figure 8 shows the LC651431L and LC651432L RC oscillator characteristics.
However, the LC651431L and LC651432L have the following RC oscillator frequency sample-to-sample variations.

V_{DD} = 2.2 to 6.0 V, Ta = –40 to 85°C
When the external circuit constants are: Cext = 220 pF, and
Rext = 12 kΩ, the frequency range will be:
200 kHz ≤ f_{MOSC} ≤ 790 kHz

Note that only the above circuit constants are guaranteed.

If using other values for these constants is unavoidable, use values in the following ranges.
Cext = 150 to 390 pF
Rext = 3 to 20 kΩ
(See figure 8.)

Notes: 10. The oscillator frequency must be in the range 350 to 500 kHz when V_{DD} = 5.0 V and Ta = 25°C.
11. Applications must assure adequate margins so that oscillator frequency falls in the operating clock frequency range (in the oscillator divider option table) for the ranges V_{DD} = 2.2 to 6.0 V and Ta = –40 to 85°C.

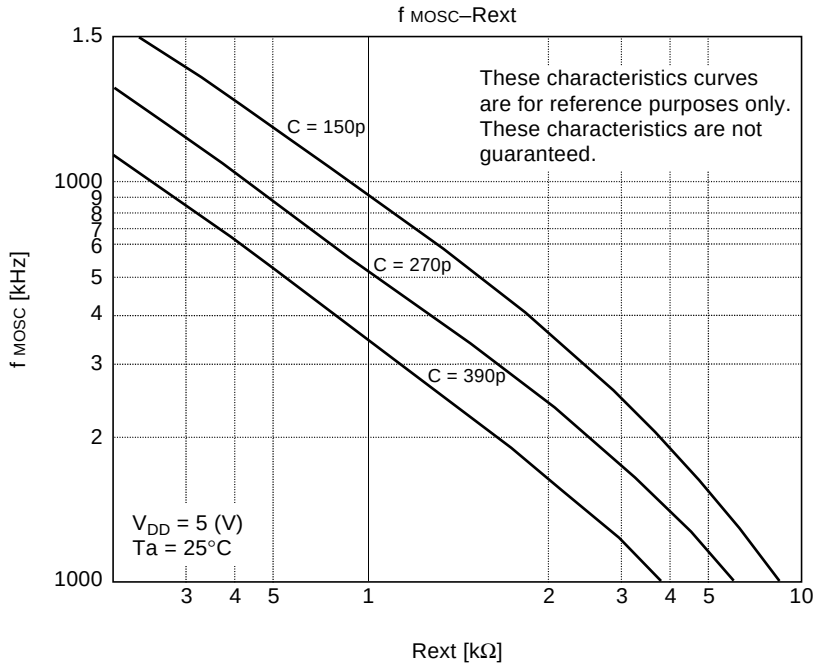
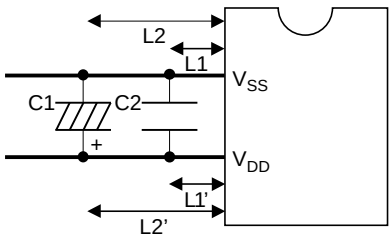


Figure 8 RC Oscillator Frequency Data (representative values)

Notes on PCB Construction

This section presents notes on noise as seen from the microcontroller itself and methods for reducing such noise when designing the printed circuit board for a mass-produced product using these microcontrollers. The design techniques presented here can be effective for preventing or avoiding problems (such as microcontroller malfunction and program runaway) due to noise.

1. V_{DD} and V_{SS}: Power supply pins
   Insert capacitors that meet the following conditions between the V_{DD} and V_{SS} pins.
   - For each of the capacitors C1 and C2, make the wiring lengths from the IC as close to equal as possible (L1 = L1' and L2 = L2'), and keep these lines as short as possible as well.
   - Insert the capacitors C1, a large capacitor, and C2, a small capacitor, in parallel.
   - The V_{DD} and V_{SS} lines in the printed circuit board pattern should be wider than any other lines.



2. OSC1 and OSC2: Clock input and output pins
   When the ceramic oscillator option is selected (figure 2-1)
   - Keep the length (L_{OSC}) of the connection lines between the clock I/O pins (input: OSC1, output: OSC2) and the external components as short as possible.
   - Keep the length (L_{VSS} + L1 (L2)) from the V_{SS} side of the capacitor connected to the oscillator element to the V_{SS} pin as short as possible.
   - V_{SS} line for the oscillator circuit and other V_{SS} lines should branch from a point nearest to the V_{SS} pin.
   - There are cases where the values of the oscillator circuit components (the capacitors C1 and C2, the limit resistor Rd, and other components) must be modified from the values recommended in this document to adjust the oscillator frequency. Consult with the oscillator element manufacturer when determining the component values.

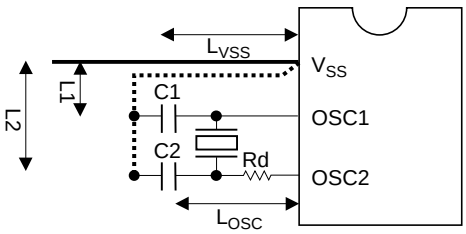


Figure 2-1 Oscillator Circuit Example 1 (ceramic oscillator)

   When the 2-pin RC oscillator option is selected (figure 2-2)
   - Keep the length (L_{OSC}) of the connection lines between the clock I/O pins (input: OSC1, output: OSC2) and the external components (the capacitor Cext and the resistor Rext) as short as possible.
   - Keep the length (L_{VSS} + Lc) from the V_{SS} side of the capacitor connected to the oscillator element to the V_{SS} pin as short as possible.

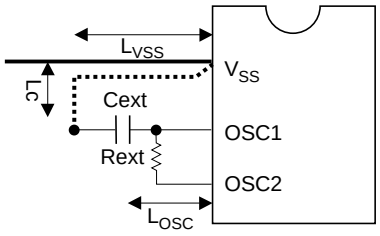


Figure 2-2 Oscillator Circuit Example 2 (2-pin RC oscillator)

   - V_{SS} line for the oscillator circuit and other V_{SS} lines should branch from a point nearest to the V_{SS} pin.

When the external oscillator option is selected (figure 2-3)

- Keep the length (L_{OSC}) of the line between the external oscillator and the IC clock input pin (OSC1) as short as possible.
- Also keep the length (L_{OSC}) of the lines between the external oscillator and the V_{DD} and V_{SS} used as short as possible.

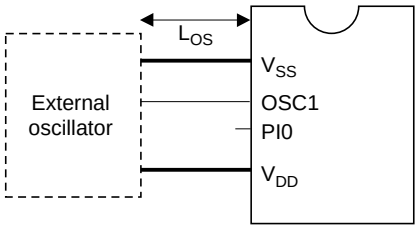


Figure 2-3 Oscillator Circuit Example 3 (external oscillator)

Other common points:

- Keep signals that change rapidly and large-amplitude signals connected to medium-voltage handling ports as far away from the oscillator circuit as possible and do not allow such lines to cross lines related to clock signals.

3. $\overline{RES}$: Reset pin
   - Keep the line from the external reset circuit to the $\overline{RES}$ pin as short as possible.
   - Keep the length (L1, L2) of the lines from the capacitor (Cres) inserted between $\overline{RES}$ and V_{SS} as short as possible.

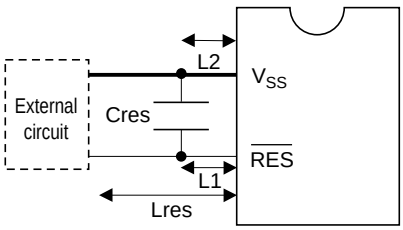


Figure 3 $\overline{RES}$ Pin Wiring

4. TEST: Test pin
   - Keep the line that connects the TEST pin to V_{SS} as short as possible.
   - Take the line that connects the TEST pin to V_{SS} from a location as close to the V_{SS} pin as possible.

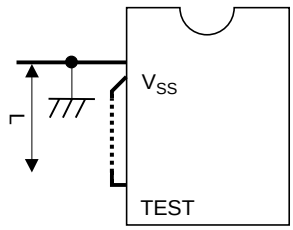


Figure 4 TEST Pin Wiring

5. I/O pins

All of the pins on these microcontrollers are shared-function I/O pins.

- When used as input pins, insert limiting resistors and keep the connection lines as short as possible.

Supplement: This can be effective in preventing or avoiding microcontroller problems (such as malfunctions and program runaway), not only in printed circuit board design, but in selecting the microcontroller option types discussed below and when considering application program specifications.

- If signals are input when the microcontroller power supply is unstable, select the medium-voltage (n-channel open drain) output as the output circuit type for that pin, and also insert a limiting resistor as close to the pin as possible.
- Always adopt key bounce elimination techniques when inputting external signals to any microcontroller pin.
- Periodically refresh the pin output data with an output instruction (OP or SPB).
- When reading data input to a shared-function (bidirectional) I/O pin, set the value of the output data for that pin to 1 on every read operation with an output instruction (OP or SPB).

6. Unused pins

- Refer to the pin functions table in the user's manual for the product itself or in the relevant Sanyo Semiconductor Development Report.

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