STV7801S

PLASMA DATA POWER SWITCH

PRELIMINARY DATA

FEATURES

- High Voltage - Low Power Pulse Generator
- 100V Absolute Maximum Supply
- High Load Drive Capability (25nF)
- 5V Compatible Input Logic
- Very Low Stand-by Current
- Power Recovery High Current (±7A)
- Totem Pole High Output Current (±5A)
- Built-in Timing Control & Thermal Protection
- BCD Technology
- Packaging: Multiwatt 15, Power SO20

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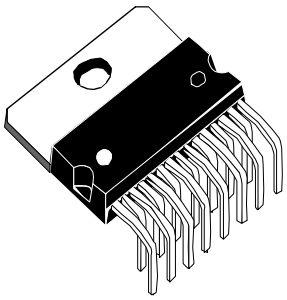


MULTIWATT 15 (Plastic Package)

ORDER CODE: STV7801S

DESCRIPTION

STV7801 is a monolithic integrated circuit implemented in STMicroelectronics BCD proprietary technology designed as a switched power supply generator for data drivers in a Plasma Display Panel (P.D.P.) application.

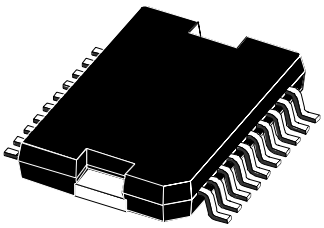
The high load drive capability of the STV7801 reduces the number of devices necessary to drive a complete PDP (4 to 6 devices for a 42" VGA 16/9 PDP monitor).

The STV7801 high current drive capability provides a high power recovery efficiency coefficient superior to 85% on constant capacitive load.

To limit the number of external components, the device integrates level shifters driven with 5V CMOS compatible levels.

To increase the reliability of the system, the device integrates several protections such as output over-voltage, over-temperature, power-ON protection.

Customer samples will be available by september 2000



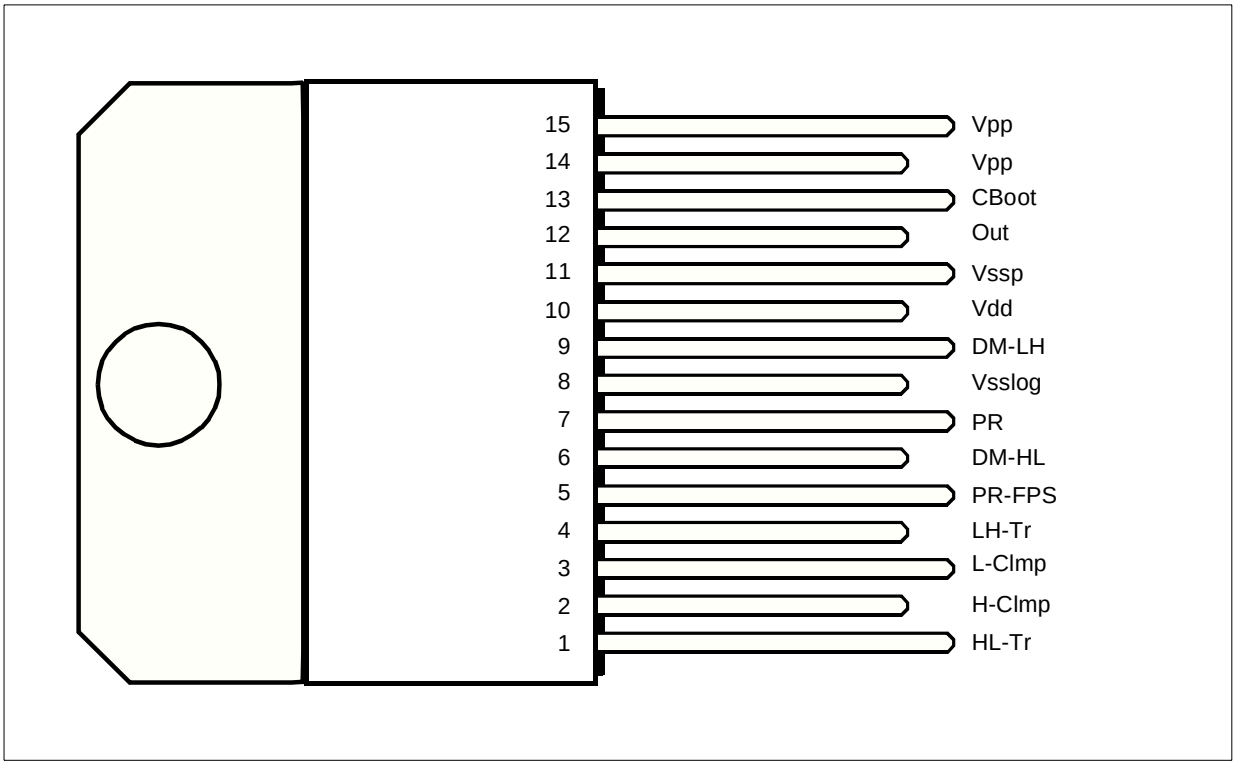
POWERSO20 (Plastic Package)

ORDER CODE: STV7801SP

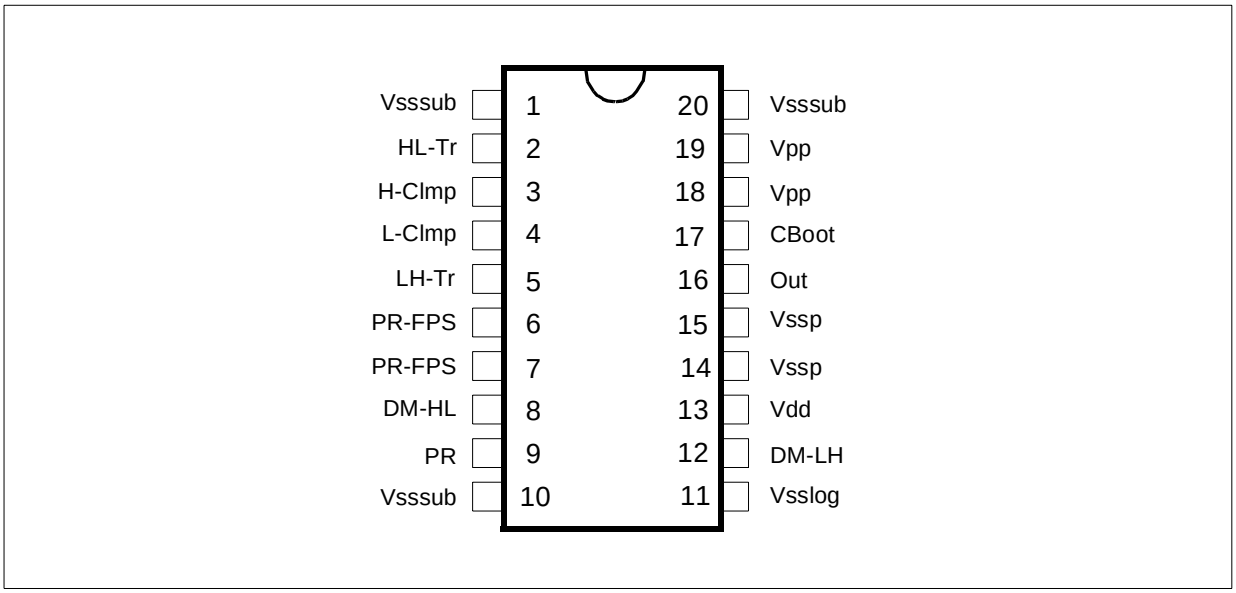
Revision 3.3

1 - PIN CONNECTION

Multiwatt 15

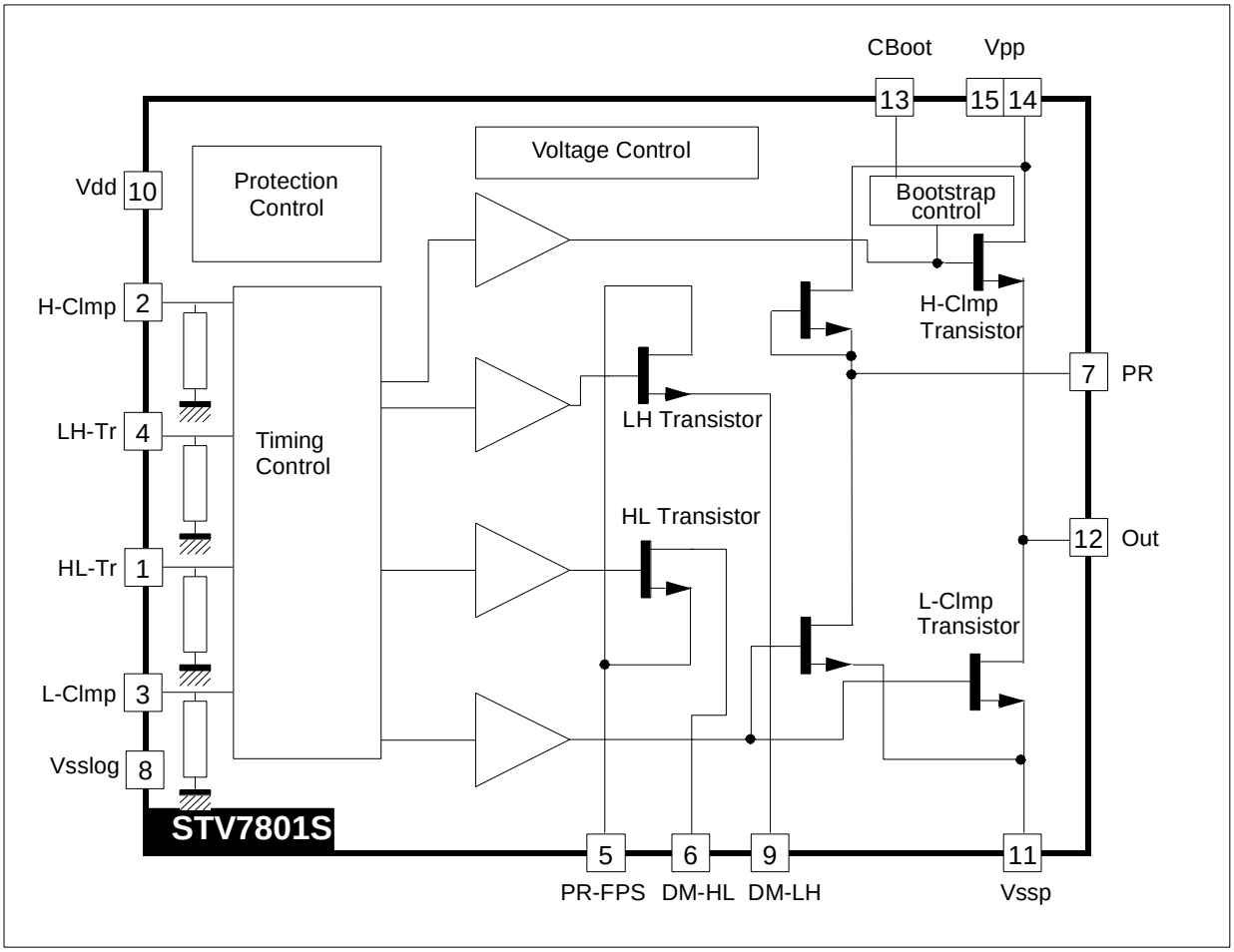


PowerSO20



2 - BLOC DIAGRAM

MULTIWATT 15



3 - PIN DESCRIPTION

Multiwatt 15

Pin Number	Pin Name	Function	Description
1	HL-Tr	Input	Power Recovery High Level/Low Level Transition
2	H-Clmp	Input	Main Switch High-Side Clamp Input
3	L-Clmp	Input	Main Switch Low-Side Clamp Input
4	LH-Tr	Input	Power Recovery Low Level/High Level Transition
5	PR-FPS	Input	Power Recovery Floating Supply
6	DM-HL	Input	Current Recirculation- Input Pin - High/Low Transition
7	PR	Output	Power Recirculation Output Stage
8	Vsslog	Ground	Logic Ground/Substrate Ground
9	DM-LH	Output	Current Recirculation- Output Pin - Low/High Transition
10	Vdd	Supply	Logic Supply
11	Vssp	Ground	Power Ground
12	Out	Output	Main Switch Output
13	CBoot	Input	Bootstrap Capacitor Input Pin
14	Vpp	Supply	High Voltage Supply
15	Vpp	Supply	High Voltage Supply

PowerSO20

Pin Number	Pin Name	Function	Description
1	Vssub	Ground	Substrate Ground
2	HL-Tr	Input	Power Recovery High Level/Low Level Transition
3	H-Clmp	Input	Main Switch High-Side Clamp Input
4	L-Clmp	Input	Main Switch Low-Side Clamp Input
5	LH-Tr	Input	Power Recovery Low Level/High Level Transition
6	PR-FPS	Input	Power Recovery Floating Supply
7	PR-FPS	Input	Power Recovery Floating Supply
8	DM-HL	Input	Current Recirculation- Input Pin - High/Low Transition
9	PR	Output	Power Recirculation Output Stage
10	Vssub	Ground	Substrate Ground
11	Vsslog	Ground	Logic Ground/Substrate Ground
12	DM-LH	Output	Current Recirculation- Output Pin - Low/High Transition
13	Vdd	Supply	Logic Supply
14	Vssp	Ground	Power Ground
15	Vssp	Ground	Power Ground
16	Out	Output	Main Switch Output
17	CBoot	Input	Bootstrap Capacitor Input Pin

Pin Number	Pin Name	Function	Description
18	Vpp	Supply	High Voltage Supply
19	Vpp	Supply	High Voltage Supply
20	Vssub	Ground	Substrate Ground

4 - CIRCUIT DESCRIPTION

STV7801 is a monolithic integrated circuit implemented in ST Microelectronics BCD proprietary technology designed as a switched power supply generator for data drivers in a Plasma Display Panel (P.D.P.) application.

The high load drive capability of STV7801 reduces the number of devices necessary to drive a complete PDP (4 to 6 devices for a 42" VGA 16/9 PDP monitor).

STV7801 high current drive capability provides a high power recovery efficiency coefficient superior to 85% on constant capacitive load. The structure of the output stage is implemented with 2 DMOS transistors to minimise the die size. External components like bootstrap capacitor can also be implemented to increase the performances of the circuit.

STV7801 integrates level shifters driven with 5V CMOS compatible levels. This feature reduces the number of discrete components such as voltage translators.

STV7801 integrates several protections like output over-voltage, timing control and over-temperature to increase the reliability of the system.

Over-voltage protection consists in clamping diodes connected between Vpp, Vssp and critical nodes of the devices.

Timing control consists in a monitoring of the output stage control signals to avoid any cross-conduction.

Over-temperature protection is activated when junction temperature reaches the threshold values fixed internally and sets the device in tri-state mode.

STV7801 can drive several data drivers connected to column electrodes of the panel. The maximum amount of data drivers is given by the Power Recovery Current of the device and then the maximum rise/fall time of the signal. The rise and fall time of the AC supply signal is adjusted by the value of the inductance connected to the panel capacitance through the data drivers. The amount of STV7801 needed to generate the AC supply can be reduced by increasing the rise/fall time of the generated AC supply.

5 - CONTROL SIGNALS TRUTH TABLE

HL-Tr	LH-Tr	L-Clmp	H-Clmp	Device Output	Comments
L	H	L	L	Low to High Transition	Power Saving Mode
H	L	L	L	High to Low Transition	Power Saving Mode
L	X	L	H	Vpp	Power Supply Clamp
X	L	H	L	Vssp	Power Ground Clamp
X	X	H	H	Tri-State	Protection Mode
X	H	H	X	Tri-State	Protection Mode
H	X	X	H	Tri-State	Protection Mode
L	L	L	L	Tri-State	Protection Mode

6 - POWER ON SEQUENCE

If Vpp is switched ON before Vdd, the circuit remains in Tri-State mode until Vdd reaches Vdd threshold.
If Vddis switched ON before Vpp, the circuit remains in Tri-State mode until Vpp reaches Vpp threshold.

7 - ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vdd	Logic Supply Range	-0.3,+14	V
Vpp	Driver Supply Range	-0.3 , + 100	V
VIn	Logic Input Voltage Range	-0.3, Vdd+0.3	°C
Ih-Out	Main Switch High Side Current	-5	A
Il-Out	Main Switch Low Side Current	5	A
Ipr-Hi	Power Recovery Current (note1)	-7	A
Ipr-Lo	Power Recovery current (note1)	7	A
$V_{CBoot-Vout}$	Difference between Boot voltage and output voltage	14	V
Tjmax	Maximum Junction Temperature (note2)	Internally protected	°C
Top	Operating Temperature Range	-20, +70	°C
Tstg	Storage Temperature Range	-50, +150	°C

Note 1 Peak current as defined in Figure 1 on page 9

Note 2 These parameters are measured during ST's internal qualification which includes temperature characterization on standard and corner batches of the process. These parameters are not tested on the parts.

Remark: ESD susceptibility
Human body Model: 100pF, 1.5kΩ
Vpp pin (14-15: Multiwatt 15) V_{ESD}= 200V
DM-LH pin (9: Multiwatt 15) V_{ESD}=400V
By connecting a 1nF decoupling capacitor, the circuit withstands V_{ESD}=2.2kV on all pins.

8 - THERMAL DATA

Symbol	Parameter	Value		Unit
		PowerSO20	MW15	
$R_{th(j-a)}$	Junction - Ambient Thermal Resistance	40(note3)	35 (note4)	°C/W
$R_{th(j-c)}$	Junction - Case Thermal Resistance	+0.6, +2.5	-0.6, +2.4	

Note 3 Multilayer PCB.

Note 4 Package floating in the air.

9 - ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, Vdd=12 V, Vpp=90 V, Vsslog=Vssub=0 V, Vssp=0 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
Vdd	Logic Supply Voltage		11	12	13	V
Vpp	Power Output Supply Voltage		20	-	100	V
Idd	Logic Biasing Current without Transition (Stand-by-mode)		-	5	-	mA
Ipp	Power Biasing Current without Transition (Stand-by-mode)		-	6	-	mA
BOOTSTRAPPED SUPPLY VOLTAGE						
$V_{CBoot-Vout}$	Bootstrap supply voltage				12	V
$I_{lkg1Boot}$	Boot leakage current Hiz mode	Hiz mode Vpp=100V, VCBoot-Vout = 10V	-5	0	5	µA
$I_{lkg2Boot}$	Boot leakage current HClmp	HClmp = high Vpp=100V, VCBoot-Vout = 10V	15	30	50	µA
OUTPUTS						
V_{satH}	Output Saturation Voltage (high level) Voltage Drop vs $_{Vpp}$ iH@-1A iH@-3A iH@-4A			 1.5 4.5 6.5		 V V V
V_{satL}	Output Saturation Voltage (low level) iL@1A iL@3A iL@4A			 1.5 4.5 6.5		 V V V
V_{satHL}	Power recirculation - Voltage drop (high to low level) iL@1A iL@3A iL@6A	V_{PR-FPS}=Vpp/2		 0.8 2.5 5		 V V V
V_{satLH}	Power recirculation - Voltage drop (low to high level) iL@-1A iL@-3A iL@-6A	V_{PR-FPS}=Vpp/2		 0.8 2 5		 V V V
PROTECTION						
Tth	Thermal protection temperature threshold		-	170	-	°C
$Vdd_{threshold}$	Power ON threshold voltage on $_{Vdd}$			7.5		V
$Vpp_{threshold}$	Power ON threshold voltage on Vpp			13.3		V
INPUTS						
Vih	Input high level (CMOS compatible)		4		V_{dd}	V
Vil	Input low level (CMOS compatible)				0.9	V
Iih	High level inut current (Vih=$_{Vdd}$)	Vih=Vdd=12V	80	120	150	µA
Iil	Low level input current (Vil=0)		-2	0	+2	µA

10 - AC TIME REQUIREMENTS

(T_{amb} = 25°C, Vdd=12 V, Vpp=90 V, Vsslog=Vssub=0 V, Vssp=0 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{LH}	Low/High transition high level control pulse		10	-	-	ns
t_{HL}	High/Low transition high level control pulse		10	-	-	ns
t_{H}	Duration of high voltage clamp control pulse at high level		10	-	-	ns
tL	Duration of low voltage clamp control pulse at low level		10	-	-	ns
t_{Hsetup}	Set-up time of Vpp voltage clamp after low to high transition		10	-	-	ns
t_{Lsetup}	Set-up time of Vssp voltage clamp after high to low transition		100	-	-	ns
t_{Hhold}	Hold time Vout low before high voltage clamp control pulse		TBD			
t_{Lhold}	Hold time Vout high before low voltage clamp control pulse		TBD			

11 - AC TIMING CHARACTERISTICS

(T_{amb} = 25°C, Vdd=12 V, Vpp=90 V, Vsslog=Vssub=0 V, Vssp=0 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{ON-LH}	Delay of power output change after recirculation low to high transition	Vpp=40V	-	140	-	ns
$t_{ON-HClmp}$	Delay of power output clamp at Vpp after output stage high side ON		-	160	-	ns
t_{ON-HL}	Delay of power output change after recirculation high to low transition		-	140	-	ns
$t_{ON-LClmp}$	Delay of power output clamp at GND after output stage low side ON		-	60	-	ns

12 - AC CHARACTERISTIC WAVEFORMS

Figure 1.

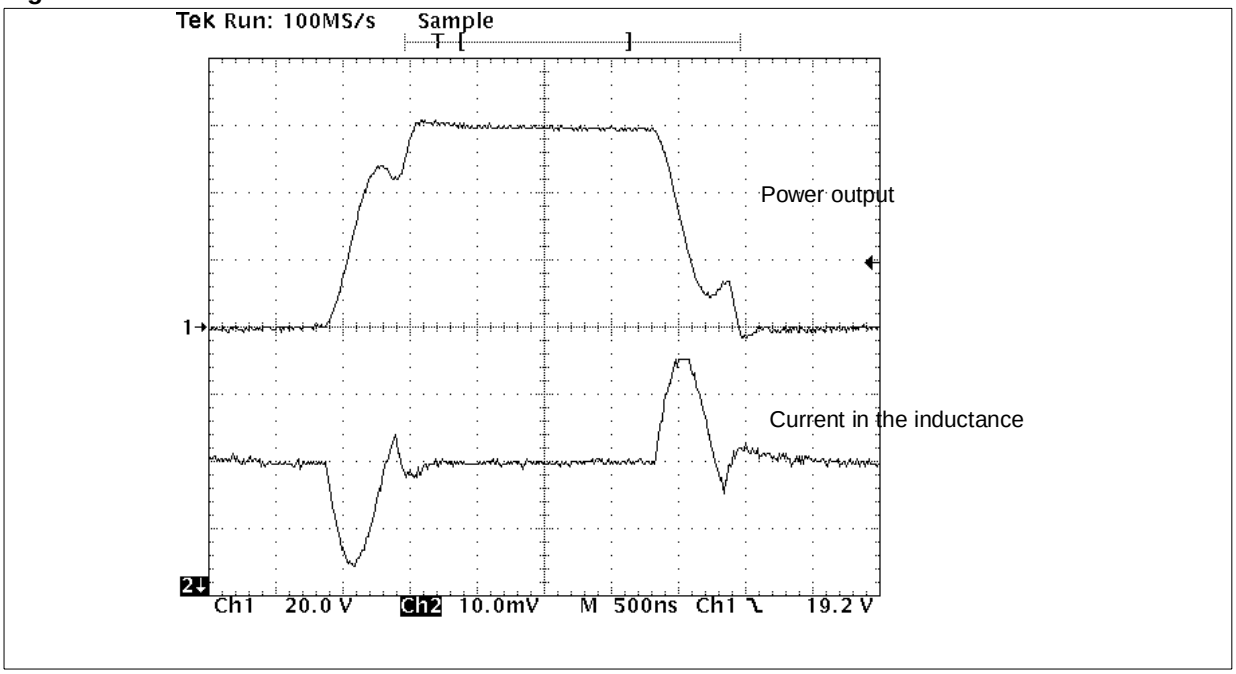


Figure 2.

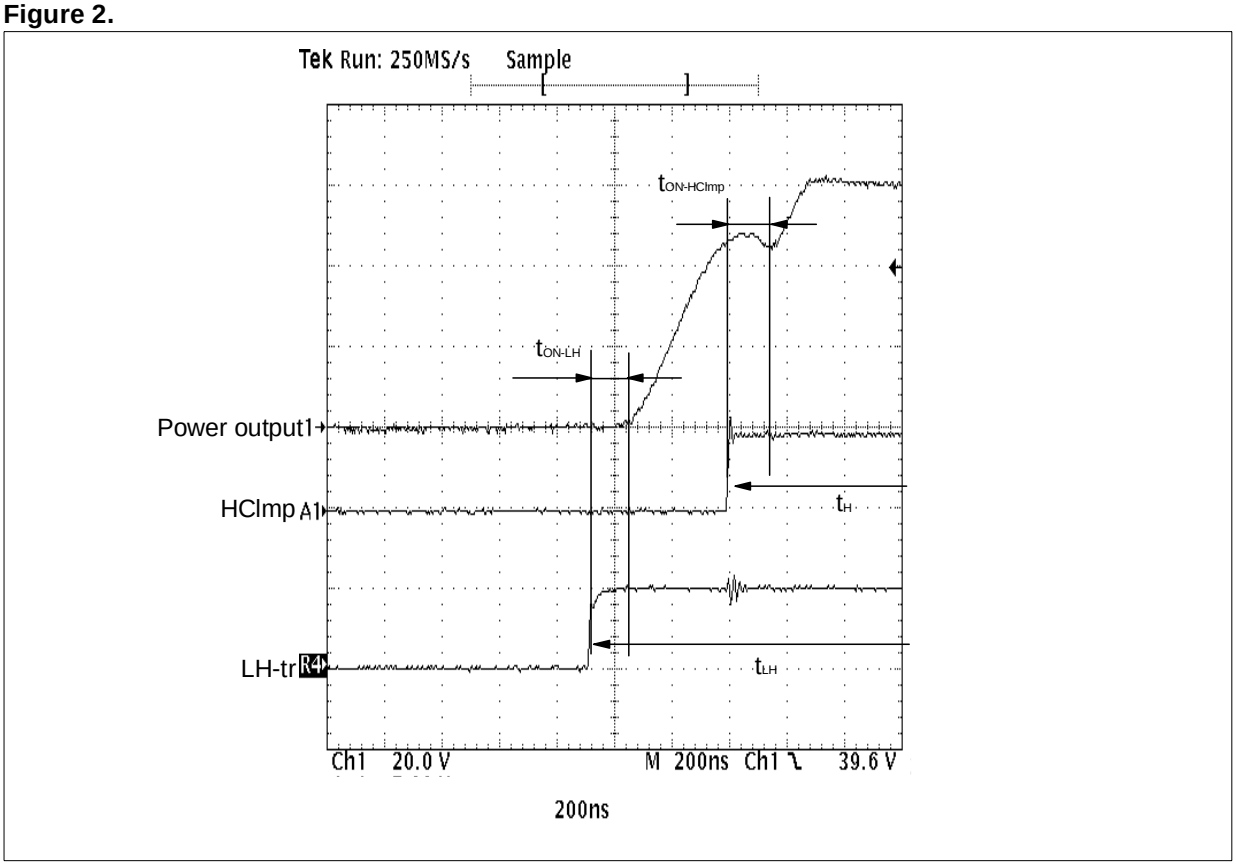
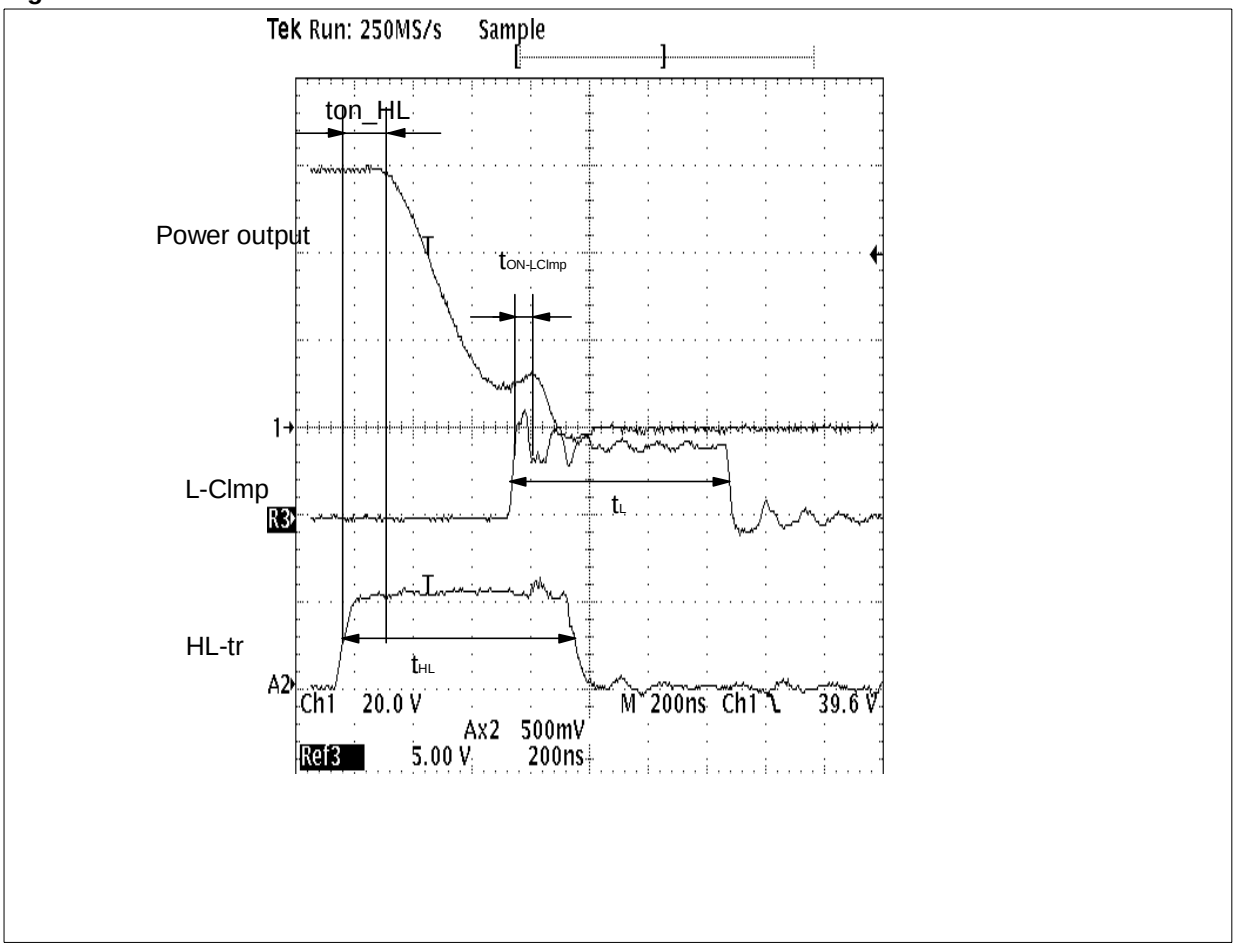
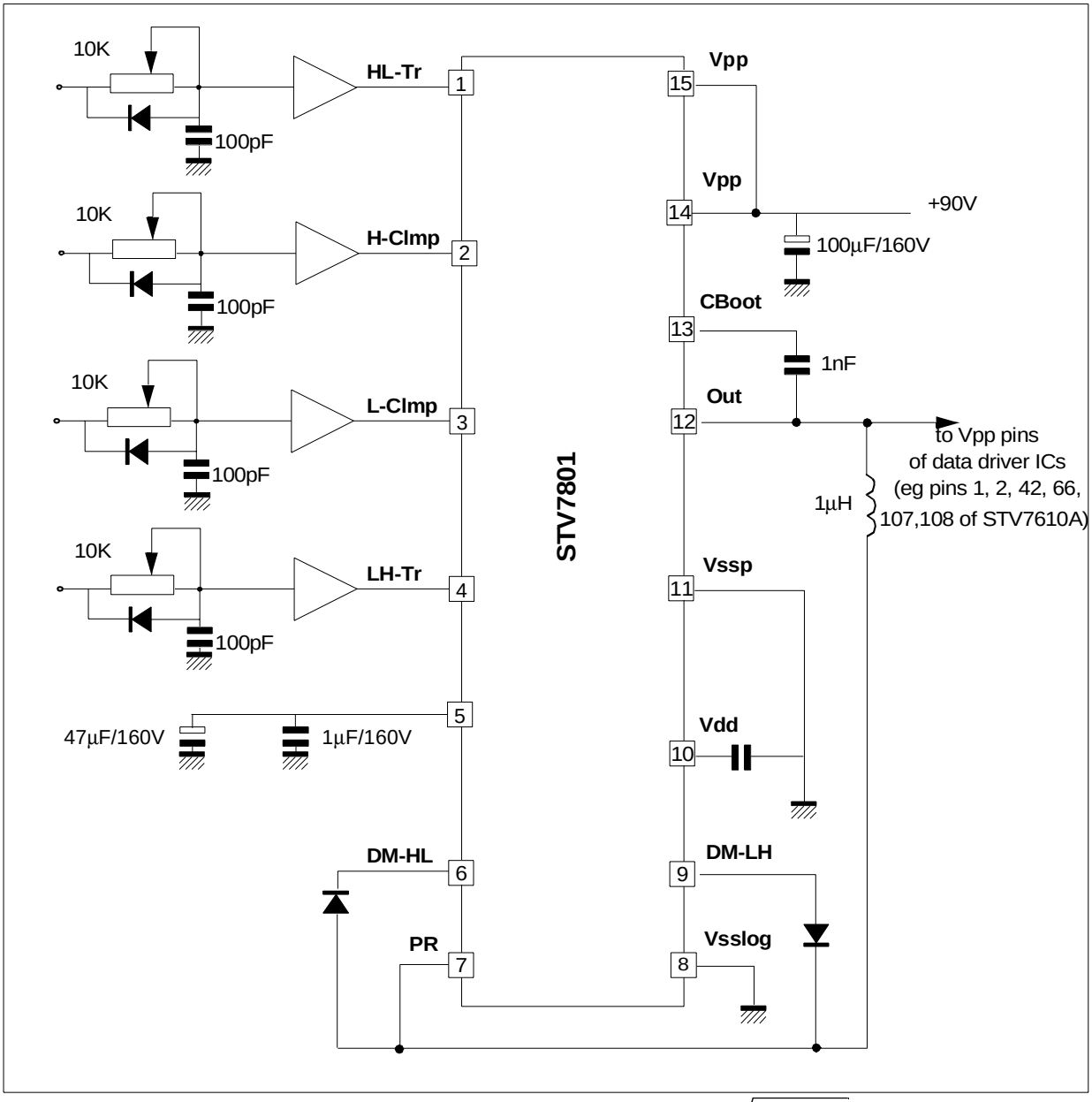


Figure 3.


Tek Run: 250MS/s Sample
ton_HL
Power output
tON-LClmp
1
L-Clmp
R3
tL
HL-tr
tHL
A2
Ch1 20.0 V
Ax2 500mV
M 200ns Ch1 39.6 V
Ref3
5.00 V 200ns

13 - APPLICATION DIAGRAM



The diodes for the recirculation current directly impact the device performances. High Voltage diodes with recovery time inferior to 50ns are recommended. Shorter recovery times will improve the power efficiency of the application.

The rise and fall time of the output signal is adjusted by the value of the inductance for a given capacitive load.

trise (tfall) is calculated by the following formula :

$$t_{rise} = \pi x \sqrt{LxCload}$$

A 1nF bootstrap capacitor is recommended.
The bootstrap capacitor allows the output signal to reach the Vpp value. For a given output level, the power efficiency will be increased.

A 47µF capacitor is recommended. The ripple on the tank capacitor is reduced by increasing the tank capacitor value.

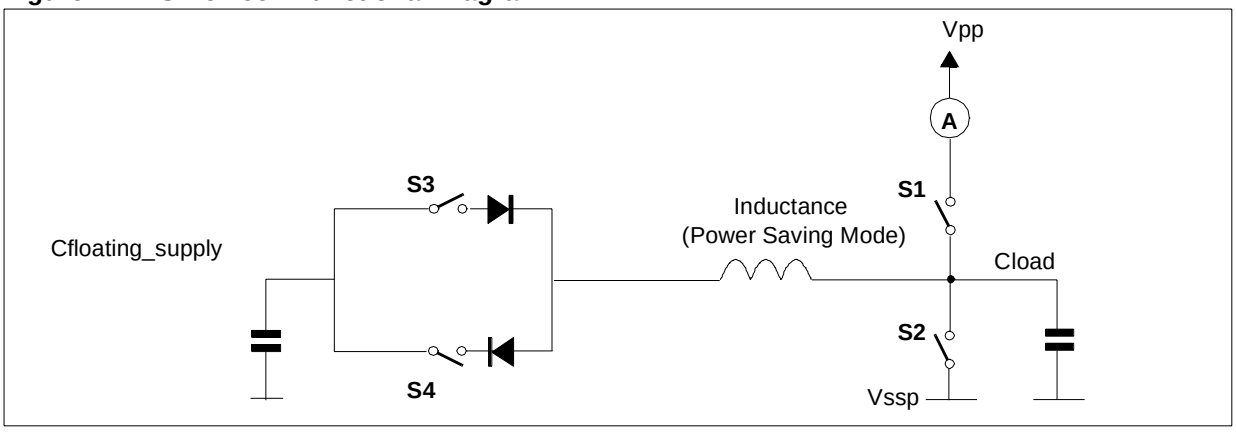
Decoupling capacitors on the power supplies will minimise the overshoots.

The timing of the control signals will be adjusted by the trimmers of the RC cells. It is recommended to enable the clamp signals (H-Clmp, L-Clmp) after the rising (falling) edge of the output signal has reached its maximum (minimum) value.

14 - RECOVERY FACTOR MEASUREMENT CONDITIONS

An idealised schematic of the Power Recovery application is defined below. The inductance (power saving mode) and the 2 capacitors (load, floating_supply) are external components for the D.P.S. device.

Figure 4. DPS Device : Functional Diagram



The Power Recovery Factor (PRF) in % is given by the formula :

$$PRF = 100 \times (Pc - Pr) / Pc.$$

– Pc is the theoretical capacitive power dissipated in the switches S1, S2 of the Data Power Switch device when S3, S4 are not activated. Pc is calculated by the formula :

$$P_C = Cload \times Vpp^2 xF$$

with F=switching frequency.

Cload = equivalent panel capacitance

– Pr is the power dissipated in the Data Power Switch device when it is configured in a power recovery mode (S1, S2, S3, S4 activated). Pr is calculated by multiplying the average current given by the current sensor A and the value of the supply voltage Vpp.

PRF is affected by the external components of the DPS device such as the inductance and the decoupling capacitors, also the layout of the application.

15 - RESULTS OF POWER EFFICIENCY

15.1 Power recovery factor for different inductance values

Figure 5. STV7801- Power Recovery Factor, L=1.1µH, T=3.3µs, BYW80-200 diodes

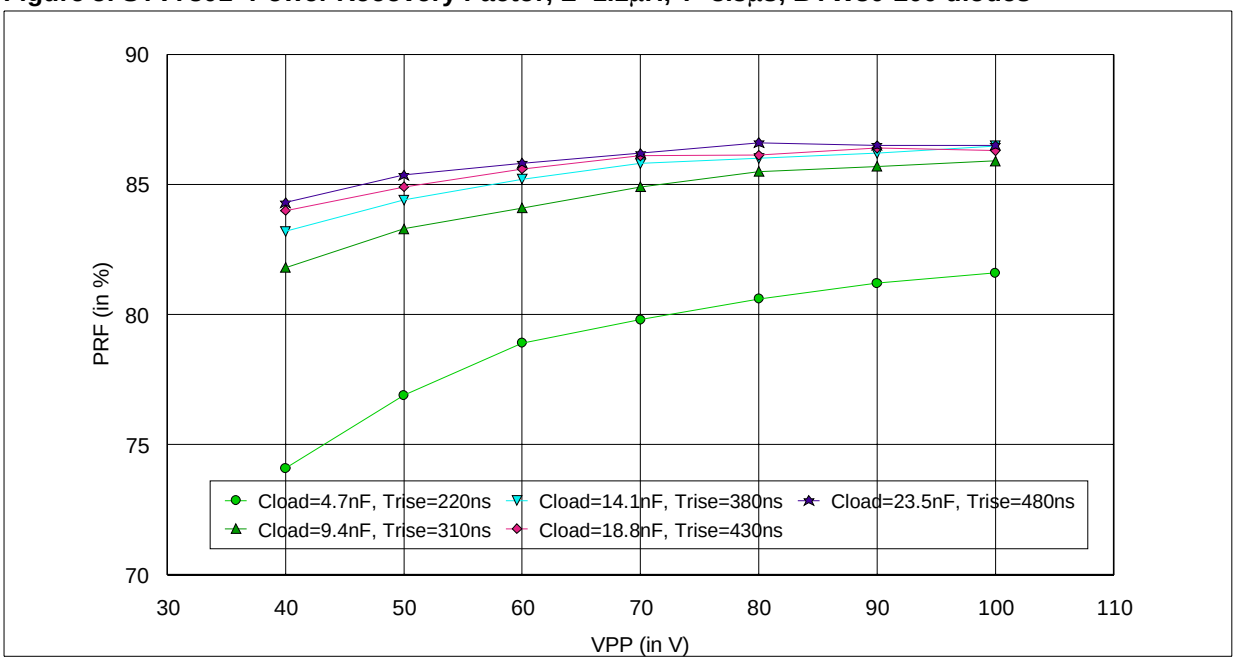


Figure 6. STV7801- Power Recovery Factor. L=0.66µH, T=3.3µs, BYW80-200 diodes

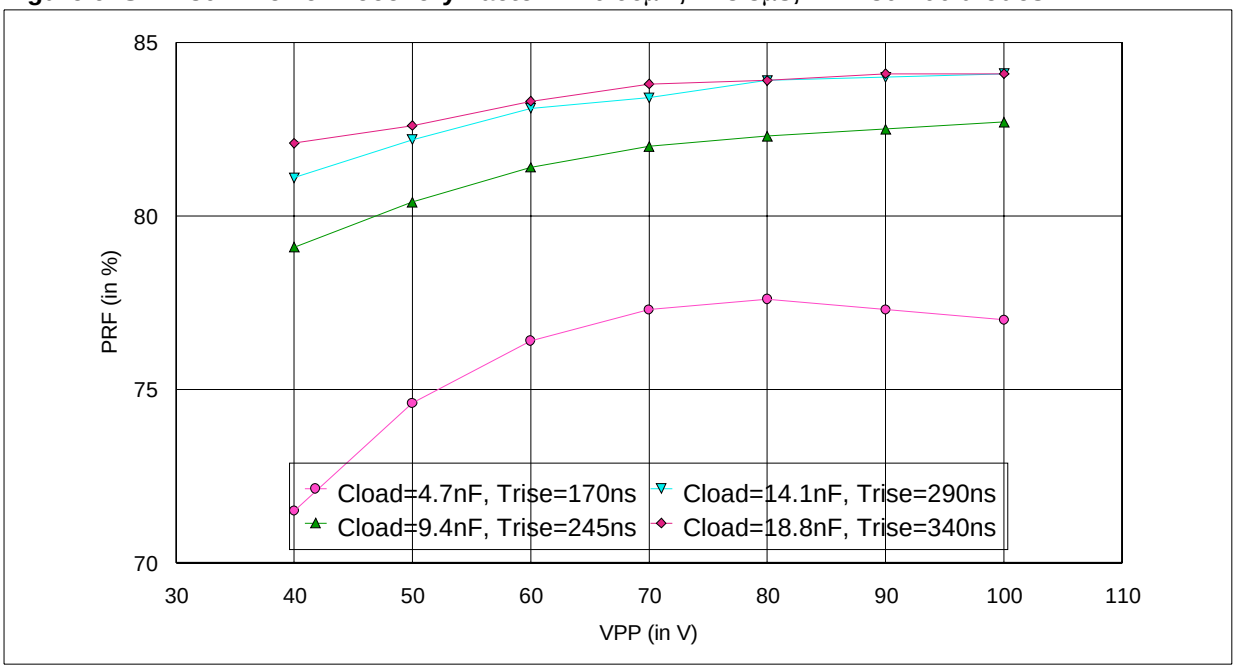
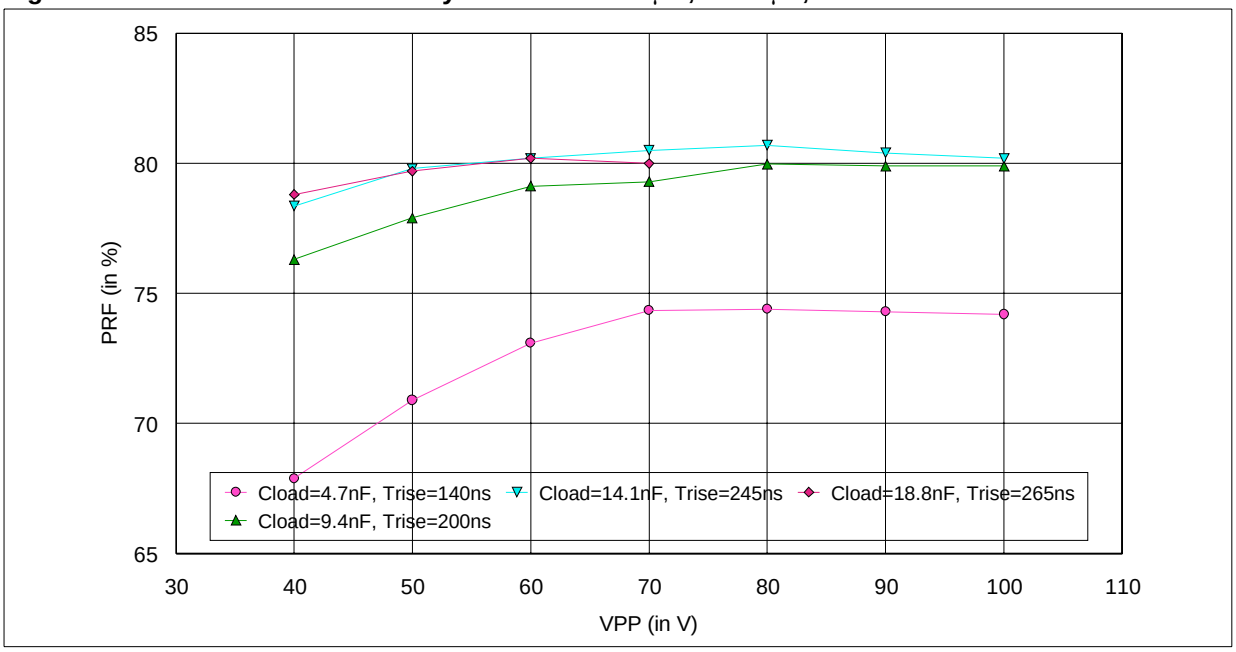
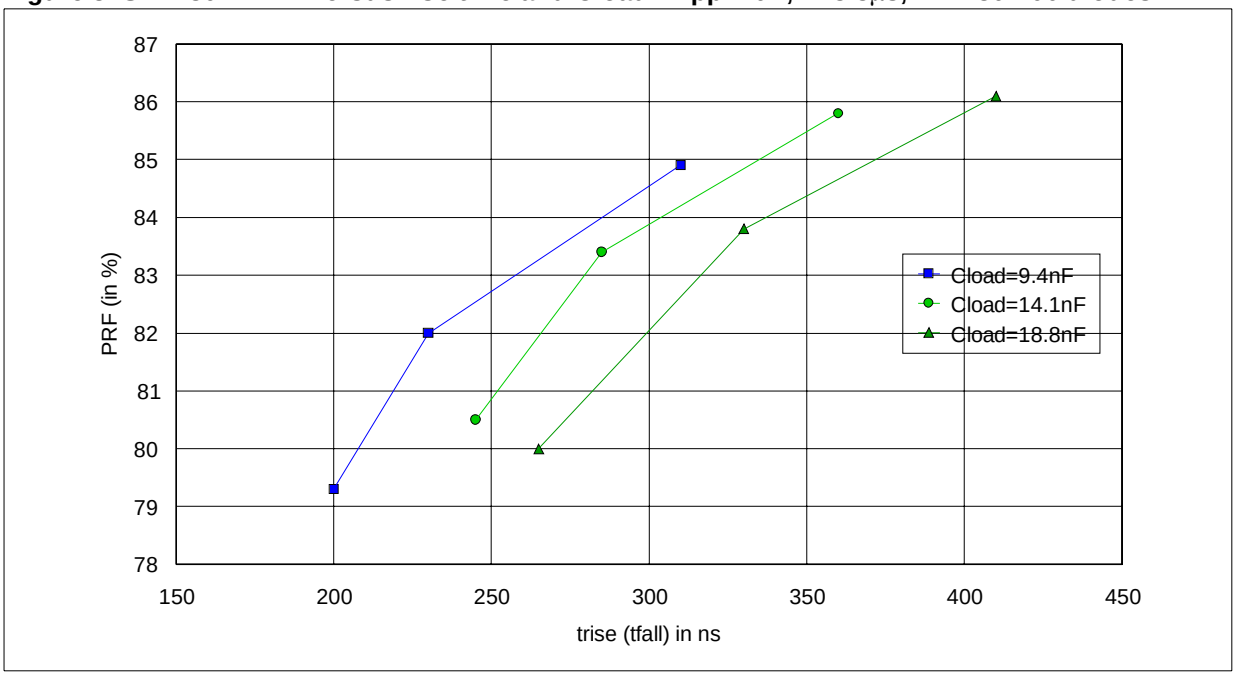


Figure 7. STV7801- Power Recovery Factor - L=0.36µH, T=3.3µs, BYW80-200 diodes



15.2 Power recovery factor (PRF) versus time and Cload

Figure 8. STV7801- PRF versus rise time and Cload - Vpp=70V, T=3.3µs, BYW80-200 diodes



15.3 Power recovery factor (PRF) for fixed rise (fall) time

Figure 9. PRF versus Cload and L values - Trise (fall) = 260ns, T=3.3µs, BYW 80-200 diodes

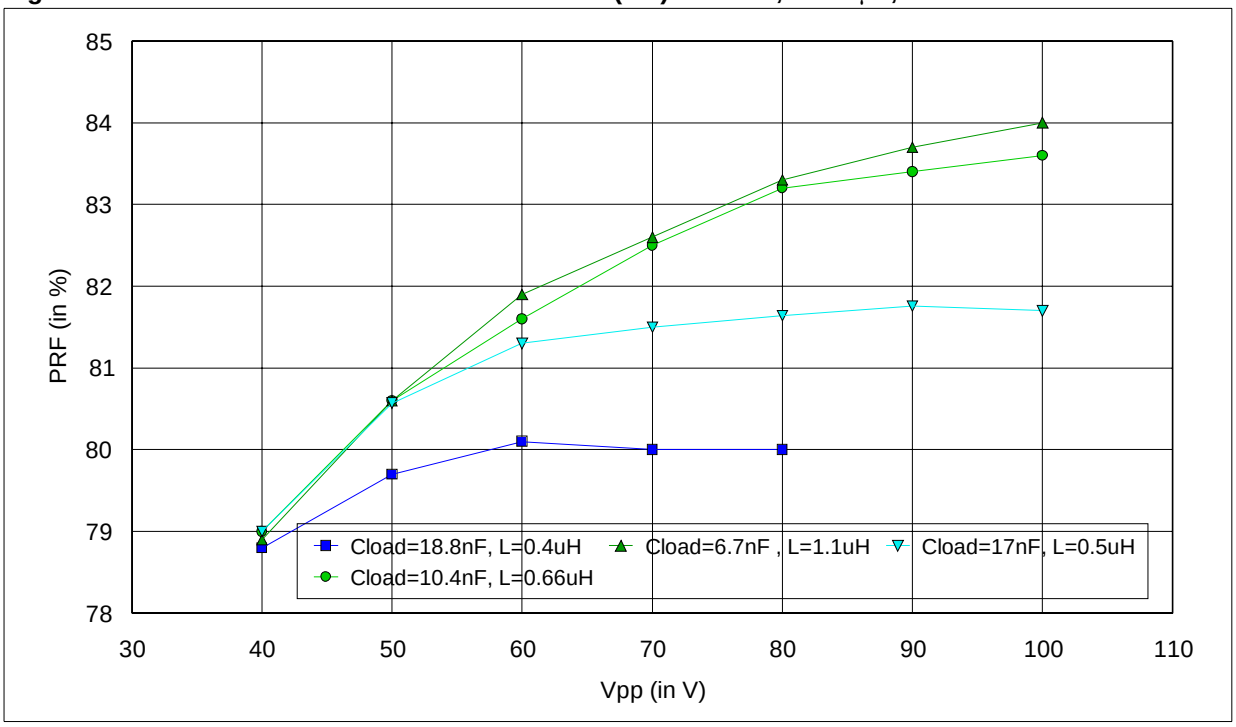
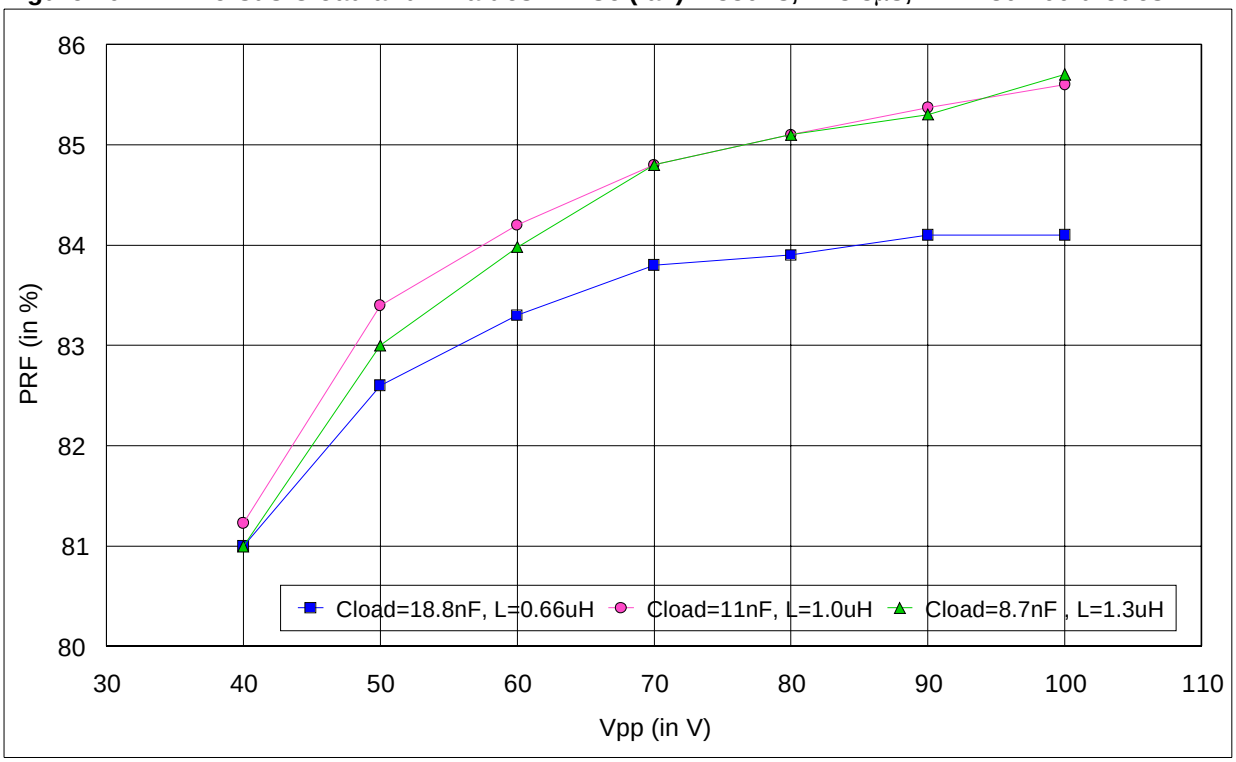
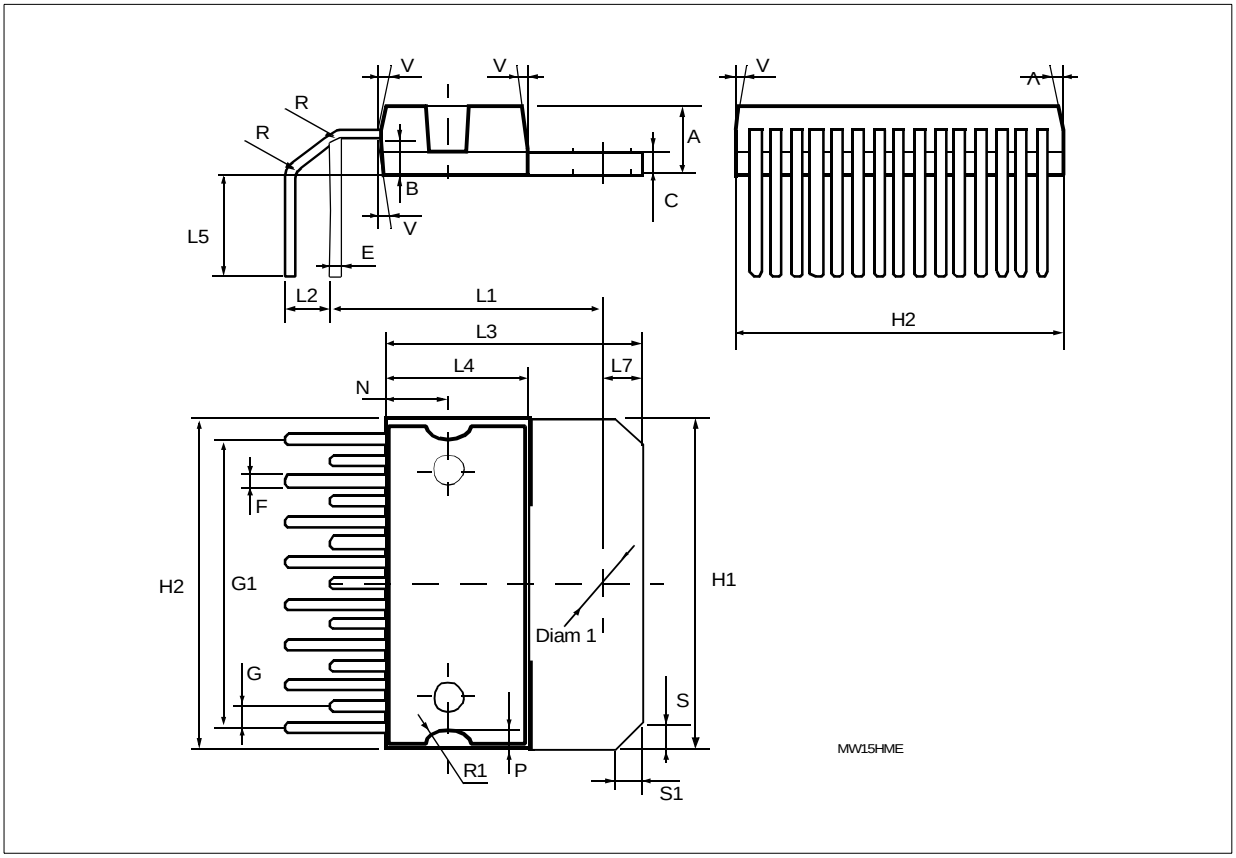


Figure 10. PRF versus Cload and L values - Trise (fall) = 330ns, T=3.3µs, BYW 80-200 diodes



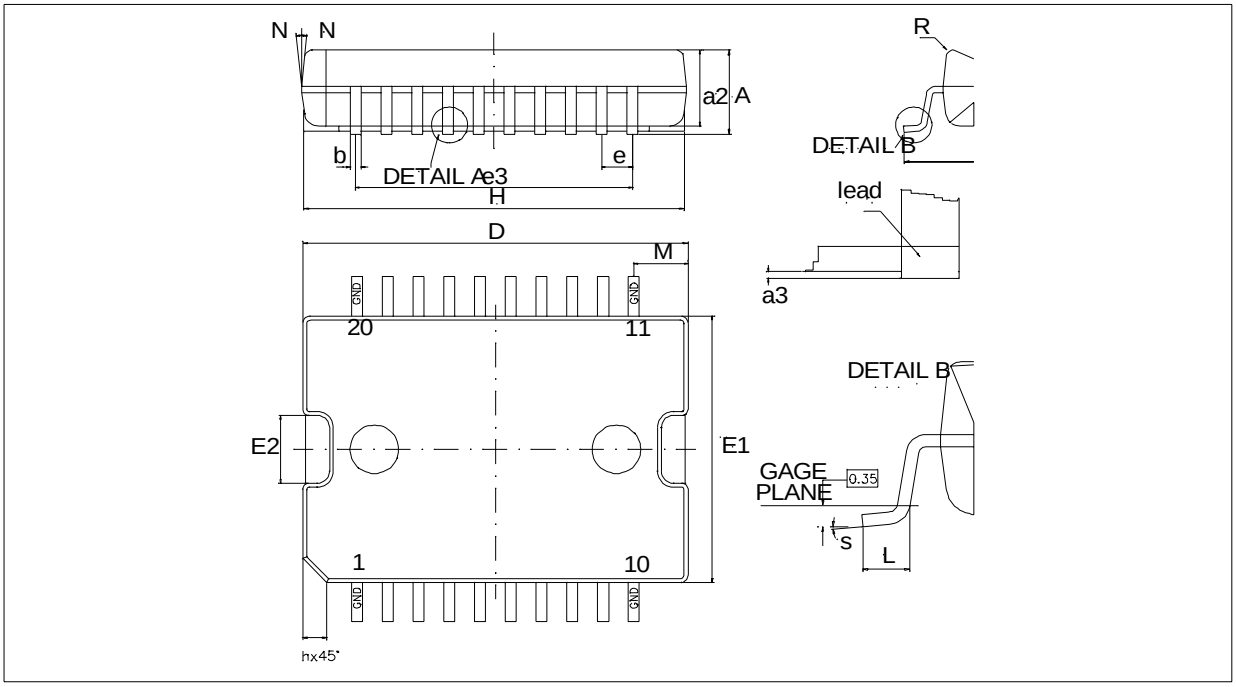
16 - PACKAGE MECHANICAL DATA

Multiwatt 15 horizontal, shortleads



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.709
H1	19.6		20.2	0.772		0.795
H2	19.6		20.2	0.772		0.795
L1	17.8	18	18.2	0.701	0.709	0.717
L2	2.3	2.5	2.8	0.091	0.098	0.110
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5	2.7	3	3.3	0.106	0.118	0.130
L7	2.65		2.9	0.104		0.114
R		1.5			0.059	
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

PowerSO20



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.50			0.138
a1	0.20		0.275	0.008		0.011
a2	3.10		3.20	0.122		0.126
a3	0		0.075	0		0.003
b	0.42		0.50	0.0165		0.020
c	0.24		0.28	0.009		0.011
D(1)	15.85		15.95	0.624		0.628
D1	9.45		9.75	0.372		0.384
E	14.10	14.20	14.35	0.555	0.559	0.565
e		1.27			0.050	
e3		11.43			0.450	
E1(1)	10.85		11.05	0.431		0.435
E2			2.85			0.112
E3	5.85		6.15	0.230		0.242
G	0		0.075	0		0.003
H	15.55		15.85	0.612		0.624
h					0.039	
L	0.85		1.05	0.033		0.041
M	2.10		2.30	0.083		0.090
N			9d.			9d.
R		0.30			0.012	
S	3d.	5d.	7d.	3d.	5d.	7d.
T		10.00			0.394	

Note 5 “D” and “E1” do not include mold flash or protrusions
-Mold flash or protrusions shall not exceed 0.15mm (0.006inc.)
-Critical dimensions: “E”, “G” and “a3”