

# 1

## PRODUCT OVERVIEW

### S3C8-SERIES MICROCONTROLLERS

Samsung's S3C8 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode release by interrupt
- Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

### S3C80F7/C80F9/C80G7/C80G9 Microcontroller

The S3C80F7/C80F9/C80G7/C80G9 single-chip CMOS microcontroller is fabricated using a highly advanced CMOS process and is based on Samsung's newest CPU architecture.

The S3C80F9/C80G9 is the microcontroller which has 32-Kbyte mask-programmable ROM and S3C80F7/C80G7 is the microcontroller which has 24-Kbyte mask-programmable ROM.

The S3P80F9/P80G9 is the microcontroller which has 32-Kbyte one-time-programmable EPROM and S3P80F7/P80G7 is the microcontroller which has 24-Kbyte one-time-programmable EPROM.

Using a proven modular design approach, Samsung engineers developed S3C80F7/C80F9/C80G7/C80G9 by integrating the following peripheral modules with the powerful SAM87 RC core:

- Internal LVD circuit and 16 bit-programmable pins for external interrupts.
- One 8-bit basic timer for oscillation stabilization and watchdog function (system reset).
- One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.
- One 8-bit counter with auto-reload function and one-shot or repeat control.

The S3C80F7/C80F9/C80G7/C80G9 is a versatile general-purpose microcontroller which is especially suitable for use as remote transmitter controller. It is currently available in a 32-pin SOP, 42-pin SDIP and 44-pin QFP package.

## FEATURES

### CPU

- SAM87RC CPU core

### Memory

- 32-Kbyte internal ROM (S3C80F9/C80G9)  
: 0000H–7FFFH
- 24-Kbyte internal ROM (S3C80F7/C80G7)  
: 0000H–5FFFH
- Data memory: 272-byte RAM (318 register)

### Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

### Instruction Execution Time

- 500 ns at 8-MHz  $f_{OSC}$  (minimum)

### Interrupts

- 22 interrupt sources with 16 vector and 7 level.

### I/O Ports

- Three 8-bit I/O ports (P0–P2), one 8-bit output port(P4) and 6-bit port (P3) for a total of 38 bit-programmable pins.(44-QFP)
- Three 8-bit I/O ports (P0–P2), one 8-bit output port(P4) and 4-bit port (P3) for a total of 36 bit-programmable pins.(42-SDIP)
- Three 8-bit I/O ports (P0–P2) and one 2-bit I/O port (P3) for a total of 26-bit programmable pins.(32-SOP)

### Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function
- One 8-bit timer/counter (Timer 0) with three operating modes; Interval mode, Capture and PWM mode.
- One 16-bit timer/counter (Timer1) with two operating modes; Interval mode and Capture.

### Carrier Frequency Generator

- One 8-bit counter with auto-reload function and one-shot or repeat control (Counter A)

### Back-up mode

- When  $V_{DD}$  is lower than  $V_{LVD}$ , the chip enters Back-up mode to block oscillation and reduce the current consumption.  
In S3C80G7/C80G9, this function is disabled when operating state is "STOP mode".
- When RESET pin is lower than Input Low Voltage ( $V_{IL}$ ), the chip enters Back-up mode to block oscillation and reduce the current consumption.

### Low Voltage Detect Circuit

- Low voltage detect to get into Back-up mode.
- Low level detect voltage
  - S3C80F7/C80F9: 2.20 V (Typ)  $\pm$  200mV
  - S3C80G7/C80G9: 1.90 V (Typ)  $\pm$  200mV

### Operating Temperature Range

- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### Operating Voltage Range

- 1.7V to 5.0V at 4 MHz  $f_{OSC}$  (S3C80G7/C80G9)
- 2.0V to 5.0V at 8 MHz  $f_{OSC}$  (S3C80F7/C80F9)

### Package Type

- 44-pin QFP-1010B
- 42-pin SDIP
- 32-pin SOP

**BLOCK DIAGRAM**

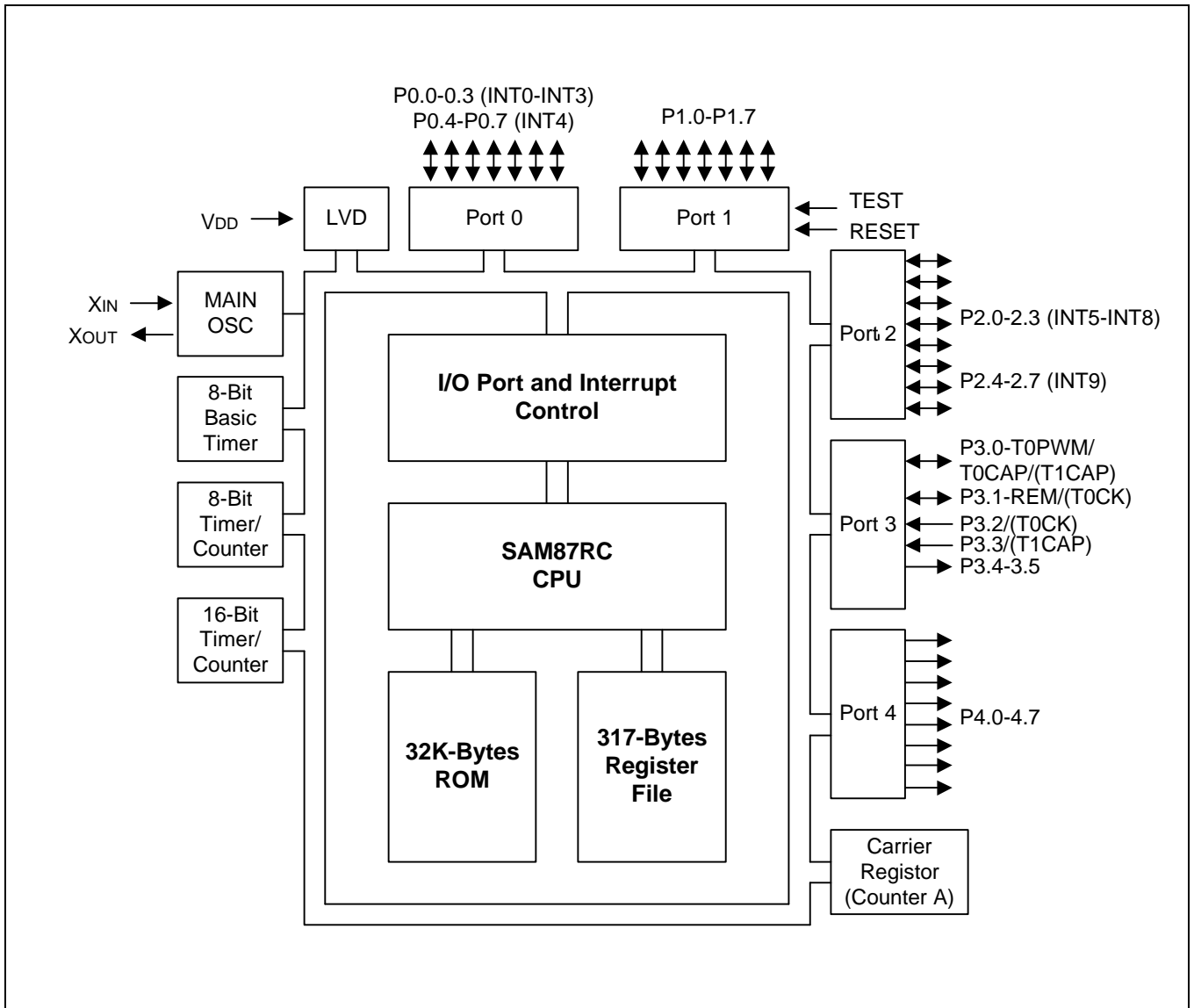


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

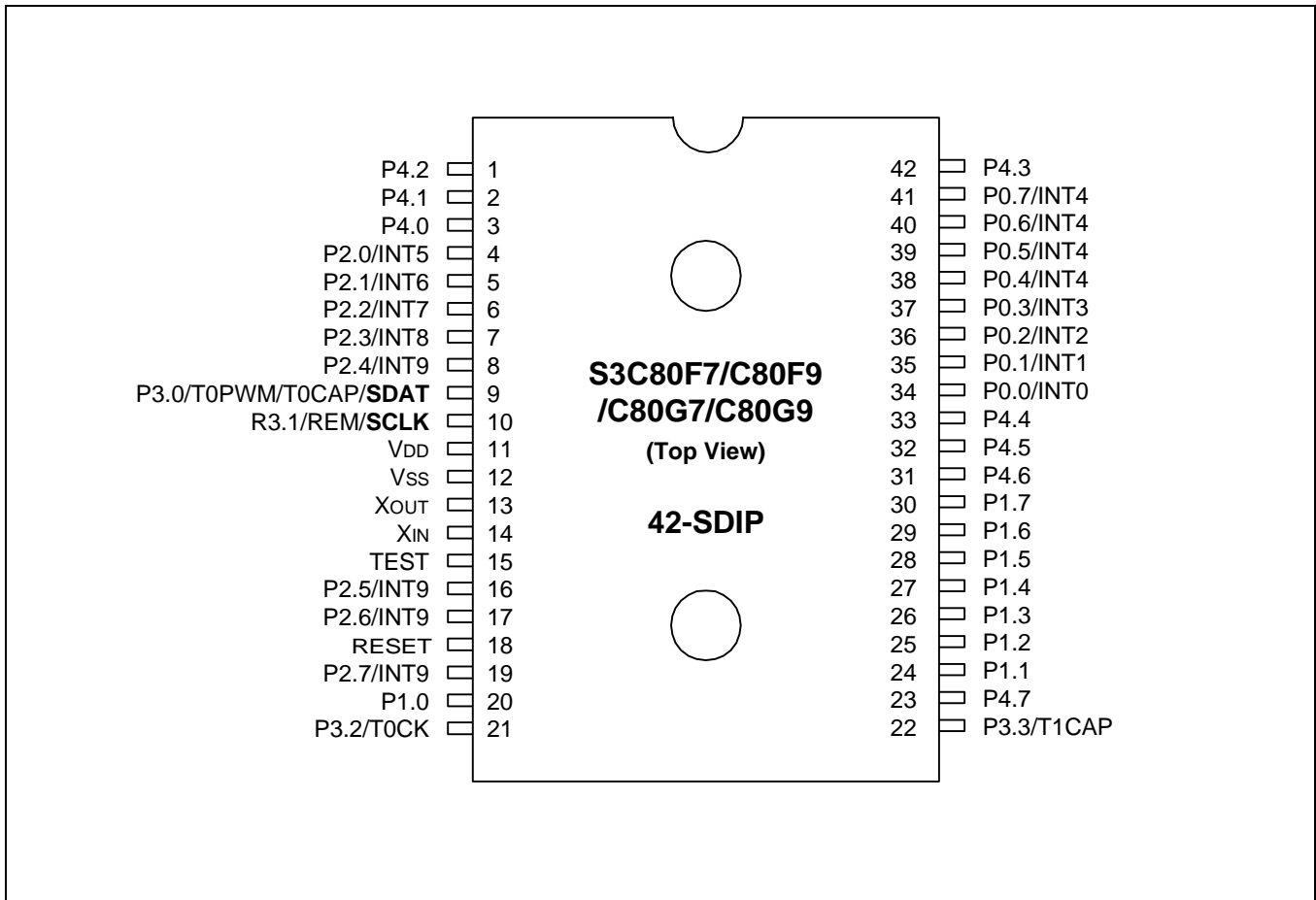


Figure 1-2. Pin Assignment Diagram (42-Pin SDIP Package)

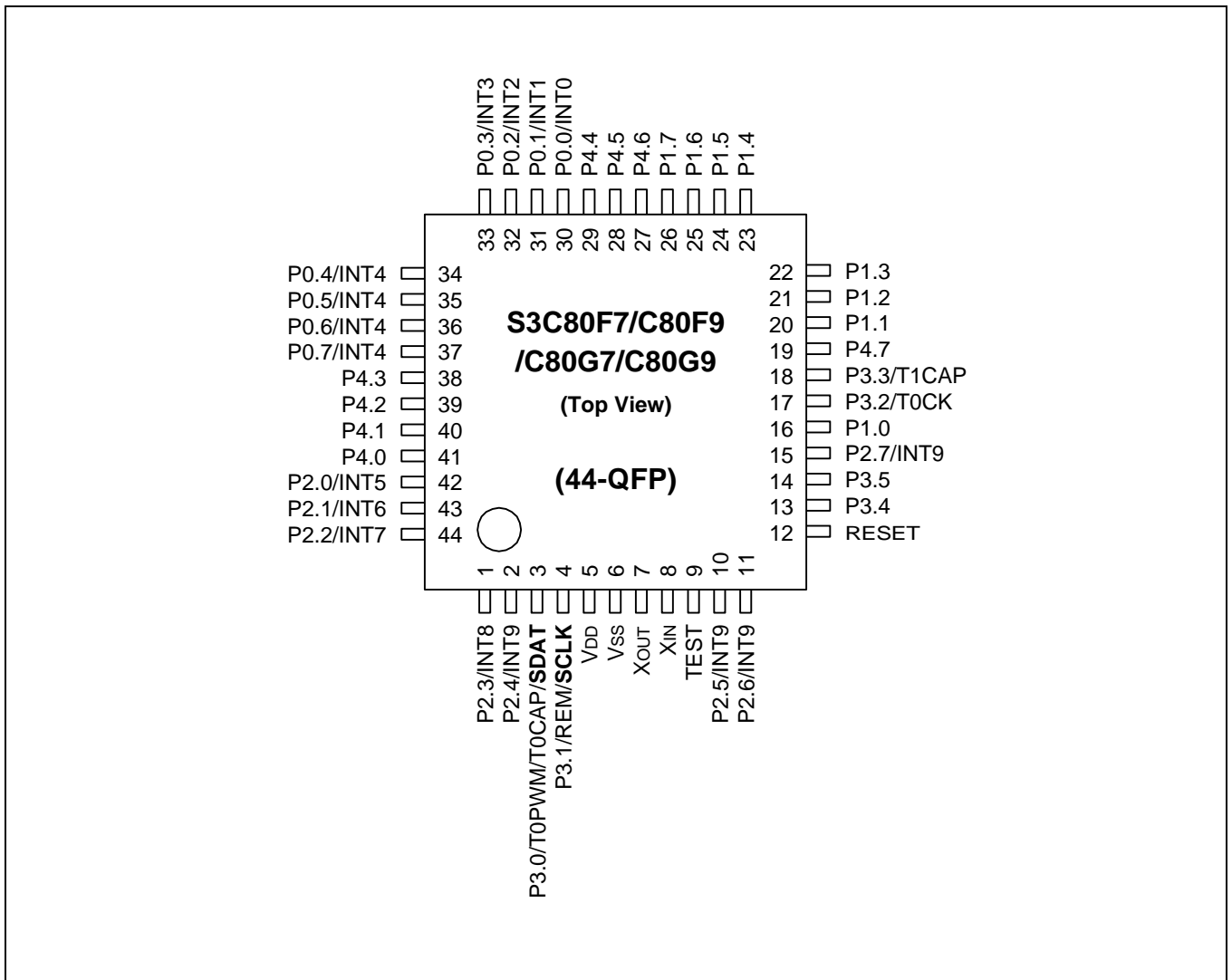


Figure 1-3. Pin Assignment Diagram (44-Pin QFP Package)

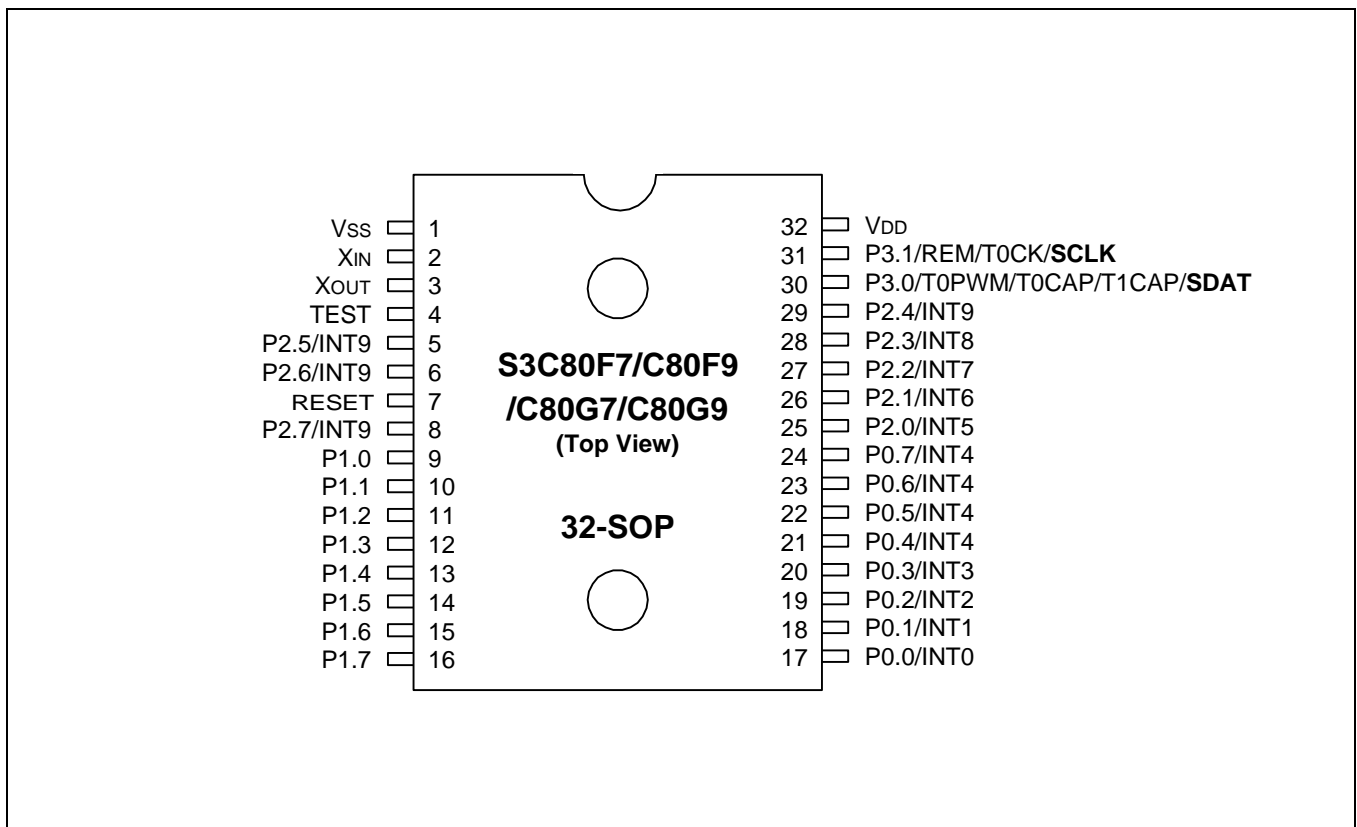


Figure 1-4. Pin Assignment Diagram (32-Pin SOP Package)

Table 1-1. Pin Descriptions of 44-QFP and 42-SDIP

Pin Names	Pin Type	Pin Description	Circuit Type	42 Pin No.	44 Pin No.	Shared Functions
P0.0–P0.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors can be assigned by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control. SED & R circuit built in P0 for STOP releasing.	1	34–41	30–37	Ext. INT (INT0 - 4)
P1.0–P1.7	I/O	I/O port with bit-programmable pins. Configurable to input mode or output mode. Pin circuits are either push-pull or n-channel open-drain type.	2	20 24–30	16 20–26	–
P2.0–P2.3 P2.4–P2.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors can be assigned by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control. SED & R circuit built in P2 for STOP releasing.	1	4–8, 16, 17 19	42–44 1,2, 10,11, 15	Ext. INT (INT5–9)
P3.0 P3.1	I/O	2-bit I/O port with bit-programmable pins. Configurable to input mode, push-pull output mode, or n-channel open-drain output mode. Input mode with pull-up resistors can be assigned by software. The two port 3 pins have high current drive capability	3 4	9–10	3–4	T0PWM/ T0CAP REM
P3.2–P3.3	I	C-MOS Input port with pull-up resistors	5	21 22	17 18	(T0CK) (T1CAP)
P3.4–P3.5	O	Open drain output port for high current drive	6	None	13–14	–
P4.0–P4.7	O	8-bit-programmable output pins. Configurable to open drain output port or push-pull output port.	7	1–3 42,23 31-33	41–38 27–29 19	–
X <sub>IN</sub> , X <sub>OUT</sub>	–	System clock input and output pins	–	13,14	7,8	–
RESET	I	System reset signal input pin and back-up mode input.	8	18	12	–
TEST	I	Test signal input pin (for factory use only; must be connected to V <sub>SS</sub> .)	–	15	9	–
V <sub>DD</sub>	–	Power supply input pin	–	11	5	–
V <sub>SS</sub>	–	Ground pin	–	12	6	–

Table 1-2. Pin Descriptions of 32-SOP

Pin Names	Pin Type	Pin Description	Circuit Type	32 Pin No.	Shared Functions
P0.0–P0.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors are assignable by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/ disable, and interrupt pending control. SED & R circuit built in P0 for STOP releasing.	1	17–24	Ext. INT
P1.0–P1.7	I/O	I/O port with bit-programmable pins. Configurable to input mode or output mode. Pin circuits are either push-pull or n-channel open-drain type.	2	9–16	–
P2.0–P2.3 P2.4–P2.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors can be assigned by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control. SED & R circuit built in P2 for STOP releasing.	1	25–28 29,5, 6,8	Ext. INT
P3.0 P3.1	I/O	2-bit I/O port with bit-programmable pins. Configurable to input mode, push-pull output mode, or n-channel open-drain output mode. Input mode with pull-up resistors can be assigned by software. The two port 3 pins have high current drive capability.	3 4	30,31	T0PWM/ T0CAP/T1CAP REM/T0CK
X <sub>IN</sub> , X <sub>OUT</sub>	–	System clock input and output pins	–	2,3	–
RESET	I	System reset signal input pin and back-up mode input.	8	7	–
TEST	I	Test signal input pin (for factory use only; must be connected to V <sub>SS</sub> ).	–	4	–
V <sub>DD</sub>	–	Power supply input pin	–	32	–
V <sub>SS</sub>	–	Ground pin	–	1	–



PIN CIRCUITS

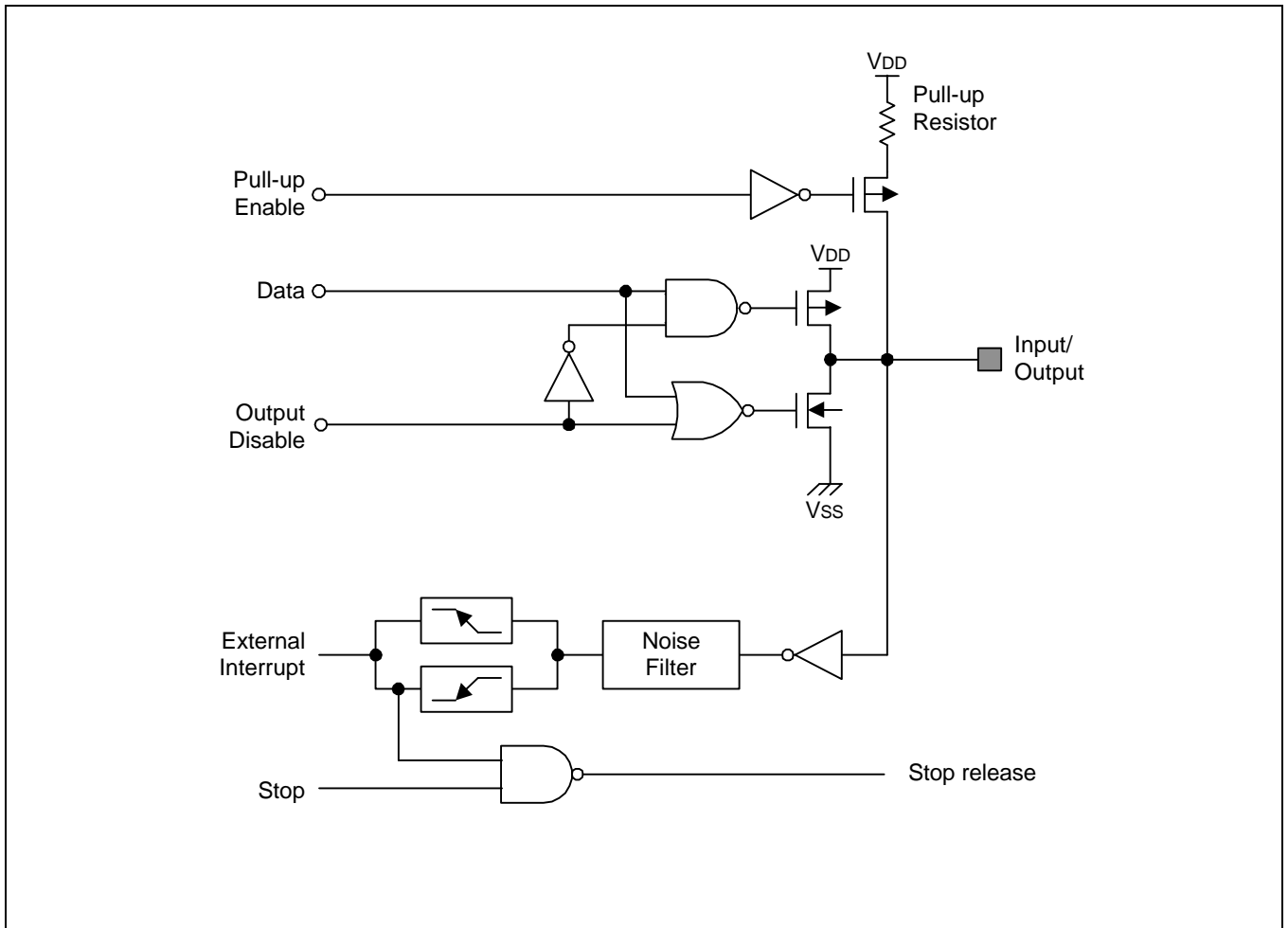


Figure 1-5. Pin Circuit Type 1 (Port 0 and Port2)

PIN CIRCUITS (Continued)

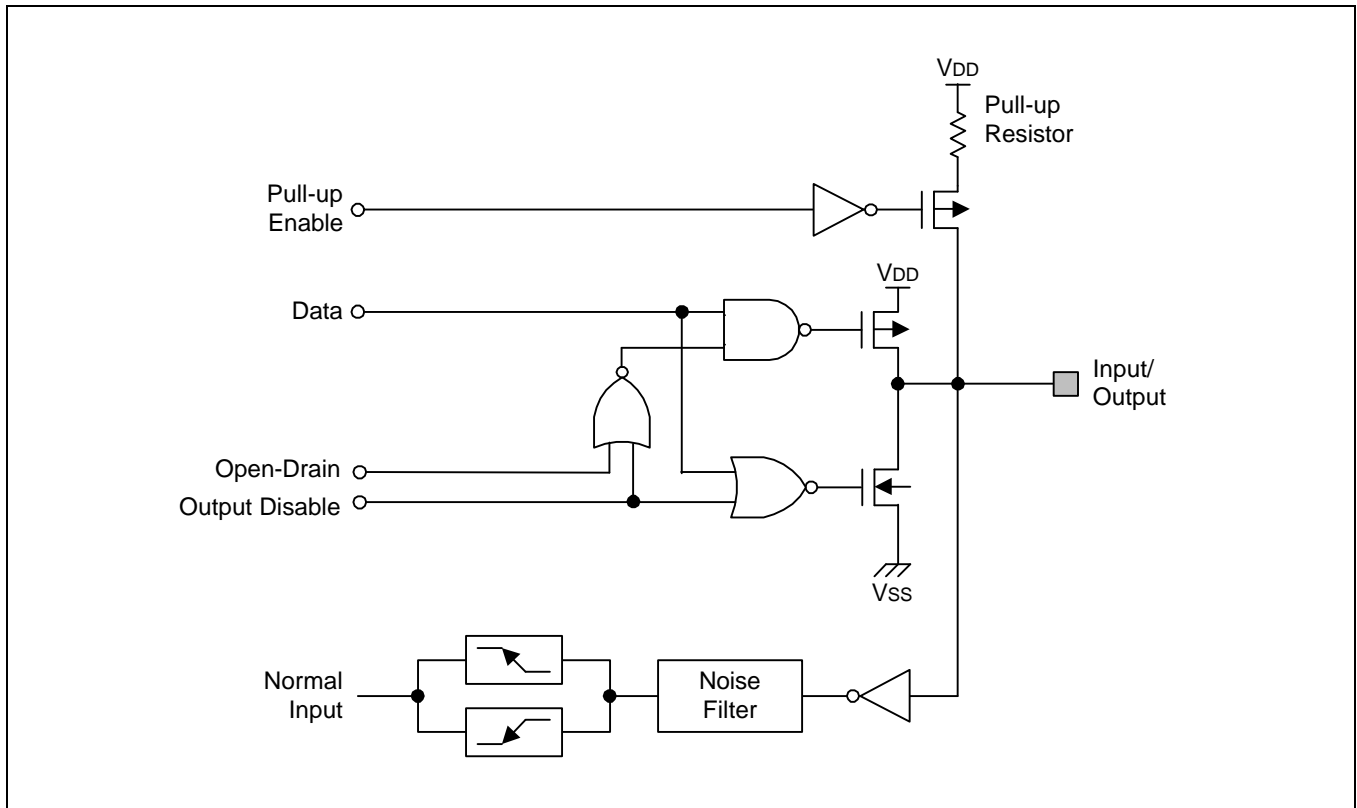
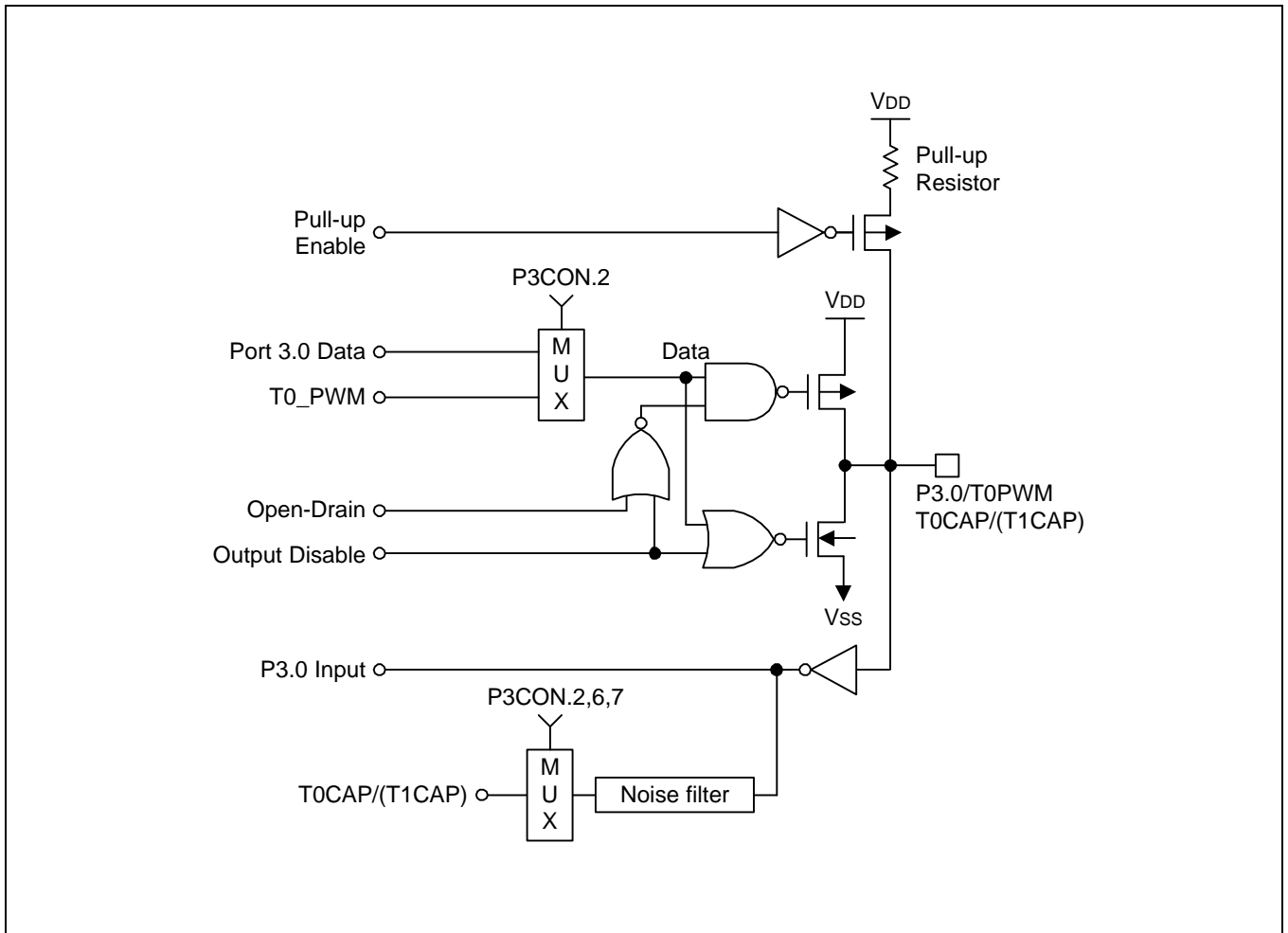


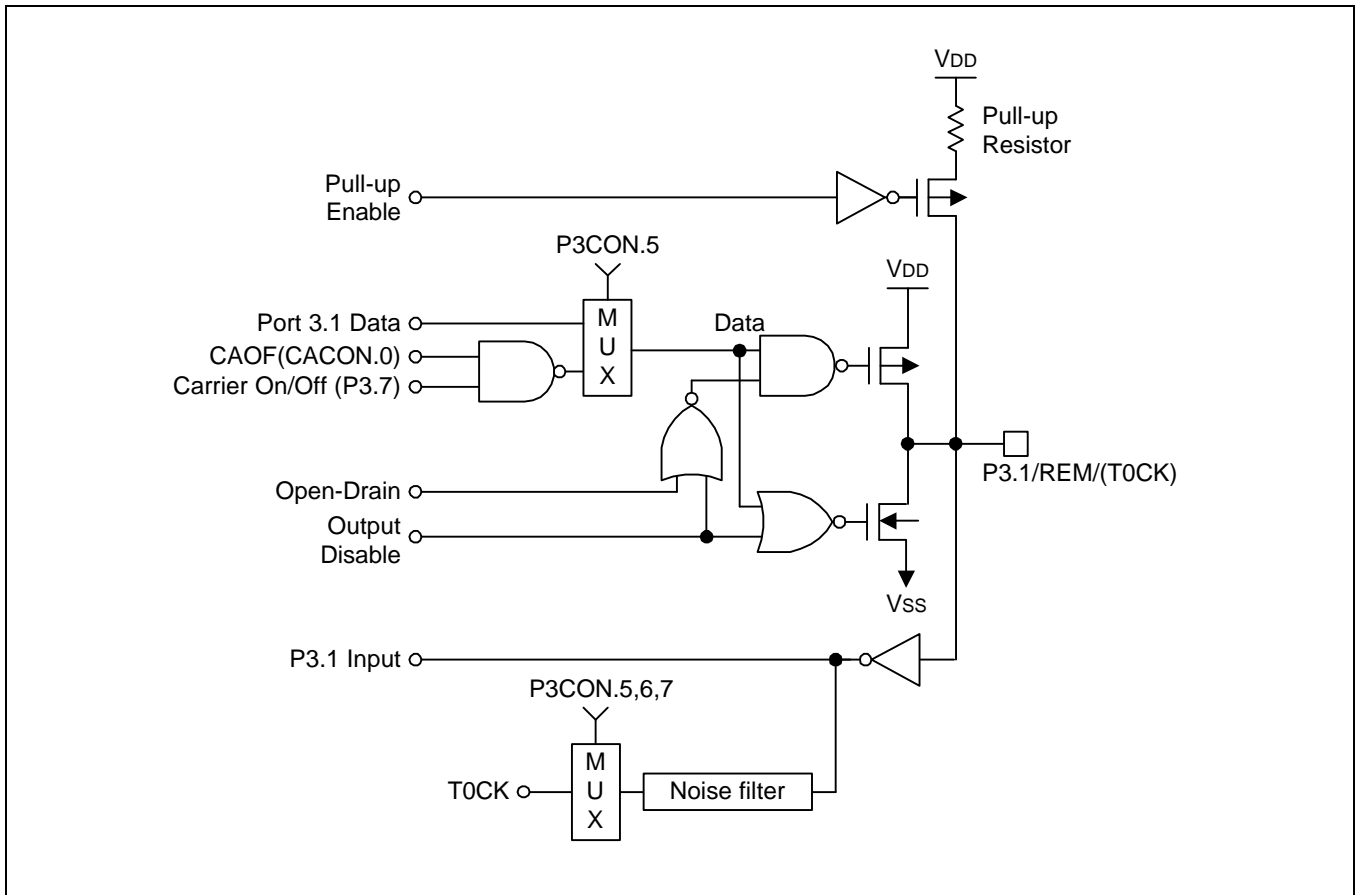
Figure 1-6. Pin Circuit Type 2 (Port 1)

**PIN CIRCUITS (Continued)**

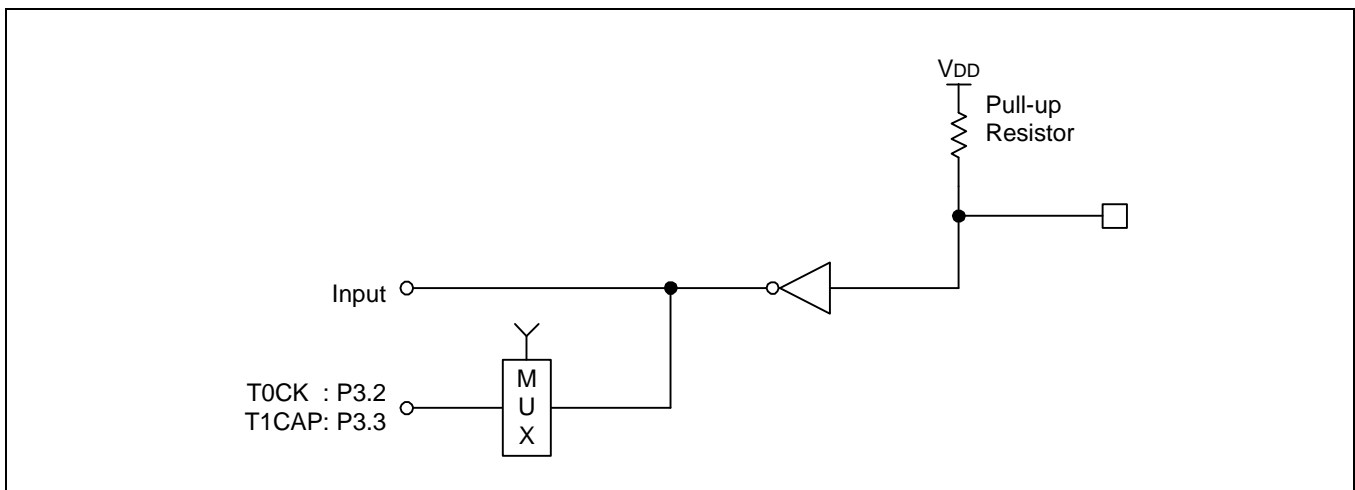


**Figure 1-7. Pin Circuit Type 3 (P3.0)**

**PIN CIRCUITS (Continued)**

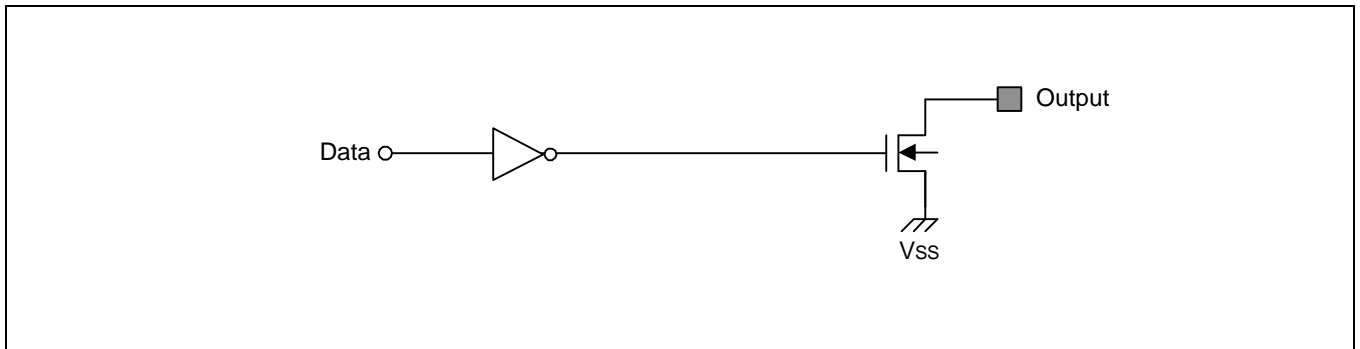


**Figure 1-8. Pin Circuit Type 4 (P3.1) Circuit**

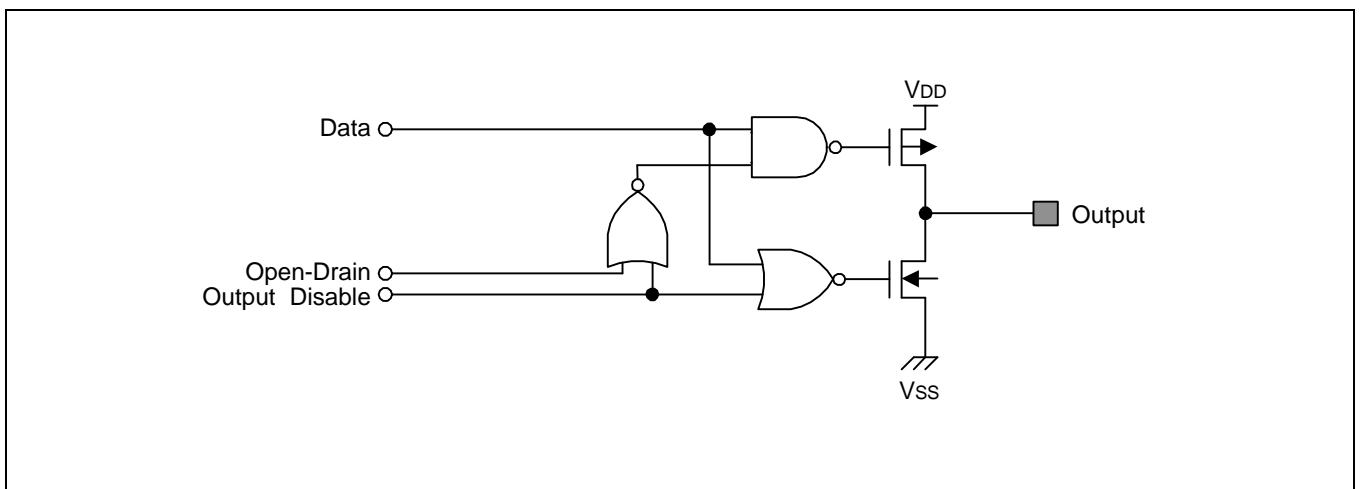


**Figure 1-9. Pin Circuit Type 5 (P3.2, P3.3)**

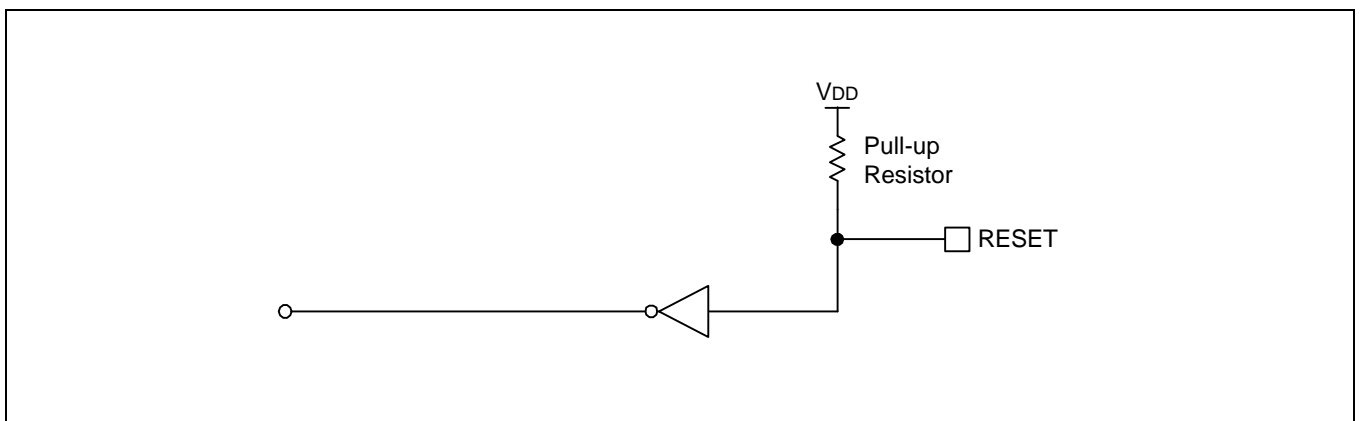
**PIN CIRCUITS (Continued)**



**Figure 1-10. Pin Circuit type 6 (P3.4, P3.5)**



**Figure 1-11. Pin Circuit type 7 (Port 4)**



**Figure 1-12. Pin Circuit type 8 (RESET)**

# 14 ELECTRICAL DATA 1 (S3C80F7/C80F9)

## OVERVIEW

In this section, S3C80F7/C80F9 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by an external interrupt
- Stop mode release timing when initiated by a Reset
- I/O capacitance
- A.C. electrical characteristics
- Input timing for external interrupts
- Input timing for RESET
- Oscillation characteristics
- Oscillation stabilization time

Table 14-1. Absolute Maximum Ratings

(T<sub>A</sub> = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V <sub>DD</sub>	–	– 0.3 to + 6.5	V
Input voltage	V <sub>IN</sub>	–	– 0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>O</sub>	All output pins	– 0.3 to V <sub>DD</sub> + 0.3	V
Output current High	I <sub>OH</sub>	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current Low	I <sub>OL</sub>	One I/O pin active	+ 30	mA
		Total pin current for ports 0, 1, and 2	+ 100	
		Total pin current for port 3	+ 40	
Operating temperature	T <sub>A</sub>	–	– 40 to + 85	°C
Storage temperature	T <sub>STG</sub>	–	– 65 to + 150	°C

Table 14-2. D.C. Electrical Characteristics

(T<sub>A</sub> = – 40 °C to + 85 °C, V<sub>DD</sub> = 2.0 V to 5.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V <sub>DD</sub>	F <sub>OSC</sub> = 8 MHz (Instruction clock = 2 MHz)	2.0	–	5.0	V
Input High voltage	V <sub>IH1</sub>	All input pins except V <sub>IH2</sub> and V <sub>IH3</sub>	0.8 V <sub>DD</sub>	–	V <sub>DD</sub>	V
	V <sub>IH2</sub>	RESET	0.85 V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH3</sub>	XIN	V <sub>DD</sub> – 0.3		V <sub>DD</sub>	
Input Low voltage	V <sub>IL1</sub>	All input pins except V <sub>IL2</sub> and V <sub>IL3</sub>	0	–	0.2 V <sub>DD</sub>	V
	V <sub>IL2</sub>	RESET			0.2 V <sub>DD</sub>	
	V <sub>IL3</sub>	XIN			0.3	
Output High voltage	V <sub>OH1</sub>	V <sub>DD</sub> = 2.4 V I <sub>OH</sub> = – 6 mA Port 3.1 only, T <sub>A</sub> = 25 °C	V <sub>DD</sub> – 0.7			V
	V <sub>OH2</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OH</sub> = – 2.2mA P3.0, P2.0–2.3 T <sub>A</sub> = 25 °C	V <sub>DD</sub> – 0.7			

Table 14-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output High voltage	V <sub>OH3</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OH</sub> = -1 mA Port0, Port1, P2.4-2.7 and Port4 T <sub>A</sub> = 25°C	V <sub>DD</sub> - 1.0	-	-	V
Output Low voltage	V <sub>OL1</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OL</sub> = 12 mA, port 3.1 only, T <sub>A</sub> = 25°C	-	0.4	0.5	V
	V <sub>OL2</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OL</sub> = 5 mA P3.0, P3.4-3.5, P2.0-2.3 T <sub>A</sub> = 25°C		0.4	0.5	
	V <sub>OL3</sub>	I <sub>OL</sub> = 2mA Port 0, Port1, P2.4-2.7 and Port4 T <sub>A</sub> = 25°C		0.4	1	
Input High leakage current	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub> All input pins except X <sub>IN</sub> and X <sub>OUT</sub>	-	-	1	μA
	I <sub>LIH2</sub>	V <sub>IN</sub> = V <sub>DD</sub> , X <sub>IN</sub> and X <sub>OUT</sub>			20	
Input Low leakage current	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V All input pins except X <sub>IN</sub> , X <sub>OUT</sub> , and RESET	-	-	-1	μA
	I <sub>LIL2</sub>	V <sub>IN</sub> = 0 V X <sub>IN</sub> and X <sub>OUT</sub>			-20	
Output High leakage current	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub> All output pins	-	-	1	μA
Output Low leakage current	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V All output pins	-	-	-1	μA
Pull-up resistors	R <sub>L1</sub>	V <sub>IN</sub> = 0 V, V <sub>DD</sub> = 2.4 V T <sub>A</sub> = 25°C, Ports 0-2, P3.2-3.3	44	55	95	kΩ



Table 14-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (note)	I <sub>DD1</sub>	Operating mode V <sub>DD</sub> = 5.0 V 8 MHz crystal	-	6	11	mA
		4 MHz crystal		4.5	9	
	I <sub>DD2</sub>	Idle mode V <sub>DD</sub> = 5.0 V 8 MHz crystal		1.8	3.5	
		4 MHz crystal		1.6	3.0	
	I <sub>DD3</sub>	Stop mode; V <sub>DD</sub> = 5.0 V	-	18	25	uA
		V <sub>DD</sub> = 3.6 V		12	15	
		V <sub>DD</sub> = 2.4 V		4.5	8	
		V <sub>DD</sub> = 0.7 V		1	1.5	

**NOTE:** Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 14-3. Characteristics of Low Voltage Detect circuit

(T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresys Voltage of LVD (Slew Rate of LVD)	ΔV	-	-	100	300	mV
Low level detect voltage	V <sub>LVD</sub>	-	2.00	2.20	2.40	V

Table 14-4. Data Retention Supply Voltage in Stop Mode

(T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V <sub>DDDR</sub>	-	1.0	-	5.0	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.0 V Stop mode	-	-	1	μA

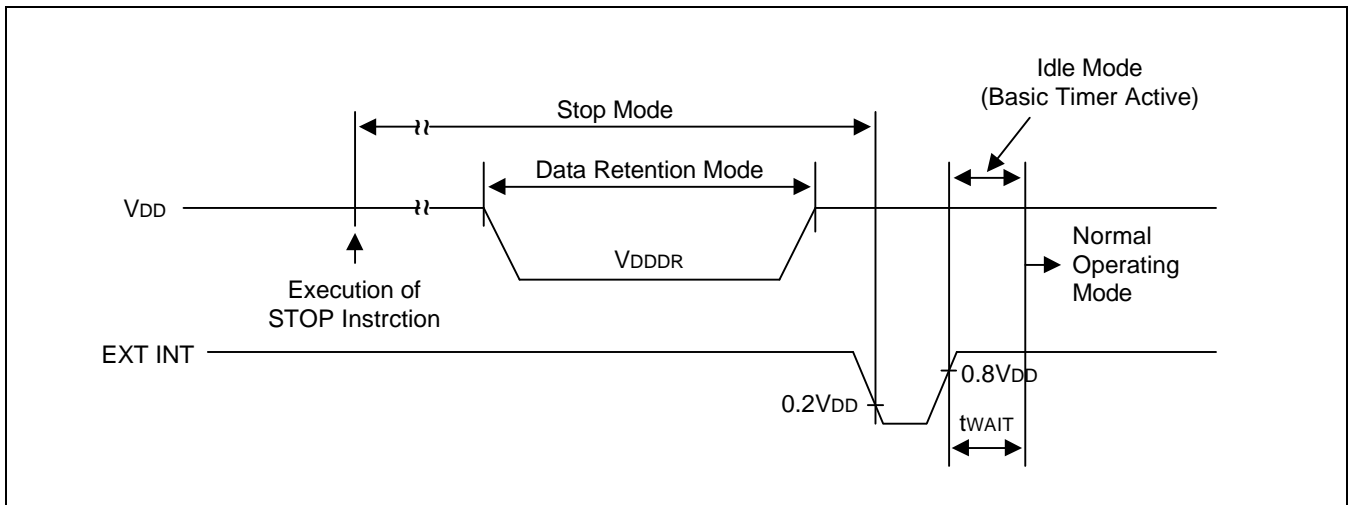


Figure 14-1. Stop Mode Release Timing When Initiated by an External Interrupt

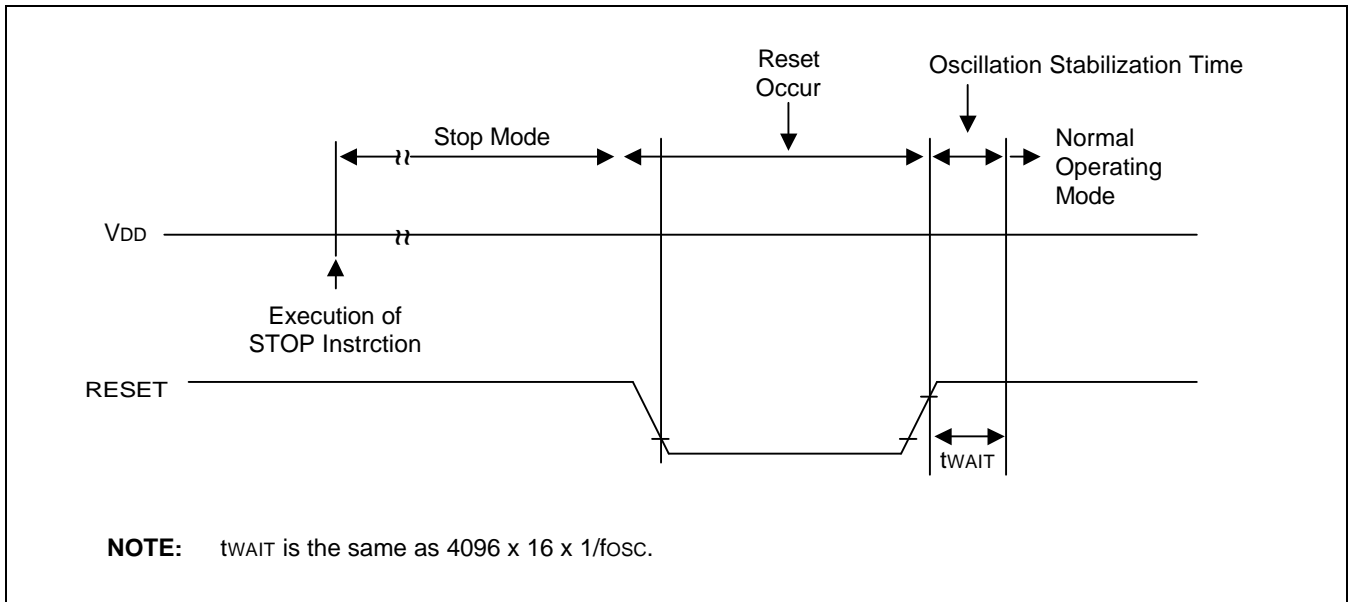


Figure 14-2. Stop Mode Release Timing When Initiated by a RESET

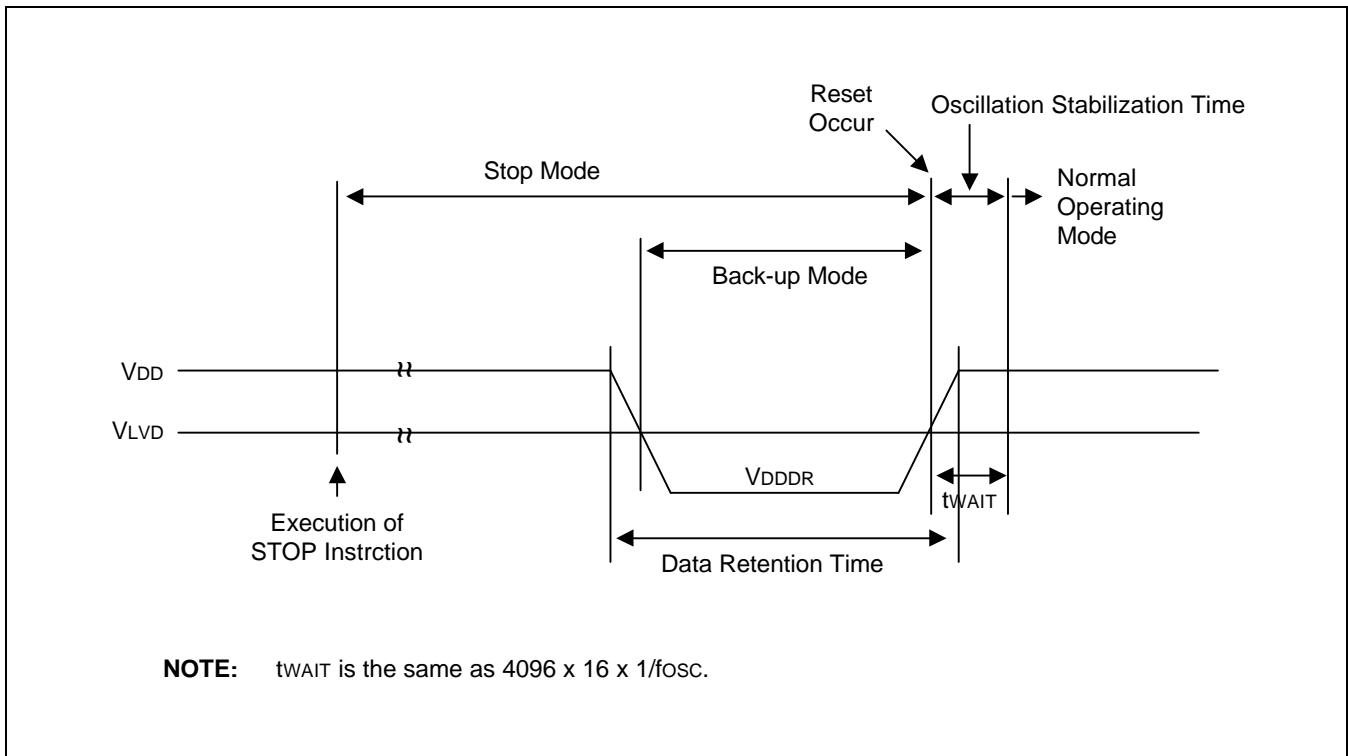


Figure 14-3. Stop Mode Release Timing When Initiated by a LVD

Table 14-5. Input/Output Capacitance

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 0\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	$C_{IN}$	f = 1 MHz; unmeasured pins are connected to $V_{SS}$	-	-	10	pF
Output capacitance	$C_{OUT}$					
I/O capacitance	$C_{IO}$					

Table 14-6. A.C. Electrical Characteristics

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input, High, Low width	$t_{INTH}$ , $t_{INTL}$	P0.0–P0.7, P2.3–P2.0 $V_{DD} = 5.0\text{ V}$	200	300	-	ns
RESET input Low width	$t_{RSL}$	Input $V_{DD} = 5.0\text{ V}$	1000	-	-	

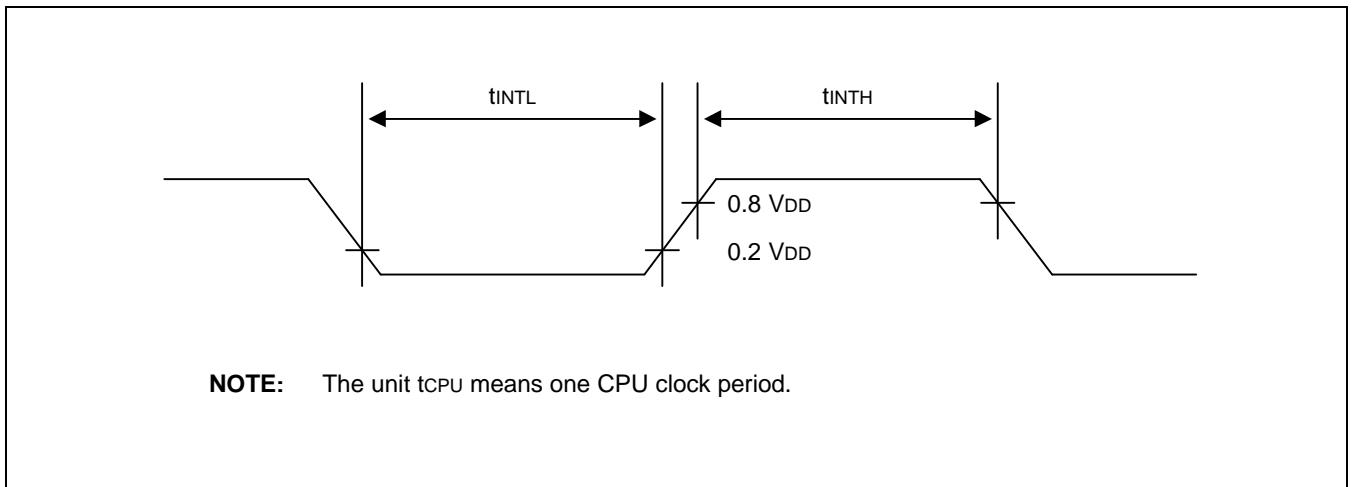


Figure 14-4. Input Timing for External Interrupts (Port 0, P2.3–P2.0)

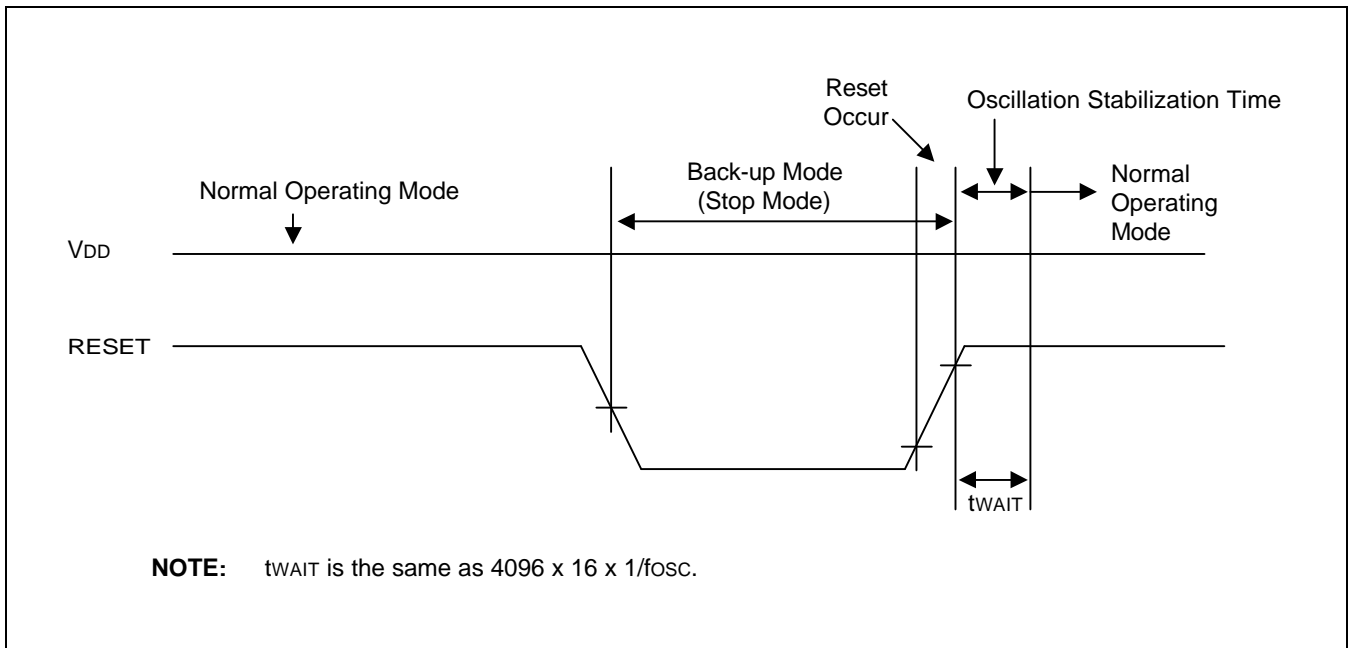


Figure 14-5. Input Timing for RESET

Table 14-7. Oscillation Characteristics

 $(T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C})$ 

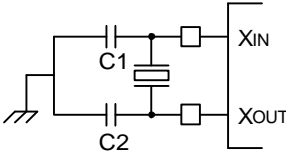
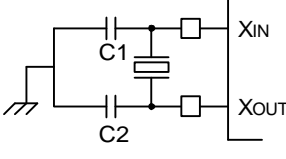
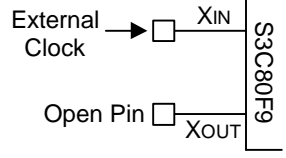
Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	1	–	8	MHz
Ceramic		CPU clock oscillation frequency	1	–	8	MHz
External clock		X <sub>IN</sub> input frequency	1	–	8	MHz

Table 14-8. Oscillation Stabilization Time

 $(T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}, V_{DD} = 4.5\text{ V to } 5.0\text{ V})$ 

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	$f_{OSC} > 400\text{ kHz}$	–	–	20	ms
Main ceramic	Oscillation stabilization occurs when $V_{DD}$ is equal to the minimum oscillator voltage range.	–	–	10	ms
External clock (main system)	X <sub>IN</sub> input High and Low width ( $t_{XH}$ , $t_{XL}$ )	25	–	500	ns
Oscillator stabilization wait time	$t_{WAIT}$ when released by a reset <sup>(1)</sup>	–	$2^{16}/f_{OSC}$	–	ms
	$t_{WAIT}$ when released by an interrupt <sup>(2)</sup>	–	–	–	ms

**NOTES:**

- $f_{OSC}$  is the oscillator frequency.
- The duration of the oscillation stabilization time ( $t_{WAIT}$ ) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.

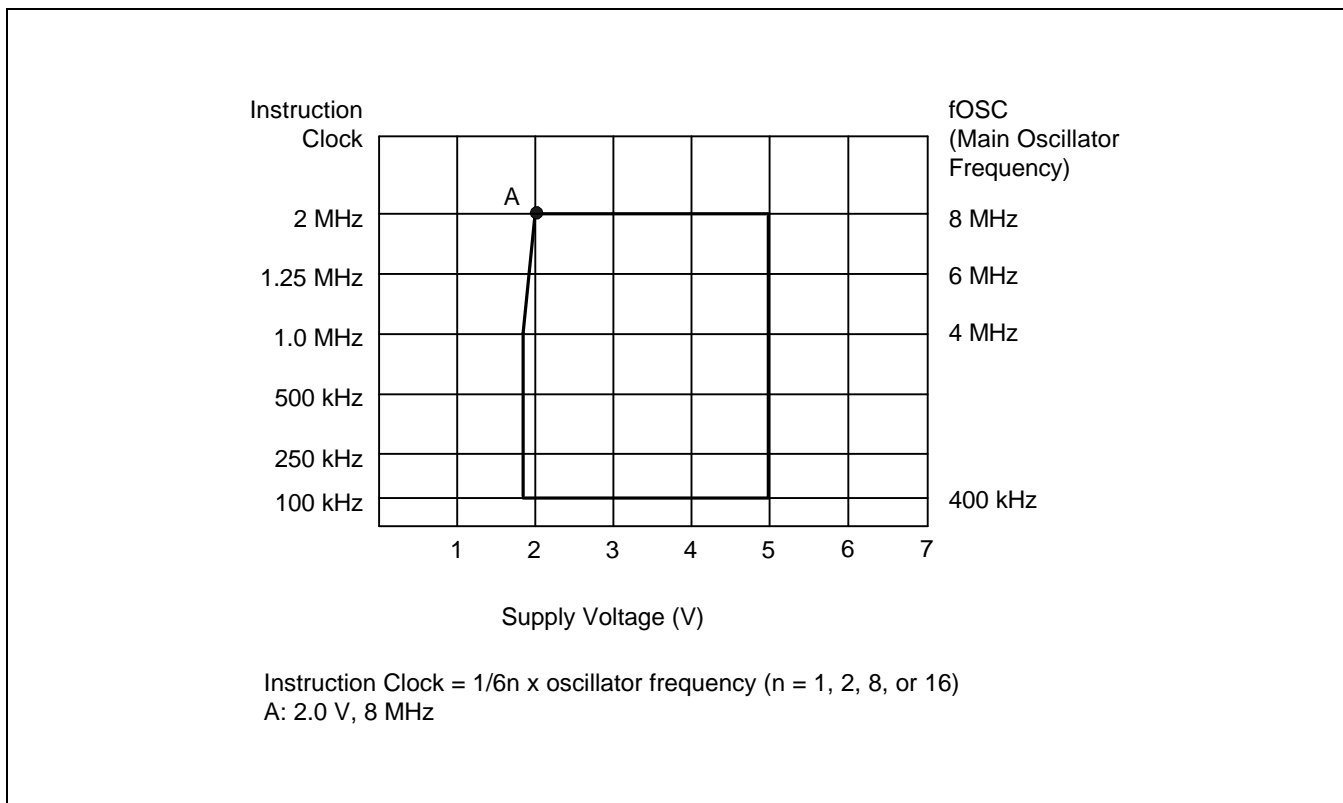


Figure 14-6. Operating Voltage Range of S3C80F9

# 15

## ELECTRICAL DATA 2 (S3C80G7/C80G9)

### OVERVIEW

In this section, S3C80G7/C80G9 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by an external interrupt
- Stop mode release timing when initiated by a Reset
- I/O capacitance
- A.C. electrical characteristics
- Input timing for external interrupts
- Input timing for RESET
- Oscillation characteristics
- Oscillation stabilization time

Table 15-1. Absolute Maximum Ratings

(T<sub>A</sub> = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V <sub>DD</sub>	–	– 0.3 to + 6.5	V
Input voltage	V <sub>IN</sub>	–	– 0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>O</sub>	All output pins	– 0.3 to V <sub>DD</sub> + 0.3	V
Output current High	I <sub>OH</sub>	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current Low	I <sub>OL</sub>	One I/O pin active	+ 30	mA
		Total pin current for ports 0, 1, and 2	+ 100	
		Total pin current for port 3	+ 40	
Operating temperature	T <sub>A</sub>	–	– 40 to + 85	°C
Storage temperature	T <sub>STG</sub>	–	– 65 to + 150	°C

Table 15-2. D.C. Electrical Characteristics

(T<sub>A</sub> = – 40 °C to + 85 °C, V<sub>DD</sub> = 2.0 V to 5.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V <sub>DD</sub>	F <sub>OSC</sub> = 4 MHz (Instruction clock = 1 MHz)	1.7	–	5.0	V
Input High voltage	V <sub>IH1</sub>	All input pins except V <sub>IH2</sub> and V <sub>IH3</sub>	0.8 V <sub>DD</sub>	–	V <sub>DD</sub>	V
	V <sub>IH2</sub>	RESET	0.85 V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH3</sub>	XIN	V <sub>DD</sub> – 0.3		V <sub>DD</sub>	
Input Low voltage	V <sub>IL1</sub>	All input pins except V <sub>IL2</sub> and V <sub>IL3</sub>	0	–	0.2 V <sub>DD</sub>	V
	V <sub>IL2</sub>	RESET			0.2 V <sub>DD</sub>	
	V <sub>IL3</sub>	XIN			0.3	
Output High voltage	V <sub>OH1</sub>	V <sub>DD</sub> = 2.4 V I <sub>OH</sub> = – 6 mA Port 3.1 only, T <sub>A</sub> = 25°C	V <sub>DD</sub> – 0.7			V
	V <sub>OH2</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OH</sub> = – 2.2mA P3.0, P2.0–2.3 T <sub>A</sub> = 25°C	V <sub>DD</sub> – 0.7			



Table 15-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output High voltage	V <sub>OH3</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OH</sub> = -1 mA Port0, Port1, P2.4-2.7 and Port4 T <sub>A</sub> = 25°C	V <sub>DD</sub> - 1.0	-	-	V
Output Low voltage	V <sub>OL1</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OL</sub> = 12 mA, port 3.1 only, T <sub>A</sub> = 25°C	-	0.4	0.5	V
	V <sub>OL2</sub>	V <sub>DD</sub> = 2.4 V, I <sub>OL</sub> = 5 mA P3.0, P3.4-3.5, P2.0-2.3 T <sub>A</sub> = 25°C		0.4	0.5	
	V <sub>OL3</sub>	I <sub>OL</sub> = 2mA Port 0, Port1, P2.4-2.7 and Port4 T <sub>A</sub> = 25°C		0.4	1	
Input High leakage current	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub> All input pins except X <sub>IN</sub> and X <sub>OUT</sub>	-	-	1	μA
	I <sub>LIH2</sub>	V <sub>IN</sub> = V <sub>DD</sub> , X <sub>IN</sub> and X <sub>OUT</sub>			20	
Input Low leakage current	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V All input pins except X <sub>IN</sub> , X <sub>OUT</sub> , and RESET	-	-	-1	μA
	I <sub>LIL2</sub>	V <sub>IN</sub> = 0 V X <sub>IN</sub> and X <sub>OUT</sub>			-20	
Output High leakage current	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub> All output pins	-	-	1	μA
Output Low leakage current	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V All output pins	-	-	-1	μA
Pull-up resistors	R <sub>L1</sub>	V <sub>IN</sub> = 0 V, V <sub>DD</sub> = 2.4 V T <sub>A</sub> = 25°C, Ports 0-2, P3.2-3.3	44	55	95	kΩ

**Table 15-2. D.C. Electrical Characteristics (Continued)**(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (note)	I <sub>DD1</sub>	Operating mode V <sub>DD</sub> = 5.0 V 4 MHz crystal	–	4.5	9	mA
	I <sub>DD2</sub>	Idle mode V <sub>DD</sub> = 5.0 V 4 MHz crystal		1.6	3.0	
	I <sub>DD3</sub>	Stop mode; V <sub>DD</sub> = 5.0 V	–	1	6	uA

**NOTE:** Supply current does not include current drawn through internal pull-up resistors or external output current loads.**Table 15-3. Characteristics of Low Voltage Detect circuit**(T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresys Voltage of LVD (Slew Rate of LVD)	ΔV	–	–	100	300	mV
Low level detect voltage	V <sub>LVD</sub>	–	1.70	1.90	2.10	V

**Table 15-4. Data Retention Supply Voltage in Stop Mode**(T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V <sub>DDDR</sub>	–	1.0	–	5.0	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.0 V Stop mode	–	–	1	μA

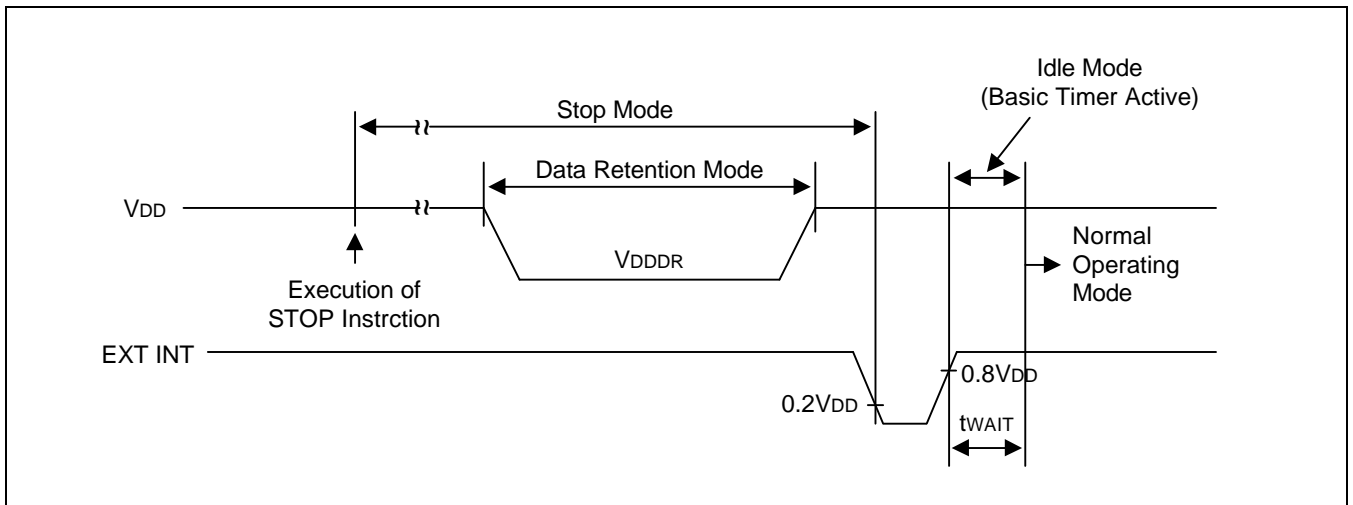
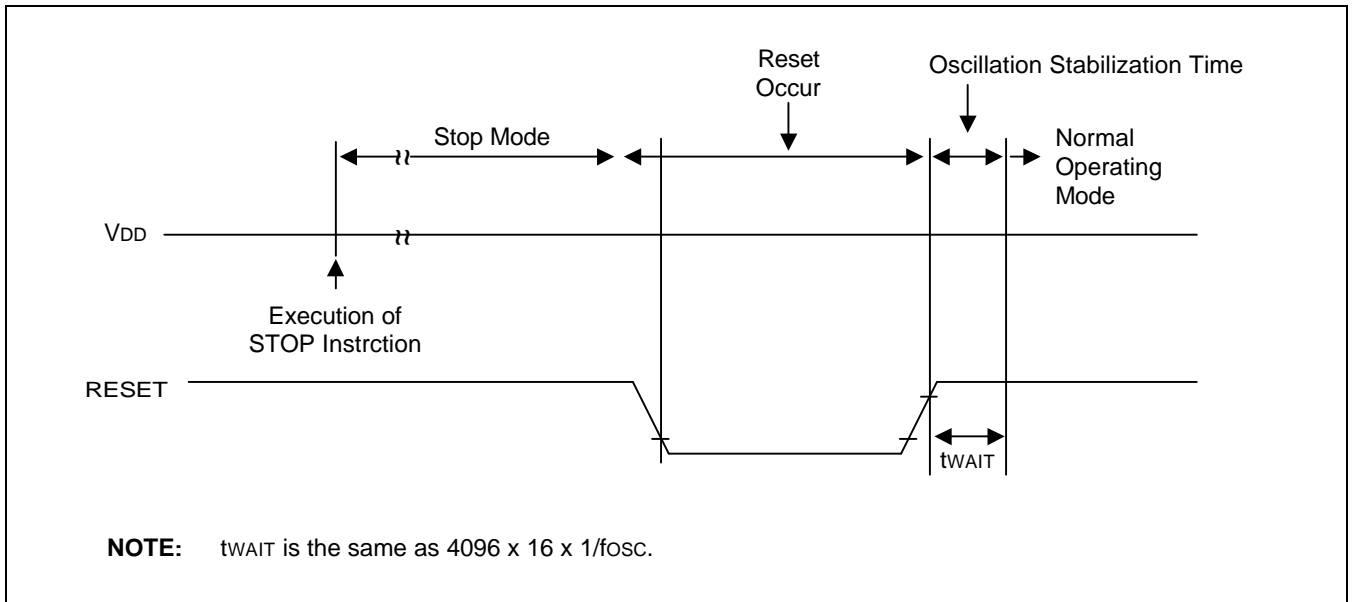


Figure 15-1. Stop Mode Release Timing When Initiated by an External Interrupt



**NOTE:** tWAIT is the same as  $4096 \times 16 \times 1/f_{osc}$ .

Figure 15-2. Stop Mode Release Timing When Initiated by a RESET

Table 15-5. Input/Output Capacitance

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C <sub>IN</sub>	f = 1 MHz; unmeasured pins are connected to V <sub>SS</sub>	-	-	10	pF
Output capacitance	C <sub>OUT</sub>					
I/O capacitance	C <sub>IO</sub>					

Table 15-6. A.C. Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input, High, Low width	t <sub>INTH</sub> , t <sub>INTL</sub>	P0.0–P0.7, P2.3–P2.0 V <sub>DD</sub> = 5.0 V	200	300	-	ns
RESET input Low width	t <sub>RSL</sub>	Input V <sub>DD</sub> = 5.0 V	1000	-	-	

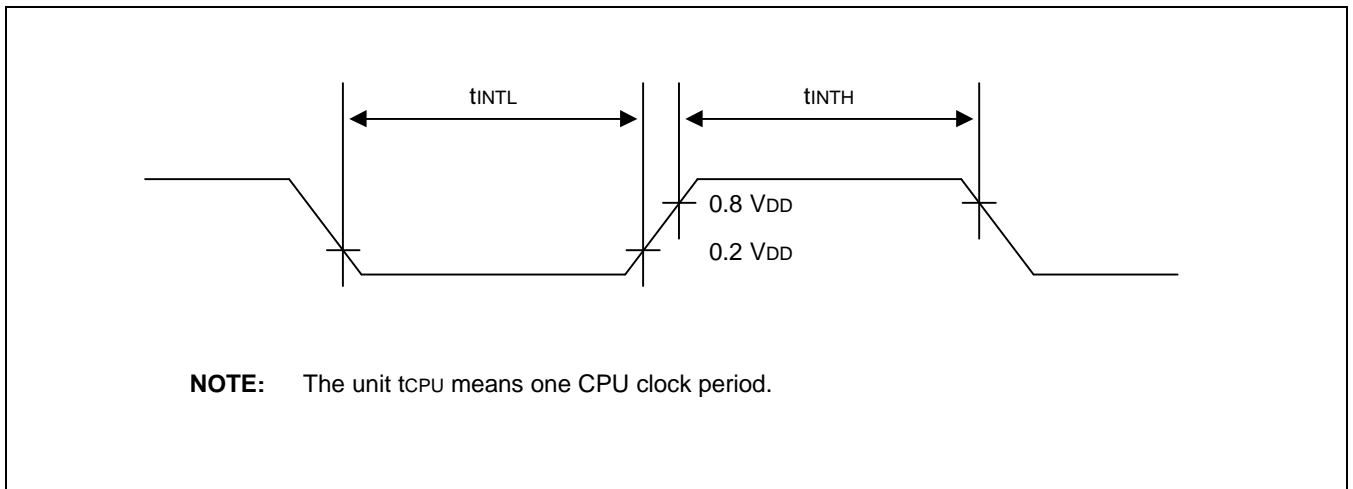


Figure 15-3. Input Timing for External Interrupts (Port 0, P2.3–P2.0)

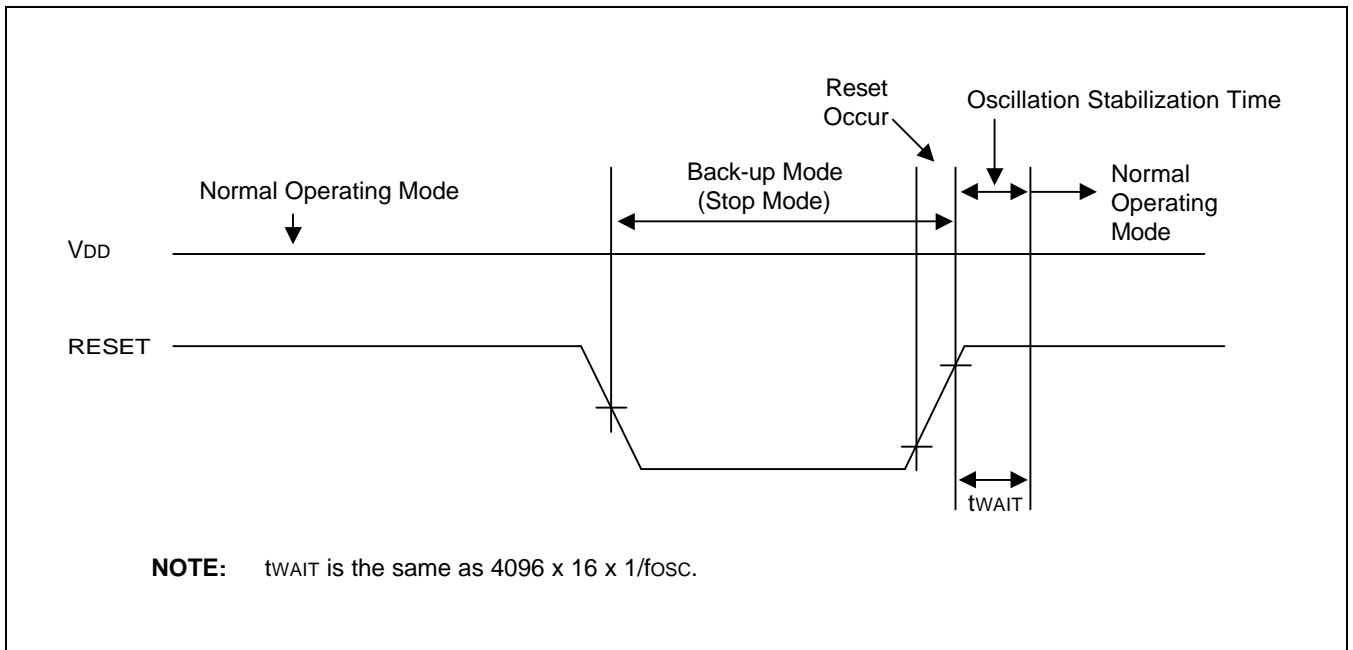


Figure 15-4. Input Timing for RESET

Table 15-7. Oscillation Characteristics

(T<sub>A</sub> = -40 °C + 85 °C)

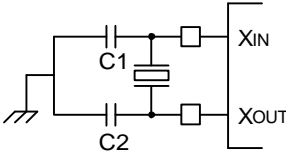
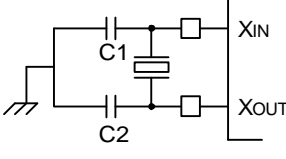
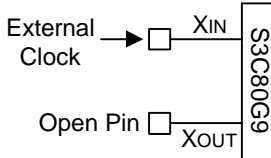
Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	1	–	4	MHz
Ceramic		CPU clock oscillation frequency	1	–	4	MHz
External clock		X <sub>IN</sub> input frequency	1	–	4	MHz

Table 15-8. Oscillation Stabilization Time

(T<sub>A</sub> = -40 °C + 85 °C, V<sub>DD</sub> = 4.5 V to 5.0 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	f <sub>OSC</sub> > 400 kHz	–	–	20	ms
Main ceramic	Oscillation stabilization occurs when V <sub>DD</sub> is equal to the minimum oscillator voltage range.	–	–	10	ms
External clock (main system)	X <sub>IN</sub> input High and Low width (t <sub>XH</sub> , t <sub>XL</sub> )	25	–	500	ns
Oscillator stabilization wait time	t <sub>WAIT</sub> when released by a reset <sup>(1)</sup>	–	2 <sup>16</sup> / f <sub>OSC</sub>	–	ms
	t <sub>WAIT</sub> when released by an interrupt <sup>(2)</sup>	–	–	–	ms

**NOTES:**

- f<sub>OSC</sub> is the oscillator frequency.
- The duration of the oscillation stabilization time (t<sub>WAIT</sub>) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.

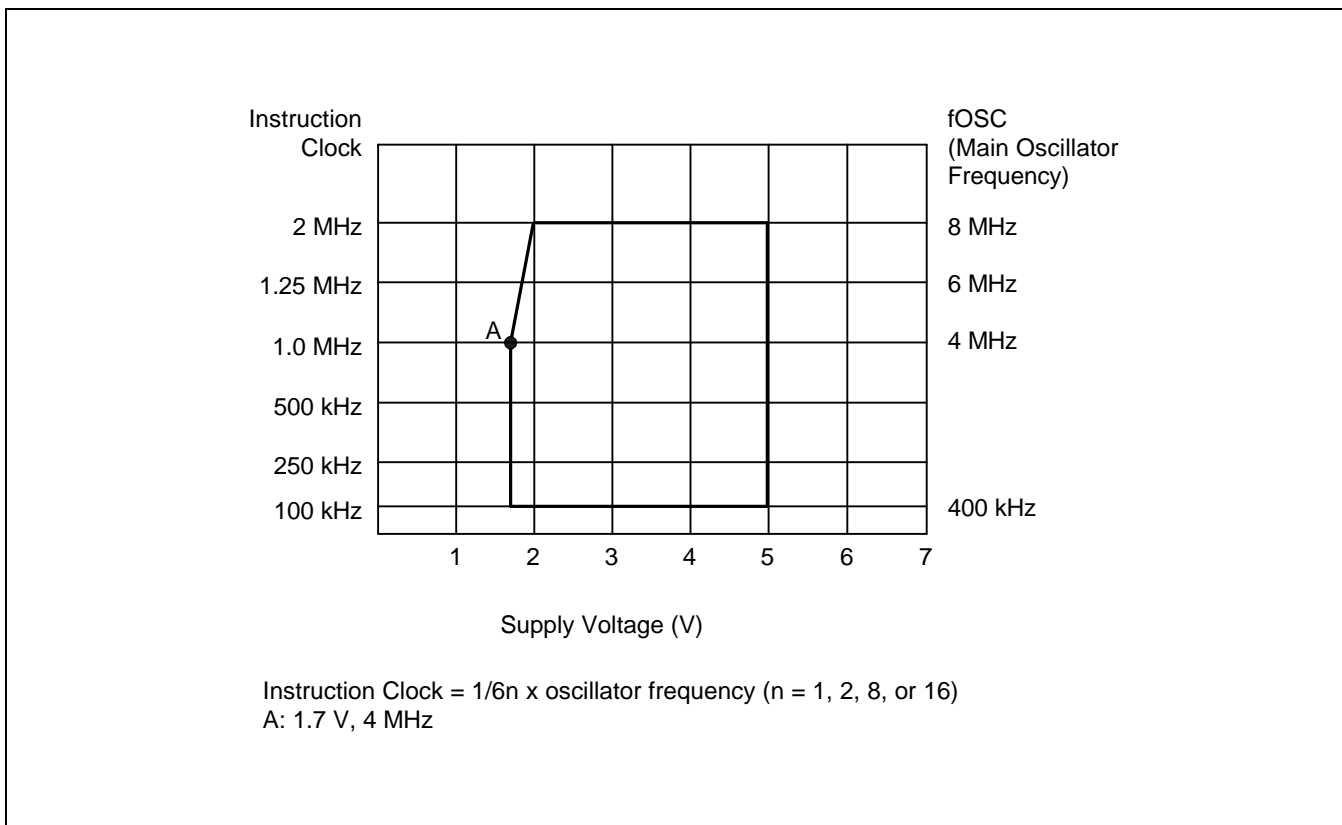


Figure 15-6. Operating Voltage Range of S3C80G9

# 16 MECHANICAL DATA

## OVERVIEW

The S3C80F7/C80F9/C80G7/C80G9 microcontroller is currently available in a 32-pin SOP, 42-pin SDIP and 44-pin QFP package.

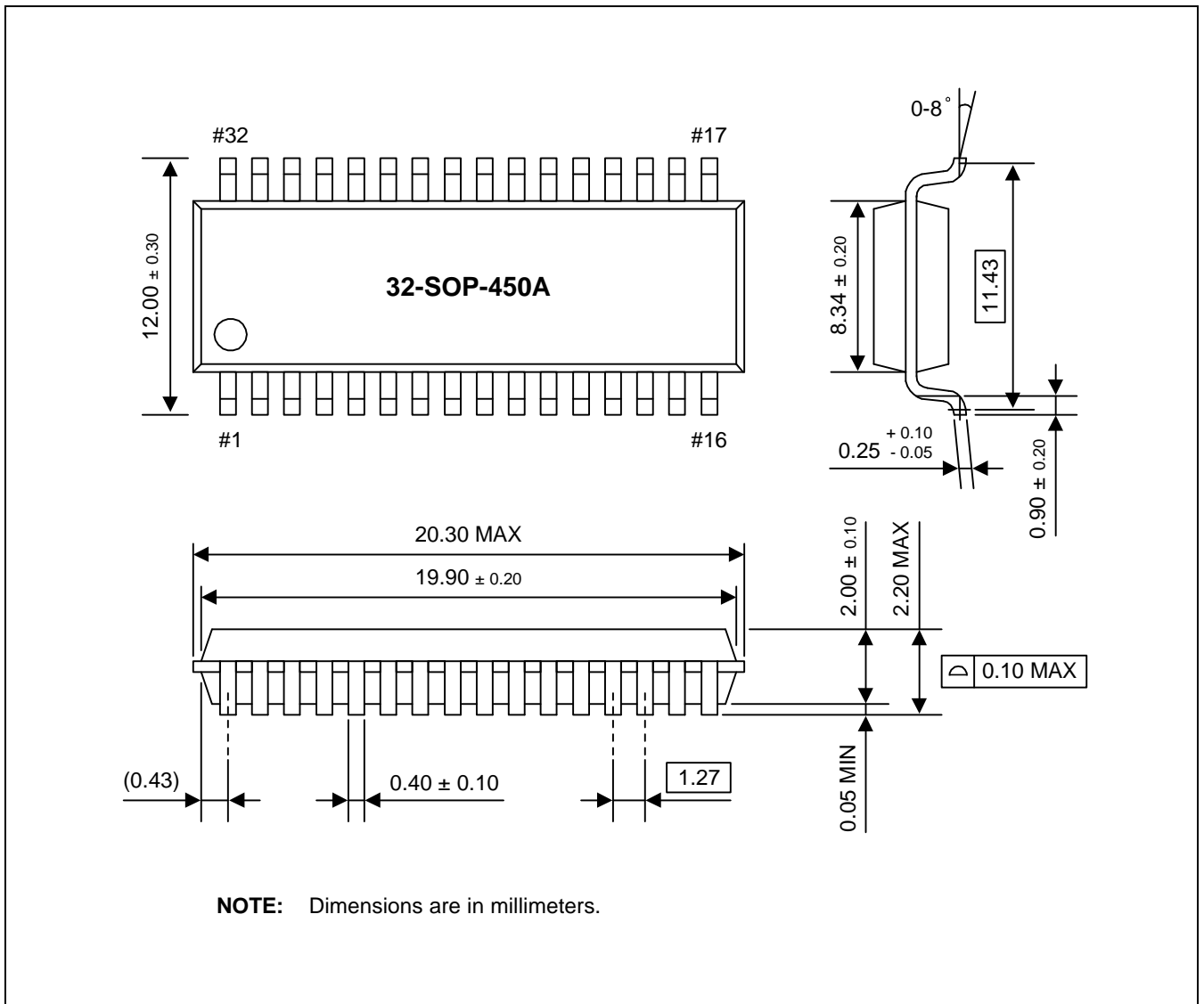


Figure 16-1. 32-Pin SOP Package Dimension



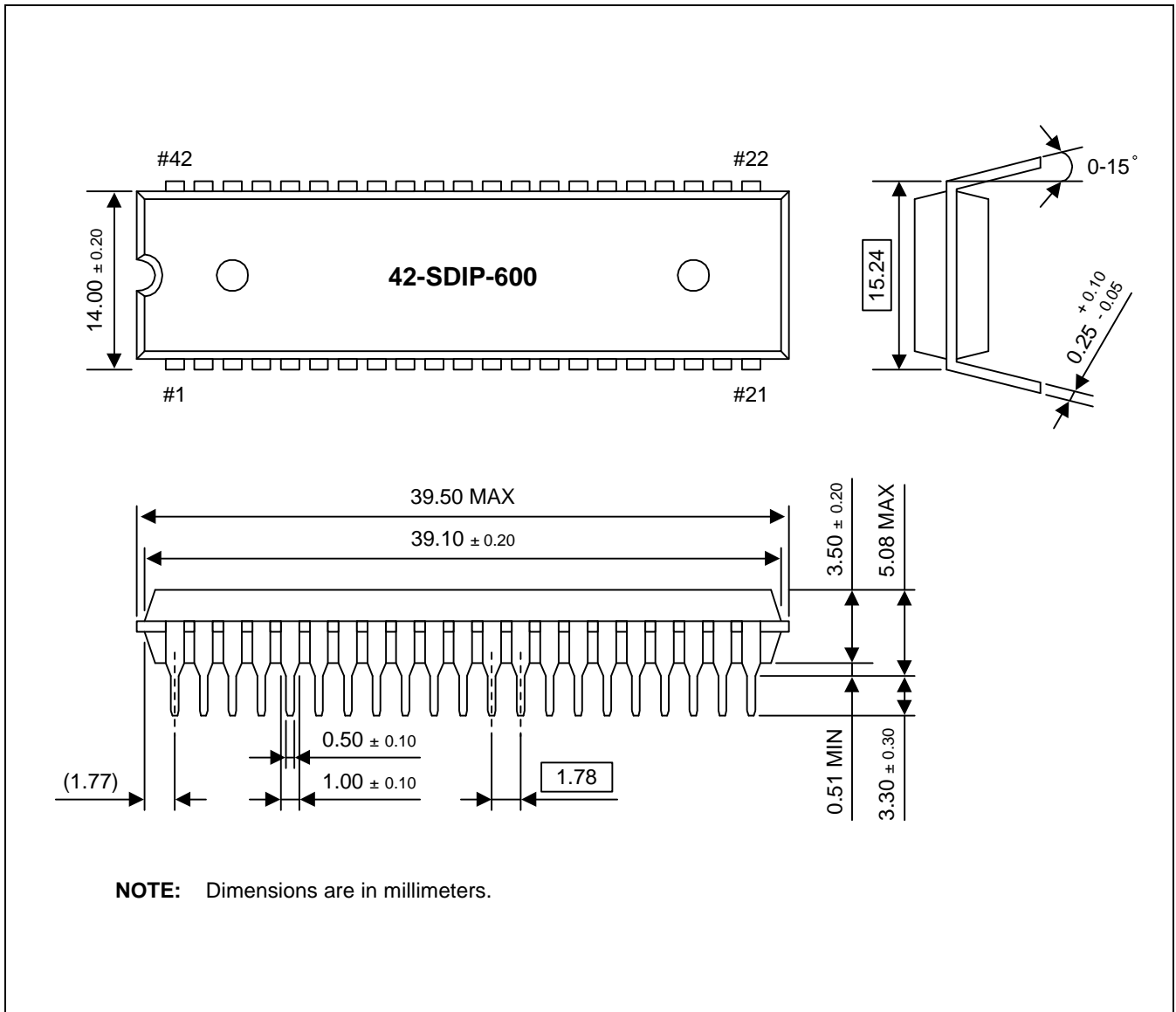


Figure 16-2. 42-Pin SDIP Package Dimension

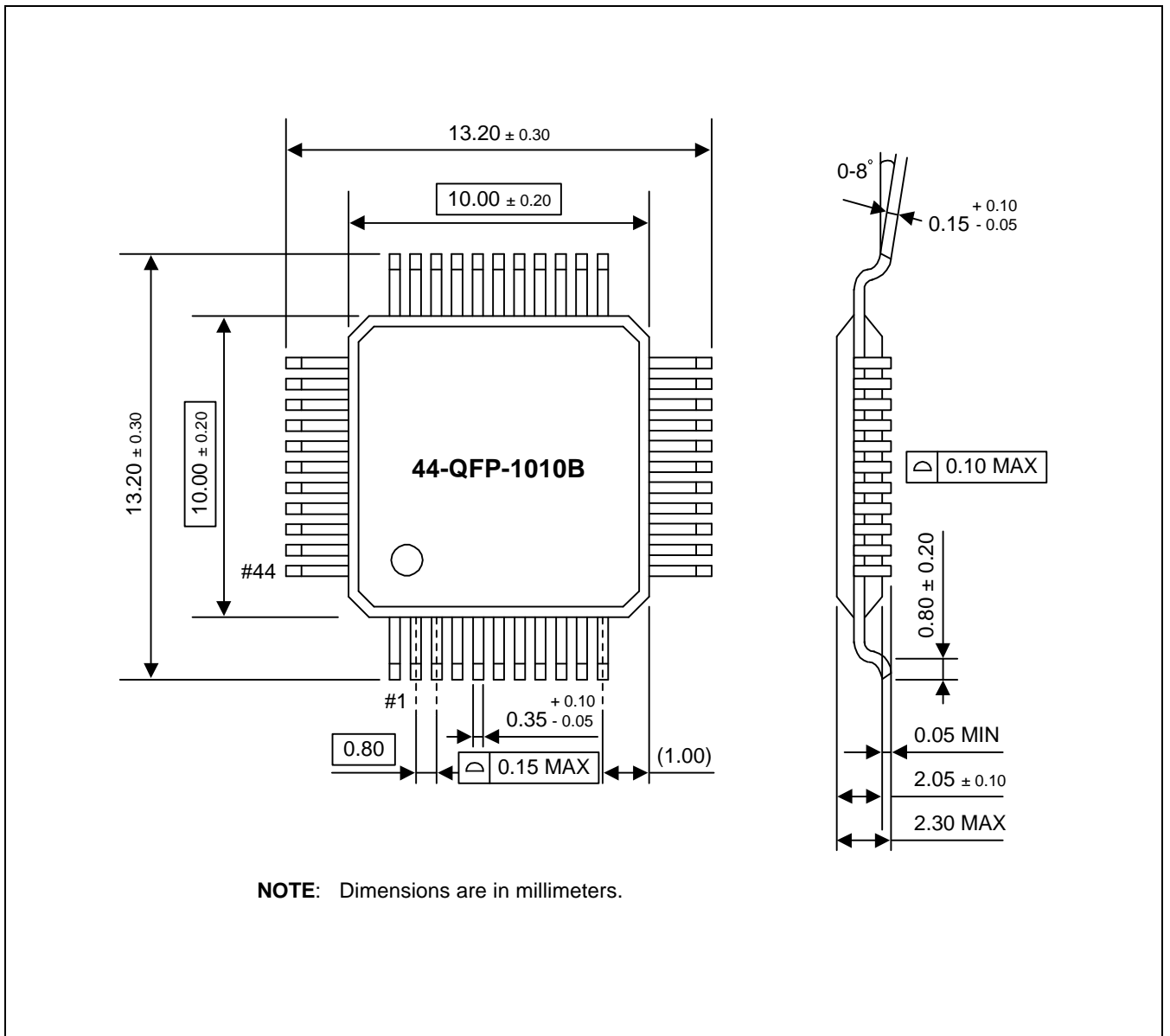


Figure 16-3. 44-Pin SQFP Package Dimension