

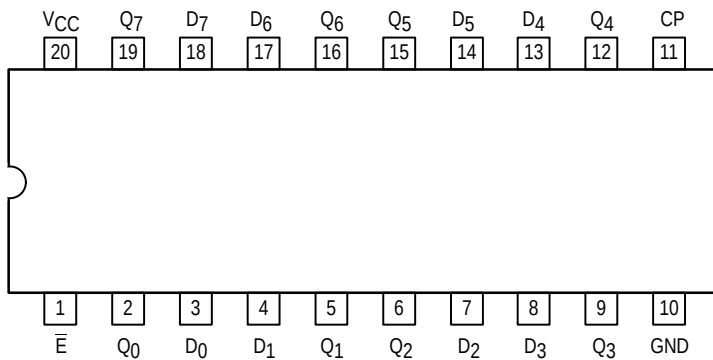


OCTAL D FLIP-FLOP WITH ENABLE

The MC74F377 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable (E) is LOW. This device is supplied in a 20-pin package.

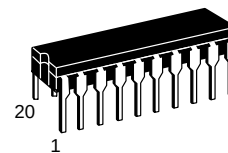
- High Impedance NPN Base Inputs for Reduced Loading (20 μ A in HIGH and LOW States)
- Ideal for Addressable Register Applications
- Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- See: MC74F373 for Transparent Latch Version
MC74F374 for 3-State Version

CONNECTION DIAGRAM (TOP VIEW)

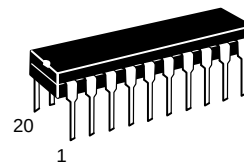


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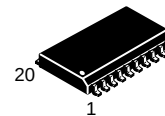
OCTAL D FLIP-FLOP
WITH ENABLE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

FUNCTION TABLE

Operating Mode	Inputs			Outputs
	CP	$\bar{E}$	D_n	Q_n
Load "1"	↑	L	h	H
Load "0"	↑	L	L	L
Hold (do nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH voltage level steady state; h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition; L = LOW voltage level steady state; l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition; X = Don't Care; ↑ = LOW-to-HIGH clock transition

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FUNCTIONAL DESCRIPTION

The MC74F377 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Enable ($\bar{E}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The $\bar{E}$ input must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — HIGH	74			−1.0	mA
I _{OL}	Output Current — LOW	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				−1.2	V	I _{IN} = −18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	2.5	2.5			V	I _{OH} = −1.0 mA	V _{CC} = 4.5 V
		2.7	2.7					V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current				20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
I _{IL}	Input LOW Current				−20	μA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Total Supply Current		I _{CCH}	55	72	mA	D _n = 4.5 V, CP = ↑, $\bar{E}$ = GND	V _{CC} = MAX
			I _{CCL}	70	90	mA	D _n = $\bar{E}$ = GND, CP = ↑	

NOTES:

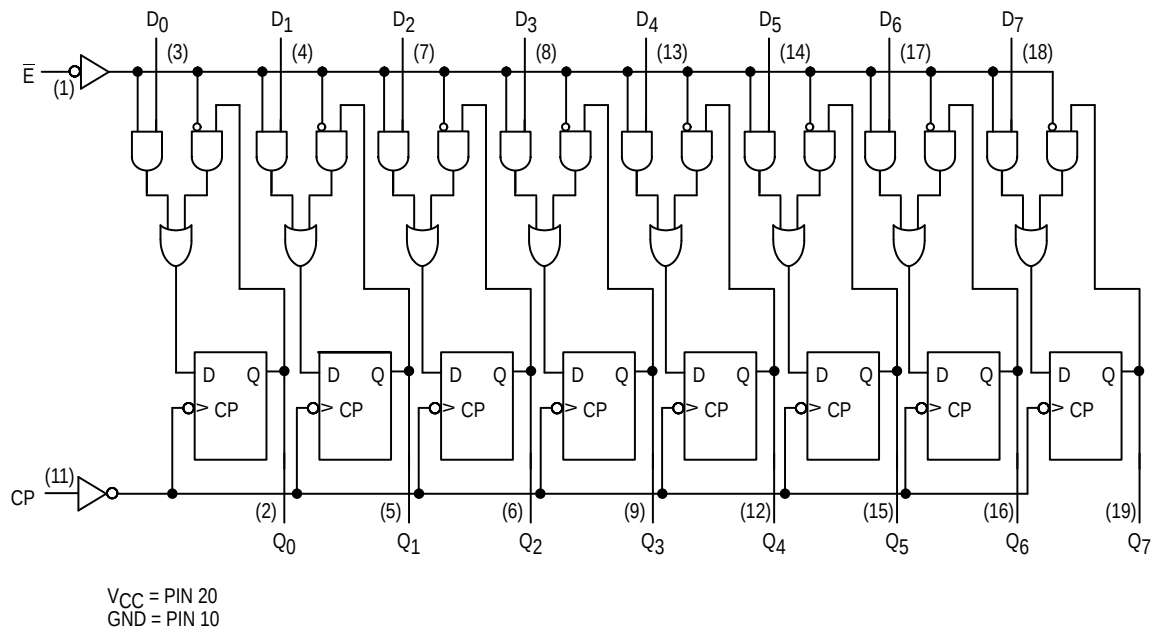
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0 to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	110	120		100		MHz
t _{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10	ns
t _{PHL}	CP to Q _n	4.0	7.0	9.0	4.0	10.5	

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LOGIC DIAGRAM



AC OPERATING REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = 5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0			3.0			ns
t _S (L)	D _n to CP	3.0			3.0			
t _h (H)	Hold Time, HIGH or LOW	1.0			1.0			ns
t _h (L)	D _n to CP	1.0			1.0			
t _S (H)	Setup Time, HIGH or LOW	2.5			2.5			ns
t _S (L)	$\overline{E}$ to CP	4.0			4.0			
t _h (H)	Hold Time, HIGH or LOW	0			0			ns
t _h (L)	$\overline{E}$ to CP	0			0			
t _w (H)	Clock Pulse Width	4.0			5.0			ns
t _w (L)	HIGH or LOW	4.0			5.0			