

M56710FP

F2F MAGNETIC STRIPE ENCODING CARD READER

DESCRIPTION

The M56710FP is a semiconductor integrated circuit of BiCMOS structure having an F2F demodulator function for magnetic card reader.

FEATURES

- Low current dissipation (0.7mA when on standby as a standard)
- Provided with glance-over selection input (4, 8, and 16 bits)
- Provided with output polarity ("L" active or "H" active) switching input
- Miniature mini-mold package
- Wide operating temperature range $T_a = -20 - 75^{\circ}\text{C}$

APPLICATION

Magnetic card reader

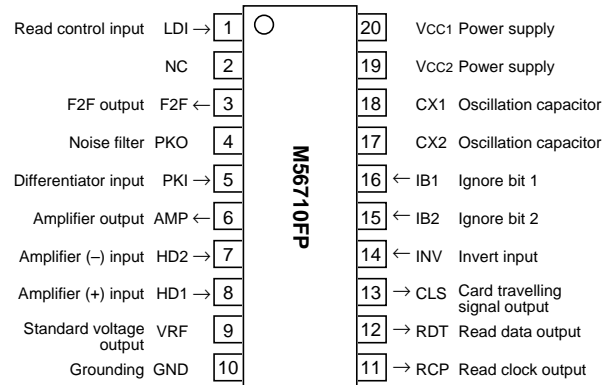
FUNCTION

Data signal which is read from magnetic card via magnetic head is input from HD2 and HD1 pins, and converted into F2F pattern signal by analog processing in amplifier OP1, differentiator OP2, sensitivity setting circuit and waveform shaping circuit. If F2F signal is input, the logic section glances over the prescribed number of bits set by IB1 and IB2 input before performing digital processing, and then outputs card reading signal CLS, read clock signal RCP, and read data signal RDT. INV turning to "L" switches each output of CLS, RCP and RDT from "L" active to "H" active.

STANDARD BITS:

Let the number of glance-over bits set by IB1 and IB2 be M.
 Let the Mth FC (flux change) through M+1st FC after LDI input is turned from "L" to "H" be a standard bit with a time width of T_{B0} .
 I/O is discriminated from the next bit to this standard bit as a data bit.

PIN CONFIGURATION (TOP VIEW)



Outline 20P2N-A

NC: no connection

I/O discrimination

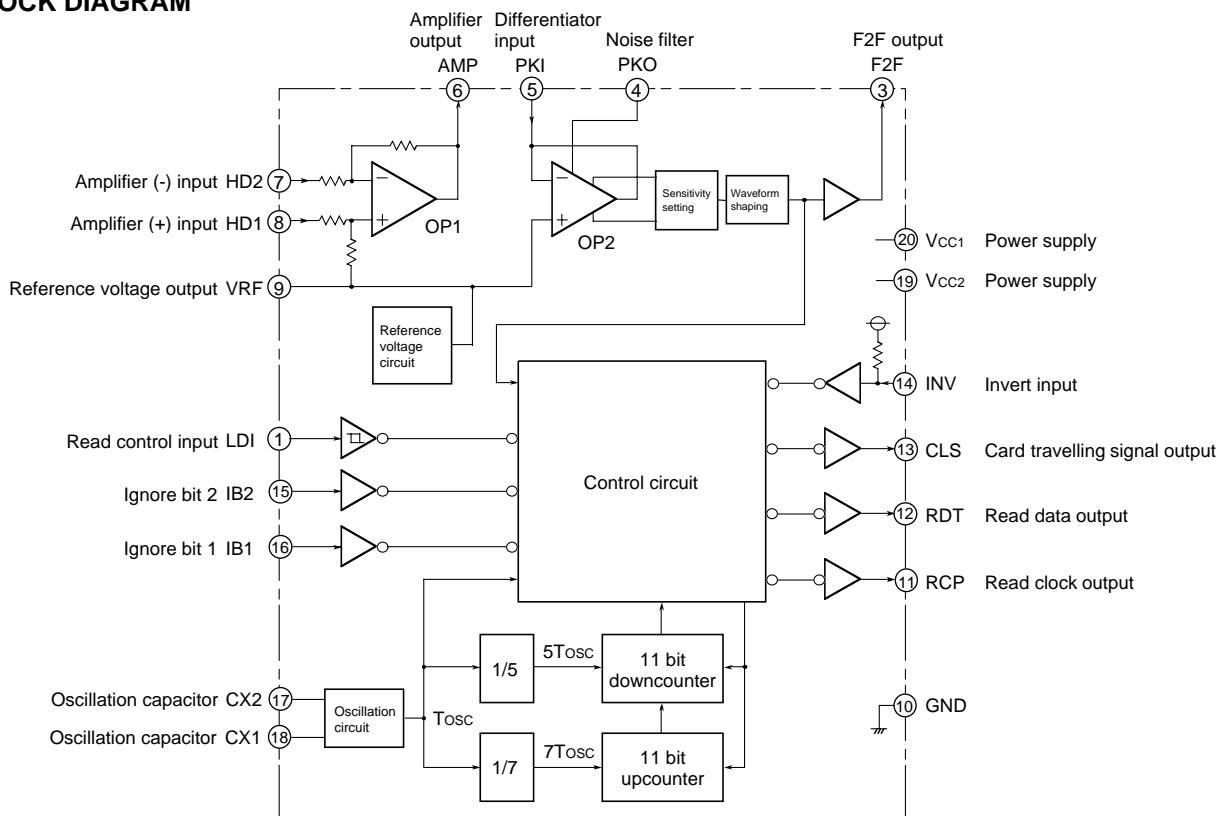
Let the data bit time width of a data bit be T_{Bn} , and if there is one next FC between the FC at the end of that bit (i.e. the beginning of the next bit) to $5/7T_{Bn}$, let the next bit (B_{n+1}) be data "1", and, if there is no FC, be data "0".

Output signal time width

When letting the oscillation cycle of oscillation circuit be T_{osc} ,

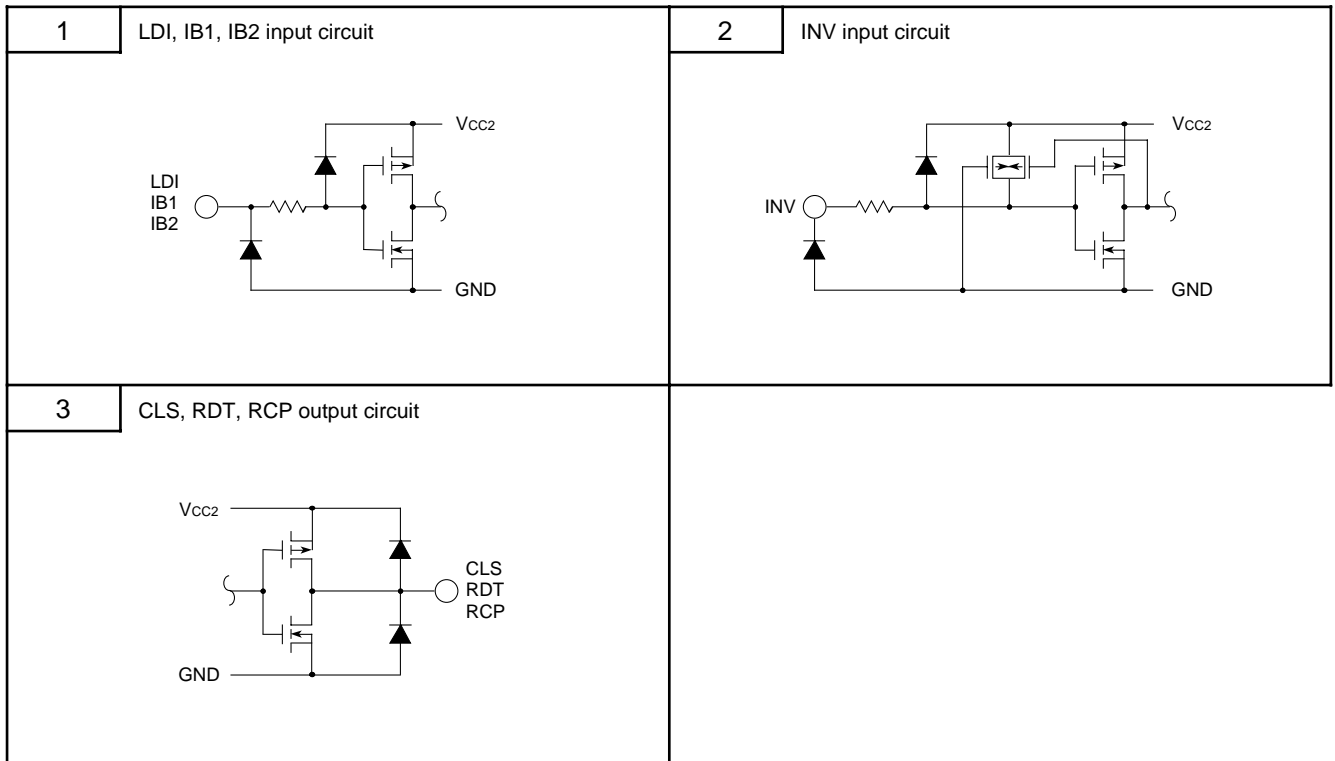
- RCP output pulse width T_{OW} about $16T_{osc}$
- RCP delay time to RDT about $8T_{osc}$

BLOCK DIAGRAM



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I/O CIRCUIT



PIN FUNCTION DESCRIPTION

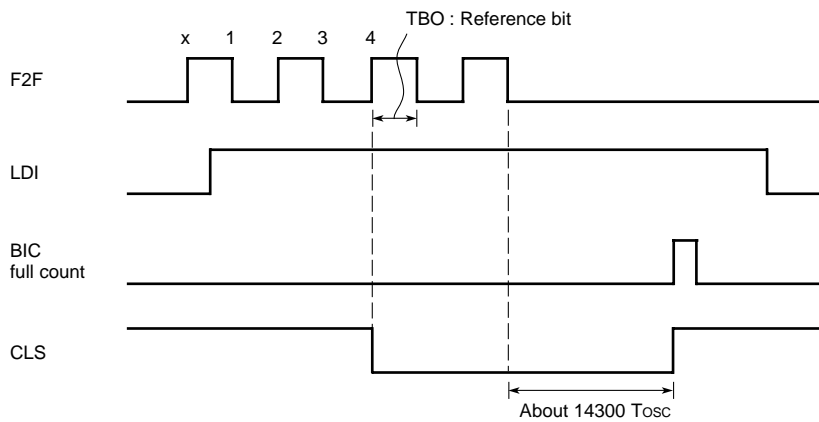
Pin No.	Pin name	Name	Function
①	LDI	Read control input	Schmidt trigger input. At "L", reset the internal digital circuit. At "H", F2F modulation is possible.
③	F2F	F2F output	F2F signal output that has amplified, differentiated and further waveform-shaped the magnetic head signal.
④	PKO	Noise filter	Connect noise removing capacitor CNF between PKI and PKO.
⑤	PKI	Differentiator input	Refer to PKO and AMP.
⑥	AMP	Amplifier output	Connect resistor RPK and capacitor CPK between AMP and PKI.
⑦	HD2	Amplifier (-) input	Connect magnetic head between HD1 and HD2.
⑧	HD1	Amplifier (+) input	Connect magnetic head between HD1 and HD2.
⑨	VRF	Reference voltage output	Reference voltage output of Vcc 1/2
⑩	GND	Grounding	
⑪	RCP	Read clock output	Clock pulse output after F2F modulation
⑫	RDT	Read data output	Data output after F2F modulation
⑬	CLS	Card travelling signal output	Signal output indicating that card is travelling
⑭	INV	Invert input	CLS, RDT and RCP output becomes "L" active at "H" (OPEN), and "H" active at "L".
⑮	IB2	Ignore bit 2	Glance-over bit setting pin
⑯	IB1	Ignore bit 1	Glance-over bit setting pin
⑰	CX2	Oscillation capacitor	Connect capacitor Cosc between CX1 and CX2 to set oscillation frequency.
⑱	CX1	Oscillation capacitor	Connect capacitor Cosc between CX1 and CX2 to set oscillation frequency.
⑲	Vcc2	Power supply	Digital circuit section power supply pin. Supply voltage is Vcc.
⑳	Vcc1	Power supply	Analog circuit section power supply pin. Supply voltage is Vcc (same voltage as Vcc2).

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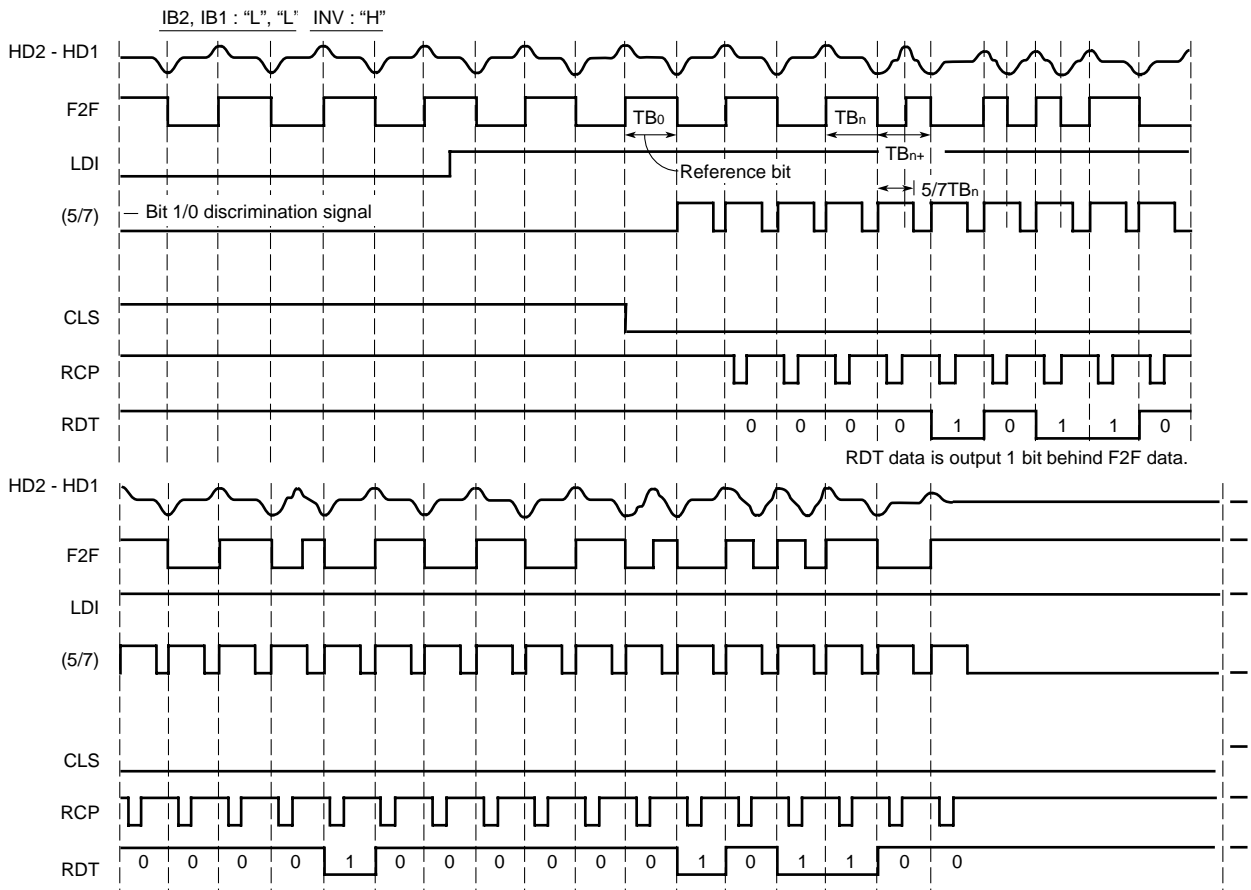
GLANCE-OVER BIT SETTING AND TIMING BY IB1 AND IB2

IB2 input	IB1 input	Number of glance-over bits	Description
L	L	4	<ul style="list-style-type: none"> Internal digital circuit is reset with LDI input at "L". LDI input may be at "H" at all times. CLS output turns to "L" after counting the flux change FC (change in the status of F2F) of the number of glance-over bits, and returns to "H" when BIC (bit interval counter) has fully counted. (At "L" active).
L	H	8	
H	L	16	
H	H	—	—

• IB2, IB1: "L", "L"



OPERATING TIMING DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Ta = -20 – 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	Vcc1, Vcc2	-0.3 – +6.5	V
Vi	Input voltage	LDI, IB1, IB2, INV	-0.3 – Vcc+0.3	V
Vi	Input voltage	HD1, HD2	-0.3 – Vcc+0.3	V
Io	Output voltage	CLS, RDT, RCP	-10 – +10	mA
V _{ID}	Differential input voltage	Between HD2 and HD1 pins	-1.2 – +1.2	V
T _{opr}	Operating temperature		-20 – 75	°C
T _{stg}	Storage temperature		-55 – 125	°C

Note 1: Voltage is based on GND pin of the circuit (0V), unless otherwise noted.

2: Direction of the current flowing into the circuit is represented by “positive” (without code) and that flowing out of the circuit by “negative” (- code).

RECOMMENDED OPERATING CONDITION (Ta = -20 – 75°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
Vcc	Supply voltage	Vcc1, Vcc2	Vcc1 and Vcc2 shall have the identical voltage.	4.0	5	5.5	V
Vi	Input voltage	LDI		0		Vcc	V
V _{IH}	“H” input voltage	IB1, IB2, INV		0.8Vcc		Vcc	V
V _{IL}	“L” input voltage	IB1, IB2, INV		0		0.2Vcc	V
I _{OH}	“H” output current	CLS, RDT, RCP		-0.5		0	mA
I _{OL}	“L” output current	CLS, RDT, RCP		0		5	mA
V _{IN}	Differential input voltage	HD2-HD1		3		80	mVp-p
f _{IN}	Input frequency	HD2-HD1		0.3		15	kHz
f _{osc}	Oscillation frequency		f _{osc} = 1/T _{osc}	0.2		2	MHz
C _{osc}	External capacitor	CX1, CX2	f _{osc} ∞ 1/C _{osc}	25		100	pF
C _{osc}	External capacitor	CX1, CX2	Reference value when corresponding to 210BPI		33		pF
R _{PK}	External resistor	AMP	Reference value when corresponding to 210BPI		470		Ω
C _{PK}	External capacitor	PKI	Reference value when corresponding to 210BPI		0.033		μF
C _{NF}	External capacitor	PKI, PKO	Reference value		220		pF
R _{PF}	External resistor	PKI, F2F	Reference value		4.7		MΩ
–	–				–		
C _{VC}	External capacitor	Vcc1, Vcc2	Reference value		0.1		μF
C _{VR}	External capacitor	VRF	Reference value	0.8	1	2	μF

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ELECTRICAL CHARACTERISTICS (Ta = -20 – 75°C and Vcc = 5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Test circuit	Limits			Unit	
					Min.	Typ.*	Max.		
VTH	Threshold voltage	IB1, IB2, INV	Vcc = 4 – 5.5V	–	0.3Vcc	–	0.7Vcc	V	
Vol	“L” output voltage	CLS, RDT, RCP	Vcc = 4V	IOL = 10μA	2	–	–	0.2	V
				IOL = 5mA	2	–	–	0.4	V
VoH	“H” output voltage	CLS, RDT, RCP	Vcc = 4V	IOH = -10μA	2	3.8	–	–	V
				IOH = -0.5mA	2	3.2	–	–	V
IIL	“L” input current	LDI, IB1, IB2	Vcc = 5.5V, Vi = 0V	2	-10	–	+10	μA	
IIL	“L” input current	INV	Vcc = 5.5V, Vi = 0V	2	-80	–	-10	mA	
IIH	“H” input current	LDI, IB1, IB2, INV	Vcc = 5.5V, Vi = 5.5V	2	-10	–	+10	μA	
IIT+	Positive threshold current	INV	Vcc = 5.5V, Vi = VTH	2	-250	–	-50	μA	
VREF	Reference voltage	VRF	VIN = 0mVp-p	1	2.3	2.5	2.7	V	
GV11	Voltage gain 1	OP1	fin = 1kHz VIN = 80mVp-p sine wave	3	18	20	24	Double	
GV21	Voltage gain 2	OP1	fin = 15kHz VIN = 80mVp-p sine wave	3	18	20	24	Double	
RIN1	Input resistance	OP1	fin = 1kHz VIN = 80mVp-p sine wave	3	7	10	14	kΩ	
VOPP1	Maximum output voltage	OP1	fin = 1kHz sine wave THD AMP = 5%	3	2	–	–	Vp-P	
IIL2	“L” sensitivity current	PKI – F2F	VM, F2F < 0.5V	4	–	–	-0.3	μA	
IIH2	“H” sensitivity current	PKI – F2F	VM, F2F > 4.5V	4	0.3	–	–	μA	
VTH+2	Positive threshold voltage	PKI – F2F	On the VRF basis	5	0.2	0.45	0.7	V	
VTH-2	Negative threshold voltage	PKI – F2F	On the VRF basis	5	-0.7	-0.45	-0.2	V	
VTHD2	Threshold differential voltage	PKI – F2F	(VTH+2) - VTH-2	–	-0.15	–	0.15	V	
VPKO	Pin voltage range	PKO	On the VRF basis IPKI = 1mA – +1mA	4	-1.2	–	1.2	V	
VOL3	“L” output voltage	F2F	VPKI = 0V, IF2F = 0.5mA	5	–	–	0.5	V	
VOH3	“H” output voltage	F2F	VPKI = 5V, IF2F = -0.5mA	5	4.5	–	–	V	
VTH+4	Positive threshold voltage	LDI		6	2.5	–	3.5	V	
VTH-4	Negative threshold voltage	LDI		6	1.5	–	2.7	V	
VHY4	Hysteresis width	LDI	(VTH+4) - (VTH-4)	–	0.5	–	1.5	V	
ICCW	Standby circuit current	Vcc1, Vcc2	VIN = 0mVp-p	1	–	0.7	1.0	mA	
ICCR	Operating circuit current	Vcc1, Vcc2	fin = 8.2kHz VIN = 68mVp-p sine wave fosc = 1MHz	1	–	1.9	2.4	mA	
fosc	Oscillation frequency	RCP	Cosc = 33pF	1	0.75	–	1.5	MHz	
TOW	Output pulse width	RCP	fosc = 1MHz	7	15	16	17	μs	
TOD	Intra-output delay time	RDT, RCP	fosc = 1MHz	7	7	8	9	μs	
TNW	Input noise width	INV		7	0.5	–	–	μs	

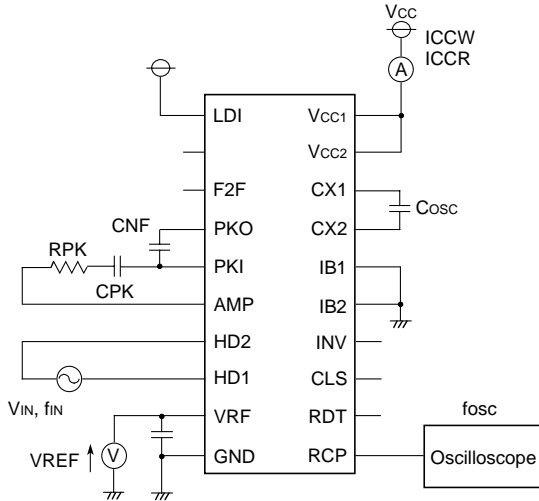
Note: Min. and max. limits do not represent absolute values.

*: Typ. limits represent standard values when Ta = 25°C and Vcc = 5V.

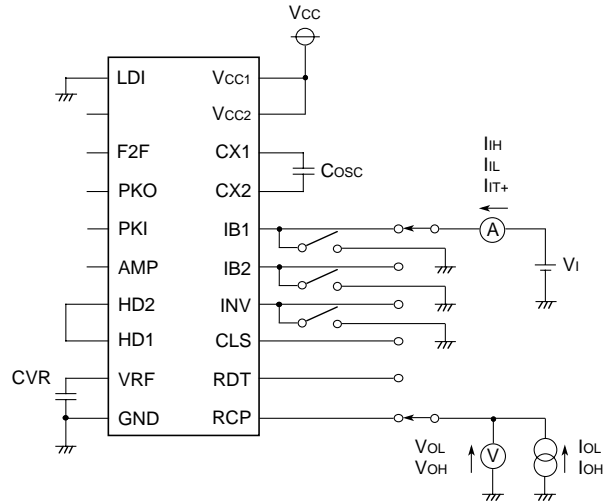
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TEST CIRCUIT: On the following drawing, $C_{osc} = 33\text{pF}$, $R_{PK} = 470\Omega$, $C_{PK} = 0.033\mu\text{F}$, $C_{NF} = 470\text{pF}$, $C_{VR} = 1\mu\text{F}$

1. Testing of VREF, ICCW, ICCR, fosc

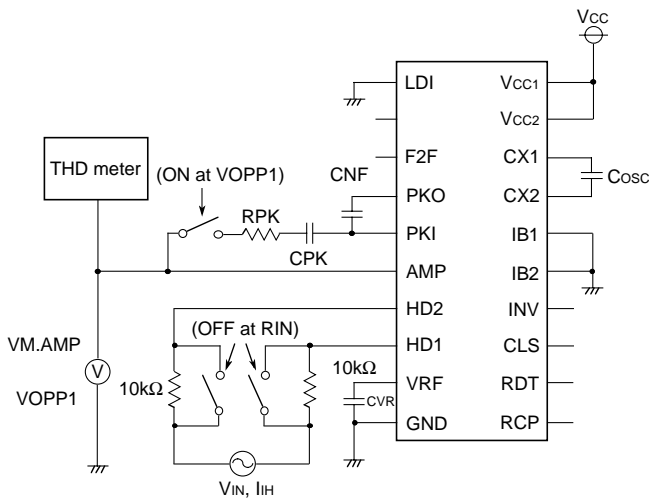


2. Testing of VOL, VOH, IIL, IIH, IIT+



Note: Short the IB1 and IB2 to the GND when those pins are not used for testing.

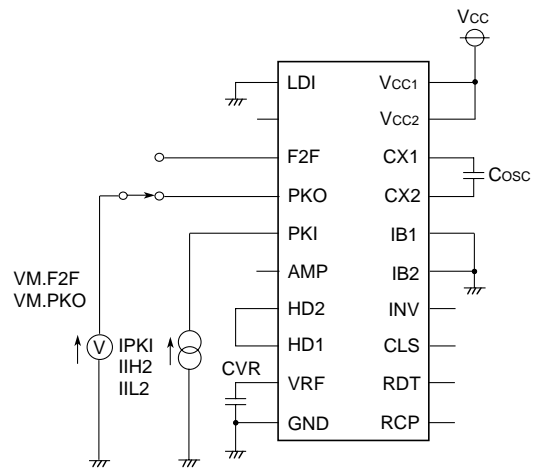
3. Testing of GV11, GV21, RIN1, VOPP1



$$GV11 = \frac{VM.AMP}{V_{IN}}$$

$$RIN1 = \frac{2VM.AMP}{GV11 \cdot V_{IN} - VM.AMP} \times 10(k\Omega)$$

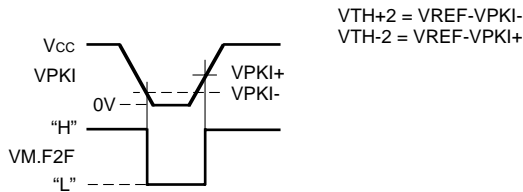
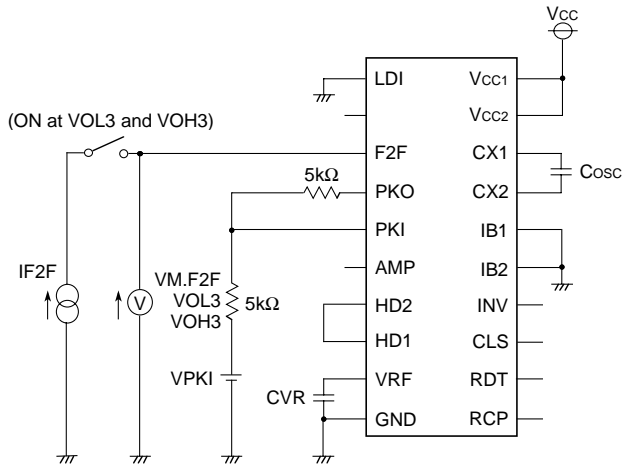
4. Testing of IIH2, IIL2, VPKO



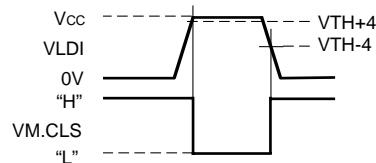
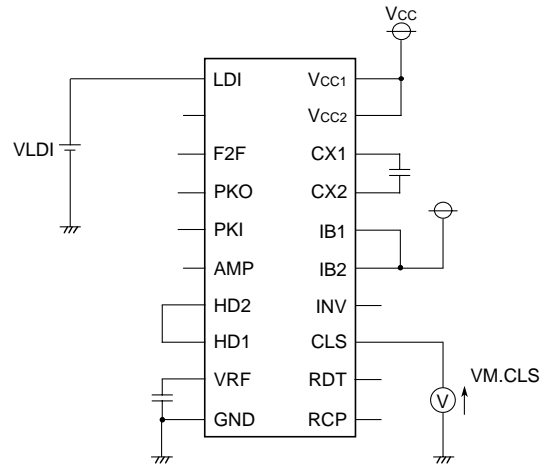
IIL2 is PKI input current providing $VM.F2F < 0.5V$.
 IIH2 is PKI input current providing $VM.F2F > 4.5V$.
 $VPKO = VM.PKO - VREF$

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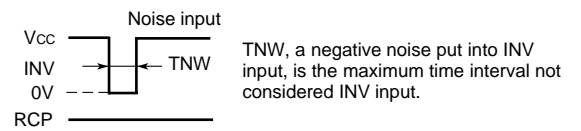
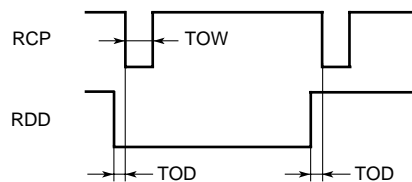
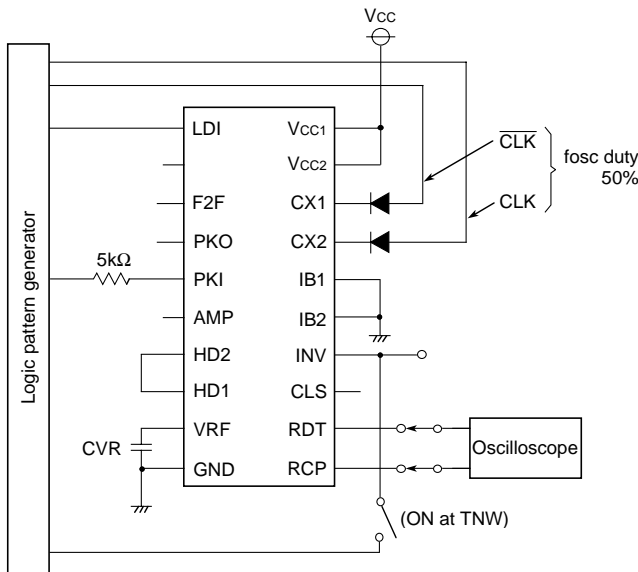
5. Testing of VTH+2, VTH-2, VOL3, VOH3



6. Testing of VTH+4, VTH-4



7. Testing of TOW, TOD, TNW



APPLICATION EXAMPLE

When setting the glance-over bit to 16 bits to let it be "L" active output

