

HN62W454 Series

524288-word $\times$ 8-bit/ 262144-word $\times$ 16-bit CMOS
Mask Programmable ROM

HITACHI

ADE-203-403A (Z)
Rev. 1.0
May. 9, 1996

Description

The HN62W454 is a 4-Mbit CMOS mask-Programmable ROM organized either as 262144 words by 16 bits or 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

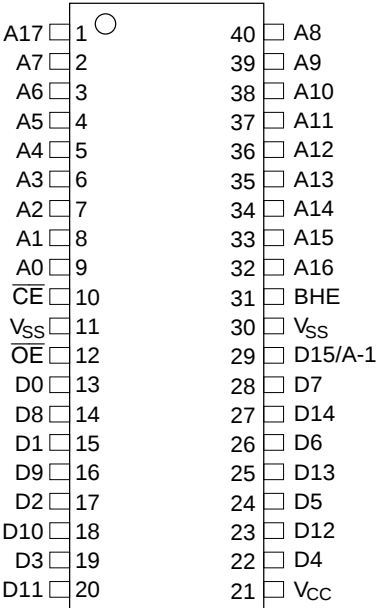
- Low voltage operation
 - Operating supply voltage: 3.3 V $\pm$ 0.3 V
- High speed
 - Access time: 120/150 ns (max)
- Low power
 - Active: 216 mW (max)
 - Standby: 108 μ W (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly LVTTL compatible
 - All inputs and outputs

Ordering Information

Type No.	Access time	Package
HN62W454P-12 HN62W454P-15	120 ns 150 ns	600 mil 40-pin plastic DIP (DP-40)
HN62W454FA-12 HN62W454FA-15	120 ns 150 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62W454TT-12 HN62W454TT-15	120 ns 150 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

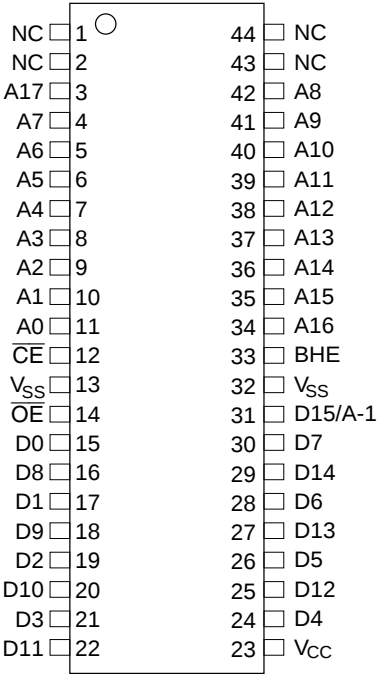
Pin Arrangement

HN62W454P Series



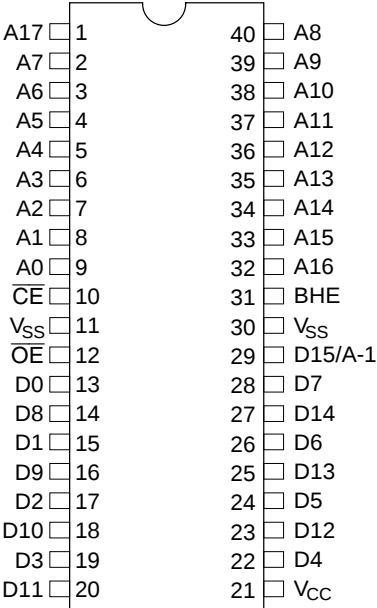
(Top view)

HN62W454TT Series



(Top view)

HN62W454FA Series

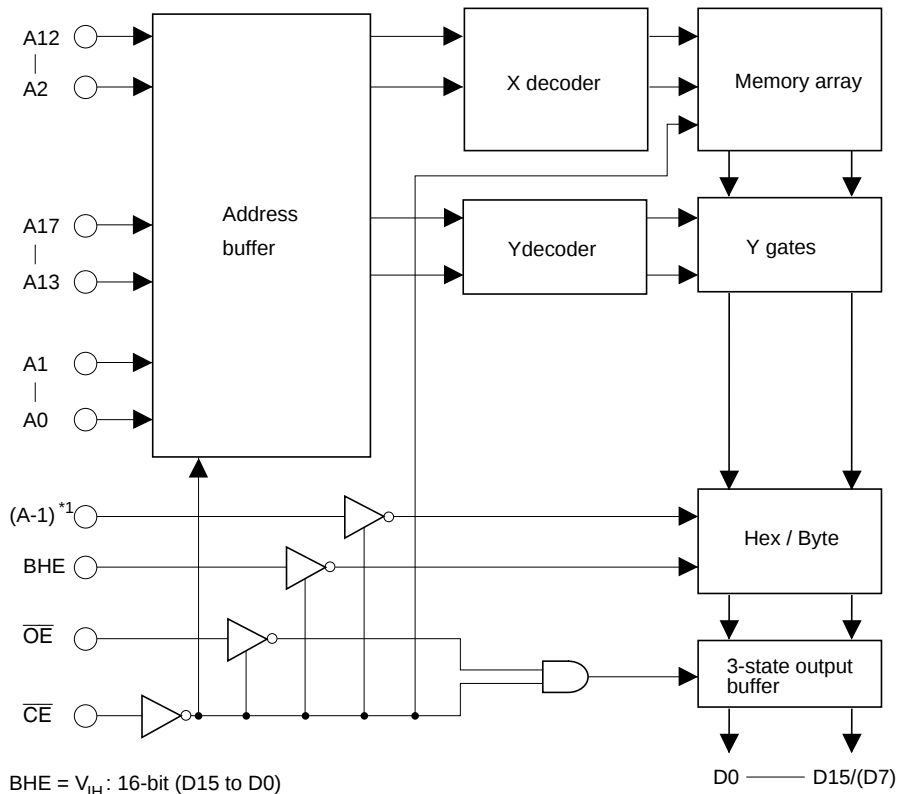


(Top view)

Pin Description

Pin name	Function
A-1, A0 to A17	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

Mode	Pin				Data output		Address input	
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	$\times^{*1}$	$\times$	$\times$	High-Z ^{*2}	High-Z	—	—
Output disable	L	H	$\times$	$\times$	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

Notes: 1. $\times$: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{*1}	V_{DD}	−0.3 to + 5.5	V
All input and output voltage ^{*1}	$V_{\text{in}}, V_{\text{out}}$	−0.3 to $V_{\text{DD}} + 0.3$	V
Operating temperature range	T_{opr}	0 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 125	°C
Temperature under bias	T_{bias}	−20 to + 85	°C

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_{\text{a}} = 0 \text{ to } + 70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	$V_{\text{DD}} + 0.3$	V
	V_{IL}	−0.3	—	0.8	V

DC Characteristics ($V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to } +70^{\circ}\text{C}$)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{DD}	—	60/50	mA	$V_{DD} = 3.6\text{ V}$, $I_{DOUT} = 0\text{ mA}$, $t_{RC} = 120/150\text{ ns}$
	Standby	I_{SB1}	—	30	μA	$V_{DD} = 3.6\text{ V}$, $\overline{CE} \geq V_{DD} - 0.2\text{ V}$
	Standby	I_{SB2}	—	3	mA	$V_{DD} = 3.6\text{ V}$, $\overline{CE} \geq 2.2\text{ V}$
Input leakage current		$ I_{IL} $	—	10	μA	$V_{in} = 0\text{ to } V_{DD}$
Output leakage current		$ I_{OL} $	—	10	μA	$\overline{CE} = 2.2\text{ V}$, $V_{out} = 0\text{ to } V_{DD}$
Output voltage		V_{OH}	2.4	—	V	$I_{OH} = -2.0\text{ mA}$
		V_{OL}	—	0.4	V	$I_{OL} = 2.0\text{ mA}$

Capacitance ($V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^{\circ}\text{C}$, $V_{in} = 0\text{ V}$, $f = 1\text{ MHz}$)

Parameter		Symbol	Min	Max	Unit
Input capacitance*1		Cin	—	10	pF
Output capacitance*1		Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics ($V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to } +70^{\circ}\text{C}$)

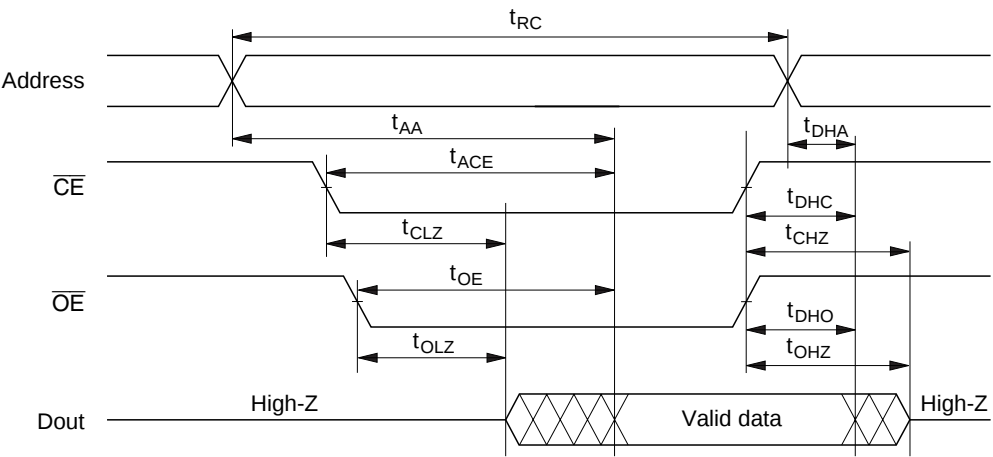
- Output load: 1TTL + $C_L = 100\text{ pF}$ (including jig)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference levels: 1.4 V
- Input rise and fall time: 5 ns

Parameter	Symbol	HN62W454-12		HN62W454-15		Unit	Note
		Min	Max	Min	Max		
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access	t_{AA}	—	120	—	150	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns	
BHE access time	t_{BHE}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	50	—	60	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	50	—	60	ns	1
BHE to output in high-Z	t_{BHZ}	—	50	—	60	ns	1
$\overline{CE}$ to output in low-Z	t_{CHZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

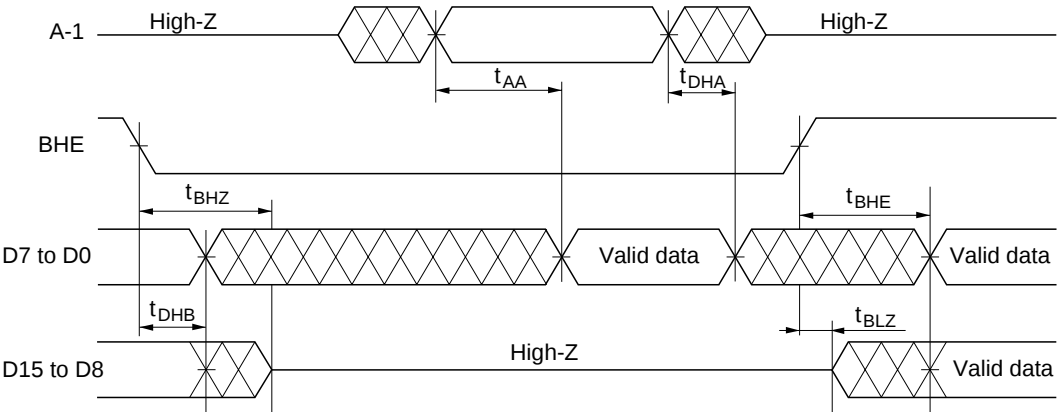
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



- Notes:
- 1. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
 - 2. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
 - 3. t_{CLZ} , t_{OLZ} : Determined by slower.

Word Mode, Byte Mode Switch



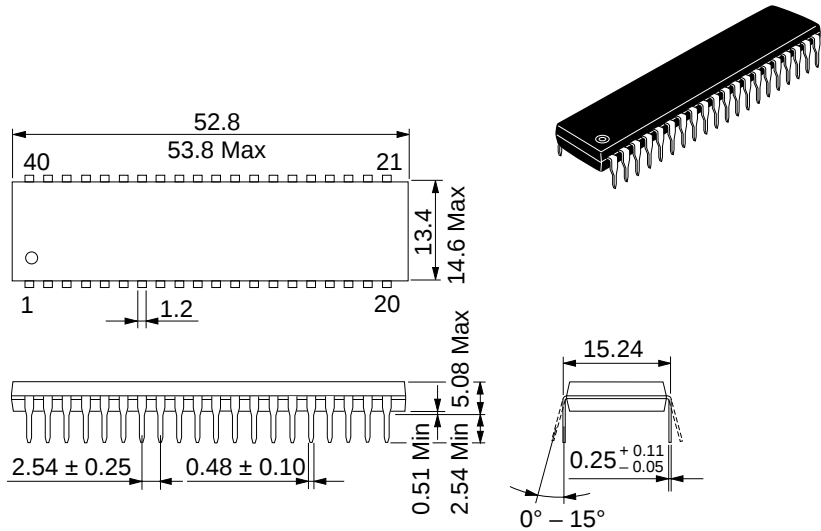
- Notes:
- 1. $\overline{CE}$ and $\overline{OE}$ are enable, A17 to A0 are valid.
 - 2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN62W454 Series

Package Dimensions

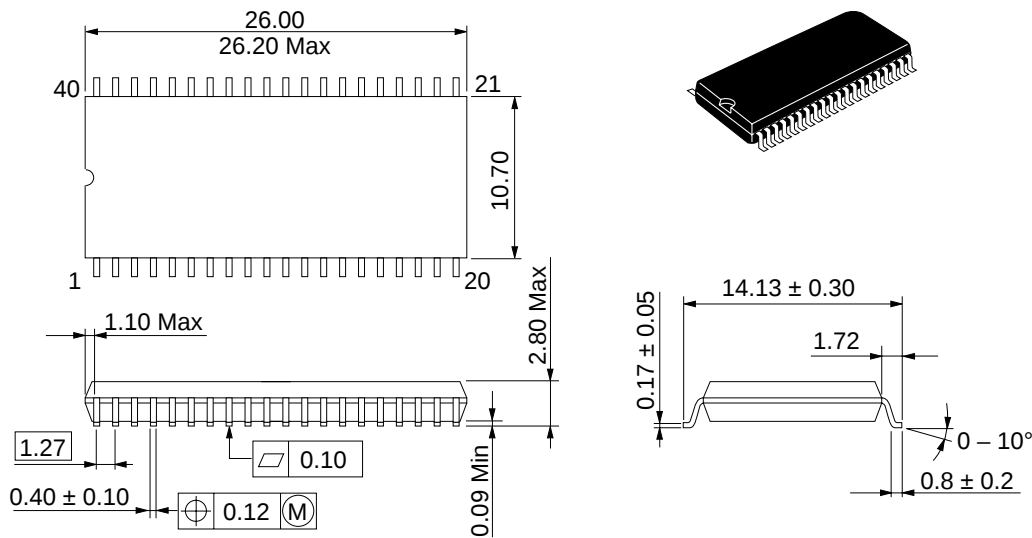
HN62W454P Series (DP-40)

Unit: mm



HN62W454FA Series (FP-40D)

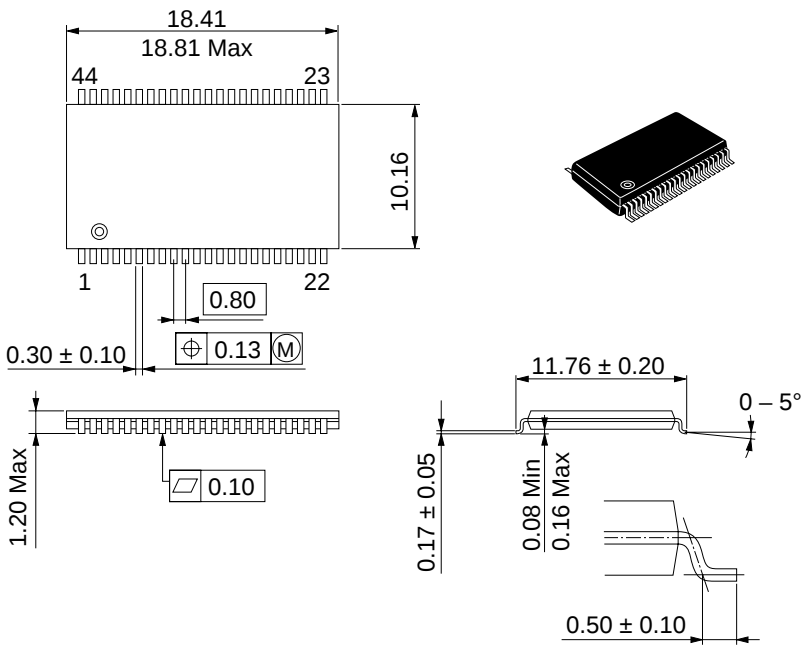
Unit: mm



Package Dimensions (cont.)

HN62W454TT Series (TTP-44D)

Unit: mm



When using this document, keep the following in mind:

- 1. This document may, wholly or partially, be subject to change without notice.
- 2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
- 3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
- 4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
- 5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
- 6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 21, 1995	Initial issue	M. Sirai	T. Wada
1.0	May. 9, 1996	Change of format Deletion of Preliminary		