

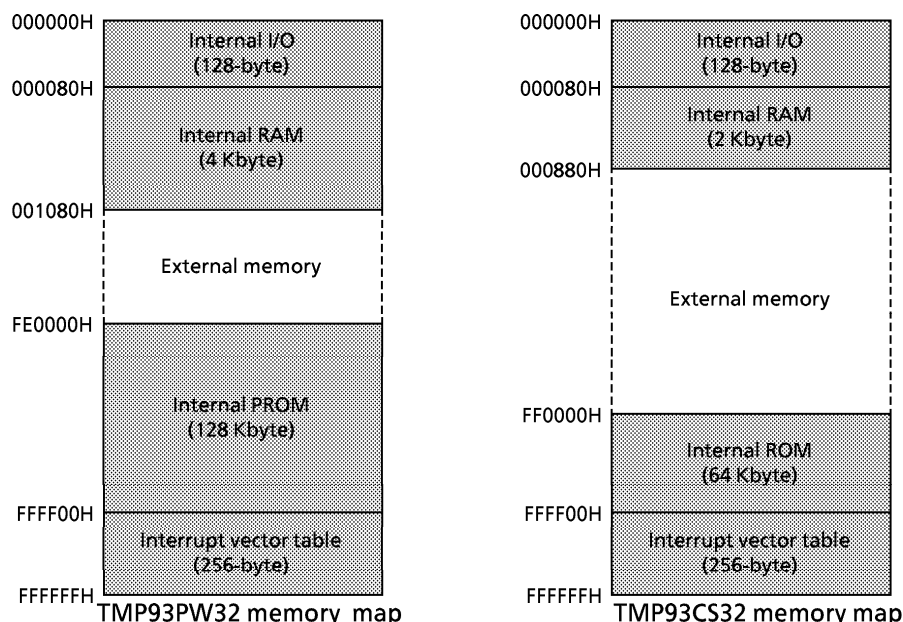
Low Voltage / Low Power CMOS 16-bit Micro-controller

### TMP93PW32F

**1. Outline and Device Characteristics**

The TMP93PW32 is OTP type MCU which includes 128 Kbyte One-time PROM. Using the adapter-socket (BM11132), you can write and verify the data for the TMP93PW32. The TMP93PW32F has the same pin-assignment as TMP93CS32 (Mask ROM type).

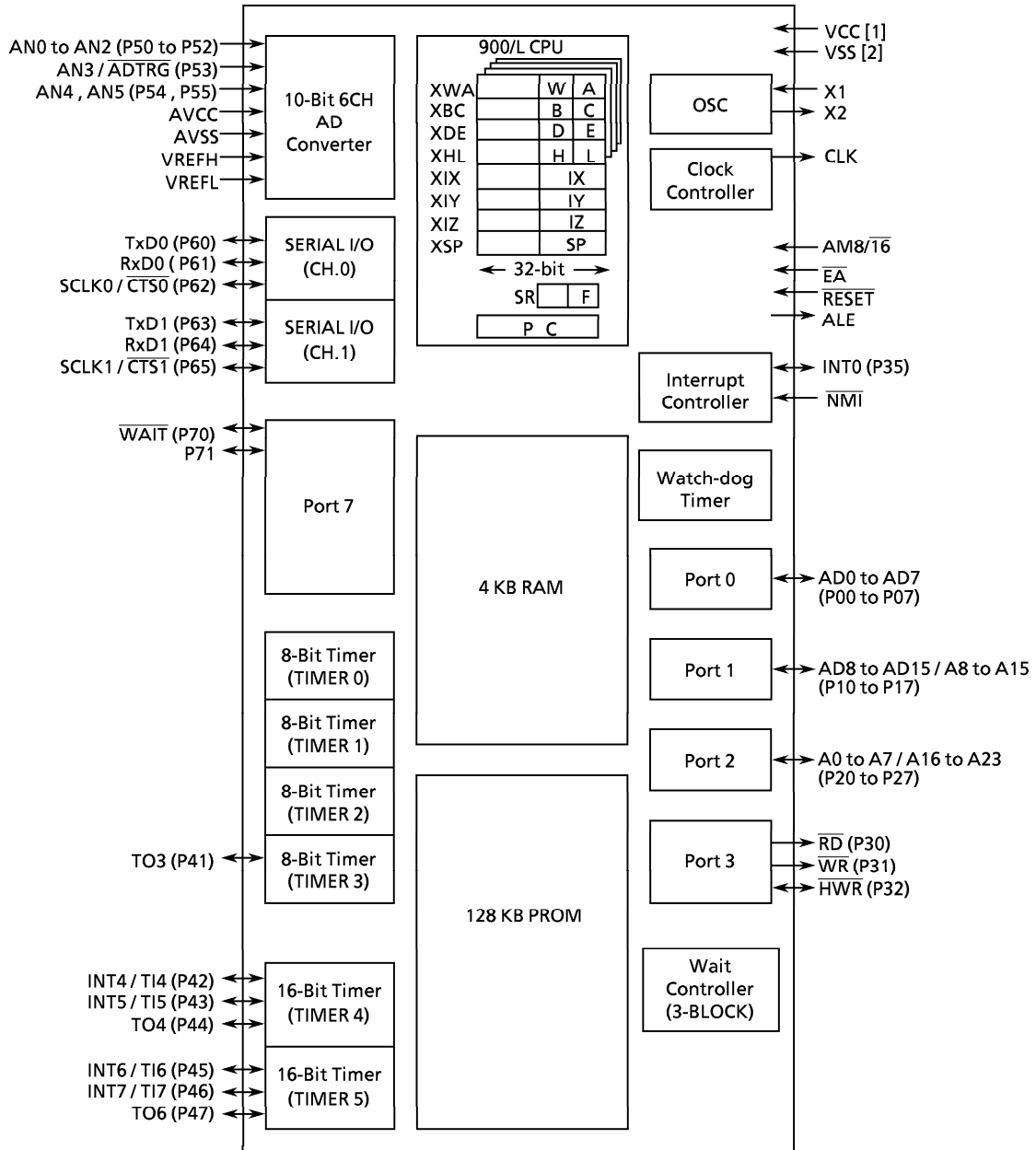
Writing the program to Built-in PROM, the TMP93PW32 operates as the same way as the TMP93CS32. The memory map and capacity of built in ROM and RAM are different between TMP93CS32 and TMP93PW32. The TMP93PW32 has the PROM of 128 Kbyte and the RAM of 4 Kbyte, and the TMP93CS32 has the ROM of 64 Kbyte and the RAM of 2 Kbyte. Following figure shows each memory map.



| MCU        | ROM           | RAM     | Package            | Adapter Socket |
|------------|---------------|---------|--------------------|----------------|
| TMP93PW32F | OTP 128 Kbyte | 4 Kbyte | P-QFP64-1414-0.80A | BM11132        |

000707EBP1

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Note: The items in parentheses ( ) are the initial setting after reset.

Figure 1.1 TMP93PW32 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for the TMP93PW32, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PW32F.

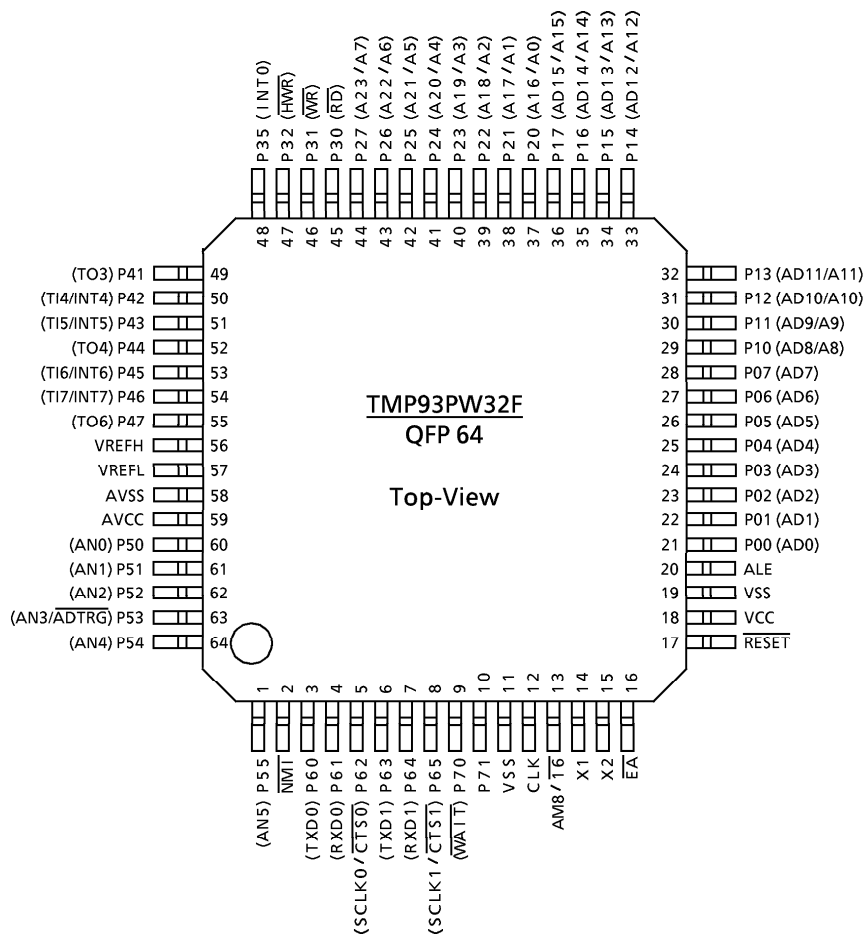


Figure 2.1.1 Pin Assignment (64-pin QFP)

## 2.2 Pin Names and Functions

The TMP93PW32 has MCU mode and PROM mode.

- (1) Table 2.2.1 shows pin function of TMP93PW32 in MCU mode.

Table 2.2.1 Pin Names and Function (1/3)

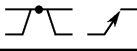
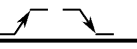

| Pin name                                   | Number of pins | I/O     | Functions  |
|--|----------------|---------|--|
| P00 to P07<br>/ AD0 to AD7                 | 8              | I/O     | Port 0: I/O port that allows selection of I/O on a bit basis   |
|  |                | 3-state | Address/data (lower): Bits 0 to 7 for address/data bus   |
| P10 to P17<br>/ AD8 to AD15<br>/ A8 to A15 | 8              | I/O     | Port 1: I/O port that allows selection of I/O on a bit basis   |
|  |                | 3-state | Address/data (upper): Bits 8 to 15 for address/data bus  |
|  |                | Output  | Address: Bits 8 to 15 for address bus  |
| P20 to P27<br>/ A0 to A7<br>/ A16 to A23   | 8              | I/O     | Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor)   |
|  |                | Output  | Address: Bits 0 to 7 for address bus   |
|  |                | Output  | Address: Bits 16 to 23 for address bus   |
| P30<br>/ $\overline{RD}$                   | 1              | Output  | Port 30: Output port   |
|  |                | Output  | Read: Strobe signal for reading external memory  |
| P31<br>/ $\overline{WR}$                   | 1              | Output  | Port 31: Output port   |
|  |                | Output  | Write: Strobe signal for writing data on pins AD0 to 7   |
| P32<br>/ $\overline{HWR}$                  | 1              | I/O     | Port 32: I/O port (with pull-up resistor)  |
|  |                | Output  | High write: Strobe signal for writing data on pins AD8 to 15   |
| P35<br>/ INT0                              | 1              | I/O     | Port 35: I/O port  |
|  |                | Input   | Interrupt request pin 0: Interrupt request pin with programmable level/rising edge      |
| P41<br>/ TO3                               | 1              | I/O     | Port 41: I/O port  |
|  |                | Output  | PWM output 3: 8-bit PWM timer 3 output   |
| P42<br>/ TI4<br>/ INT4                     | 1              | I/O     | Port 42: I/O port  |
|  |                | Input   | Timer input 4: Timer 4 count / capture trigger signal input  |
|  |                | Input   | Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge  |
| P43<br>/ TI5<br>/ INT5                     | 1              | I/O     | Port 43: I/O port  |
|  |                | Input   | Timer input 5: Timer 4 count / capture trigger signal input  |
|  |                | Input   | Interrupt request pin 5: Interrupt request pin with rising edge                         |
| P44<br>/ TO4                               | 1              | I/O     | Port 44: I/O port  |
|  |                | Output  | Timer output 4: Timer 4 output pin   |

Table 2.2.1 Pin Names and Function (2/3)

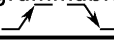

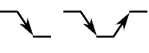
| Pin name  | Number of pins | I/O    | Functions   |
|---|----------------|--------|---|
| P45<br>/TI6<br>/INT6                                | 1              | I/O    | Port 45: I/O port   |
|   |                | Input  | Timer input 6: Timer 5 count / capture trigger signal input   |
|   |                | Input  | Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge   |
| P46<br>/TI7<br>/INT7                                | 1              | I/O    | Port 46: I/O port   |
|   |                | Input  | Timer input 7: Timer 5 count / capture trigger signal input   |
|   |                | Input  | Interrupt request pin 7: Interrupt request pin with rising edge    |
| P47<br>/TO6   | 1              | I/O    | Port 47: I/O port   |
|   |                | Output | Timer output 6: Timer 5 output pin  |
| P50 to P52,<br>P54, P55<br>/AN0 to AN2,<br>AN4, AN5 | 5              | Input  | Port 50 to Port 52, Port 54, Port 55: Input port  |
|   |                | Input  | Analog input: Analog signal input for AD converter  |
| P53<br>/AN3<br>/ADTRG                               | 1              | Input  | Port53: Input Port  |
|   |                | Input  | Analog input: Analog signal input for AD converter  |
|   |                | Input  | AD converter external start trigger input   |
| P60<br>/TXD0  | 1              | I/O    | Port 60: I/O port (with pull-up resistor)   |
|   |                | Output | Serial send data 0  |
| P61<br>/RXD0  | 1              | I/O    | Port 61: I/O port (with pull-up resistor)   |
|   |                | Input  | Serial receive data 0   |
| P62<br>/CTS0<br>/SCLK0                              | 1              | I/O    | Port 62: I/O port (with pull-up resistor)   |
|   |                | Input  | Serial data send enable 0 (Clear to Send)   |
|   |                | I/O    | Serial Clock I/O 0  |
| P63<br>/TXD1  | 1              | I/O    | Port 63: I/O port (with pull-up resistor)   |
|   |                | Output | Serial send data 1  |
| P64<br>/RXD1  | 1              | I/O    | Port 64: I/O port (with pull-up resistor)   |
|   |                | Input  | Serial receive data 1   |
| P65<br>/CTS1<br>/SCLK1                              | 1              | I/O    | Port 65: I/O port (with pull-up resistor)   |
|   |                | Input  | Serial data send enable 1 (Clear to Send)   |
|   |                | I/O    | Serial clock I/O 1  |
| P70<br>/WAIT  | 1              | I/O    | Port 70: I/O port (High current output available)   |
|   |                | Input  | WAIT: Pin used to request CPU bus wait (It is active in 1 WAIT + N mode. Set by the Bus-width/wait control register.)   |
| P71   | 1              | I/O    | Port 71: I/O port (High current output available)   |
| NMI   | 1              | Input  | Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program.  |
| CLK   | 1              | Output | Clock output: Outputs "f <sub>SYS</sub> ÷ 2" Clock.<br>Pulled-up during reset.<br>Can be disabled for reducing noise.   |
| EA  | 1              | Input  | "1" should be inputted with TMP93PW32   |

Table 2.2.1 Pin Names and Function (3/3)

| Pin name                  | Number of pins | I/O    | Functions  |
|---------------------------|----------------|--------|--|
| AM8 / $\overline{16}$     | 1              | Input  | Address Mode: Selects external Data Bus width.<br>"1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register. |
| ALE                       | 1              | Output | Address Latch Enable<br>Can be disabled for reducing noise.  |
| $\overline{\text{RESET}}$ | 1              | Input  | Reset: Initializes TMP93PW32. (With pull-up resistor)  |
| VREFH                     | 1              | Input  | Pin for high level reference voltage input to AD converter   |
| VREFL                     | 1              | Input  | Pin for low level reference voltage input to AD converter  |
| AVCC                      | 1              | Input  | Power supply pin for AD converter  |
| AVSS                      | 1              | Input  | GND pin for AD converter (0 V)   |
| X1                        | 1              | Input  | Oscillator connecting pin  |
| X2                        | 1              | Output | Oscillator connecting pin  |
| VCC                       | 1              | Input  | Power supply pin   |
| VSS                       | 2              | Input  | GND pin (All VSS pins are connected to the GND (0 V).)   |

Note: Built-in pull-up resistors can be released from the pins other than the  $\overline{\text{RESET}}$  pin by software.

## (2) PROM mode

Table 2.2.2 shows pin function of the TMP93PW32 in PROM mode.

Table 2.2.2 Pin Name and function of PROM mode

| Pin function  | Number of pins | Input/Output | Function                                | Pin name (MCU mode)    |
|---|----------------|--------------|---|------------------------|
| A7 to A0  | 8              | Input        | Memory address of program               | P27 to P20             |
| A15 to A8   | 8              | Input        |   | P17 to P10             |
| A16   | 1              | Input        |   | P71                    |
| D7 to D0  | 8              | I/O          | Memory data of program                  | P07 to P00             |
| $\overline{\text{CE}}$  | 1              | Input        | Chip enable                             | P32                    |
| $\overline{\text{OE}}$  | 1              | Input        | Output control                          | P30                    |
| $\overline{\text{PGM}}$   | 1              | Input        | Program control                         | P31                    |
| VPP   | 1              | Power supply | 12.75 V / 5 V (Power supply of program) | $\overline{\text{EA}}$ |
| VCC   | 2              | Power supply | 6.25 V / 5 V                            | VCC, AVCC              |
| VSS   | 3              | Power supply | 0 V                                     | VSS, AVSS              |
| Pin function  | Number of pins | Input/Output | Disposal of pin                         |                        |
| P60   | 1              | Input        | Fix to low level (security pin)         |                        |
| $\overline{\text{RESET}}$   | 1              | Input        | Fix to low level (PROM mode)            |                        |
| CLK   | 1              | Input        |   |                        |
| ALE   | 1              | Output       | Open                                    |                        |
| X1  | 1              | Input        | Self oscillation with resonator         |                        |
| X2  | 1              | Output       |   |                        |
| P65 to P61<br>AM8 / $\overline{\text{T6}}$  | 6              | Input        | Fix to high level                       |                        |
| P35<br>P47 to P41<br>P55 to P50<br>P70<br>VREFH<br>VREFL<br>$\overline{\text{NMI}}$ | 18             | I/O          | Open                                    |                        |

### 3. Operation

This section describes the functions and basic operational blocks of the TMP93PW32.

The TMP93PW32 has PROM in place of the mask ROM which is included in the TMP93CS32. The other configuration and functions are the same as the TMP93CS32. Regarding the functions of the TMP93PW32 (not described), see the part of TMP93CS32.

The TMP93PW32 has two operational modes: MCU mode and PROM mode.

#### 3.1 MCU mode

##### (1) Mode-setting and function

The MCU mode is set by opening the CLK pin (pin open). In the MCU mode, the operation is same as TMP93CS32 except the followings.

##### (2) Memory-map

The memory map of TMP93PW32 is not same as that of TMP93CS32. Figure 3.1.1 shows the memory map in MCU mode. Figure 3.1.2 show that in PROM mode.

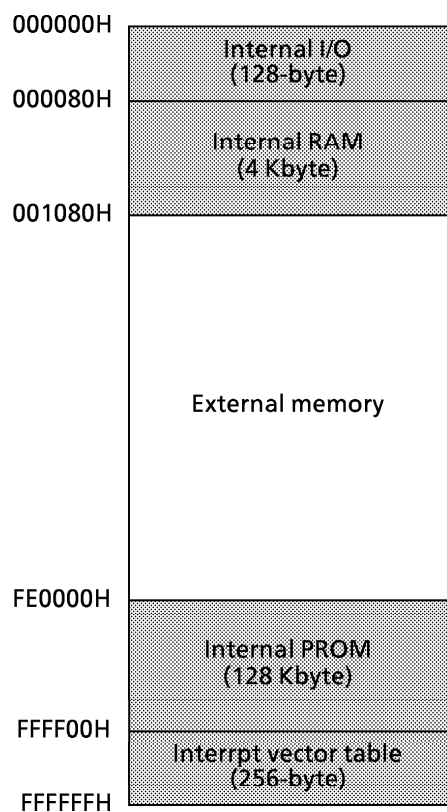


Figure 3.1.1 Memory map in MCU mode

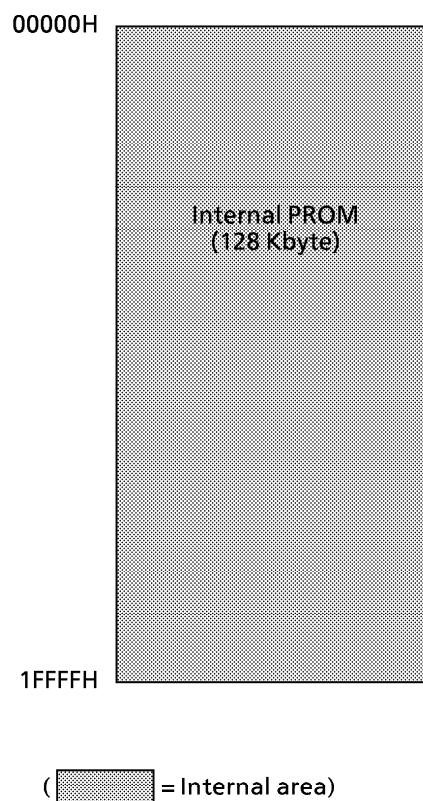


Figure 3.1.2 Memory map in PROM mode



(3) Care point of bus width / wait controller

The built in RAM capacity of the TMP93PW32 is larger than that of the TMP93CS32, therefor the following point is different about the accessing area of WAITC1.

Setting WAITC1 <B1C1to 0> to "00"

|                |              |
|----------------|--------------|
| TMP93PW32      | TMP93CS32    |
| 1080H to 7FFFH | 880 to 7FFFH |

WAITC0 and WAITC2 addressing area are the same as TMP93CS32.

## 4. Electrical Characteristics

## 4.1 Absolute Maximum Ratings (TMP93PW32)

“X” used in an expression shows a cycle of clock  $f_{PPH}$ . If a clock gear or a low speed oscillator is selected, a value of “X” is different. The value as an example is gear = 1/ $f_c$  (SYSCR1 < GEAR 2 to 0 > = “000”).

| Parameter                            | Symbol              | Rating        | Unit                           |
|--------------------------------------|---------------------|---------------|--------------------------------|
| Power Supply Voltage                 | V <sub>CC</sub>     | - 0.5 to 6.5  | V                              |
| Input Voltage                        | V <sub>IN</sub>     | except EA pin | - 0.5 to V <sub>CC</sub> + 0.5 |
|                                      |                     | EA pin        | - 0.5 to 14.0                  |
| Output current (Per 1 pin) P7        | I <sub>OL1</sub>    | 20            | mA                             |
| Output current (Per 1 pin) except P7 | I <sub>OL2</sub>    | 2             | mA                             |
| Output Current (total)               | ∑ I <sub>OL</sub>   | 120           | mA                             |
| Output Current (total)               | ∑ I <sub>OH</sub>   | - 80          | mA                             |
| Power Dissipation (Ta = 85°C)        | P <sub>D</sub>      | 350           | mW                             |
| Soldering Temperature (10 s)         | T <sub>SOLDER</sub> | 260           | °C                             |
| Storage Temperature                  | T <sub>STG</sub>    | - 65 to 150   | °C                             |
| Operating Temperature                | T <sub>OPR</sub>    | - 40 to 85    | °C                             |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (1/2)

Ta = - 40 to 85°C

| Parameter  | Symbol                  | Condition   | Min  | Typ. (Note)           | Max                   | Unit |
|--|-------------------------|---|--|-----------------------|-----------------------|------|
| Power Supply Voltage<br>(AV <sub>CC</sub> = V <sub>CC</sub><br>AV <sub>SS</sub> = V <sub>SS</sub> = 0 V) | V <sub>CC</sub>         | f <sub>c</sub> = 4 to 20 MHz  | 4.5  |                       | 5.5                   | V    |
|  |                         | f <sub>c</sub> = 4 to 12.5 MHz  | 2.7  |                       |                       |      |
| Input<br>Low Voltage   | AD0 to 15               | V <sub>IL</sub>   | V <sub>CC</sub> ≥ 4.5 V<br>V <sub>CC</sub> < 4.5 V |                       | 0.8<br>0.6            | V    |
|  | Port2 to 7 (except P35) | V <sub>IL1</sub>  | V <sub>CC</sub> = 2.7 to 5.5 V                     | - 0.3                 | 0.3 V <sub>CC</sub>   |      |
|  | RESET, NMI, INTO        | V <sub>IL2</sub>  |  |                       | 0.25 V <sub>CC</sub>  |      |
|  | EA, AM8/16              | V <sub>IL3</sub>  |  |                       | 0.3                   |      |
|  | X1                      | V <sub>IL4</sub>  |  |                       | 0.2 V <sub>CC</sub>   |      |
| Input<br>High Voltage  | AD0 to 15               | V <sub>IH</sub>   | V <sub>CC</sub> ≥ 4.5 V<br>V <sub>CC</sub> < 4.5 V | 2.2<br>2.0            | V <sub>CC</sub> + 0.3 | V    |
|  | Port2 to 7 (except P35) | V <sub>IH1</sub>  | V <sub>CC</sub> = 2.7 to 5.5 V                     | 0.7 V <sub>CC</sub>   |                       |      |
|  | RESET, NMI, INTO        | V <sub>IH2</sub>  |  | 0.75 V <sub>CC</sub>  |                       |      |
|  | EA, AM8/16              | V <sub>IH3</sub>  |  | V <sub>CC</sub> - 0.3 |                       |      |
|  | X1                      | V <sub>IH4</sub>  |  | 0.8 V <sub>CC</sub>   |                       |      |
| Output Low Voltage   | V <sub>OL</sub>         | I <sub>OL</sub> = 1.6 mA<br>(V <sub>CC</sub> = 2.7 to 5.5 V)                            |  |                       | 0.45                  | V    |
| Output Low current (P7)  | I <sub>OL7</sub>        | V <sub>OL</sub> = 1.0 V; (V <sub>CC</sub> = 5 V ± 10%)<br>(V <sub>CC</sub> = 3 V ± 10%) | 16<br>7  |                       |                       | mA   |
| Output High Voltage  | V <sub>OH1</sub>        | I <sub>OH</sub> = - 400 μA<br>(V <sub>CC</sub> = 3 V ± 10%)                             | 2.4  |                       |                       | V    |
|  | V <sub>OH2</sub>        | I <sub>OH</sub> = - 400 μA<br>(V <sub>CC</sub> = 5 V ± 10%)                             | 4.2  |                       |                       |      |

Note: Typical values are for Ta = 25°C and V<sub>CC</sub> = 5 V unless otherwise noted.

## 4.2 DC Characteristics (2/2)

| Parameter  | Symbol               | Condition  | Min   | Typ.(Note1)                                  | Max      | Unit          |     |    |
|--|----------------------|--|---|--|----------|---------------|-----|----|
| Darlington Drive Current<br>(8 Output Pins max.) | $I_{DAR}$<br>(Note2) | $V_{EXT} = 1.5\text{ V}$<br>$R_{EXT} = 1.1\text{ k}\Omega$<br>( $V_{CC} = 5\text{ V} \pm 10\%$ only) | -1.0  |  | -3.5     | mA            |     |    |
| Input Leakage Current                            | $I_{LI}$             | $0.0 \leq V_{IN} \leq V_{CC}$  |   | 0.02   | $\pm 5$  | $\mu\text{A}$ |     |    |
| Output Leakage Current                           | $I_{LO}$             | $0.2 \leq V_{IN} \leq V_{CC} - 0.2$  |   | 0.05   | $\pm 10$ |               |     |    |
| Power Down Voltage<br>(at STOP, RAM Back up)     | $V_{STOP}$           | $V_{IL2} = 0.2 V_{CC}$ ,<br>$V_{IH2} = 0.8 V_{CC}$   | 2.0   |  | 6.0      | V             |     |    |
| $\overline{\text{RESET}}$<br>Pull Up Resistance  | $R_{RST}$            | $V_{CC} = 5.5\text{ V}$  | 45  |  | 130      | k $\Omega$    |     |    |
|  |                      | $V_{CC} = 4.5\text{ V}$  | 50  |  | 160      |               |     |    |
|  |                      | $V_{CC} = 3.3\text{ V}$  | 70  |  | 280      |               |     |    |
|  |                      | $V_{CC} = 2.7\text{ V}$  | 90  |  | 400      |               |     |    |
| Pin Capacitance                                  | $C_{IO}$             | $f_c = 1\text{ MHz}$   |   |  | 10       | pF            |     |    |
| Schmitt Width<br>RESET, NMI, INTO                | $V_{TH}$             |  | 0.4   | 1.0  |          | V             |     |    |
| Programmable<br>Pull Up Resistance               | $R_{KH}$             | $V_{CC} = 5.5\text{ V}$  | 45  |  | 130      | k $\Omega$    |     |    |
|  |                      | $V_{CC} = 4.5\text{ V}$  | 50  |  | 160      |               |     |    |
|  |                      | $V_{CC} = 3.3\text{ V}$  | 70  |  | 280      |               |     |    |
|  |                      | $V_{CC} = 2.7\text{ V}$  | 90  |  | 400      |               |     |    |
| NORMAL (Note3)                                   | $I_{CC}$             | $V_{CC} = 5\text{ V} \pm 10\%$<br>$f_c = 20\text{ MHz}$  |   | 25   | 30       | mA            |     |    |
| RUN  |                      |  |   | 22   | 27       |               |     |    |
| IDLE2  |                      |  |   | 13   | 17       |               |     |    |
| IDLE1  |                      |  |   | 3.4  | 5        |               |     |    |
| NORMAL (Note3)                                   |                      |  | $V_{CC} = 3\text{ V} \pm 10\%$<br>$f_c = 12.5\text{ MHz}$<br>(Typ.: $V_{CC} = 3.0\text{ V}$ ) |  | 8.0      |               | 11  |    |
| RUN  |                      |  |   |  | 7.0      |               | 10  |    |
| IDLE2  |                      |  |   | 4.2  | 6        |               |     |    |
| IDLE1  |                      |  |   | 1.2  | 1.8      |               |     |    |
| STOP   |                      | $T_a \leq 50^\circ\text{C}$  |   | $V_{CC} = 2.7\text{ V}$<br>to $5.5\text{ V}$ |          |               |     | 10 |
|  |                      | $T_a \leq 70^\circ\text{C}$  |   |  |          |               | 0.2 | 20 |
|  |                      | $T_a \leq 85^\circ\text{C}$  |   |  |          |               | 50  |    |

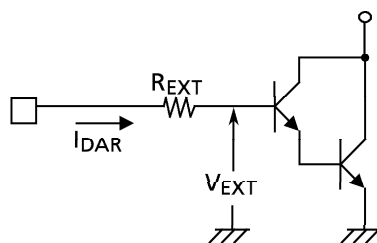
Note 1: Typical values are for  $T_a = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$  unless otherwise noted.

Note 2:  $I_{DAR}$  is guranteed for total of up to 8 ports.

Note 3:  $I_{CC}$  measurement conditions (NORMAL, SLOW):

Only CPU is operational ; output pins are open and input pins are fixed.

(Reference) Definition of  $I_{DAR}$



## 4.3 AC Electrical Characteristics

(1)  $V_{CC} = 5\text{ V} \pm 10\%$ 

| No. | Parameter  | Symbol            | Variable  |            | 16 MHz |     | 20 MHz |     | Unit |
|-----|--|-------------------|-----------|------------|--------|-----|--------|-----|------|
|     |  |                   | Min       | Max        | Min    | Max | Min    | Max |      |
| 1   | Osc. Period (= x)  | t <sub>OSC</sub>  | 50        | 31250      | 62.5   |     | 50     |     | ns   |
| 2   | CLK pulse width  | t <sub>CLK</sub>  | 2x - 40   |            | 85     |     | 60     |     | ns   |
| 3   | A0 to 23 Valid → CLK Hold  | t <sub>AK</sub>   | 0.5x - 20 |            | 11     |     | 5      |     | ns   |
| 4   | CLK Valid → A0 to 23 Hold  | t <sub>KA</sub>   | 1.5x - 70 |            | 24     |     | 5      |     | ns   |
| 5   | A0 to 15 Valid → ALE fall  | t <sub>AL</sub>   | 0.5x - 15 |            | 16     |     | 10     |     | ns   |
| 6   | ALE fall → A0 to 15 Hold   | t <sub>LA</sub>   | 0.5x - 20 |            | 11     |     | 5      |     | ns   |
| 7   | ALE High pulse width   | t <sub>LL</sub>   | x - 40    |            | 23     |     | 10     |     | ns   |
| 8   | ALE fall → RD/WR fall  | t <sub>LC</sub>   | 0.5x - 25 |            | 6      |     | 0      |     | ns   |
| 9   | RD/WR rise → ALE rise  | t <sub>CL</sub>   | 0.5x - 20 |            | 11     |     | 5      |     | ns   |
| 10  | A0 to 15 Valid → RD/WR fall  | t <sub>ACL</sub>  | x - 25    |            | 38     |     | 25     |     | ns   |
| 11  | A0 to 23 Valid → RD/WR fall  | t <sub>ACH</sub>  | 1.5x - 50 |            | 44     |     | 25     |     | ns   |
| 12  | RD/WR rise → A0 to 23 Hold   | t <sub>CA</sub>   | 0.5x - 25 |            | 6      |     | 0      |     | ns   |
| 13  | A0 to 15 Valid → D0 to 15 input  | t <sub>ADL</sub>  |           | 3.0x - 55  |        | 133 |        | 95  | ns   |
| 14  | A0 to 23 Valid → D0 to 15 input  | t <sub>ADH</sub>  |           | 3.5x - 65  |        | 154 |        | 110 | ns   |
| 15  | RDfall → D0 to 15 input  | t <sub>RD</sub>   |           | 2.0x - 60  |        | 65  |        | 40  | ns   |
| 16  | RD Low pulse width   | t <sub>RR</sub>   | 2.0x - 40 |            | 85     |     | 60     |     | ns   |
| 17  | RDrise → D0 to 15 Hold   | t <sub>HR</sub>   | 0         |            | 0      |     | 0      |     | ns   |
| 18  | RDrise → A0 to 15output  | t <sub>RAE</sub>  | x - 15    |            | 48     |     | 35     |     | ns   |
| 19  | WR Low pulse width   | t <sub>WW</sub>   | 2.0x - 40 |            | 85     |     | 60     |     | ns   |
| 20  | D0 to 15 Valid → WR rise   | t <sub>DW</sub>   | 2.0x - 55 |            | 70     |     | 45     |     | ns   |
| 21  | WR rise → D0 to 15 Hold  | t <sub>WD</sub>   | 0.5x - 15 |            | 16     |     | 10     |     | ns   |
| 22  | A0 to 23 Valid → $\overline{\text{WAIT}}$ input <sup>(1 WAIT + n mode)</sup> | t <sub>AWH</sub>  |           | 3.5x - 90  |        | 129 |        | 85  | ns   |
| 23  | A0 to 15 Valid → $\overline{\text{WAIT}}$ input <sup>(1 WAIT + n mode)</sup> | t <sub>AWL</sub>  |           | 3.0x - 80  |        | 108 |        | 70  | ns   |
| 24  | RD/WR fall → $\overline{\text{WAIT}}$ Hold <sup>(1 WAIT + n mode)</sup>      | t <sub>CW</sub>   | 2.0x + 0  |            | 125    |     | 100    |     | ns   |
| 25  | A0 to 23 Valid → PORT input  | t <sub>APH</sub>  |           | 2.5x - 120 |        | 36  |        | 5   | ns   |
| 26  | A0 to 23 Valid → PORT Hold   | t <sub>APH2</sub> | 2.5x + 50 |            | 206    |     | 175    |     | ns   |
| 27  | WR rise → PORT Valid   | t <sub>CP</sub>   |           | 200        |        | 200 |        | 200 | ns   |

## AC Measuring Conditions

- Output Level: High 2.2 V / Low 0.8 V, CL = 50 pF  
(However CL = 100 pF for AD0 to AD15, A0 to A23, ALE,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{HWR}}$ , CLK)
- Input Level: High 2.4 V / Low 0.45 V (AD0 to AD15)  
High  $0.8 \times V_{CC}$  / Low  $0.2 \times V_{CC}$  (Except for AD0 to AD15)

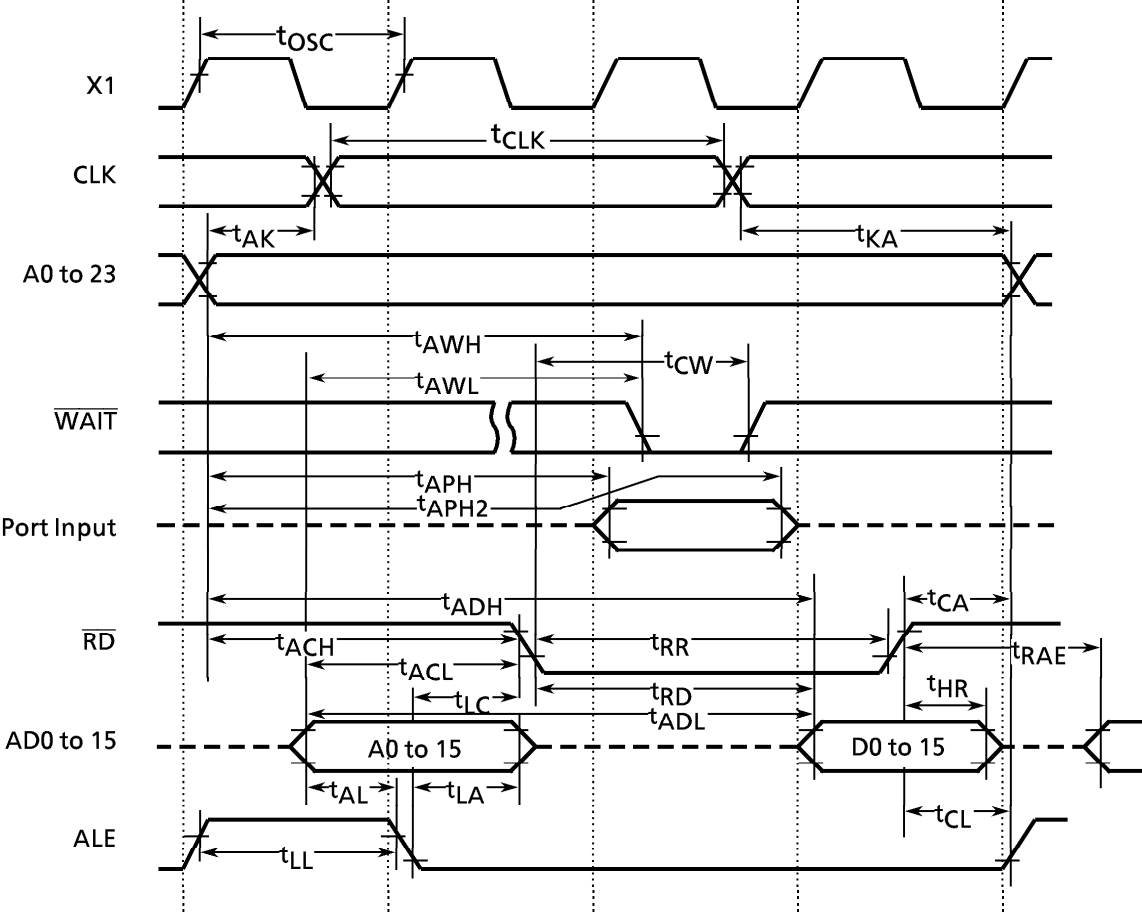
(2)  $V_{CC} = 3\text{ V} \pm 10\%$ 

| No. | Parameter   | Symbol     | Variable     |              | 12.5 MHz |     | Unit |
|-----|---|------------|--------------|--------------|----------|-----|------|
|     |   |            | Min          | Max          | Min      | Max |      |
| 1   | Osc. Period (= x)   | $t_{OSC}$  | 80           | 31250        | 80       |     | ns   |
| 2   | CLK pulse width   | $t_{CLK}$  | $2x - 40$    |              | 120      |     | ns   |
| 3   | A0 to 23 Valid → CLK Hold   | $t_{AK}$   | $0.5x - 30$  |              | 10       |     | ns   |
| 4   | CLK Valid → A0 to 23 Hold   | $t_{KA}$   | $1.5x - 80$  |              | 40       |     | ns   |
| 5   | A0 to 15 Valid → ALE fall   | $t_{AL}$   | $0.5x - 35$  |              | 5        |     | ns   |
| 6   | ALE fall → A0 to 15 Hold  | $t_{LA}$   | $0.5x - 35$  |              | 5        |     | ns   |
| 7   | ALE High pulse width  | $t_{LL}$   | $x - 60$     |              | 20       |     | ns   |
| 8   | ALE fall → RD/WR fall   | $t_{LC}$   | $0.5x - 35$  |              | 5        |     | ns   |
| 9   | RD/WR rise → ALE rise   | $t_{CL}$   | $0.5x - 40$  |              | 0        |     | ns   |
| 10  | A0 to 15 Valid → RD/WR fall   | $t_{ACL}$  | $x - 50$     |              | 30       |     | ns   |
| 11  | A0 to 23 Valid → RD/WR fall   | $t_{ACH}$  | $1.5x - 50$  |              | 70       |     | ns   |
| 12  | RD/WR rise → A0 to 23 Hold  | $t_{CA}$   | $0.5x - 40$  |              | 0        |     | ns   |
| 13  | A0 to 15 Valid → D0 to 15 input   | $t_{ADL}$  |              | $3.0x - 110$ |          | 130 | ns   |
| 14  | A0 to 23 Valid → D0 to 15 input   | $t_{ADH}$  |              | $3.5x - 125$ |          | 155 | ns   |
| 15  | $\overline{RD}$ fall → D0 to 15 input   | $t_{RD}$   |              | $2.0x - 115$ |          | 45  | ns   |
| 16  | $\overline{RD}$ Low pulse width   | $t_{RR}$   | $2.0x - 40$  |              | 120      |     | ns   |
| 17  | $\overline{RD}$ rise → D0 to 15 Hold  | $t_{HR}$   | 0            |              | 0        |     | ns   |
| 18  | $\overline{RD}$ rise → A0 to 15 output  | $t_{RAE}$  | $x - 25$     |              | 55       |     | ns   |
| 19  | WR Low pulse width  | $t_{WW}$   | $2.0x - 40$  |              | 120      |     | ns   |
| 20  | D0 to 15 Valid → WR rise  | $t_{DW}$   | $2.0x - 120$ |              | 40       |     | ns   |
| 21  | WR rise → D0 to 15 Hold   | $t_{WD}$   | $0.5x - 40$  |              | 0        |     | ns   |
| 22  | A0 to 23 Valid → WAIT input $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{WAIT mode}\right)$                                 | $t_{AWH}$  |              | $3.5x - 130$ |          | 150 | ns   |
| 23  | A0 to 15 Valid → WAIT input $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{WAIT mode}\right)$                                 | $t_{AWL}$  |              | $3.0x - 100$ |          | 140 | ns   |
| 24  | $\overline{RD}/\overline{WR}$ fall → $\overline{WAIT}$ Hold $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{WAIT mode}\right)$ | $t_{CW}$   | $2.0x + 0$   |              | 160      |     | ns   |
| 25  | A0 to 23 Valid → PORT input   | $t_{APH}$  |              | $2.5x - 195$ |          | 5   | ns   |
| 26  | A0 to 23 Valid → PORT Hold  | $t_{APH2}$ | $2.5x + 50$  |              | 250      |     | ns   |
| 27  | $\overline{WR}$ rise → PORT Valid   | $t_{CP}$   |              | 200          |          | 200 | ns   |

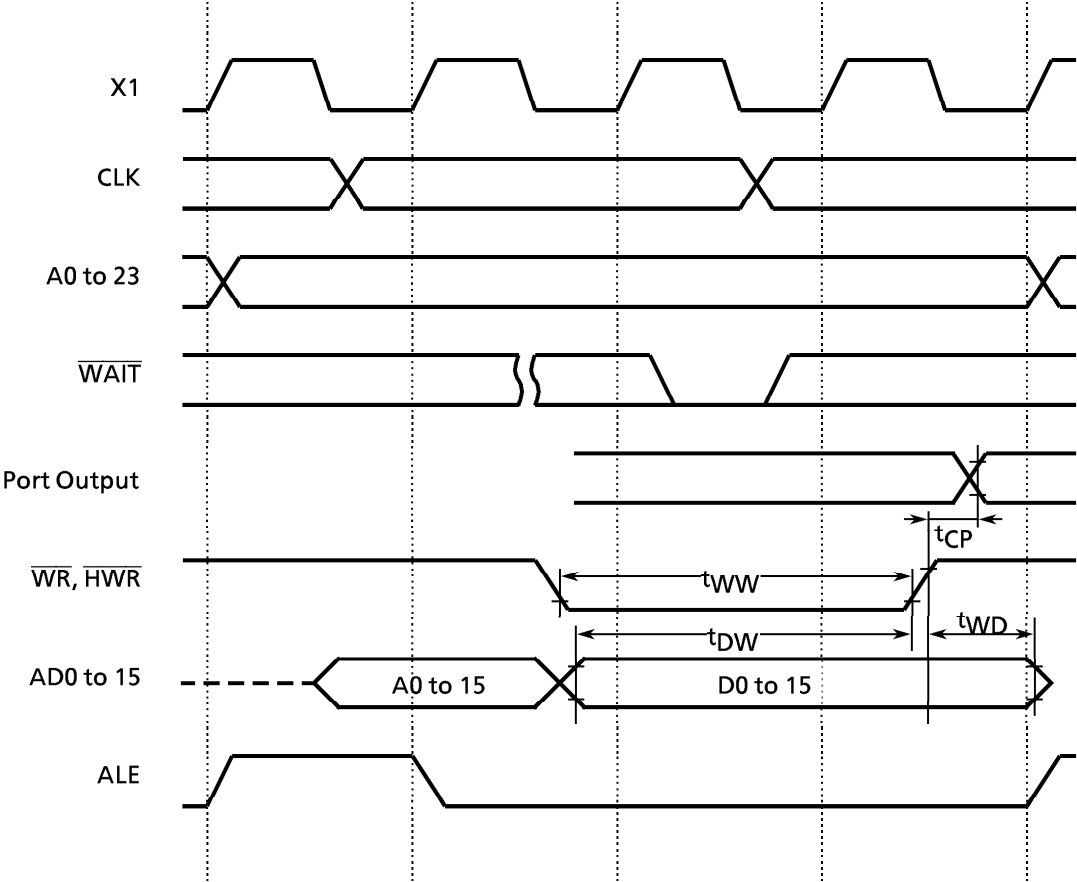
## AC Measuring Conditions

- Output Level: High  $0.7 \times V_{CC}$  / Low  $0.3 \times V_{CC}$ , CL = 50 pF
- Input Level: High  $0.9 \times V_{CC}$  / Low  $0.1 \times V_{CC}$

(3) Read Cycle



(4) Write Cycle



4.4 Serial Channel Timing

(1) I/O Interface Mode

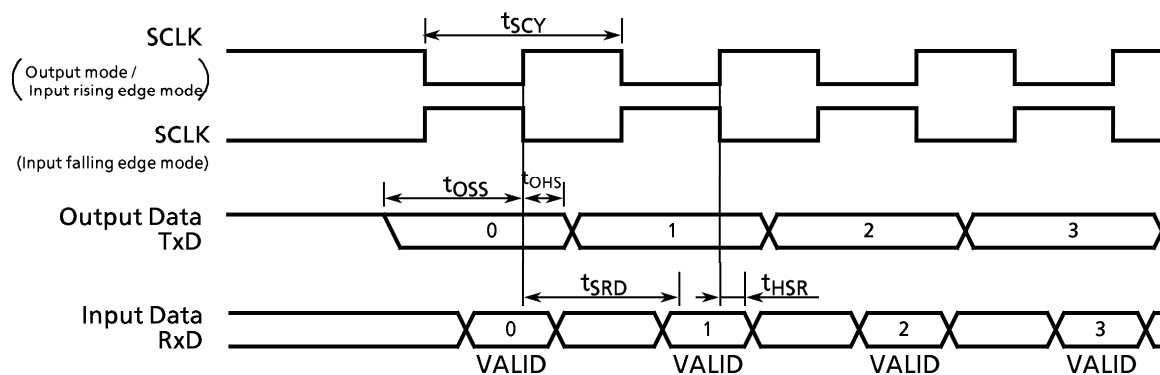
① SCLK Input Mode

| Parameter   | Symbol    | Variable              |                      | 12.5 MHz |     | 20 MHz |     | Unit    |
|---|-----------|-----------------------|----------------------|----------|-----|--------|-----|---------|
|   |           | Min                   | Max                  | Min      | Max | Min    | Max |         |
| SCLK cycle  | $t_{SCY}$ | 16X                   |                      | 1.28     |     | 0.8    |     | $\mu s$ |
| Output Data → Rising / falling edge of SCLK       | $t_{OSS}$ | $t_{SCY}/2 - 5X - 50$ |                      | 190      |     | 100    |     | ns      |
| SCLK rising / falling edge → Output Data hold     | $t_{OHS}$ | 5X - 100              |                      | 300      |     | 150    |     | ns      |
| SCLK rising / falling edge → Input Data hold      | $t_{HSR}$ | 0                     |                      | 0        |     | 0      |     | ns      |
| SCLK rising / falling edge → effective data input | $t_{SRD}$ |                       | $t_{SCY} - 5X - 100$ |          | 780 |        | 450 | ns      |

Note: SCLK rising / falling timing ; SCLK rising in the rising mode of SCLK,  
SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

| Parameter                               | Symbol    | Variable             |                      | 12.5 MHz |        | 20MHz |       | Unit    |
|---|-----------|----------------------|----------------------|----------|--------|-------|-------|---------|
|   |           | Min                  | Max                  | Min      | Max    | Min   | Max   |         |
| SCLK cycle (programmable)               | $t_{SCY}$ | 16X                  | 8192X                | 1.28     | 655.36 | 0.8   | 409.6 | $\mu s$ |
| Output Data → SCLK rising edge          | $t_{OSS}$ | $t_{SCY} - 2X - 150$ |                      | 970      |        | 550   |       | ns      |
| SCLK rising edge → Output Data hold     | $t_{OHS}$ | 2X - 80              |                      | 80       |        | 20    |       | ns      |
| SCLK rising edge → Input Data hold      | $t_{HSR}$ | 0                    |                      | 0        |        | 0     |       | ns      |
| SCLK rising edge → effective data input | $t_{SRD}$ |                      | $t_{SCY} - 2X - 150$ |          | 970    |       | 550   | ns      |



(2) UART Mode ( SCLK0, 1 are external input)

| Parameter                   | Symbol     | Variable  |     | 12.5 MHz |     | 20 MHz |     | Unit |
|-----------------------------|------------|-----------|-----|----------|-----|--------|-----|------|
|                             |            | Min       | Max | Min      | Max | Min    | Max |      |
| SCLK cycle                  | $t_{SCY}$  | $4x + 20$ |     | 340      |     | 220    |     | ns   |
| SCLK Low level pulse width  | $t_{SCYL}$ | $2x + 5$  |     | 165      |     | 105    |     | ns   |
| SCLK High level pulse width | $t_{SCYH}$ | $2x + 5$  |     | 165      |     | 105    |     | ns   |



## 4.5 AD Conversion Characteristics

$$AV_{CC} = V_{CC}, AV_{SS} = V_{SS}$$

| Parameter   | Symbol                            | Power Supply              | Min              | Typ.      | Max              | Unit    |
|---|-----------------------------------|---------------------------|------------------|-----------|------------------|---------|
| Analog reference voltage (+)                                | $V_{REFH}$                        | $V_{CC} = 5 V \pm 10\%$   | $V_{CC} - 1.5 V$ | $V_{CC}$  | $V_{CC}$         | V       |
|   |                                   | $V_{CC} = 3 V \pm 10\%$   | $V_{CC} - 0.2 V$ | $V_{CC}$  | $V_{CC}$         |         |
| Analog reference voltage (-)                                | $V_{REFL}$                        | $V_{CC} = 5 V \pm 10\%$   | $V_{SS}$         | $V_{SS}$  | $V_{SS} + 0.2 V$ |         |
|   |                                   | $V_{CC} = 3 V \pm 10\%$   | $V_{SS}$         | $V_{SS}$  | $V_{SS} + 0.2 V$ |         |
| Analog input voltage range                                  | $V_{AIN}$                         |                           | $V_{REFL}$       |           | $V_{REFH}$       |         |
| Analog current for analog reference voltage<br><VREFON> = 1 | $I_{REF}$<br>( $V_{REFL} = 0 V$ ) | $V_{CC} = 5 V \pm 10\%$   |                  | 0.5       | 1.5              | mA      |
|   |                                   | $V_{CC} = 3 V \pm 10\%$   |                  | 0.3       | 0.9              |         |
| <VREFON> = 0  |                                   | $V_{CC} = 2.7$ to $5.5 V$ |                  | 0.02      | 5.0              | $\mu A$ |
| Error<br>(except quantization errors)                       | -                                 | $V_{CC} = 5 V \pm 10\%$   |                  | $\pm 1.0$ | $\pm 3.0$        | LSB     |
|   |                                   | $V_{CC} = 3 V \pm 10\%$   |                  | $\pm 1.0$ | $\pm 5.0$        |         |

Note 1:  $1LSB = (V_{REFH} - V_{REFL}) / 2^{10} [V]$

Note 2: The operation above is guaranteed for  $f_{PPH} \geq 4$  MHz.

Note 3: The value  $I_{CC}$  includes the current which flows through the AVCC pin.

## 4.6 Event Counter Input Clock (external input clock: TI4, TI5, TI6, TI7)

| Parameter                    | Symbol     | Variable   |     | 12.5 MHz |     | 20 MHz |     | Unit |
|------------------------------|------------|------------|-----|----------|-----|--------|-----|------|
|                              |            | Min        | Max | Min      | Max | Min    | Max |      |
| Clock Cycle                  | $t_{VCK}$  | $8X + 100$ |     | 740      |     | 500    |     | ns   |
| Low level clock Pulse width  | $t_{VCKL}$ | $4X + 40$  |     | 360      |     | 240    |     | ns   |
| High level clock Pulse width | $t_{VCKH}$ | $4X + 40$  |     | 360      |     | 240    |     | ns   |

## 4.7 Interrupt and Capture Operation

(1)  $\overline{NMI}$ , INT0 Interrupts

| Parameter                                      | Symbol      | Variable |     | 12.5 MHz |     | 20 MHz |     | Unit |
|--|-------------|----------|-----|----------|-----|--------|-----|------|
|  |             | Min      | Max | Min      | Max | Min    | Max |      |
| $\overline{NMI}$ , INT0 Low level Pulse width  | $t_{INTAL}$ | $4X$     |     | 320      |     | 200    |     | ns   |
| $\overline{NMI}$ , INT0 High level Pulse width | $t_{INTAH}$ | $4X$     |     | 320      |     | 200    |     | ns   |

## (2) INT4 to 7 Interrupts and Capture

| Parameter                           | Symbol      | Variable   |     | 12.5 MHz |     | 20 MHz |     | Unit |
|-------------------------------------|-------------|------------|-----|----------|-----|--------|-----|------|
|                                     |             | Min        | Max | Min      | Max | Min    | Max |      |
| INT4 to INT7 Low level Pulse width  | $t_{INTBL}$ | $4X + 100$ |     | 420      |     | 300    |     | ns   |
| INT4 to INT7 High level Pulse width | $t_{INTBH}$ | $4X + 100$ |     | 420      |     | 300    |     | ns   |

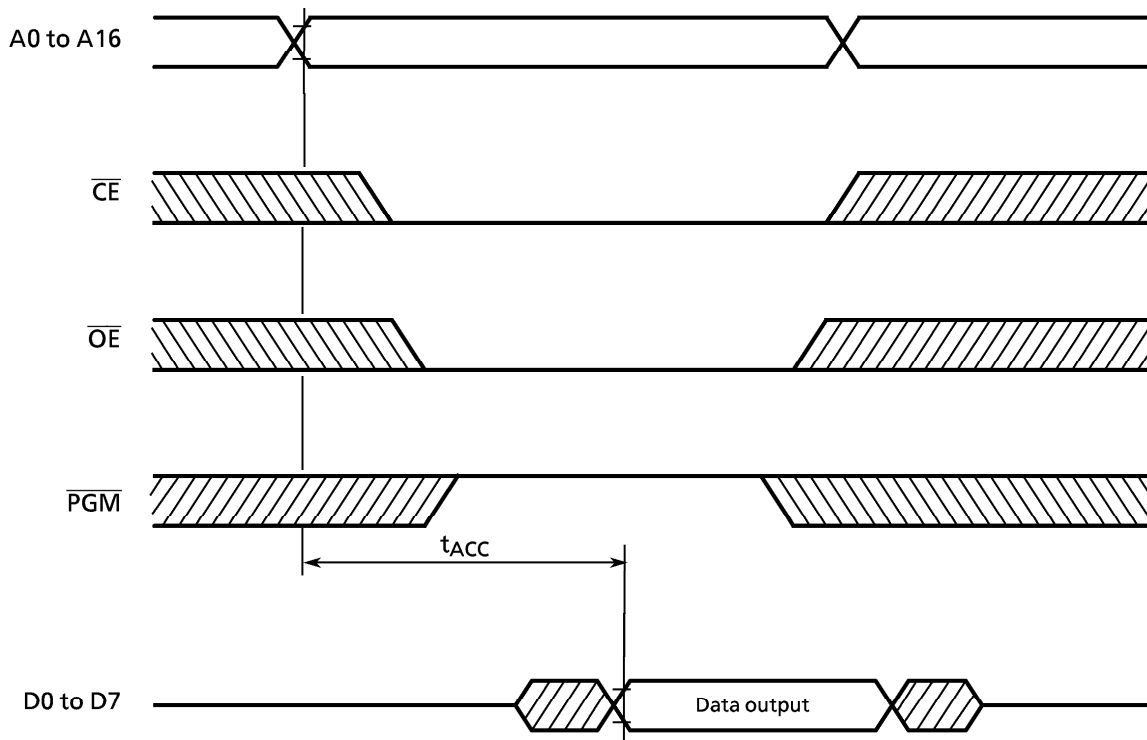
4.8 Read operation in PROM Mode

DC / AC characteristics

Ta = 25 ± 5°C Vcc = 5 V ± 10%

| Parameter   | Symbol           | Condition              | Min  | Max                      | Unit |
|---|------------------|------------------------|------|--------------------------|------|
| V <sub>PP</sub> Read Voltage  | V <sub>PP</sub>  | -                      | 4.5  | 5.5                      | V    |
| Input High Voltage (A0 to A16, $\overline{CE}$ , $\overline{OE}$ , PGM) | V <sub>IH1</sub> | -                      | 2.2  | V <sub>CC</sub> + 0.3    | V    |
| Input Low Voltage (A0 to A16, $\overline{CE}$ , $\overline{OE}$ , PGM)  | V <sub>IL1</sub> | -                      | -0.3 | 0.8                      | V    |
| Address to Output Delay   | t <sub>ACC</sub> | C <sub>L</sub> = 50 pF | -    | 2.25T <sub>CYC</sub> + α | ns   |

T<sub>CYC</sub> = 400 ns (10 MHz Clock)  
α = 200 ns

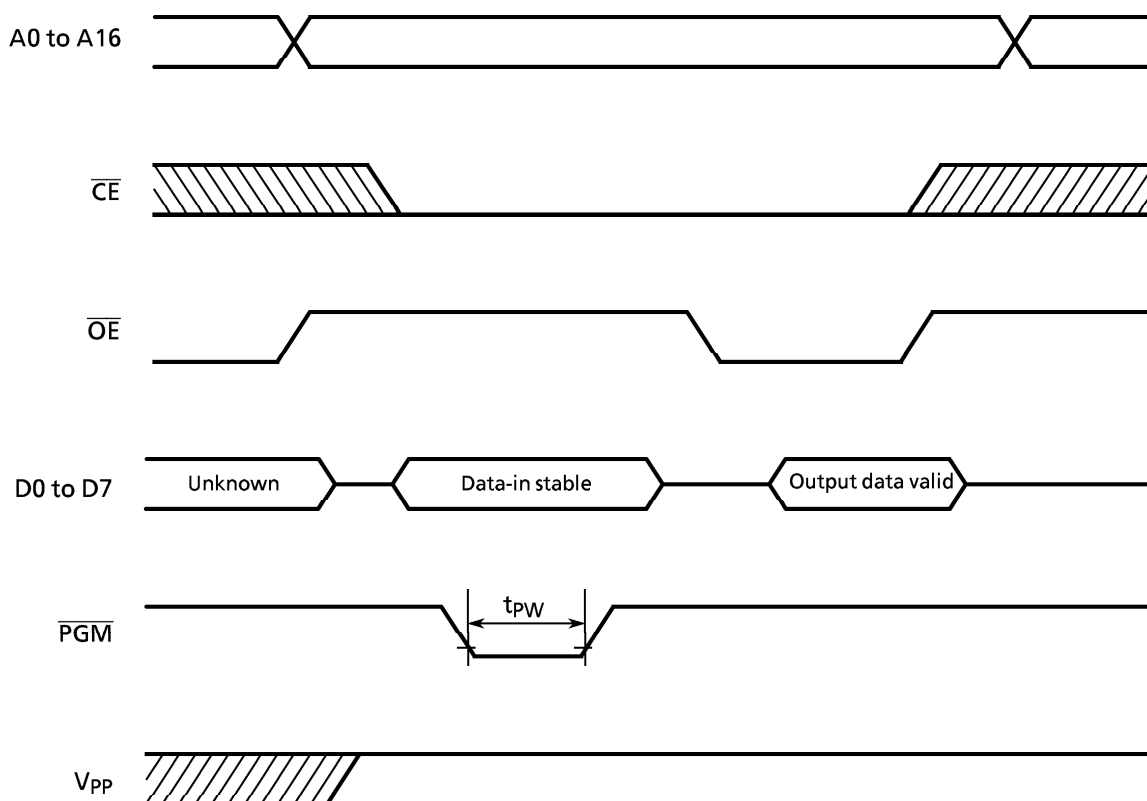


4.9 Program operation in PROM Mode

DC / AC characteristics

Ta = 25 ± 5°C Vcc = 6.25 V ± 0.25 V

| Parameter  | Symbol          | Condition                 | Min   | Typ.  | Max                   | Unit |
|--|-----------------|---------------------------|-------|-------|-----------------------|------|
| Programming Supply Voltage   | V <sub>PP</sub> | -                         | 12.50 | 12.75 | 13.00                 | V    |
| Input High Voltage<br>(D0 to D7, A0 to A16, $\overline{CE}$ , $\overline{OE}$ , $\overline{PGM}$ ) | V <sub>IH</sub> | -                         | 2.6   |       | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage<br>(D0 to D7, A0 to A16, $\overline{CE}$ , $\overline{OE}$ , $\overline{PGM}$ )  | V <sub>IL</sub> | -                         | - 0.3 |       | 0.8                   | V    |
| V <sub>CC</sub> Supply Current   | I <sub>CC</sub> | f <sub>c</sub> = 10 MHz   | -     |       | 50                    | mA   |
| V <sub>PP</sub> Supply Current   | I <sub>PP</sub> | V <sub>PP</sub> = 13.00 V | -     |       | 50                    | mA   |
| $\overline{PGM}$ Program Pulse Width   | t <sub>PW</sub> | C <sub>L</sub> = 50 pF    | 0.095 | 0.1   | 0.105                 | ms   |



Note 1: The power supply of V<sub>PP</sub> (12.75 V) must be set power-on at the same time or the later time for a power supply of V<sub>CC</sub> and must be clear power-on at the same time or early time for a power supply of V<sub>CC</sub>.

Note 2: The pulling up/down device on condition of V<sub>PP</sub> = 12.75 V suffer a damage for the device.

Note 3: The maximum spec of V<sub>PP</sub> pin is 14.0 V. Be carefull a overshoot at the program writing.